MSP430FR203x ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 組み込みマイクロコントローラ
  - 最高 16MHz の 16 ビット RISC アーキテクチャ
  - 3.6V～1.8V の広い電源電圧範囲 (最低電源電圧は SVS レベルにより制限されます。「SVS 仕様」を参照)
- 最適化された低消費電力モード (3V 時)
  - アクティブ: 126µA/MHz
  - スタンバイ
    - LPM3.5 で VLO あり:0.4µA
    - リアルタイム・クロック (RTC) カウンタ (LPM3.5 で 32768Hz の水晶振動子を使用):0.77µA
  - シャットダウン (LPM4.5):15nA
- 低消費電力の強誘電体 RAM (FRAM)
  - 最大 15.5KB の不揮発性メモリ
  - エラー訂正コード (ECC) 搭載
  - 書き込み保護を設定可能
  - プログラム、定数、ストレージの統合メモリ
  - 書き込みサイクルの耐久性:10^{15} 回
  - 放射線耐性、非磁性
- インテリジェントなデジタル・ペリフェラル
  - IR 変調ロジック
  - 2 つの 16 ビット・タイマ、それぞれに 3 つのキャプチャ/比較レジスタを搭載 (Timer_A3)
  - 1 つの 16 ビット・カウンタ専用 RTC カウンタ
  - 16 ビットの巡回冗長性検査 (CRC)
- 拡張シリアル通信
  - 拡張 USCI A (eUSCI_A) により UART、IrDA、SPI をサポート
  - 拡張 USCI B (eUSCI_B) により SPI および I^2C をサポート
- 高性能アナログ
  - 10 チャネル、10 ビットの A/D コンバータ (ADC)
    - 内蔵の 1.5V 基準電圧
    - サンプル・アンド・ホールド 200ksps
- クロック・システム (CS)
  - オンチップの 32kHz RC 発振器 (REFO)
  - オンチップの 16MHz デジタル制御発振器 (DCO)、周波数ロック・ループ (FLL) 付き
    - オンチップの基準電圧は室温で ±1% 精度
  - オンチップの超低周波数 10kHz 発振器 (VLO)
  - オンチップの高周波数変調発振器クロック (MODCLK)
  - 外付けの 32kHz 水晶発振器 (XT1)
  - 1～128 の MCLK プリスケーラをプログラム可能
  - 1、2、4、8 のプログラマブル・プリスケーラを使って MCLK から SMCLK を生成
- 汎用入出力およびピン機能
  - 64 ピンのパッケージに計 60 の I/O を搭載
  - 16 本の割り込みピン (P1、P2) により、MCU を LPM からウェイクアップ可能
  - すべての I/O で静電容量式タッチ機能をサポート
- 開発ツールとソフトウェア
  - 無償のプロフェッショナル開発環境
- ファミリ・メンバー (「デバイスの比較」も参照)
  - MSP430FR2033:15KB のプログラム FRAM + 512B の情報 FRAM + 2KB の RAM
  - MSP430FR2032:8KB のプログラム FRAM + 512B の情報 FRAM + 1KB の RAM
- パッケージ・オプション
  - 64 ピン:LQFP (PM)
  - 56 ピン:TSSOP (G56)
  - 48 ピン:TSSOP (G48)

1.2 アプリケーション

- 煙/火災感知器
- ガラス破壊検知器
- 産業用センサ管理
- システム・スーパーバイザ、低消費電力コプロセッサ
- 温度センサ/コントローラ
- データ・ストレージ、データ統合
- ヒューマン・マシン・インターフェイス (HMI) コントローラ

1.3 概要

このTI MSP430™ファミリの低消費電力マイクロコントローラは複数のデバイスからなり、さまざまな用途に対応する多様なペリフェラル・セットを特長としています。アーキテクチャに多様な低消費電力モードを組み合わせ、携帯型測定機器で長いバッテリ駆動時間を実現するように最適化しています。強力な16ビットRISC CPU、16ビット・レジスタ、および定数ジェネレータが搭載されているため、最高水準のコード効率を実現できます。またDCOにより、低消費電力モードからアクティブ・モードへ10µs未満でウェイクアップできます。

モジュールの詳細な説明については、*『MSP430FR4xx and MSP430FR2xx Family User's Guide』* (英語) を参照してください。

製品情報(1)

型番	パッケージ	本体サイズ(2)
MSP430FR2033IPM	LQFP (64)	10mm×10mm
MSP430FR2033IG56	TSSOP (56)	14.0mm×6.1mm
MSP430FR2033IG48	TSSOP (48)	12.5mm×6.1mm
MSP430FR2032IPM	LQFP (64)	10mm×10mm
MSP430FR2032IG56	TSSOP (56)	14.0mm×6.1mm
MSP430FR2032IG48	TSSOP (48)	12.5mm×6.1mm

(1) 最新の製品、パッケージ、および注文情報については、9の「*付録：パッケージ・オプション*」、またはwww.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9の「*メカニカル・データ*」を参照してください。

1.4 機能ブロック図

機能ブロック図を、図 1-1に示します。

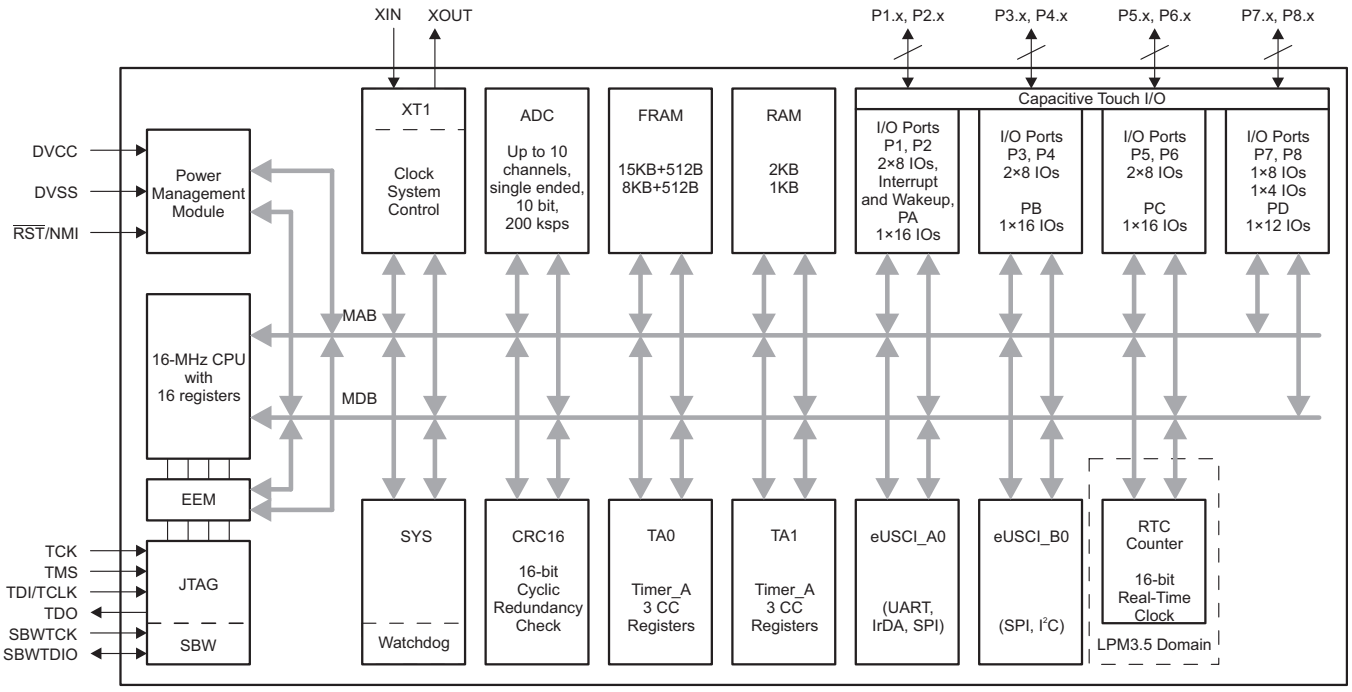


図 1-1. 機能ブロック図

- このデバイスには、DVCCおよびDVSSからなる1つの主電源ペアがあり、デジタルとアナログの両方のモジュールへ電力を供給します。バイパスおよびデカップリング・コンデンサとしては、それぞれ4.7µF～10µFおよび0.1µF、精度±5%が推奨されます。
- P1およびP2にはピン割り込み機能があり、MCUをLPM3.5からウェイクアップできます。
- 各Timer_A3には3つのCCレジスタがありますが、外部的に接続されているのはCCR1およびCCR2のみです。CCR0レジスタは、内部的な期間のタイミングと割り込みの生成にのみ使用できます。
- LPM3.5モードでは、他のペリフェラルがオフの間もRTCカウンタは機能できます。
- TSSOP-56およびTSSOP-48パッケージでは、すべてのI/Oが接合されているわけではありません(Table 4-1を参照)。すべてのI/Oは、静電容量式タッチI/Oとして構成可能です。

Table of Contents

2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

リビジョン D からリビジョン E への変更点

2019年1月22日発行分から2019年12月9日発行分への変更 **Page**

- Changed the note that begins "Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset..." in Section 5.3, *Recommended Operating Conditions* 15
- Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 5.3, *Recommended Operating Conditions* 15
- Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in Section 5.3, *Recommended Operating Conditions* 15
- Added the note "See *MSP430 32-kHz Crystal Oscillators* for details on crystal section, layout, and testing" to Table 5-3, *XT1 Crystal Oscillator (Low Frequency)* 22
- Changed the note that begins "Requires external capacitors at both terminals..." in Table 5-3, *XT1 Crystal Oscillator (Low Frequency)* 22
- Added the $t_{(int)}$ parameter in Table 5-8, *Digital Inputs* 24
- Added the $t_{TA,cap}$ parameter in Table 5-10, *Timer_A* 25
- Corrected the test conditions for the $R_{I,MUX}$ parameter in Table 5-17, *ADC, Power Supply and Input Range Conditions* 31
- Added the note that begins "$t_{Sample} = \ln(2^{n+1}) \times \tau$ ..." in Table 5-18, *ADC, 10-Bit Timing Parameters* 31

リビジョン C からリビジョン D への変更点

2018年8月30日発行分から2019年01月21日発行分への変更 **Page**

- ドキュメント全体を通して、「変調発振器 (MODOSC)」を「変調発振器クロック (MODCLK)」に変更 1
- Added "or memory corruption" to note (1) in Section 5.1, *Absolute Maximum Ratings* 15
- Added the note that begins "The VLO clock frequency is reduced by..." after Table 5-6, *Internal Very-Low-Power Low-Frequency Oscillator (VLO)* 23
- Added the $t_{TA,cap}$ parameter in Table 5-10, *Timer_A* 25
- Changed the parameter symbol from R_I to $R_{I,MUX}$ in Table 5-17, *ADC, Power Supply and Input Range Conditions* 31
- Added the $R_{I,Misc}$ parameter in Table 5-17, *ADC, Power Supply and Input Range Conditions* 31
- Removed ADCDIV from the formula for the $t_{CONVERT}$ TYP value, because ADCCLK is after division, in Table 5-18, *ADC, 10-Bit Timing Parameters* 31
- Added note (2) for R_I calculation in Table 5-18, *ADC, 10-Bit Timing Parameters* 31
- Removed "±3°C" on both temperatures in the note that begins "The device descriptor structure contains..." in Table 5-19, *ADC, 10-Bit Linearity Parameters* 32
- Add "10b" for ADCSSEL bit in Table 6-6, *Clock Distribution* 39
- Added Figure 6-1, *Clock Distribution Block Diagram* 39
- Corrected the spelling of the IRDSSEL bit in the paragraph that begins "The IR functions are controlled by..." in Section 6.9.8, *Timers (Timer0_A3, Timer1_A3)* 44
- Changed two instances of "ADC 1.5-V Reference Temperature" to "ADC 1.5-V Reference Temperature Sensor" in Table 6-29, *Device Descriptors* 62

リビジョン B からリビジョン C への変更点

2015年8月15日発行分から2018年08月29日発行分への変更 **Page**

- Updated Section 3.1, *Related Products* 7
- Replaced all notes on Section 5.11, *Thermal Characteristics* 19
- Added note to V_{SVSH-} and V_{SVSH+} parameters in Table 5-1, *PMM, SVS and BOR* 20
- Added the $t_{TA,cap}$ parameter in Table 5-10, *Timer_A* 25
- Updated the link to the BSL user's guide in Section 6.4, *Bootloader (BSL)* 36
- Changed all instances of "bootstrap loader" to "bootloader" throughout document 36
- Corrected the ADCINCHx column heading in Table 6-12, *ADC Channel Connections* 45

- 8「デバイスおよびドキュメントのサポート」のデバイス別情報とリンクを更新 76

リビジョン A からリビジョン B への変更点

2014年12月23日発行分から2015年08月14日発行分への変更	Page

- Corrected "10-BIT ADC CHANNELS" column for MSP430FR2032IPM in Table 3-1, *Device Comparison* 7
- Added T_{stg} MIN and MAX values 15
- Added Section 5.2, *ESD Ratings* 15
- Changed all graphs in Section 5.9, *Typical Characteristics, Low-Power Mode Supply Currents*, for new measurements 18
- Added $V_{REF,\ 1.2V}$ parameter to Table 5-1, *PMM, SVS and BOR* 20
- Added the $t_{TA,cap}$ parameter in Table 5-10, *Timer_A* 25
- Changed $t_{STE,LEAD}$ MIN value at 2 V from 40 ns to 50 ns 28
- Changed $t_{STE,LEAD}$ MIN value at 3 V from 24 ns to 45 ns 28
- Changed $t_{VALID,SO}$ MAX value at 2 V from 55 ns to 65 ns 28
- Changed $t_{VALID,SO}$ MAX value at 3 V from 30 ns to 40 ns 28
- Changed the f_{ADCOSC} TYP value from 4.5 MHz to 5.0 MHz 31
- In Table 6-1, *Operating Modes*, changed the entry for "Power Consumption at 25°C, 3 V" in AM from 100 µA/MHz to 126 µA/MHz 34
- In Table 6-1, *Operating Modes*, added "with RTC only" to the entry for "Power Consumption at 25°C, 3 V" in LPM3.5 34
- In Table 6-2, *Interrupt Sources, Flags, and Vectors*, removed "FRAM access time error" (ACCTEIFG) from the "System NMI" row 35

初版からリビジョン A への変更点

2014年10月3日発行分から2014年12月22日発行分への変更	Page

- Moved T_{stg} to Absolute Maximum Ratings 15
- Added the $t_{TA,cap}$ parameter in Table 5-10, *Timer_A* 25
- Changed link to BSL user's guide in Section 6.4, *Bootloader (BSL)* 36
- Added note (1) to Table 6-6 39
- Changed the values of ADC Calibration Tag and ADC Calibration Length in the ADC Calibration row 62
- Added Calibration Tag, Calibration Length, and 1.5-V Reference in the Reference and DCO Calibration row 63
- Added row for BSL memory to Table 6-30 63

3 Device Comparison

Table 3-1 summarizes the features of the available family members.

Table 3-1. Device Comparison(1)(2)

DEVICE	PROGRAM FRAM + INFORMATION FRAM (BYTES)	SRAM (BYTES)	TA0, TA1	eUSCI_A	eUSCI_B	10-BIT ADC CHANNELS	I/O	PACKAGE
MSP430FR2033IPM	15360 + 512	2048	3 × CCR(3)	1	1	10	60	PM (LQFP64)
MSP430FR2033IG56	15360 + 512	2048	3 × CCR(3)	1	1	8	52	G56 (TSSOP56)
MSP430FR2033IG48	15360 + 512	2048	3 × CCR(3)	1	1	8	44	G48 (TSSOP48)
MSP430FR2032IPM	8192 + 512	1024	3 × CCR(3)	1	1	10	60	PM (LQFP64)
MSP430FR2032IG56	8192 + 512	1024	3 × CCR(3)	1	1	8	52	G56 (TSSOP56)
MSP430FR2032IG48	8192 + 512	1024	3 × CCR(3)	1	1	8	44	G48 (TSSOP48)

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in 9, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers

High-performance low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing & measurement MCUs

One platform. One ecosystem. Endless possibilities.

Companion products for MSP430FR2033

Review products that are frequently purchased or used with this product.

Reference designs for MSP430FR2033

Find reference designs leveraging the best in TI technology to solve your system-level challenges.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the 64-pin PM package.

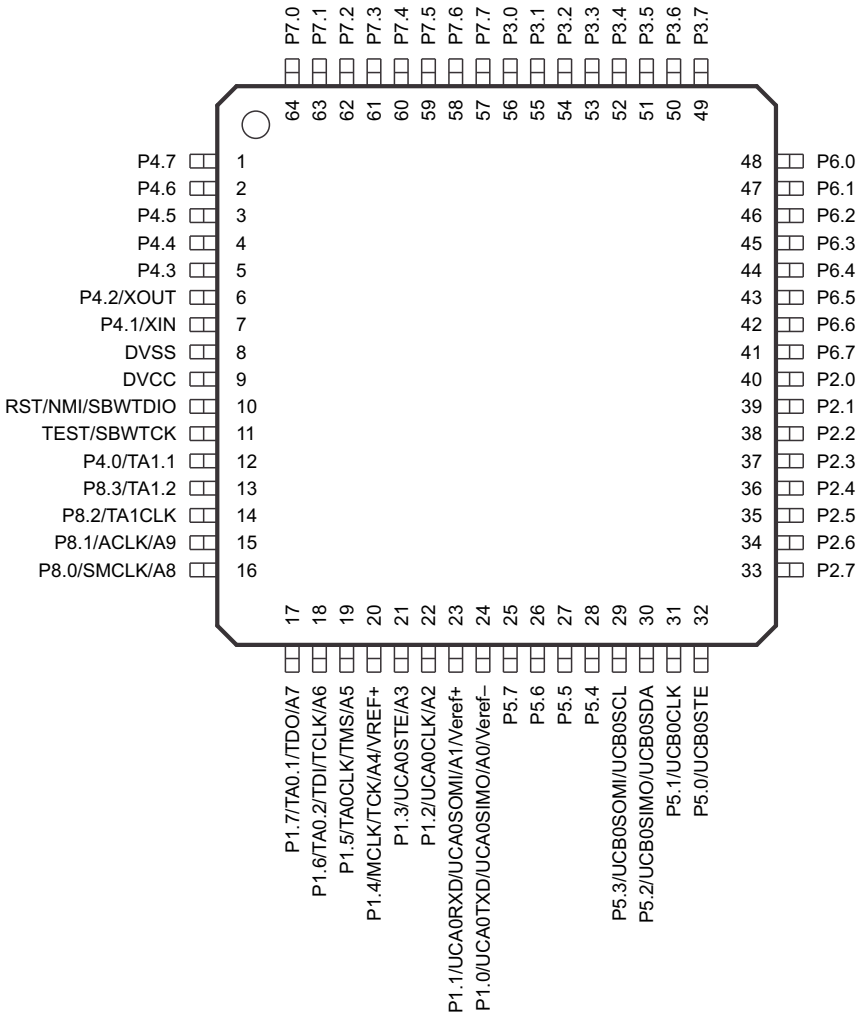


Figure 4-1. 64-Pin PM (LQFP) Designation (Top View)

Figure 4-2 shows the 56-pin G56 package.

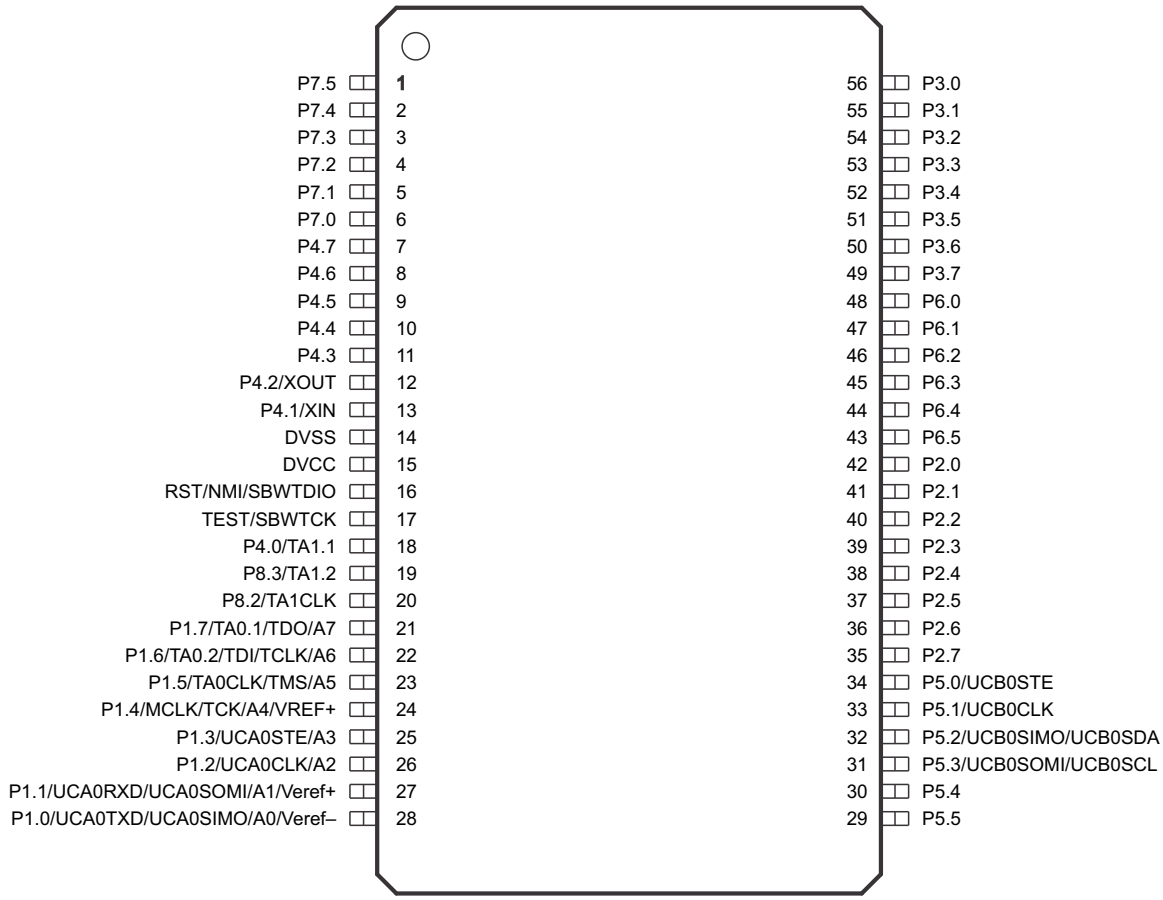


Figure 4-2. 56-Pin DGG (TSSOP) Designation (Top View)

Figure 4-3 shows the 48-pin G48 package.

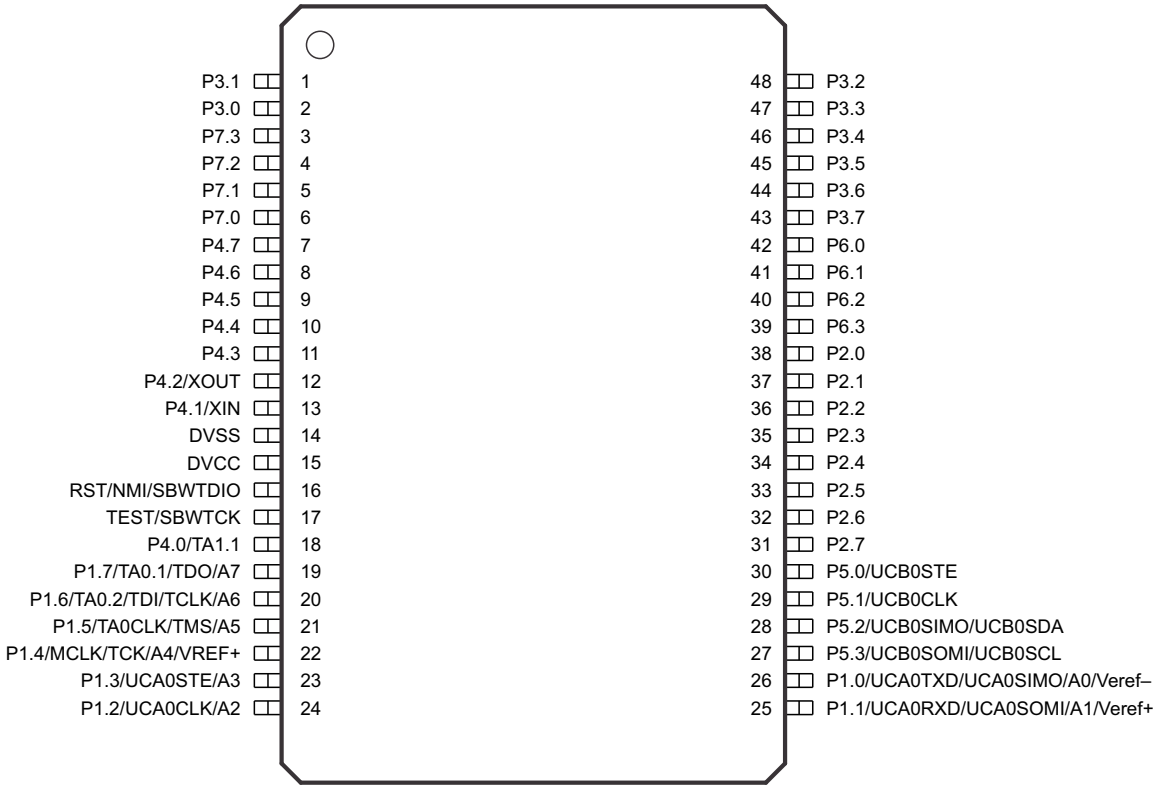


Figure 4-3. 48-Pin DGG (TSSOP) Designation (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

TERMINAL				I/O	DESCRIPTION
NAME	PACKAGE SUFFIX				
	PM	G56	G48		
P4.7	1	7	7	I/O	General-purpose I/O
P4.6	2	8	8	I/O	General-purpose I/O
P4.5	3	9	9	I/O	General-purpose I/O
P4.4	4	10	10	I/O	General-purpose I/O
P4.3	5	11	11	I/O	General-purpose I/O
P4.2/XOUT	6	12	12	I/O	General-purpose I/O Output terminal for crystal oscillator
P4.1/XIN	7	13	13	I/O	General-purpose I/O Input terminal for crystal oscillator
DVSS	8	14	14		Power ground
DVCC	9	15	15		Power supply
$\overline{\text{RST}}$/NMI/SBWTDIO	10	16	16	I/O	Reset input, active low Nonmaskable interrupt input Spy-Bi-Wire data input/output
TEST/SBWTCK	11	17	17	I	Test Mode pin – selected digital I/O on JTAG pins Spy-Bi-Wire input clock
P4.0/TA1.1	12	18	18	I/O	General-purpose I/O Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs
P8.3/TA1.2 (1)	13	19		I/O	General-purpose I/O Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs
P8.2/TA1CLK (1)	14	20		I/O	General-purpose I/O Timer clock input TACLK for TA1
P8.1/ACLK/A9 (1)	15			I/O	General-purpose I/O ACLK output Analog input A9
P8.0/SMCLK/A8 (1)	16			I/O	General-purpose I/O SMCLK output Analog input A8
P1.7/TA0.1/TDO/A7 (2)	17	21	19	I/O	General-purpose I/O (2) Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs Test data output Analog input A7
P1.6/TA0.2/TDI/TCLK/A6 (2)	18	22	20	I/O	General-purpose I/O (2) Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs Test data input or test clock input Analog input A6

(1) Any pin that is not bonded out in a smaller package must be initialized by software after reset to achieve the lowest leakage current.
(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	PACKAGE SUFFIX				
	PM	G56	G48		
P1.5/TA0CLK/TMS/A5 (2)	19	23	21	I/O	General-purpose I/O (2) Timer clock input TACLK for TA0 Test mode select Analog input A5
P1.4/MCLK/TCK/A4/VREF+ (2)	20	24	22	I/O	General-purpose I/O (2) MCLK output Test clock Analog input A4 Output of positive reference voltage with ground as reference
P1.3/UCA0STE/A3	21	25	23	I/O	General-purpose I/O eUSCI_A0 SPI slave transmit enable Analog input A3
P1.2/UCA0CLK/A2	22	26	24	I/O	General-purpose I/O eUSCI_A0 SPI clock input/output Analog input A2
P1.1/UCA0RXD/UCA0SOMI/ A1/Veref+	23	27	25	I/O	General-purpose I/O eUSCI_A0 UART receive data eUSCI_A0 SPI slave out/master in Analog input A1, and ADC positive reference
P1.0/UCA0TXD/UCA0SIMO/ A0/Veref-	24	28	26	I/O	General-purpose I/O eUSCI_A0 UART transmit data eUSCI_A0 SPI slave in/master out Analog input A0, and ADC negative reference
P5.7 (1)	25			I/O	General-purpose I/O
P5.6 (1)	26			I/O	General-purpose I/O
P5.5 (1)	27	29		I/O	General-purpose I/O
P5.4 (1)	28	30		I/O	General-purpose I/O
P5.3/UCB0SOMI/UCB0SCL	29	31	27	I/O	General-purpose I/O eUSCI_B0 SPI slave out/master in; eUSCI_B0 I^2C clock
P5.2/UCB0SIMO/UCB0SDA	30	32	28	I/O	General-purpose I/O eUSCI_B0 SPI slave in/master out; eUSCI_B0 I^2C data
P5.1/UCB0CLK	31	33	29	I/O	General-purpose I/O eUSCI_B0 clock input/output
P5.0/UCB0STE	32	34	30	I/O	General-purpose I/O eUSCI_B0 slave transmit enable
P2.7	33	35	31	I/O	General-purpose I/O
P2.6	34	36	32	I/O	General-purpose I/O
P2.5	35	37	33	I/O	General-purpose I/O
P2.4	36	38	34	I/O	General-purpose I/O
P2.3	37	39	35	I/O	General-purpose I/O
P2.2	38	40	36	I/O	General-purpose I/O
P2.1	39	41	37	I/O	General-purpose I/O

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	PACKAGE SUFFIX				
	PM	G56	G48		
P2.0	40	42	38	I/O	General-purpose I/O
P6.7(1)	41			I/O	General-purpose I/O
P6.6(1)	42			I/O	General-purpose I/O
P6.5(1)	43	43		I/O	General-purpose I/O
P6.4(1)	44	44		I/O	General-purpose I/O
P6.3	45	45	39	I/O	General-purpose I/O
P6.2	46	46	40	I/O	General-purpose I/O
P6.1	47	47	41	I/O	General-purpose I/O
P6.0	48	48	42	I/O	General-purpose I/O
P3.7	49	49	43	I/O	General-purpose I/O
P3.6	50	50	44	I/O	General-purpose I/O
P3.5	51	51	45	I/O	General-purpose I/O
P3.4	52	52	46	I/O	General-purpose I/O
P3.3	53	53	47	I/O	General-purpose I/O
P3.2	54	54	48	I/O	General-purpose I/O
P3.1	55	55	1	I/O	General-purpose I/O
P3.0	56	56	2	I/O	General-purpose I/O
P7.7(1)	57			I/O	General-purpose I/O
P7.6(1)	58			I/O	General-purpose I/O
P7.5(1)	59	1		I/O	General-purpose I/O
P7.4(1)	60	2		I/O	General-purpose I/O
P7.3	61	3	3	I/O	General-purpose I/O
P7.2	62	4	4	I/O	General-purpose I/O
P7.1	63	5	5	I/O	General-purpose I/O
P7.0	64	6	6	I/O	General-purpose I/O

4.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see Section 6.9.12.

4.4 Connection of Unused Pins

Table 4-2 shows the correct termination of unused pins.

Table 4-2. Connection of Unused Pins(1)

PIN	POTENTIAL	COMMENT
Px.0 to Px.7	Open	Set to port function, output direction (PxDIR.n = 1)
$\overline{\text{RST}}$/NMI	DVCC	47-kΩ pullup or internal pullup selected with 10-nF (or 1.1-nF) pulldown(2)
TEST	Open	This pin always has an internal pulldown enabled.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage applied at DVCC pin to V_{SS}	–0.3	4.1	V
Voltage applied to any pin(2)	–0.3	V_{CC} + 0.3 (4.1 Maximum)	V
Diode current at any device pin		±2	mA
Maximum junction temperature, T_J		85	°C
Storage temperature, T_{stg}(3)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage or memory corruption to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage applied at DVCC pin(1)(2)(3)(4)		1.8		3.6	V
V_{SS}	Supply voltage applied at DVSS pin			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{DVCC}	Recommended capacitor at DVCC(5)		4.7	10		µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(6)	No FRAM wait states (NWAITSx = 0)	0		8	MHz
		With FRAM wait states (NWAITSx = 1)(7)	0		16(8)	
f_{ACLK}	Maximum ACLK frequency				40	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(8)	MHz

(1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor C_{DVCC} limits the slopes accordingly.
(2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(4) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in Table 5-1.
(5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
(8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current(1)

PARAMETER	EXECUTION MEMORY	TEST CONDITIONS	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)						UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM,\ FRAM}$(0%)	FRAM 0% cache hit ratio	3 V, 25°C	504		2874		3156	3700	µA
		3 V, 85°C	516		2919		3205		
$I_{AM,\ FRAM}$(100%)	FRAM 100% cache hit ratio	3 V, 25°C	209		633		1056	1298	µA
		3 V, 85°C	217		647		1074		
$I_{AM,\ RAM}$(2)	RAM	3 V, 25°C	231		809		1450		µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. Characterized with program executing typical data processing.
f_{ACLK} = 32786 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency
Program and data entirely reside in FRAM. All execution is from FRAM.
(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

5.5 Active Mode Supply Current Per MHz

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$dI_{AM,FRAM}/df$	Active mode current consumption per MHz, execution from FRAM, no wait states(1)	(($I_{AM,\ 75\%\ cache\ hit\ rate}$ at 8 MHz) – ($I_{AM,\ 75\%\ cache\ hit\ rate}$ at 1 MHz)) / 7 MHz	126	µA/MHz

(1) All peripherals are turned on in default settings.

5.6 Low-Power Mode LPM0 Supply Currents Into V_{CC} Excluding External Current

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)(1)(2)

PARAMETER		V_{CC}	FREQUENCY (f_{SMCLK})						UNIT
			1 MHz		8 MHz		16 MHz		
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	Low-power mode LPM0 supply current	2 V	158		307		415		µA
		3 V	169		318		427		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32786 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} at specified frequency.

5.7 Low-Power Mode LPM3 and LPM4 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		V_{CC}	–40°C		25°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT1}$	Low-power mode 3, includes SVS (2)(3)(4)	3 V	1.13		1.31	1.99	3.00		µA
		2 V	1.06		1.21		2.94		
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS (5)	3 V	0.92		1.00	1.75	2.89		µA
		2 V	0.86		1.00		2.75		
$I_{LPM3,\ RTC}$	Low-power mode 3, RTC, excludes SVS (6)	3 V	1.08		1.25		3.04		µA
$I_{LPM4,\ SVS}$	Low-power mode 4, includes SVS	3 V	0.65		0.75		1.88		µA
		2 V	0.63		0.73		1.85		
I_{LPM4}	Low-power mode 4, excludes SVS	3 V	0.51		0.58		1.51		µA
		2 V	0.50		0.57		1.49		

(1) All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Golledge MS1V-TK/I_32.768KHZ crystal with a load capacitance chosen to closely match the required load.
(4) Low-power mode 3, includes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 3, VLO, excludes SVS test conditions:
Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) RTC periodically wakes up every second with external 32768-Hz as source.

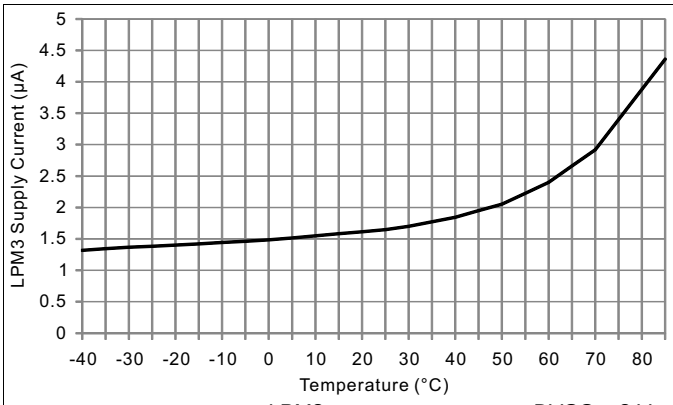
5.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	–40°C		25°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5,\ XT1}$	Low-power mode 3.5, includes SVS (1)(2) (3) (also see Figure 5-2)	3 V	0.71		0.77	1.25	1.06	2.06	µA
		2 V	0.66		0.70		0.95		
$I_{LPM4.5,\ SVS}$	Low-power mode 4.5, includes SVS (4)	3 V	0.23		0.25	0.375	0.32	0.43	µA
		2 V	0.20		0.20		0.24		
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS (5)	3 V	0.010		0.015	0.070	0.073	0.140	µA
		2 V	0.008		0.013		0.060		

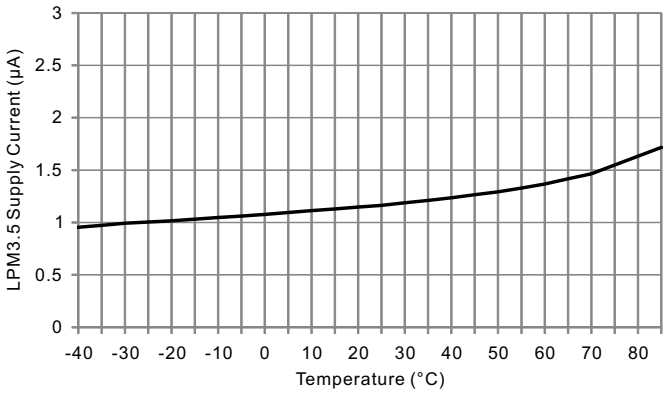
(1) Not applicable for devices with HF crystal oscillator only.
(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance chosen to closely match the required load.
(3) Low-power mode 3.5, includes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz

5.9 Typical Characteristics, Low-Power Mode Supply Currents



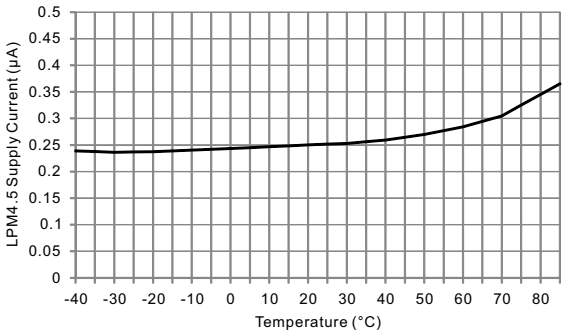
LPM3 DVCC = 3 V
SVS disabled RTC counter on

Figure 5-1. LPM3 Supply Current vs Temperature



LPM3.5 DVCC = 3 V
12.5-pF crystal on XT1 SVS enabled

Figure 5-2. LPM3.5 Supply Current vs Temperature



LPM4.5 DVCC = 3 V SVS enabled

Figure 5-3. LPM4.5 Supply Current vs Temperature

5.10 Typical Characteristics - Current Consumption Per Module

MODULE	TEST CONDITIONS	REFERENCE CLOCK	TYP	UNIT
Timer_A		Module input clock	5	µA/MHz
eUSCI_A	UART mode	Module input clock	7	µA/MHz
eUSCI_A	SPI mode	Module input clock	5	µA/MHz
eUSCI_B	SPI mode	Module input clock	5	µA/MHz
eUSCI_B	I^2C mode, 100 kbaud	Module input clock	5	µA/MHz
RTC		32 kHz	85	nA
CRC	From start to end of operation	MCLK	8.5	µA/MHz

5.11 Thermal Characteristics

THERMAL METRIC(1)		PACKAGE	VALUE(2)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air	LQFP-64 (PM)	61.7	°C/W
$\theta_{JC, (TOP)}$	Junction-to-case (top) thermal resistance		25.4	°C/W
θ_{JB}	Junction-to-board thermal resistance		32.7	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		32.4	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		2.5	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air	TSSOP-56 (DGG56)	62.4	°C/W
$\theta_{JC, (TOP)}$	Junction-to-case (top) thermal resistance		18.7	°C/W
θ_{JB}	Junction-to-board thermal resistance		31.4	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		31.1	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.8	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air	TSSOP-48 (DGG48)	68.9	°C/W
$\theta_{JC, (TOP)}$	Junction-to-case (top) thermal resistance		23	°C/W
θ_{JB}	Junction-to-board thermal resistance		35.8	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		35.3	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		1.1	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) The values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

5.12 Timing and Switching Characteristics

5.12.1 Power Supply Sequencing

Figure 5-4 shows the power supply reset parameters.

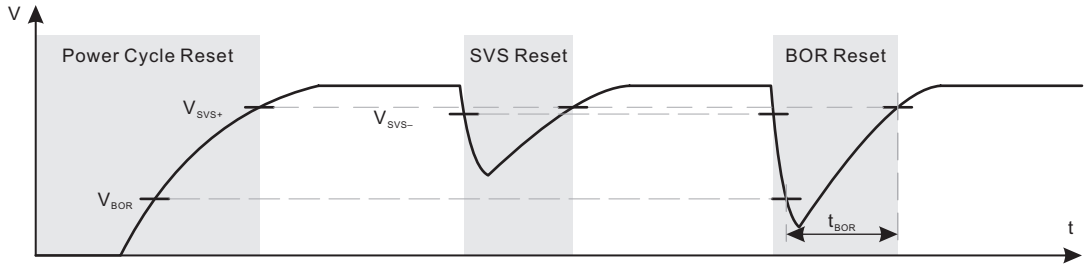


Figure 5-4. Power Cycle, SVS, and BOR Reset Conditions

Table 5-1. PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR, safe}$	Safe BOR power-down level(1)		0.1			V
$t_{BOR, safe}$	Safe BOR reset delay(2)		10			ms
$I_{SVSH,AM}$	SVS_H current consumption, active mode	V_{CC} = 3.6 V			1.5	µA
$I_{SVSH,LPM}$	SVS_H current consumption, low-power modes	V_{CC} = 3.6 V		240		nA
V_{SVSH-}	SVS_H power-down level(3)		1.71	1.81	1.87	V
V_{SVSH+}	SVS_H power-up level(3)		1.76	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis			70		mV
$t_{PD,SVSH, AM}$	SVS_H propagation delay, active mode				10	µs
$t_{PD,SVSH, LPM}$	SVS_H propagation delay, low-power modes				100	µs
$V_{REF, 1.2V}$	1.2-V REF voltage(4)		1.158	1.200	1.242	V

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.
(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+}.
(3) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.
(4) This is a characterized result with external 1-mA load to ground from –40°C to 85°C.

5.12.2 Reset Timing

Table 5-2. Wake-Up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wakeup (1)		3 V		10		µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		3V			200 ns + 2.5/f_{DCO}	
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (2)		3 V		10		µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode		3 V		10		µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		3 V		350		µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	3 V		350		µs
		SVSHE = 0	3 V		1		ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode (2)		3 V		1		ms
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		3 V	2			µs

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

5.12.3 Clock Specifications

Table 5-3. XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{XT1,\ LF}$	XT1 oscillator crystal, low frequency	LFXTBYPASS = 0		32768		Hz
$DC_{XT1,\ LF}$	XT1 oscillator LF duty cycle	Measured at MCLK, f_{LFXT} = 32768 Hz	30%		70%	
$f_{XT1,SW}$	XT1 oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 (3)(4)		32768		Hz
$DC_{XT1,\ SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1	40%		60%	
OA_{LFXT}	Oscillation allowance for LF crystals (5)	LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF		200		kΩ
$C_{L,eff}$	Integrated effective load capacitance(6)	See (7)		1		pF
$t_{START,LFXT}$	Start-up time (8)	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF		1000		ms
$f_{Fault,LFXT}$	Oscillator fault frequency (9)	XTS = 0(10)	0		3500	Hz

(1) To improve EMI on the LFXT oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) See MSP430 32-kHz Crystal Oscillators for details on crystal section, layout, and testing.
(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT,\ SW}$.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(8) Includes start-up counter of 1024 clock cycles.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-4. DCO FLL, Frequency

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO, FLL}$	FLL lock frequency, 16 MHz, 25°C	Measured at MCLK, Internal trimmed REFO as reference	3 V	–1.0%		1.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C			–2.0%		2.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C	Measured at MCLK, XT1 crystal as reference		–0.5%		0.5%	
f_{DUTY}	Duty cycle	Measured at MCLK, XT1 crystal as reference	3 V	40%	50%	60%	
$Jitter_{cc}$	Cycle-to-cycle jitter, 16 MHz				0.25%		
$Jitter_{long}$	Long-term jitter, 16 MHz				0.022%		
$t_{FLL, lock}$	FLL lock time				120		ms

Table 5-5. REFO

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	3 V		15		µA
f_{REFO}	REFO calibrated frequency	Measured at MCLK	3 V		32768		Hz
	REFO absolute calibrated tolerance	–40°C to 85°C	1.8 V to 3.6 V	–3.5%		3.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at MCLK(1)	3 V		0.01		%/°C
df_{REFO}/d_{VCC}	REFO frequency supply voltage drift	Measured at MCLK at 25°C(2)	1.8 V to 3.6 V		1		%/V
f_{DC}	REFO duty cycle	Measured at MCLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40% to 60% duty cycle			50		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(2 V to 3.6 V) – MIN(2 V to 3.6 V)) / MIN(2 V to 3.6 V) / (3.6 V – 2 V)

Table 5-6. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at MCLK	3 V		10		kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at MCLK(1)	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at MCLK(2)	1.8 V to 3.6 V		4		%/V
$f_{VLO,DC}$	Duty cycle	Measured at MCLK	3 V		50%		

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

NOTE

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Table 5-6).

Table 5-7. Module Oscillator Clock (MODCLK)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{MODCLK}	MODCLK frequency	3 V	3.8	4.8	5.8	MHz
f_{MODCLK}/dT	MODCLK frequency temperature drift	3 V		0.102		%/°C
f_{MODCLK}/dV_{CC}	MODCLK frequency supply voltage drift	1.8 V to 3.6 V		1.02		%/V
$f_{MODCLK,DC}$	Duty cycle	3 V	40%	50%	60%	

5.12.4 Digital I/Os

Table 5-8. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.90		1.50	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2 V	0.50		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2 V	0.3		0.8	V
			3 V	0.4		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current (1) (2)		2 V, 3 V	–20		20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag) (3)	Ports with interrupt capability (see block diagram and terminal function descriptions)	2 V, 3 V	50			ns

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Table 5-9. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA (1)	2 V	1.4		2.0	V
		$I_{(OHmax)}$ = –5 mA (1)	3 V	2.4		3.0	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA (1)	2 V	0.0		0.60	V
		$I_{(OHmax)}$ = 5 mA (1)	3 V	0.0		0.60	
f_{Port_CLK}	Clock output frequency	C_L = 20 pF (2)	2 V	16			MHz
			3 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2 V		10		ns
			3 V		7		
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2 V		10		ns
			3 V		5		

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

5.12.4.1 Digital I/O Typical Characteristics

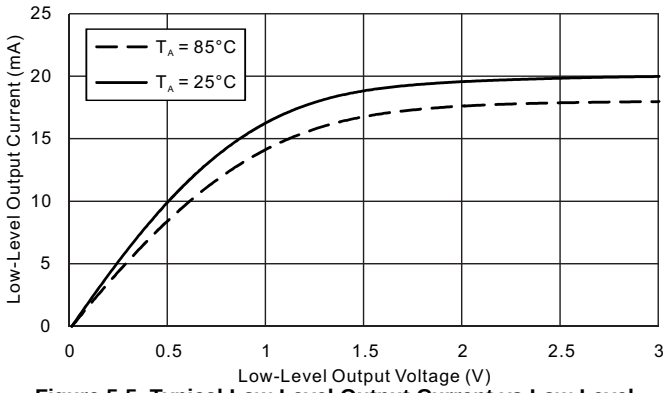


Figure 5-5. Typical Low-Level Output Current vs Low-Level Output Voltage (DVCC = 3 V)

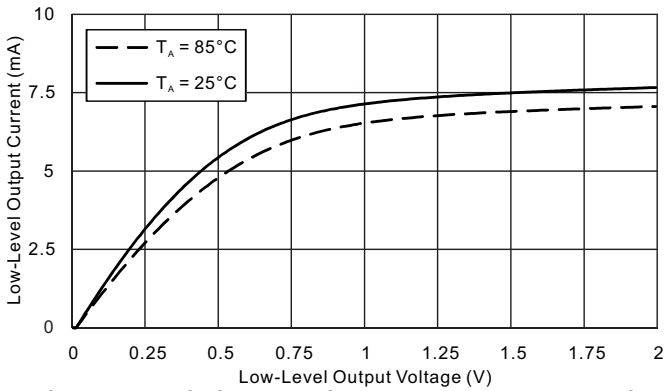


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage (DVCC = 2 V)

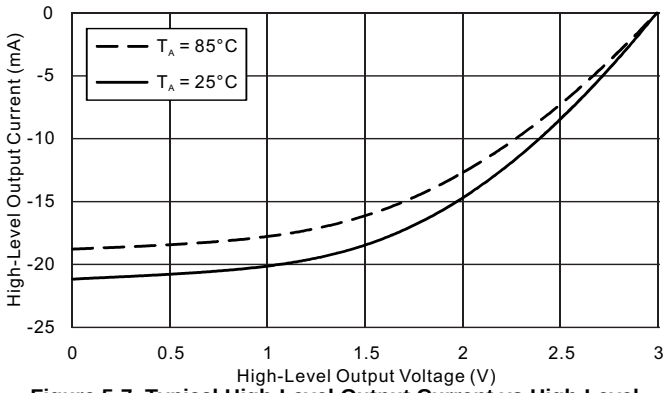


Figure 5-7. Typical High-Level Output Current vs High-Level Output Voltage (DVCC = 3 V)

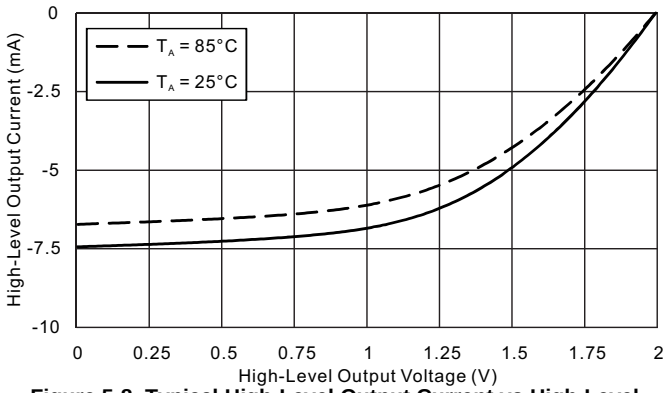


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage (DVCC = 2 V)

5.12.5 Timer_A

Table 5-10. Timer_A Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	2 V, 3 V		16	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	2 V, 3 V	20		ns

5.12.6 eUSCI

Table 5-11. eUSCI (UART Mode) Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, External: UCLK, Duty cycle = 50% ±10%	2 V, 3 V		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in Mbaud)		2 V, 3 V		5	MHz

Table 5-12. eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
t_t	UART receive deglitch time (1)	UCGLITx = 0	2 V, 3 V	12	ns
		UCGLITx = 1		40	
		UCGLITx = 2		68	
		UCGLITx = 3		110	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-13. eUSCI (SPI Master Mode) Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, Duty cycle = 50% ±10%		8	MHz

Table 5-14. eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10		1		UCxCLK cycles
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10		1		UCxCLK cycles
$t_{SU,MI}$	SOMI input data setup time		2 V	45		ns
			3 V	35		
$t_{HD,MI}$	SOMI input data hold time		2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2 V		20	ns
			3 V		20	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2 V	0		ns
			3 V	0		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-9 and Figure 5-10.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-9 and Figure 5-10.

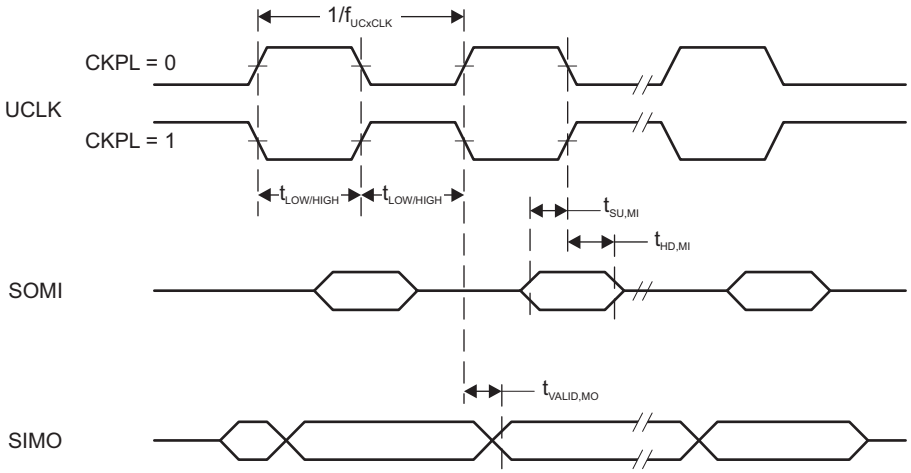


Figure 5-9. SPI Master Mode, CKPH = 0

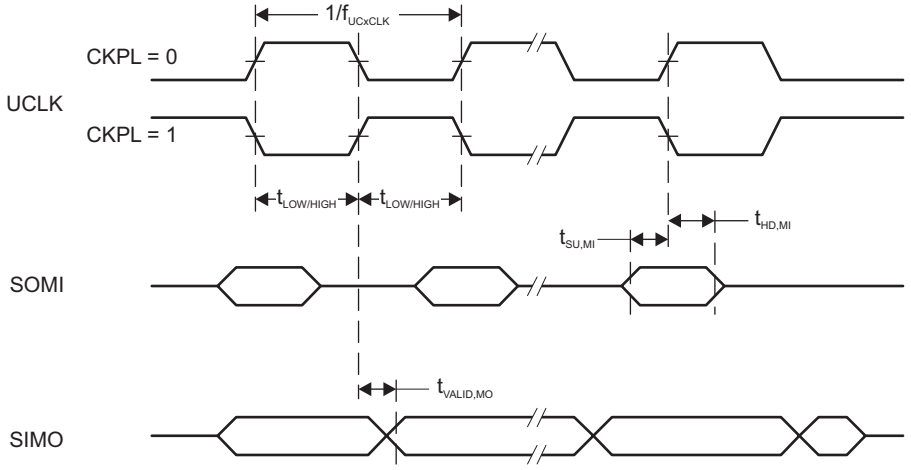


Figure 5-10. SPI Master Mode, CKPH = 1

Table 5-15. eUSCI (SPI Slave Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2 V	55		ns
			3 V	45		
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2 V	20		ns
			3 V	20		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2 V		65	ns
			3 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2 V		40	ns
			3 V		35	
$t_{SU,SI}$	SIMO input data setup time		2 V	4		ns
			3 V	4		
$t_{HD,SI}$	SIMO input data hold time		2 V	12		ns
			3 V	12		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2 V		65	ns
			3 V		40	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	2 V	5		ns
			3 V	5		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-11 and Figure 5-12.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-11 and Figure 5-12.

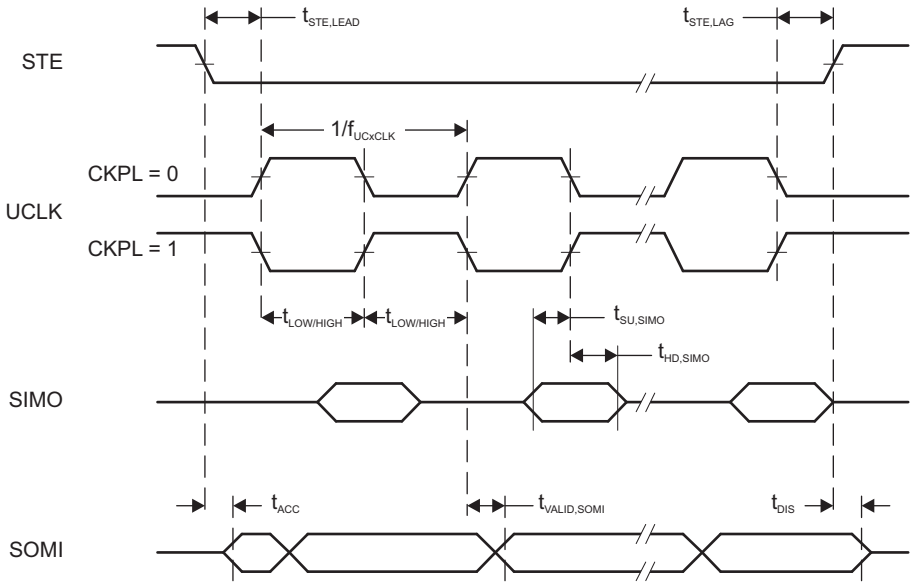


Figure 5-11. SPI Slave Mode, CKPH = 0

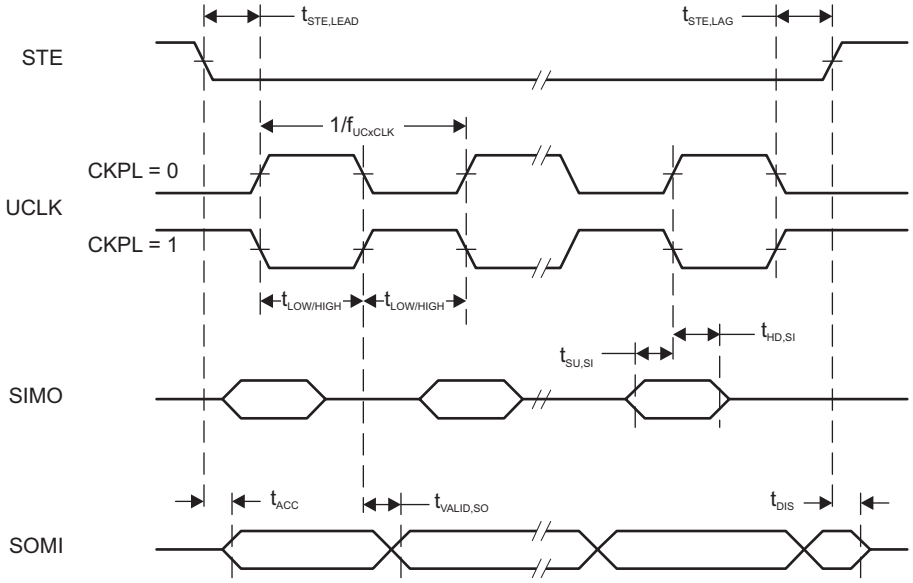


Figure 5-12. SPI Slave Mode, CKPH = 1

Table 5-16. eUSCI (I^2C Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-13)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, External: UCLK, Duty cycle = 50% ±10%				16	MHz
f_{SCL}	SCL clock frequency		2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2 V, 3 V	50		600	ns
		UCGLITx = 1		25		300	
		UCGLITx = 2		12.5		150	
		UCGLITx = 3		6.3		75	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2 V, 3 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

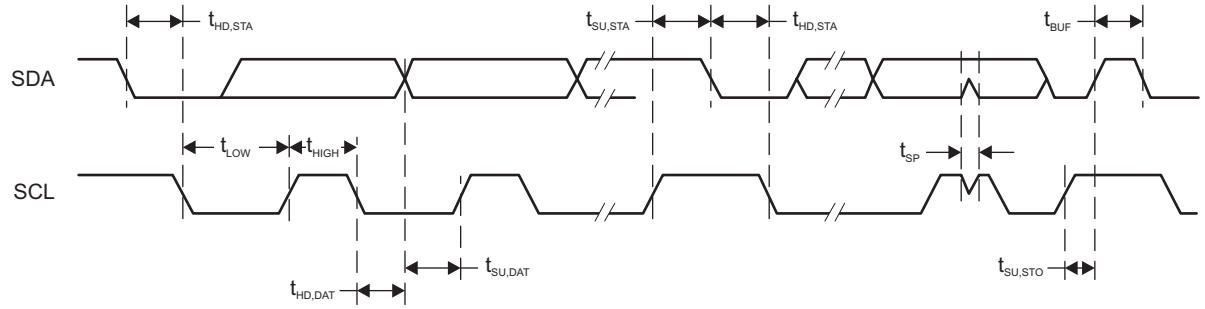


Figure 5-13. I^2C Mode Timing

5.12.7 ADC

Table 5-17. ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
DV_{CC}	ADC supply voltage			2.0		3.6	V
$V_{(Ax)}$	Analog input voltage range	All ADC pins		0		DV_{CC}	V
I_{ADC}	Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode	f_{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b	2 V		185		µA
			3 V		207		
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad	2.2 V		1.6	2.0	pF
$R_{I,MUX}$	Input MUX ON resistance	DV_{CC} = 2 V, 0 V ≤ V_{Ax} ≤ DV_{CC}				2	kΩ
$R_{I,Misc}$	Input miscellaneous resistance				34		kΩ

Table 5-18. ADC, 10-Bit Timing Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{ADCCLK}		For specified performance of ADC linearity parameters	2 V to 3.6 V	0.45	5	5.5	MHz
f_{ADCOSC}	Internal ADC oscillator (MODCLK)	ADCDIV = 0, f_{ADCCLK} = f_{ADCOSC}	2 V to 3.6 V	4.5	5.0	5.5	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f_{ADCOSC} = 4.5 MHz to 5.5 MHz	2 V to 3.6 V	2.18		2.67	µs
		External f_{ADCCLK} from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0	2 V to 3.6 V		(1)		
t_{ADCON}	Turn-on settling time of the ADC	The error in a conversion started after t_{ADCON} is less than ±0.5 LSB, Reference and input signal already settled				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I (2) = 36000 Ω, C_I = 3.5 pF, approximately 8 Tau (t) are required for an error of less than ±0.5 LSB (3)	2 V	1.5			µs
			3 V	2.0			

(1) $12 \times 1/f_{ADCCLK}$
(2) $R_I = R_{I,MUX} + R_{I,Misc}$
(3) $t_{Sample} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

Table 5-19. ADC, 10-Bit Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–2		2	LSB
	Integral linearity error (8-bit mode)		2 V to 3.6 V	–2		2	
E_D	Differential linearity error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–1		1	LSB
	Differential linearity error (8-bit mode)		2 V to 3.6 V	–1		1	
E_O	Offset error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–6.5		6.5	mV
	Offset error (8-bit mode)		2 V to 3.6 V	–6.5		6.5	
E_G	Gain error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Gain error (8-bit mode)	V_{DVCC} as reference	2 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
E_T	Total unadjusted error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Total unadjusted error (8-bit mode)	V_{DVCC} as reference	2 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
V_{SENSOR}	See (1)	ADCON = 1, INCH = 0Ch, T_A = 0°C	3 V		1.013		mV
TC_{SENSOR}	See (2)	ADCON = 1, INCH = 0Ch	3 V		3.35		mV/°C
t_{SENSOR} (sample)	Sample time required if channel 12 is selected(3)	ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, AM and all LPM above LPM3	3 V	30			µs
		ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, LPM3	3 V	100			

(1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C and 85°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, °C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.

5.12.8 FRAM

Table 5-20. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	Read and write endurance		10^{15}		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100		years
		T_J = 70°C	40		
		T_J = 85°C	10		

5.12.9 Emulation and Debug

Table 5-21. JTAG and Spy-Bi-Wire Interface Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2 V, 3 V	0		10	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2 V, 3 V	0.028		15	µs
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2 V, 3 V			110	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG (2)	2 V	0		16	MHz
		3 V	0		16	
$R_{internal}$	Internal pulldown resistance on TEST	2 V, 3 V	20	35	50	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be handled with all instructions.

6.2 Operating Modes

The MSP430 has one active mode and several software selectable low-power modes of operation. An interrupt event can wake up the device from low-power mode LPM0 or LPM3, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

Table 6-1. Operating Modes

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE	CPU OFF	STANDBY	OFF	ONLY RTC COUNTER	SHUTDOWN
Maximum System Clock		16 MHz	16 MHz	40 kHz	0	40 kHz	0
Power Consumption at 25°C, 3 V		126 µA/MHz	20 µA/MHz	1.2 µA	0.6 µA without SVS	0.77 µA with RTC only	13 nA without SVS
Wake-up time		N/A	instant	10 µs	10 µs	150 µs	150 µs
Wake-up events		N/A	All	All	I/O	RTC Counter, I/O	I/O
Power	Regulator	Full Regulation	Full Regulation	Partial Power Down	Partial Power Down	Partial Power Down	Power Down
	SVS	On	On	Optional	Optional	Optional	Optional
	Brown Out	On	On	On	On	On	On
Clock	MCLK	Active	Off	Off	Off	Off	Off
	SMCLK	Optional	Optional	Off	Off	Off	Off
	FLL	Optional	Optional	Off	Off	Off	Off
	DCO	Optional	Optional	Off	Off	Off	Off
	MODCLK	Optional	Optional	Off	Off	Off	Off
	REFO	Optional	Optional	Optional	Off	Off	Off
	ACLK	Optional	Optional	Optional	Off	Off	Off
	XT1CLK	Optional	Optional	Optional	Off	Optional	Off
	VLOCLK	Optional	Optional	Optional	Off	Optional	Off
Core	CPU	On	Off	Off	Off	Off	Off
	FRAM	On	On	Off	Off	Off	Off
	RAM	On	On	On	On	Off	Off
	Backup Memory(1)	On	On	On	On	On	Off

(1) Backup memory contains one 32-byte register in the peripheral memory space. See Table 6-31 and Table 6-49 for its memory allocation.

Table 6-1. Operating Modes (continued)

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE	CPU OFF	STANDBY	OFF	ONLY RTC COUNTER	SHUTDOWN
Peripherals	Timer0_A3	Optional	Optional	Optional	Off	Off	Off
	Timer1_A3	Optional	Optional	Optional	Off	Off	Off
	WDT	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A0	Optional	Optional	Off	Off	Off	Off
	eUSCI_B0	Optional	Optional	Off	Off	Off	Off
	CRC	Optional	Optional	Off	Off	Off	Off
	ADC	Optional	Optional	Optional	Off	Off	Off
	RTC Counter	Optional	Optional	Optional	Off	State Held	Off
I/O	General Digital Input/Output	On	Optional	State Held	State Held	Off	State Held
	Capacitive Touch I/O	Optional	Optional	Optional	Off	Off	Off

6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence

Table 6-2. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, Brownout, Supply supervisor, External reset RST, Watchdog time-out, Key violation, FRAM uncorrectable bit error detection, Software POR, FLL unlock error	SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLUNLOCKIFG	Reset	FFFEh	63, Highest
System NMI Vacant memory access, JTAG mailbox, FRAM bit error detection	VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG	Nonmaskable	FFFCh	62
User NMI External NMI, Oscillator Fault	NMIIFG OFIFG	Nonmaskable	FFFAh	61
Timer0_A3	TA0CCR0 CCIFG0	Maskable	FFF8h	60
Timer0_A3	TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)	Maskable	FFF6h	59
Timer1_A3	TA1CCR0 CCIFG0	Maskable	FFF4h	58
Timer1_A3	TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV)	Maskable	FFF2h	57
RTC Counter	RTCIFG	Maskable	FFF0h	56
Watchdog Timer Interval mode	WDTIFG	Maskable	FFEEh	55
eUSCI_A0 Receive or Transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV))	Maskable	FFECh	54

Table 6-2. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB0IV)	Maskable	FFEAh	53
ADC	ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV)	Maskable	FFE8h	52
P1	P1IFG.0 to P1IFG.7 (P1IV)	Maskable	FFE6h	51
P2	P2IFG.0 to P2IFG.7 (P2IV)	Maskable	FFE4h	50, Lowest
Reserved	Reserved	Maskable	FFE2h to FF88h	
Signatures	BSL Signature 2		0FF86h	
	BSL Signature 1		0FF84h	
	JTAG Signature 2		0FF82h	
	JTAG Signature 1		0FF80h	

6.4 Bootloader (BSL)

The BSL enables users to program the FRAM or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. Table 6-3 lists the BSL pin requirements. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 FRAM Devices Bootloader (BSL) User's Guide*.

Table 6-3. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.0	Data transmit
P1.1	Data receive
VCC	Power supply
VSS	Ground supply

6.5 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 6-4 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

Table 6-4. JTAG Pin Requirements and Function

DEVICE SIGNAL	DIRECTION	JTAG FUNCTION
P1.4/MCLK/TCK/A4/VREF+	IN	JTAG clock input
P1.5/TA0CLK/TMS/A5	IN	JTAG state control
P1.6/TA0.2/TDI/TCLK/A6	IN	JTAG data input/TCLK input
P1.7/TA0.1/TDO/A7	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6 Spy-Bi-Wire Interface (SBW)

The MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-5 shows the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

Table 6-5. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SBW FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

6.7 FRAM

The FRAM can be programmed using the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

6.8 Memory Protection

The device features memory protection that can restrict user access and enable write protection:

- Securing the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Write protection enabled to prevent unwanted write operation to FRAM contents by setting the control bits in System Configuration register 0. For more detailed information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

NOTE

The FRAM is protected by default on PUC. To write to FRAM during code execution, the application must first clear the corresponding PFWP or DFWP bit in System Configuration Register 0 to unprotect the FRAM.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.1 Power Management Module (PMM) and On-chip Reference Voltages

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as Equation 1 by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5\ V) \div 1.5\text{-}V\ Reference\ ADC\ result \quad (1)$$

A 1.2-V reference voltage can be buffered and output to P1.4/MCLK/TCK/A4/VREF+, when the ADC channel 4 is selected as the function. For more detailed information, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and on-chip asynchronous high-speed clock (MODCLK). The clock system is designed to target cost-effective designs with minimal external components. A fail-safe mechanism is designed for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): the system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODCLK can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): the subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): this clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. Table 6-6 shows the clock distribution used in this device.

Table 6-6. Clock Distribution

	CLOCK SOURCE SELECT BITS	MCLK	SMCLK	ACLK	MODCLK	XT1CLK(1)	VLOCLK	EXTERNAL PIN
Frequency Range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	5 MHz ±10%	DC to 40 kHz	10 kHz ±50%	
CPU	N/A	Default						
FRAM	N/A	Default						
RAM	N/A	Default						
CRC	N/A	Default						
I/O	N/A	Default						
TA0	TASSEL		10b	01b				00b (TA0CLK pin)
TA1	TASSEL		10b	01b				00b (TA1CLK pin)
eUSCI_A0	UCSSEL		10b or 11b		01b			00b (UCA0CLK pin)
eUSCI_B0	UCSSEL		10b or 11b		01b			00b (UCB0CLK pin)
WDT	WDTSSEL		00b	01b			10b	
ADC	ADCSSEL		10b or 11b	01b	00b			
RTC	RTCSS		01b			10b	11b	

(1) To enable XT1 functionality, configure P4SEL0.1 (XIN) and P4SEL0.2 (XOUT) before configuring the Clock System registers.

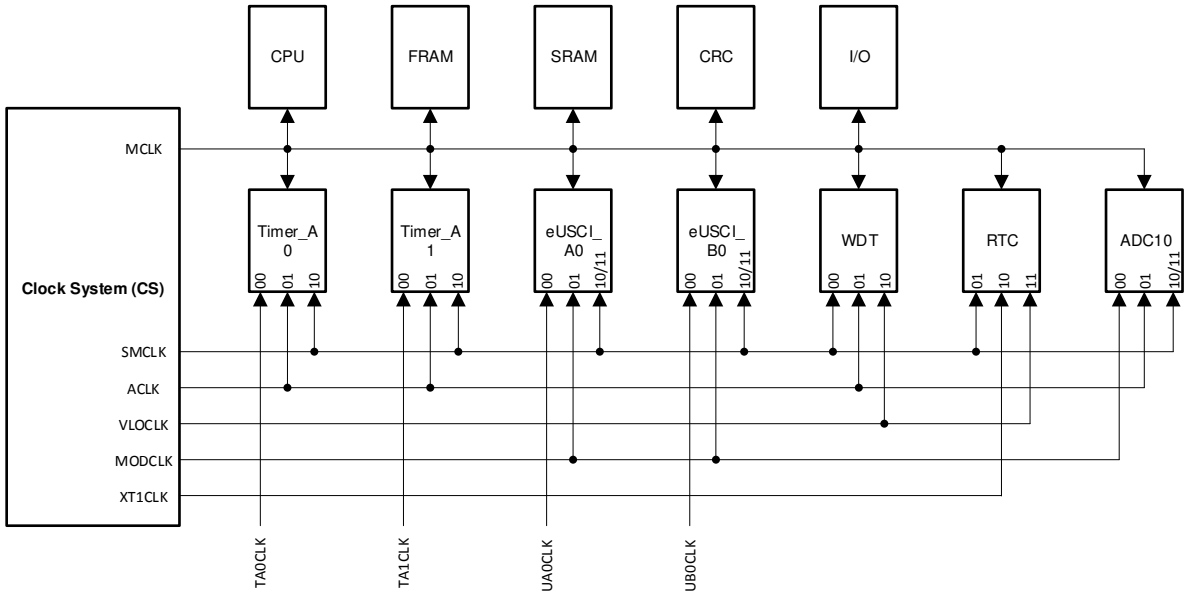


Figure 6-1. Clock Distribution Block Diagram

6.9.3 General-Purpose Input/Output Port (I/O)

There are up to 60 I/O ports implemented, depending on the package.

- P1, P2, P3, P4, P5, P6, and P7 are full 8-bit ports; P8 has 4 bits implemented.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive Touch I/O functionality is supported on all pins.

NOTE

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the *Digital I/O* chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals.

Table 6-7. WDT Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	VLOCLK

6.9.5 System Module (SYS)

The SYS module handles many of the system functions within the device. These include Power-On Reset (POR) and Power-Up Clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application.

Table 6-8. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	015Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		Reserved	22h	
		FLL unlock (PUC)	24h	
		Reserved	26h to 3Eh	Lowest

Table 6-8. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSSNIV, System NMI	015Ch	No interrupt pending	00h	
		SVS low-power reset entry	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah	
		Reserved	0Ch	
		Reserved	0Eh	
		Reserved	10h	
		VMAIFG Vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	015Ah	No interrupt pending	00h	
		NMIIFG NMI pin or SVS_H event	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h to 1Eh	Lowest

6.9.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

6.9.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or I^2C communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA.

Table 6-9. eUSCI Pin Configurations

	PIN	UART	SPI
eUSCI_A0	P1.0	TXD	SIMO
	P1.1	RXD	SOMI
	P1.2	–	SCLK
	P1.3	–	STE
	PIN	**I^2C**	**SPI**
eUSCI_B0	P5.0	–	STE
	P5.1	–	SCLK
	P5.2	SDA	SIMO
	P5.3	SCL	SOMI

6.9.8 Timers (Timer0_A3, Timer1_A3)

The Timer0_A3 and Timer1_A3 modules are 16-bit timers and counters with three capture/compare registers each. Each timer can support multiple captures or compares, PWM outputs, and interval timing. Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both TA0 and TA1 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up mode, they can be used to set the overflow value of the counter.

Table 6-10. Timer0_A3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P1.5	TA0CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	From Capacitive Touch I/O (internal)	INCLK			
		CCI0A	CCR0	TA0	
		CCI0B			Timer1_A3 CCI0B input
	DVSS	GND			
	DVCC	VCC			
P1.7	TA0.1	CCI1A	CCR1	TA1	TA0.1
	From RTC (internal)	CCI1B			Timer1_A3 CCI1B input
	DVSS	GND			
	DVCC	VCC			
P1.6	TA0.2	CCI2A	CCR2	TA2	TA0.2
	From Capacitive Touch I/O (internal)	CCI2B			Timer1_A3 INCLK Timer1_A3 CCI2B input, IR Input
	DVSS	GND			
	DVCC	VCC			

Table 6-11. Timer1_A3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P8.2	TA1CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	Timer0_A3 CCR2B output (internal)	INCLK			
		CCI0A	CCR0	TA0	
	Timer0_A3 CCR0B output (internal)	CCI0B			
	DVSS	GND			
	DVCC	VCC			
P4.0	TA1.1	CCI1A	CCR1	TA1	TA1.1
	Timer0_A3 CCR1B output (internal)	CCI1B			To ADC trigger
	DVSS	GND			
	DVCC	VCC			
P8.3	TA1.2	CCI2A	CCR2	TA2	TA1.2
	Timer0_A3 CCR2B output (internal)	CCI2B			IR Input
	DVSS	GND			
	DVCC	VCC			

The interconnection of Timer0_A3 and Timer1_A3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode. This configuration helps an application easily acquire a modulated infrared command for directly driving an external IR diode.

The IR functions are controlled by the following bits in the System Configuration 1 (SYSCFG1) register: IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data). For more information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.9 Real-Time Clock (RTC) Counter

The RTC counter is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. The RTC can periodically wake up the CPU from LPM0, LPM3, or LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0_A3 CCR1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

6.9.10 10-Bit Analog Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and four internal inputs (see Table 6-12).

Table 6-12. ADC Channel Connections

ADCINCHx	ADC CHANNELS	EXTERNAL PIN OUT
0	A0/Veref–	P1.0
1	A1/Veref+	P1.1
2	A2	P1.2
3	A3	P1.3
4	A4 (1)	P1.4
5	A5	P1.5
6	A6	P1.6
7	A7	P1.7
8	A8	P8.0 (2)
9	A9	P8.1 (2)
10	Not used	N/A
11	Not used	N/A
12	On-chip temperature sensor	N/A
13	Reference voltage (1.5 V)	N/A
14	DVSS	N/A
15	DVCC	N/A

(1) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be directly measured by A4 channel.
(2) P8.0 and P8.1 are only available in the LQFP-64 package.

The A/D conversion can be started by software or a hardware trigger. Table 6-13 shows the trigger sources that are available.

Table 6-13. ADC Trigger Signal Connections

ADCSHSx		TRIGGER SOURCE
BINARY	DECIMAL	
00	0	ADCSC bit (software trigger)
01	1	RTC event
10	2	TA1.1B
11	3	TA1.2B

6.9.11 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.9.12 Input/Output Diagrams

6.9.12.1 Port P1 Input/Output With Schmitt Trigger

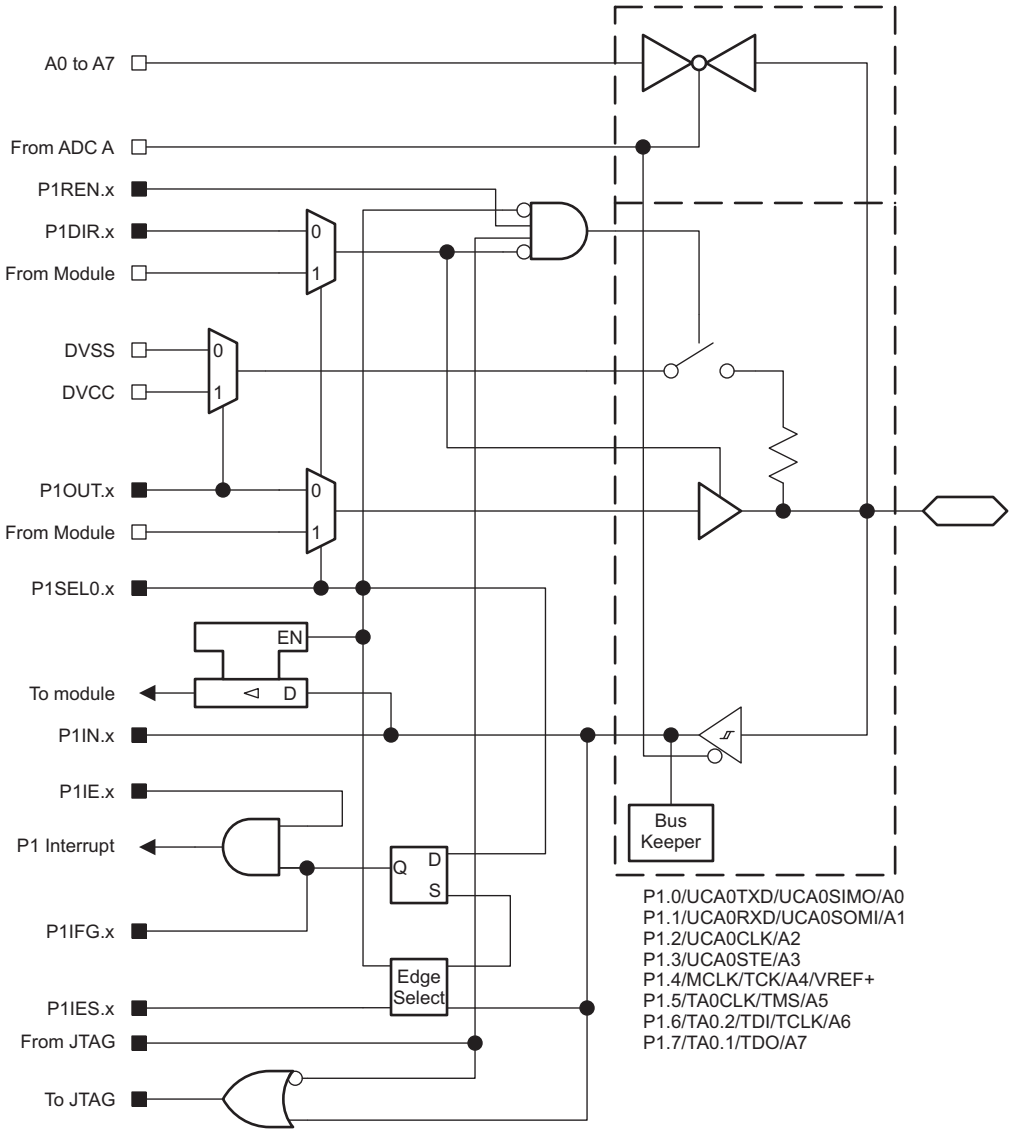


Figure 6-2. Port P1 Input/Output With Schmitt Trigger

Table 6-14. Port P1 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)			
			P1DIR.x	P1SEL0.x	ADCPCTLx(2)	JTAG
P1.0/UCA0TXD/UCA0SIMO/A0	0	P1.0 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0TXD/UCA0SIMO	X	1	0	N/A
		A0	X	X	1 (x = 0)	N/A
P1.1/UCA0RXD/UCA0SOMI/A1	1	P1.1 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0RXD/UCA0SOMI	X	1	0	N/A
		A1	X	X	1 (x = 1)	N/A
P1.2/UCA0CLK/A2	2	P1.2 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0CLK	X	1	0	N/A
		A2	X	X	1 (x = 2)	N/A
P1.3/UCA0STE/A3	3	P1.3 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0STE	X	1	0	N/A
		A3	X	X	1 (x = 3)	N/A
P1.4/MCLK/TCK/A4/VREF+	4	P1.4 (I/O)	I: 0; O: 1	0	0	Disabled
		VSS	0	1	0	Disabled
		MCLK	1			
		A4, VREF+	X	X	1 (x = 4)	Disabled
		JTAG TCK	X	X	X	TCK
P1.5/TA0CLK/TMS/A5	5	P1.5 (I/O)	I: 0; O: 1	0	0	Disabled
		TA0CLK	0	1	0	Disabled
		VSS	1			
		A5	X	X	1 (x = 5)	Disabled
		JTAG TMS	X	X	X	TMS
P1.6/TA0.2/TDI/TCLK/A6	6	P1.6 (I/O)	I: 0; O: 1	0	0	Disabled
		TA0.CCI2A	0	1	0	Disabled
		TA0.2	1			
		A6	X	X	1 (x = 6)	Disabled
		JTAG TDI/TCLK	X	X	X	TDI/TCLK
P1.7/TA0.1/TDO/A7	7	P1.7 (I/O)	I: 0; O: 1	0	0	Disabled
		TA0.CCI1A	0	1	0	Disabled
		TA0.1	1			
		A7	X	X	1 (x = 7)	Disabled
		JTAG TDO	X	X	X	TDO

(1) X = don't care
(2) Setting the ADCPCTLx bit in SYSCFG2 register disables both the output driver and the input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.12.2 Port P2 Input/Output With Schmitt Trigger

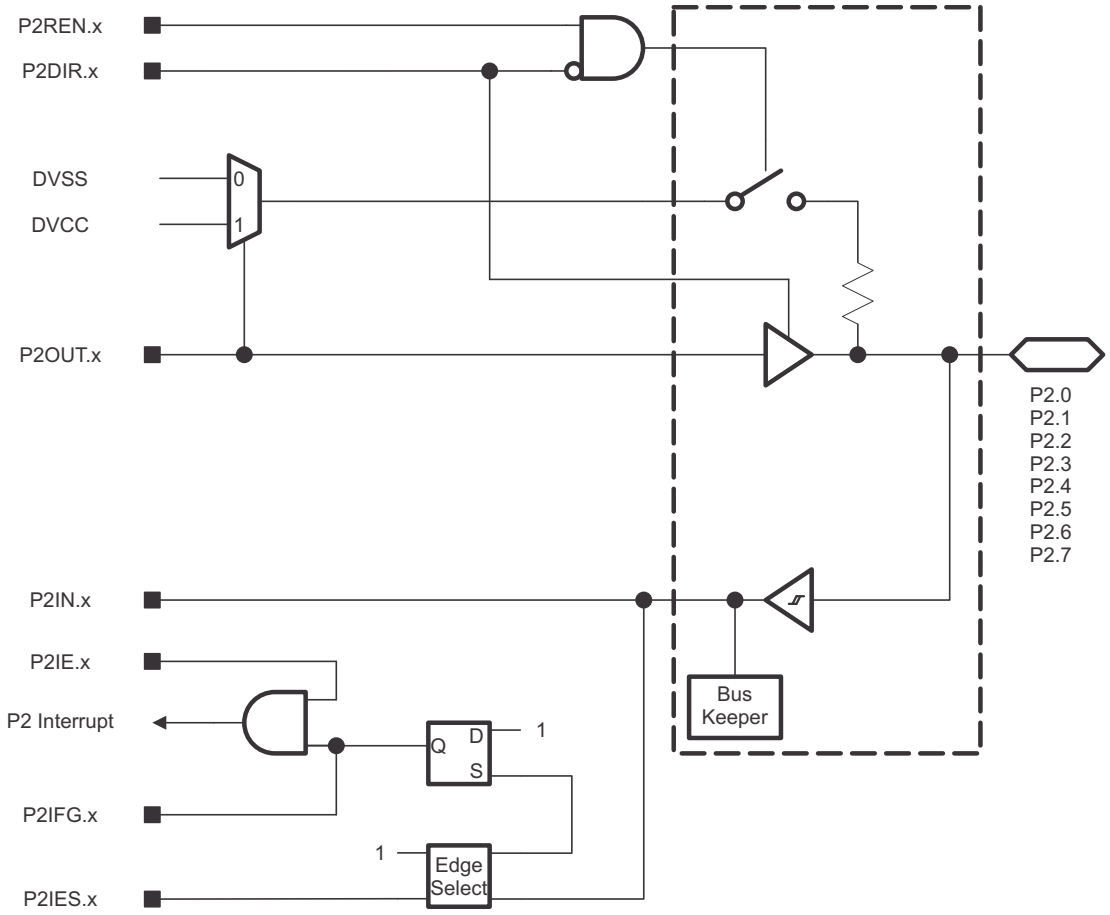


Figure 6-3. Port P2 Input/Output With Schmitt Trigger

Table 6-15. Port P2 Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P2DIR.x
P2.0	0	P2.0 (I/O)	I: 0; O: 1
P2.1	1	P2.1 (I/O)	I: 0; O: 1
P2.2	2	P2.2 (I/O)	I: 0; O: 1
P2.3	3	P2.3 (I/O)	I: 0; O: 1
P2.4	4	P2.4 (I/O)	I: 0; O: 1
P2.5	5	P2.5 (I/O)	I: 0; O: 1
P2.6	6	P2.6 (I/O)	I: 0; O: 1
P2.7	7	P2.7 (I/O)	I: 0; O: 1

6.9.12.3 Port P3 Input/Output With Schmitt Trigger

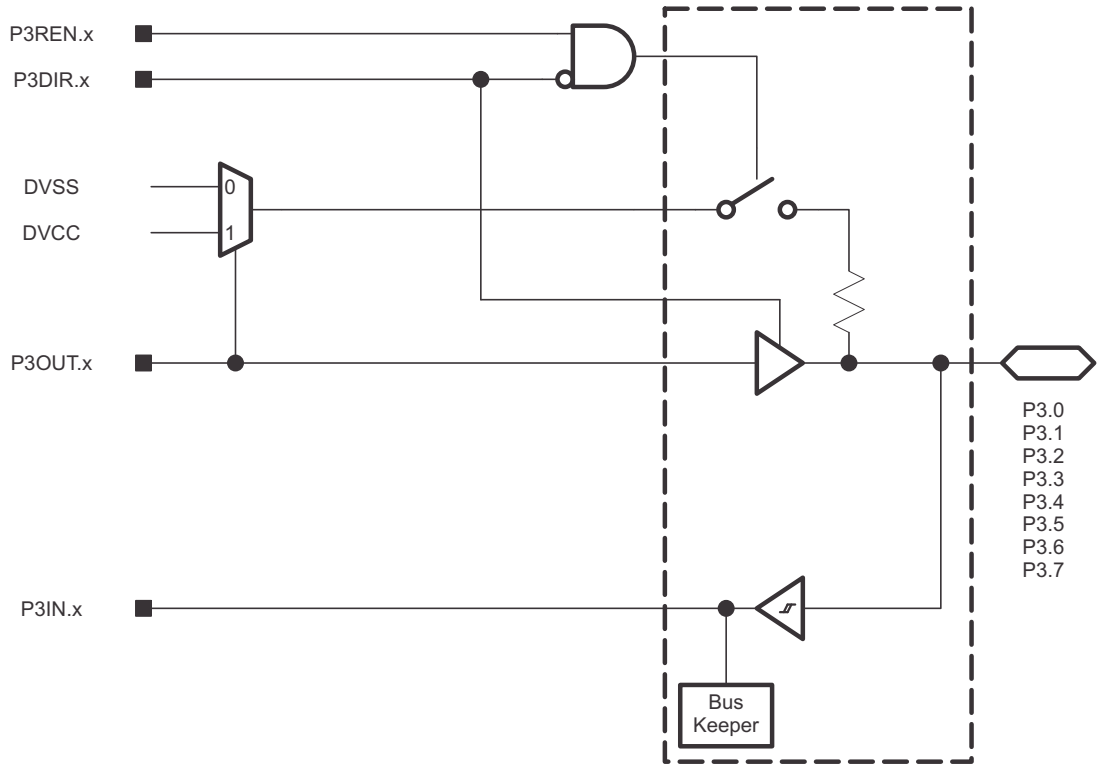


Figure 6-4. Port P3 Input/Output With Schmitt Trigger

Table 6-16. Port P3 Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P3DIR.x
P3.0	0	P3.0 (I/O)	I: 0; O: 1
P3.1	1	P3.1 (I/O)	I: 0; O: 1
P3.2	2	P3.2 (I/O)	I: 0; O: 1
P3.3	3	P3.3 (I/O)	I: 0; O: 1
P3.4	4	P3.4 (I/O)	I: 0; O: 1
P3.5	5	P3.5 (I/O)	I: 0; O: 1
P3.6	6	P3.6 (I/O)	I: 0; O: 1
P3.7	7	P3.7 (I/O)	I: 0; O: 1

6.9.12.4 Port P4.0 Input/Output With Schmitt Trigger

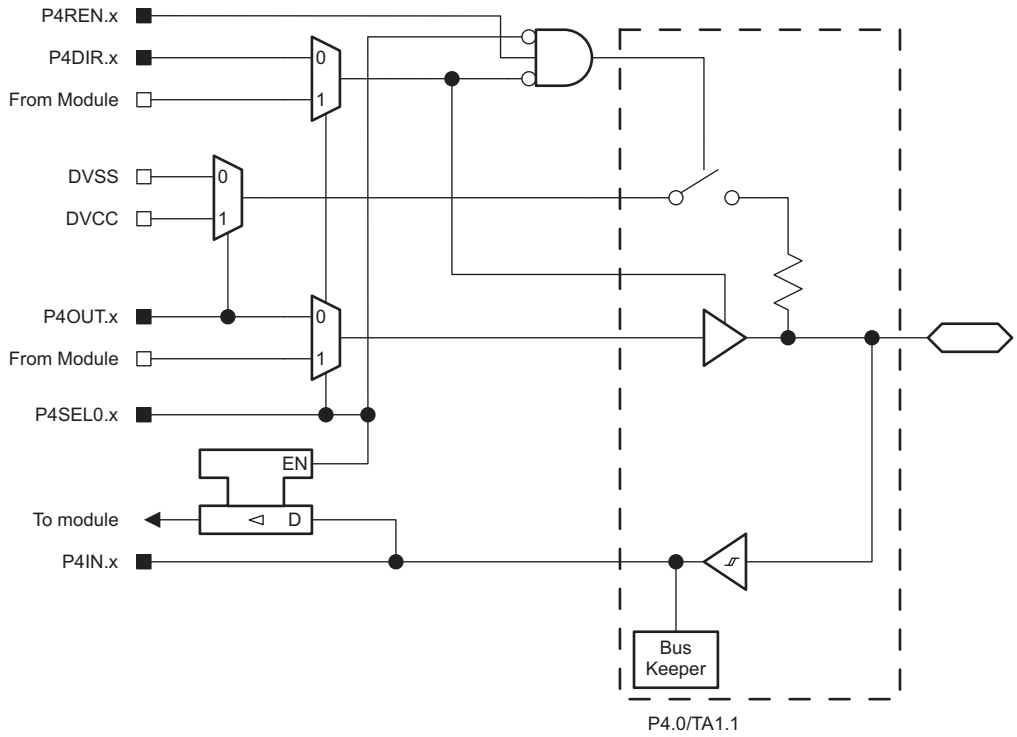


Figure 6-5. Port P4.0 Input/Output With Schmitt Trigger

Table 6-17. Port P4.0 Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS	
			P4DIR.x	P4SEL0.x
P4.0/TA1.1	0	P4.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	

6.9.12.5 Port P4.1 and P4.2 Input/Output With Schmitt Trigger

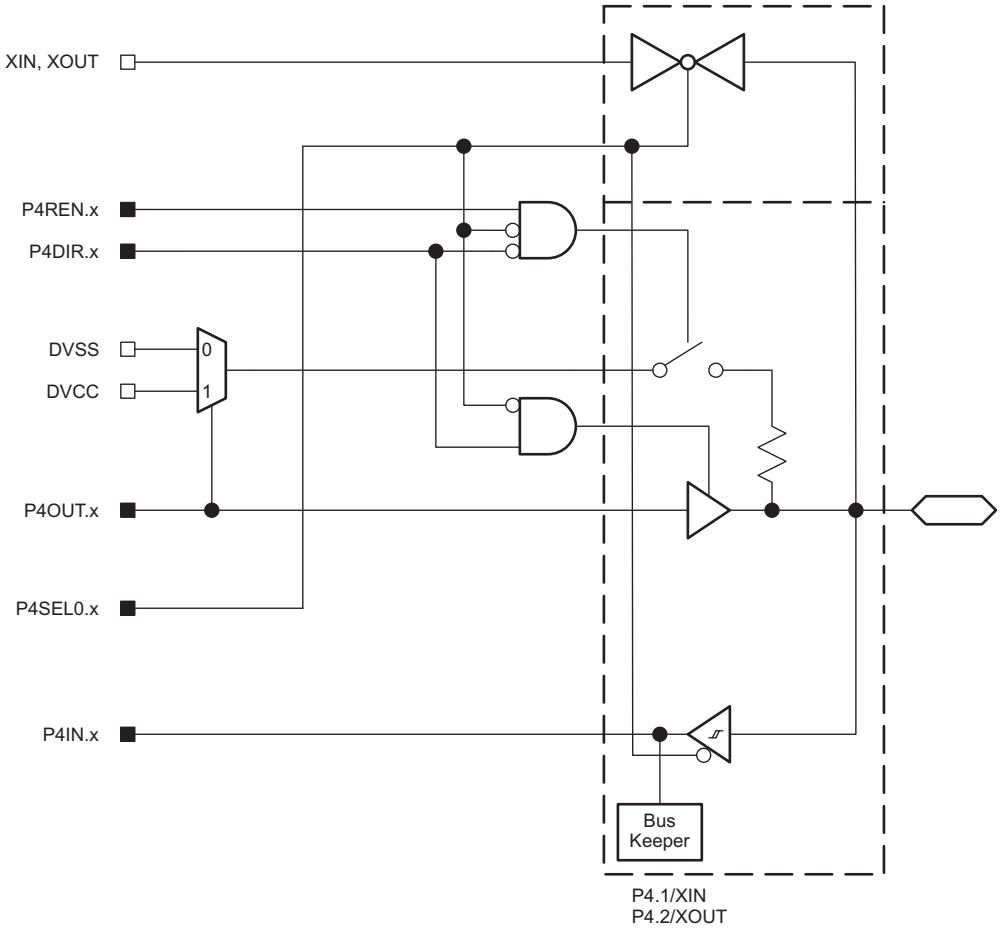


Figure 6-6. Port P4.1 and P4.2 Input/Output With Schmitt Trigger

Table 6-18. Port P4.1 and P4.2 Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P4DIR.x	P4SEL0.x
P4.1/XIN	1	P4.1 (I/O)	I: 0; O: 1	0
		XIN	X	1
P4.2/XOUT	2	P4.2 (I/O)	I: 0; O: 1	0
		XOUT	X	1

(1) X = don't care

6.9.12.6 Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

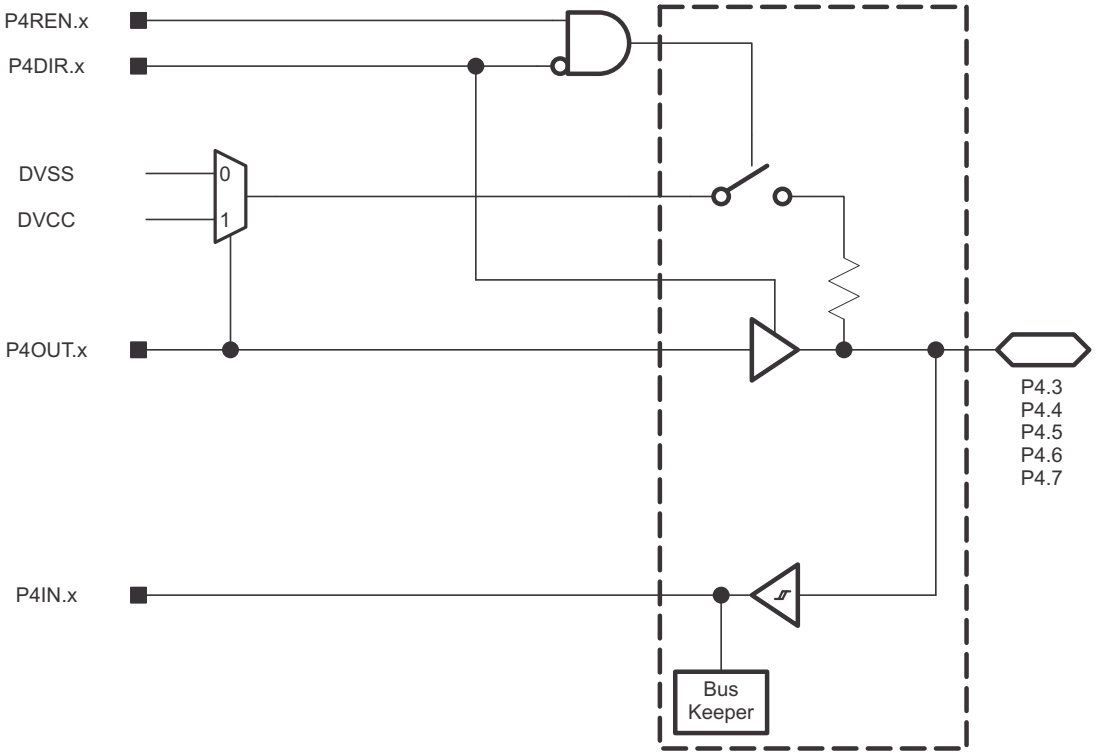


Figure 6-7. Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

Table 6-19. Port P4.3, P4.4, P4.5, P4.6, and P4.7 Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P4DIR.x
P4.3	3	P4.3 (I/O)	I: 0; O: 1
P4.4	4	P4.4 (I/O)	I: 0; O: 1
P4.5	5	P4.5 (I/O)	I: 0; O: 1
P4.6	6	P4.6 (I/O)	I: 0; O: 1
P4.7	7	P4.7 (I/O)	I: 0; O: 1

6.9.12.7 Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger

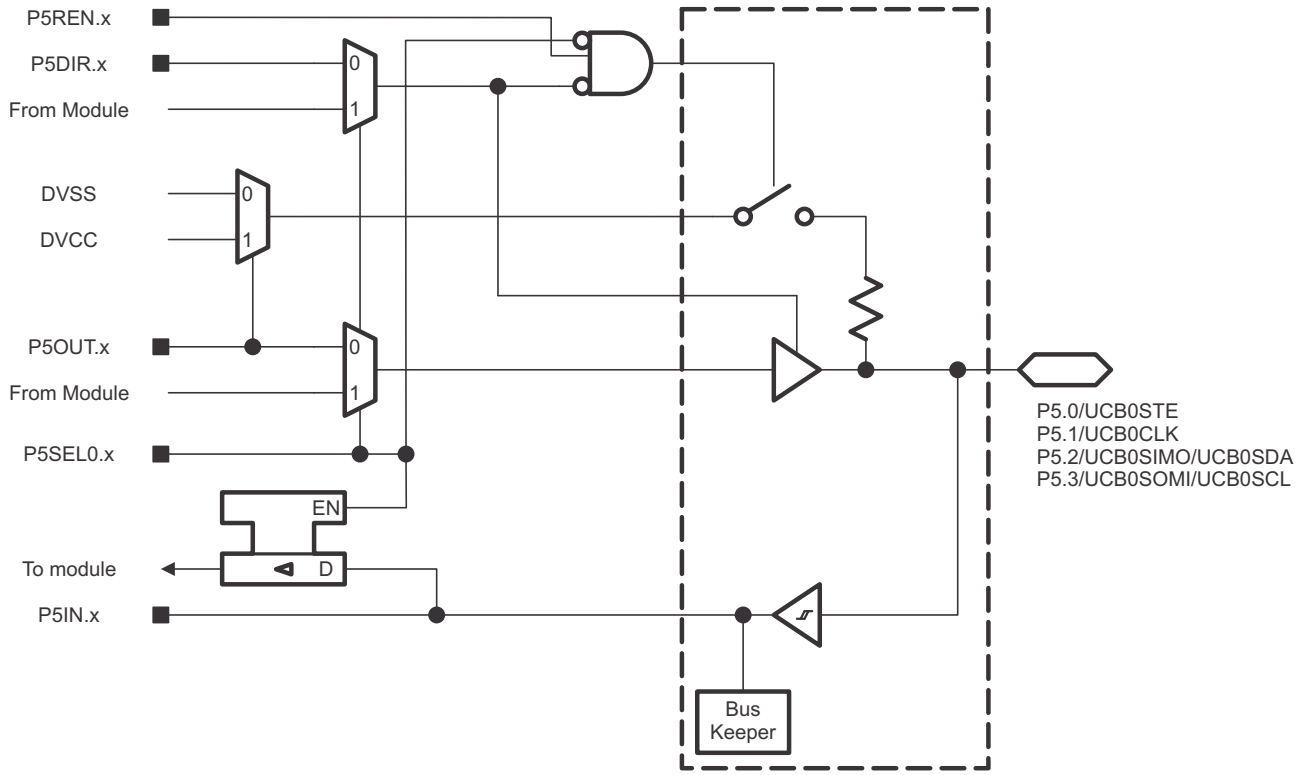


Figure 6-8. Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger

Table 6-20. Port P5.0, P5.1, P5.2, and P5.3 Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS	
			P5DIR.x	P5SEL0.x
P5.0/UCB0STE	0	P5.0 (I/O)	I: 0; O: 1	0
		UCB0STE	0	1
P5.1/UCB0CLK	1	P5.1 (I/O)	I: 0; O: 1	0
		UCB0CLK	0	1
P5.2/UCB0SIMO/UCB0SDA	2	P5.2 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA	0	1
P5.3/UCB0SOMI/UCB0SCL	3	P5.3 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL	0	1

6.9.12.8 Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger

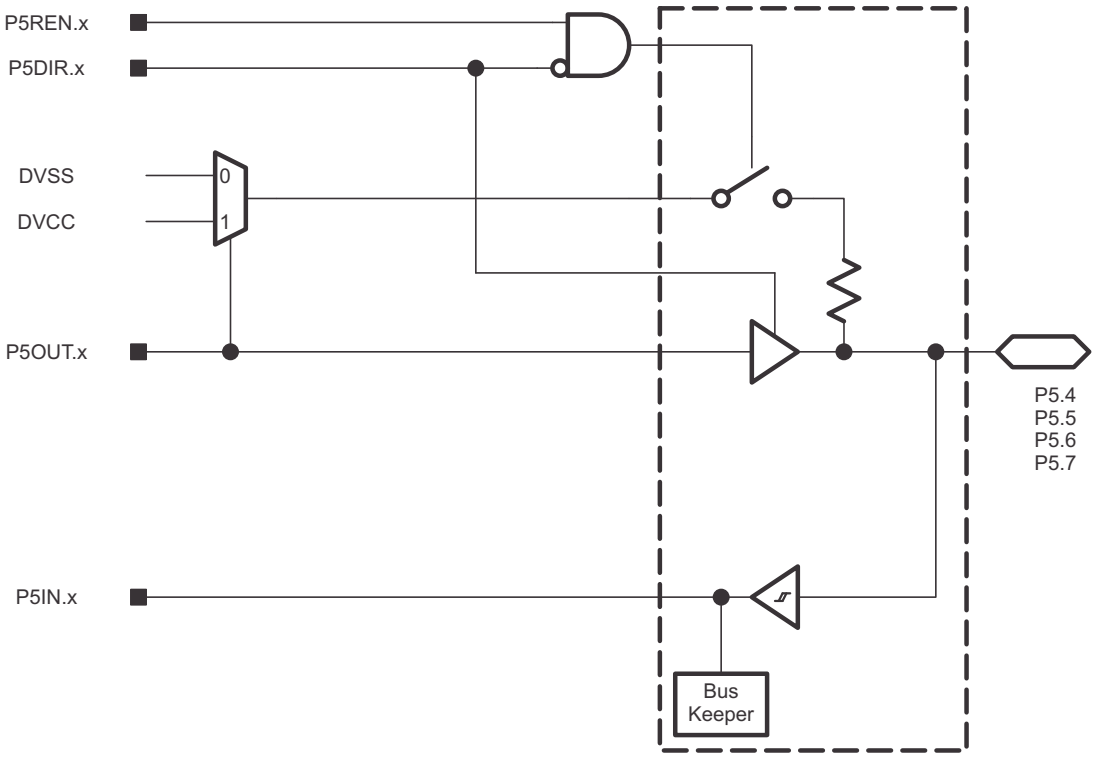


Figure 6-9. Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger

Table 6-21. Port P5.4, P5.5, P5.6, and P5.7 Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P5DIR.x
P5.4	4	P5.4 (I/O)	I: 0; O: 1
P5.5	5	P5.5 (I/O)	I: 0; O: 1
P5.6	6	P5.6 (I/O)	I: 0; O: 1
P5.7	7	P5.7 (I/O)	I: 0; O: 1

6.9.12.9 Port P6.0, P6.1, P6.2, and P6.3 Input/Output With Schmitt Trigger

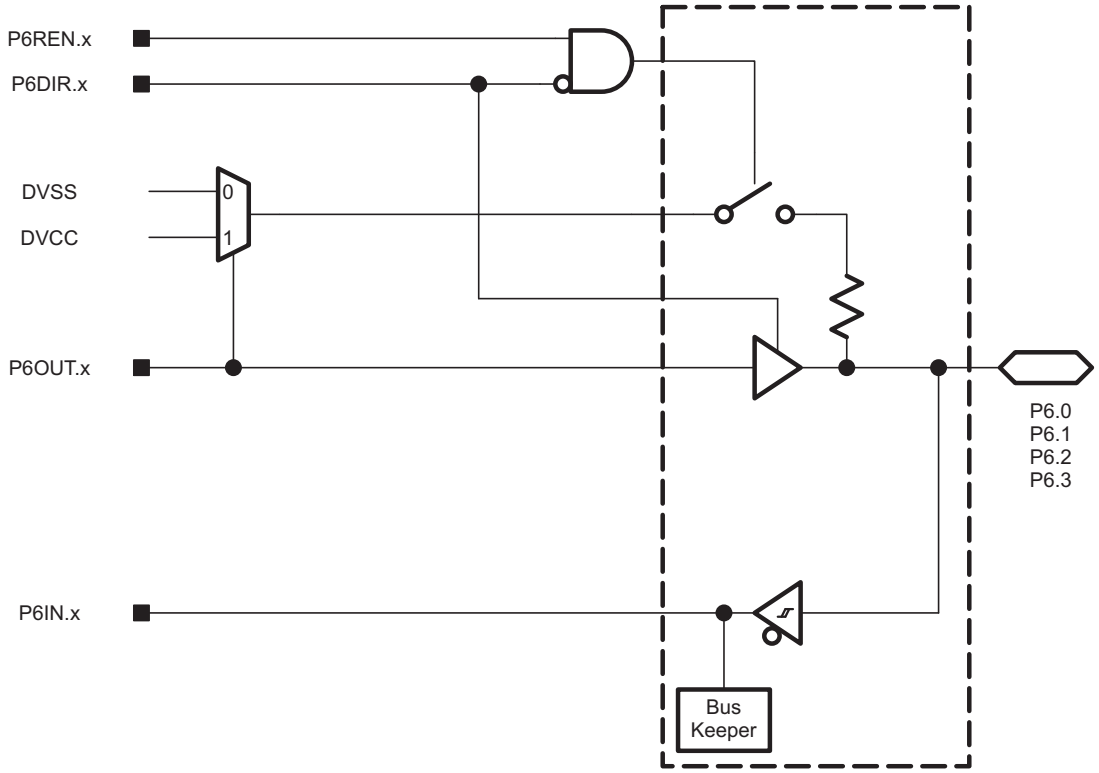


Figure 6-10. Port P6.0, P6.1, P6.2, and P6.3 Input/Output With Schmitt Trigger

Table 6-22. Port P6 Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P6DIR.x
P6.0	0	P6.0 (I/O)	I: 0; O: 1
P6.1	1	P6.1 (I/O)	I: 0; O: 1
P6.2	2	P6.2 (I/O)	I: 0; O: 1
P6.3	3	P6.3 (I/O)	I: 0; O: 1

6.9.12.10 Port P6.4, P6.5, P6.6, and P6.7 Input/Output With Schmitt Trigger

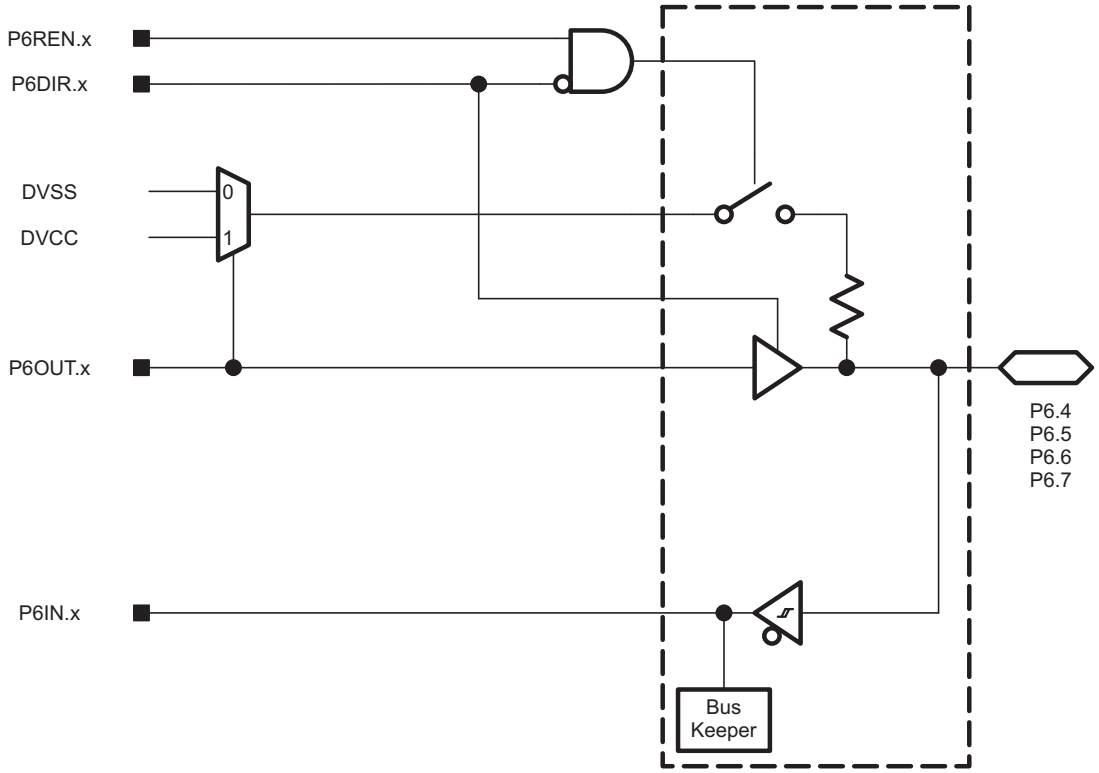


Figure 6-11. Port P6.4, P6.5, P6.6, and P6.7 Input/Output With Schmitt Trigger

Table 6-23. Port P6.4, P6.5, P6.6, and P6.7 Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P6DIR.x
P6.4	4	P6.4 (I/O)	I: 0; O: 1
P6.5	5	P6.5 (I/O)	I: 0; O: 1
P6.6	6	P6.6 (I/O)	I: 0; O: 1
P6.7	7	P6.7 (I/O)	I: 0; O: 1

6.9.12.11 Port P7.0, P7.1, P7.2, and P7.3 Input/Output With Schmitt Trigger

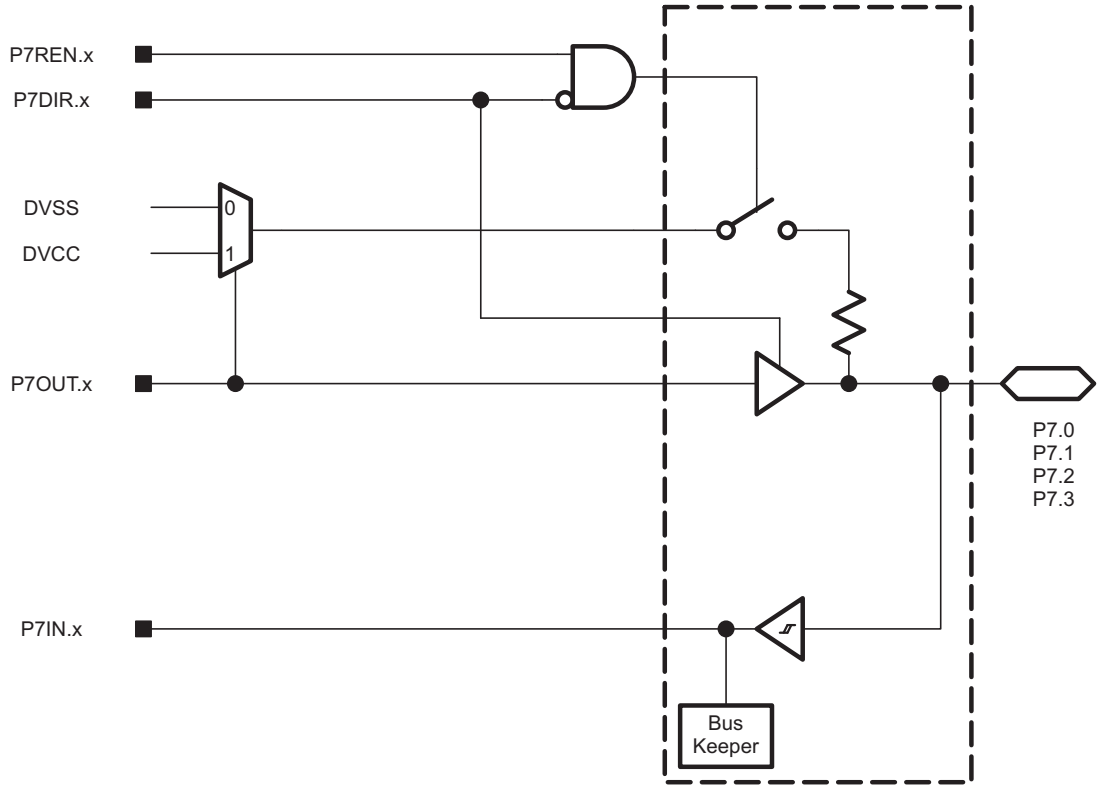


Figure 6-12. Port P7.0, P7.1, P7.2, and P7.3 Input/Output With Schmitt Trigger

Table 6-24. Port P7.0, P7.1, P7.2, and P7.3 Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P7DIR.x
P7.0	0	P7.0 (I/O)	I: 0; O: 1
P7.1	1	P7.1 (I/O)	I: 0; O: 1
P7.2	2	P7.2 (I/O)	I: 0; O: 1
P7.3	3	P7.3 (I/O)	I: 0; O: 1

6.9.12.12 Port P7.4, P7.5, P7.6, and P7.7 Input/Output With Schmitt Trigger

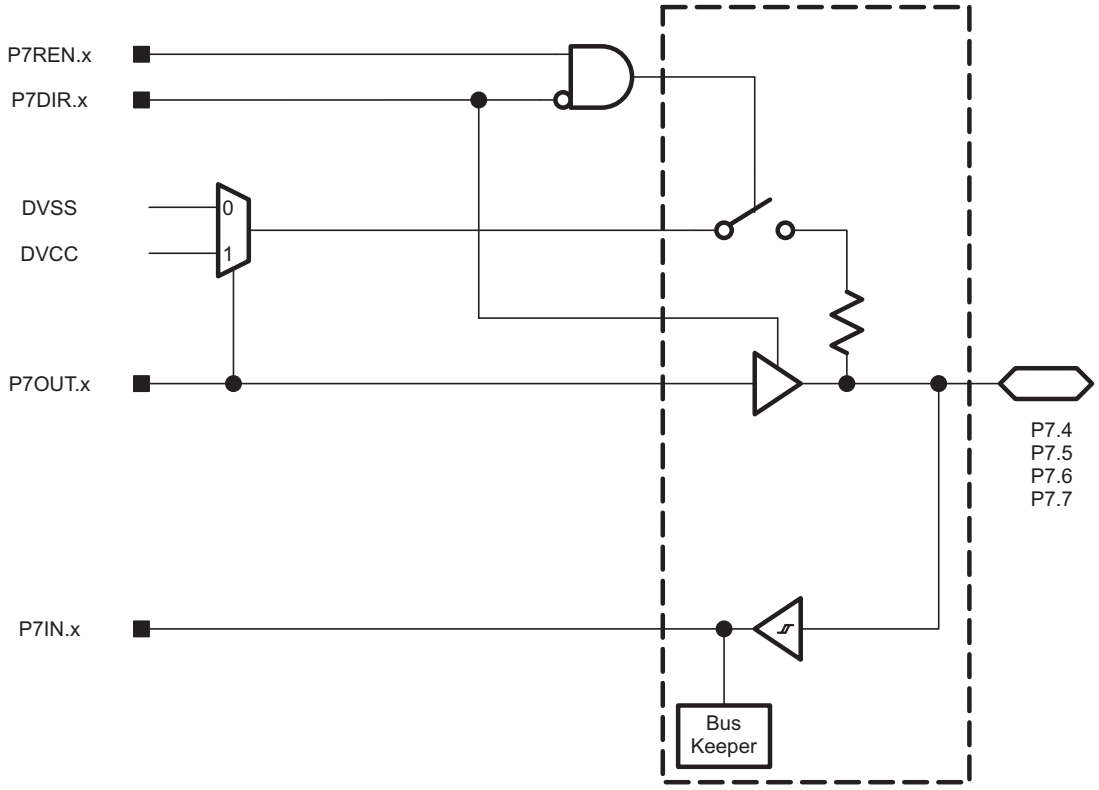


Figure 6-13. Port P7.4, P7.5, P7.6, and P7.7 Input/Output With Schmitt Trigger

Table 6-25. Port P7.4, P7.5, P7.6, and P7.7 Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS AND SIGNALS
			P7DIR.x
P7.4	4	P7.4 (I/O)	I: 0; O: 1
P7.5	5	P7.5 (I/O)	I: 0; O: 1
P7.6	6	P7.6 (I/O)	I: 0; O: 1
P7.7	7	P7.7 (I/O)	I: 0; O: 1

6.9.12.13 Port P8.0 and P8.1 Input/Output With Schmitt Trigger

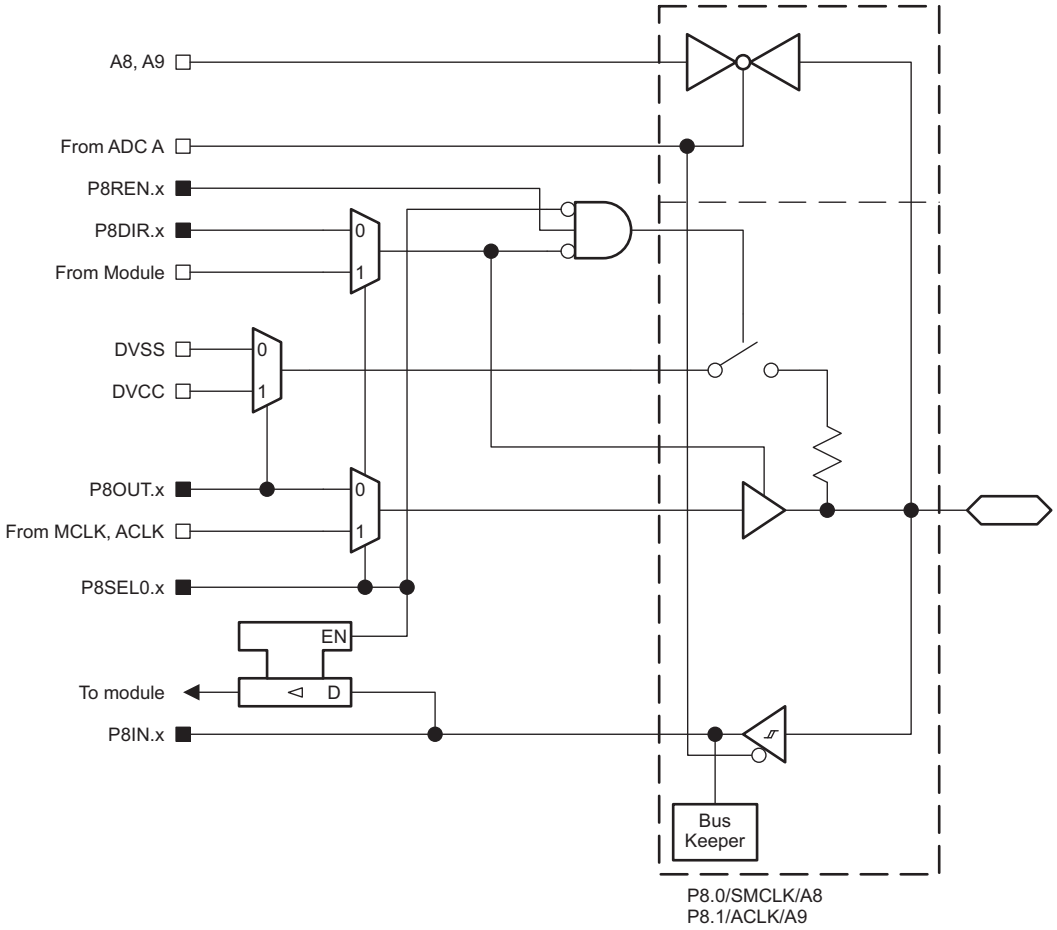


Figure 6-14. Port P8.0 and P8.1 Input/Output With Schmitt Trigger

Table 6-26. Port P8.0 and P8.1 Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P8DIR.x	P8SEL0.x	ADCPCTLx(2)
P8.0/SMCLK/A8	0	P8.0 (I/O)	I: 0; O: 1	0	0
		VSS	0	1	0
		SMCLK	1		
		A8	X	X	1 (x = 8)
P8.1/ACLK/A9	1	P8.1 (I/O)	I: 0; O: 1	0	0
		VSS	0	1	0
		ACLK	1		
		A9	X	X	1 (x = 9)

(1) X = don't care
(2) Setting the ADCPCTLx bit in SYSCFG2 register disables both the output driver and the input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.12.14 Port P8.2 and P8.3 Input/Output With Schmitt Trigger

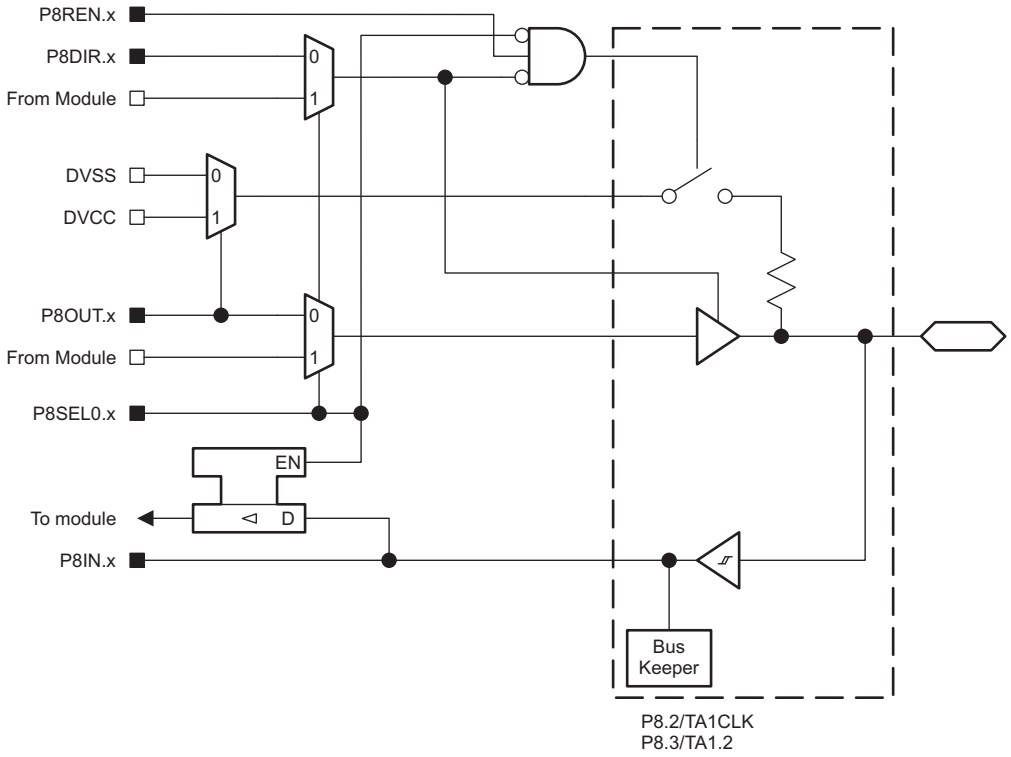


Figure 6-15. Port P8.2 and P8.3 Input/Output With Schmitt Trigger

Table 6-27. Port P8.2 and P8.3 Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS AND SIGNALS	
			P8DIR.x	P8SEL0.x
P8.2/TA1CLK	2	P8.2 (I/O)	I: 0; O: 1	0
		TA1 CLK	0	1
		VSS	1	
P8.3/TA1.2	3	P8.3 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	

6.10 Device Descriptors (TLV)

Table 6-28 lists the Device IDs of the MSP430FR203x device variants. Table 6-29 lists the contents of the device descriptor tag-length-value (TLV) structure for MSP430FR203x devices.

Table 6-28. Device IDs

DEVICE	DEVICE ID	
	1A04h	1A05h
MSP430FR2033	75h	82h
MSP430FR2032	78h	82h

Table 6-29. Device Descriptors

DESCRIPTION		MSP430FR203x	
		ADDRESS	VALUE
Information Block	Info Length	1A00h	06h
	CRC Length	1A01h	06h
	CRC Value(1)	1A02h	Per unit
		1A03h	Per unit
	Device ID	1A04h	See Table 6-28
		1A05h	
	Hardware Revision	1A06h	Per unit
	Firmware Revision	1A07h	Per unit
Die Record	Die Record Tag	1A08h	08h
	Die Record Length	1A09h	0Ah
	Lot Wafer ID	1A0Ah	Per unit
		1A0Bh	Per unit
		1A0Ch	Per unit
		1A0Dh	Per unit
	Die X Position	1A0Eh	Per unit
		1A0Fh	Per unit
	Die Y Position	1A10h	Per unit
		1A11h	Per unit
	Test Result	1A12h	Per unit
		1A13h	Per unit
ADC Calibration	ADC Calibration Tag	1A14h	11h
	ADC Calibration Length	1A15h	08h
	ADC Gain Factor	1A16h	Per unit
		1A17h	Per unit
	ADC Offset	1A18h	Per unit
		1A19h	Per unit
	ADC 1.5-V Reference Temperature Sensor 30°C	1A1Ah	Per unit
		1A1Bh	Per unit
	ADC 1.5-V Reference Temperature Sensor 85°C	1A1Ch	Per unit
		1A1Dh	Per unit

(1) The CRC value covers the checksum from 1A04h to 1A77h by applying the CRC-CCITT-16 polynomial of $x^{16} + x^{12} + x^5 + 1$.

Table 6-29. Device Descriptors (continued)

DESCRIPTION		MSP430FR203x	
		ADDRESS	VALUE
Reference and DCO Calibration	Calibration Tag	1A1Eh	12h
	Calibration Length	1A1Fh	04h
	1.5-V Reference Factor	1A20h	Per unit
		1A21h	Per unit
	DCO Tap Settings for 16 MHz, Temperature 30°C (2)	1A22h	Per unit
		1A23h	Per unit

(2) This value can be directly loaded into DCO bits in CSCTL0 register to get accurate 16-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. TI suggests using a predivider to decrease the frequency, if the temperature drift might result an overshoot beyond 16 MHz.

6.11 Memory

Table 6-30 summarizes the memory map of the MSP430FR203x devices.

Table 6-30. Memory Organization

	ACCESS	MSP430FR2033	MSP430FR2032
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Read/Write (Optional Write Protect) (1)	15KB FFFFh to FF80h FFFFh to C400h	8KB FFFFh to FF80h FFFFh to E000h
RAM	Read/Write	2KB 27FFh to 2000h	1KB 23FFh to 2000h
Information Memory (FRAM)	Read/Write (Optional Write Protect) (2)	512B 19FFh to 1800h	512B 19FFh to 1800h
Bootloader (BSL) Memory (ROM)	Read only	1KB 13FFh to 1000h	1KB 13FFh to 1000h
Peripherals	Read/Write	4KB 0FFFh to 0000h	4KB 0FFFh to 0000h

(1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details
(2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details

6.11.1 Peripheral File Map

Table 6-31 shows the base address and the memory size of the register region for each peripheral, and Table 6-32 through Table 6-50 show all of the available registers for each peripheral and their address offsets.

Table 6-31. Peripherals Summary

MODULE NAME	BASE ADDRESS	SIZE	REGISTERS
Special Functions	0100h	0010h	Table 6-32
PMM	0120h	0020h	Table 6-33
SYS	0140h	0030h	Table 6-34
CS	0180h	0020h	Table 6-35
FRAM	01A0h	0010h	Table 6-36
CRC	01C0h	0008h	Table 6-37
WDT	01CCh	0002h	Table 6-38
Port P1, P2	0200h	0020h	Table 6-39
Port P3, P4	0220h	0020h	Table 6-40
Port P5, P6	0240h	0020h	Table 6-41
Port P7, P8	0260h	0020h	Table 6-42
Capacitive Touch I/O	02E0h	0010h	Table 6-43
Timer0_A3	0300h	0030h	Table 6-44
Timer1_A3	0340h	0030h	Table 6-45
RTC	03C0h	0010h	Table 6-46
eUSCI_A0	0500h	0020h	Table 6-47
eUSCI_B0	0540h	0030h	Table 6-48
Backup Memory	0660h	0020h	Table 6-49
ADC	0700h	0040h	Table 6-50

Table 6-32. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-33. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
PMM control 2	PMMCTL2	04h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

Table 6-34. SYS Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh
System configuration 0	SYSCFG0	20h
System configuration 1	SYSCFG1	22h
System configuration 2	SYSCFG2	24h

Table 6-35. CS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control register 0	CSCTL0	00h
CS control register 1	CSCTL1	02h
CS control register 2	CSCTL2	04h
CS control register 3	CSCTL3	06h
CS control register 4	CSCTL4	08h
CS control register 5	CSCTL5	0Ah
CS control register 6	CSCTL6	0Ch
CS control register 7	CSCTL7	0Eh
CS control register 8	CSCTL8	10h

Table 6-36. FRAM Registers (Base Address: 01A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

Table 6-37. CRC Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-38. WDT Registers (Base Address: 01CCh)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-39. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pulling register enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pulling register enable	P2REN	07h
Port P2 selection 0 (1)	P2SEL0	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

(1) Port P2 selection register does not feature any valid bits. P2SEL0 presents for 16-bit Port A operation with P1SEL0.

Table 6-40. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pulling register enable	P3REN	06h
Port P3 selection 0 (1)	P3SEL0	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pulling register enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh

(1) Port P3 selection register does not feature any valid bits. P3SEL0 presents for 16-bit Port B operation with P4SEL0.

Table 6-41. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pulling register enable	P5REN	06h
Port P5 selection 0	P5SEL0	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pulling register enable	P6REN	07h
Port P6 selection 0 (1)	P6SEL0	0Bh

(1) Port P6 selection register does not feature any valid bits. P6SEL0 presents for 16-bit Port C operation with P5SEL0.

Table 6-42. Port P7, P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pulling register enable	P7REN	06h
Port P7 selection 0 (1)	P7SEL0	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 pulling register enable	P8REN	07h
Port P8 selection 0	P8SEL0	0Bh

(1) Port P7 selection register does not feature any valid bits. P7SEL0 presents for 16-bit Port D operation with P8SEL0.

Table 6-43. Capacitive Touch I/O Registers (Base Address: 02E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch I/O 0 control	CAPTIO0CTL	0Eh

Table 6-44. Timer0_A3 Registers (Base Address: 0300h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-45. Timer1_A3 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-46. RTC Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control	RTCCTL	00h
RTC interrupt vector	RTCIV	04h
RTC modulo	RTCMOD	08h
RTC counter	RTCCNT	0Ch

Table 6-47. eUSCI_A0 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI_A control word 1	UCA0CTLW1	02h
eUSCI_A control rate 0	UCA0BR0	06h
eUSCI_A control rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	lUCA0IRTCTL	12h
eUSCI_A IrDA receive control	lUCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 6-48. eUSCI_B0 Registers (Base Address: 0540h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h

Table 6-48. eUSCI_B0 Registers (Base Address: 0540h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B receive address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI_B I2C slave address	UCB0I2CSA	20h
eUSCI_B interrupt enable	UCB0IE	2Ah
eUSCI_B interrupt flags	UCB0IFG	2Ch
eUSCI_B interrupt vector word	UCB0IV	2Eh

Table 6-49. Backup Memory Registers (Base Address: 0660h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Backup Memory 0	BAKMEM0	00h
Backup Memory 1	BAKMEM1	02h
Backup Memory 2	BAKMEM2	04h
Backup Memory 3	BAKMEM3	06h
Backup Memory 4	BAKMEM4	08h
Backup Memory 5	BAKMEM5	0Ah
Backup Memory 6	BAKMEM6	0Ch
Backup Memory 7	BAKMEM7	0Eh
Backup Memory 8	BAKMEM8	10h
Backup Memory 9	BAKMEM9	12h
Backup Memory 10	BAKMEM10	14h
Backup Memory 11	BAKMEM11	16h
Backup Memory 12	BAKMEM12	18h
Backup Memory 13	BAKMEM13	1Ah
Backup Memory 14	BAKMEM14	1Ch
Backup Memory 15	BAKMEM15	1Eh

Table 6-50. ADC Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC control register 0	ADCCTL0	00h
ADC control register 1	ADCCTL1	02h
ADC control register 2	ADCCTL2	04h
ADC window comparator low threshold	ADCLO	06h
ADC window comparator high threshold	ADCHI	08h
ADC memory control register 0	ADCMCTL0	0Ah
ADC conversion memory register	ADCMEM0	12h
ADC interrupt enable	ADCIE	1Ah
ADC interrupt flags	ADCIFG	1Ch
ADC interrupt vector word	ADCIV	1Eh

6.12 Identification

6.12.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in Section 6.10.

6.12.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in Section 6.10.

6.12.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming With the JTAG Interface*.

7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430FR413x devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10-µF plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

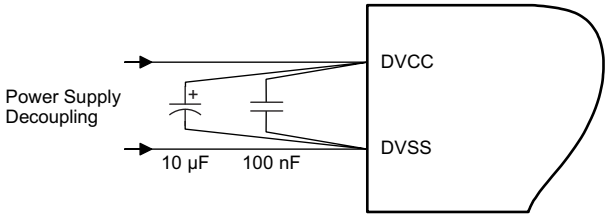


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If they are left unused, they must be terminated according to Section 4.4.

Figure 7-2 shows a typical connection diagram.

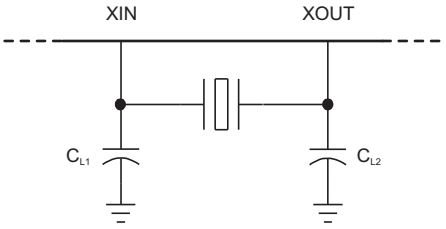


Figure 7-2. Typical Crystal Connection

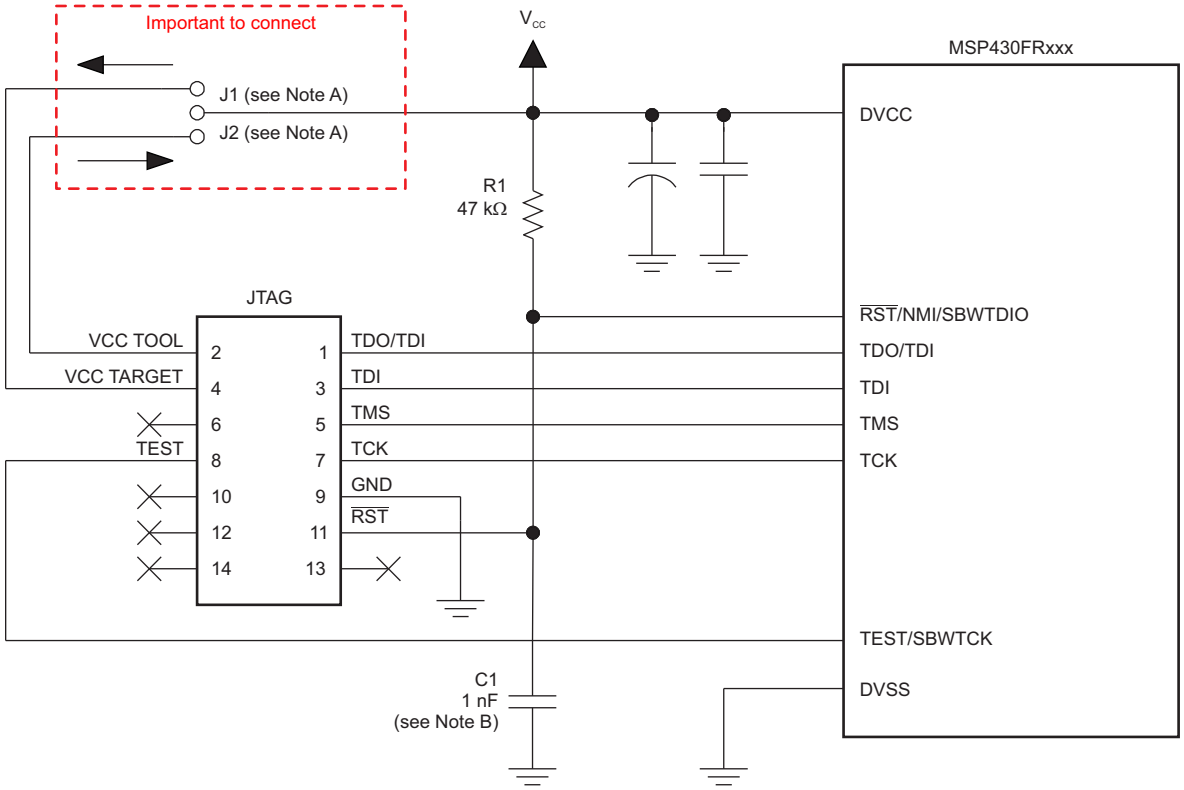
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 7-3 and Figure 7-4 show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

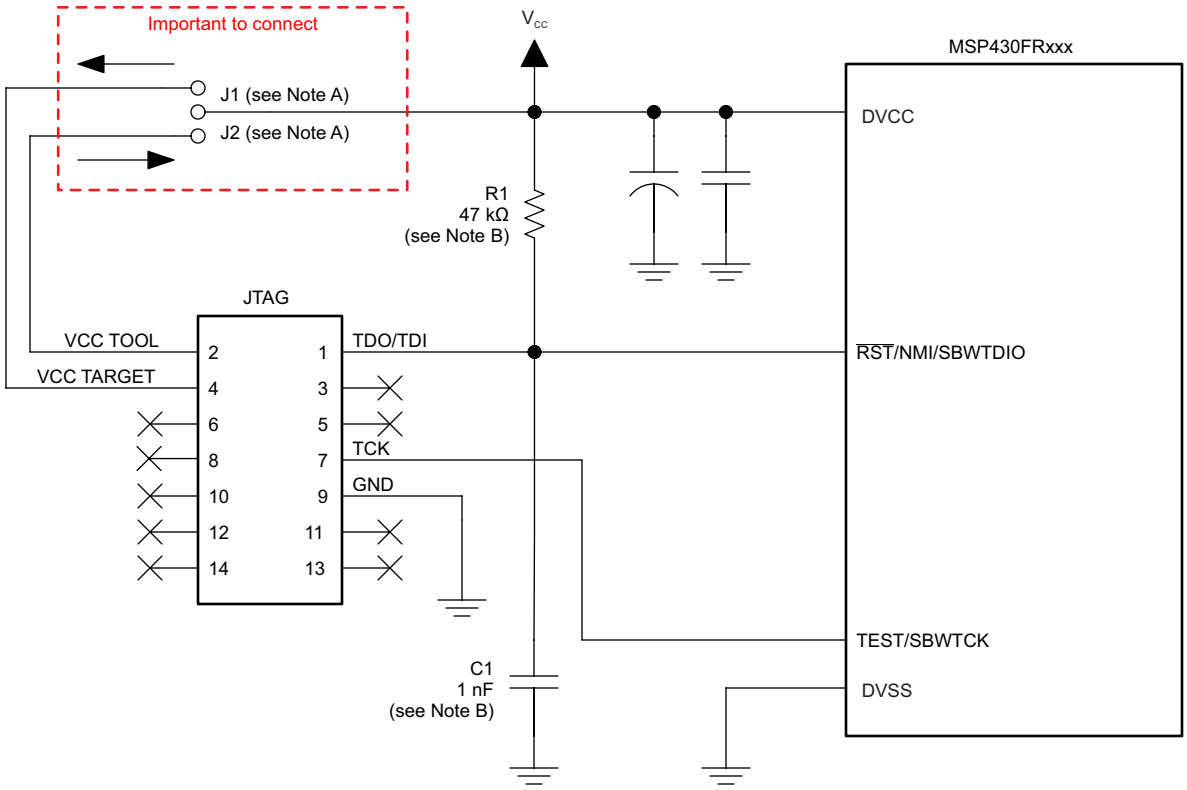
For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.



A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 1.1-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see Section 4.4.

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in Section 5.1, *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC Peripheral

7.2.1.1 Partial Schematic

Figure 7-5 shows the recommended circuit for external reference inputs to the ADC.

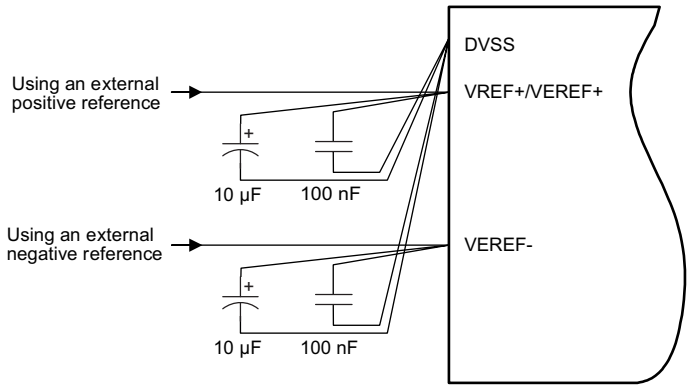


Figure 7-5. ADC Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 7.1.1 combined with the connections shown in Section 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A bypass capacitor of 100 nF is used to filter out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 7-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

8 デバイスおよびドキュメントのサポート

8.1 はじめに

MSP430 ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「MSP430™ 超低消費電力センシング / 測定マイコン - 概要」を参照してください。

8.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

XMS - 実験段階のデバイスで、最終的なデバイスの電気的仕様を表しているとは限りません。

MSP - 完全に認定済みの量産版デバイスです。

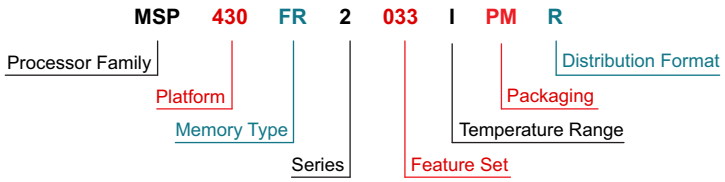
XMSデバイスは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方をに示します。



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon	
Platform	430 = TI's 16-Bit MSP430 Low-Power Microcontroller Platform	
Memory Type	FR = FRAM	
Series	2 = FRAM 2 series up to 16 MHz without LCD	
Feature Set	**First and Second Digits: ADC Channels / 16-bit Timers / I/Os** 03 = Up to 10 / 3 / Up to 60	**Third Digit: FRAM (KB) / SRAM (KB)** 3 = 16 / 2 2 = 8 / 1
Temperature Range	I = –40°C to 85°C	
Packaging	http://www.ti.com/packaging	
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray	

図 8-1. デバイスの項目表記

8.3 ツールとソフトウェア

MSP430FR203x マイクロコントローラでサポートされるデバッグ機能を表 8-1 に示します。利用可能な機能の詳細については、『Code Composer Studio™ IDE v8.x for MSP430™ MCUs』ユーザー・ガイド (英語) を参照してください。

表 8-1. ハードウェアの特長

MSP430のアーキテクチャ	4線式JTAG	2線式JTAG	ブレーク・ポイント (N)	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMX.5デバッグ・サポート
MSP430Xv2	○	○	3	○	○	×	×	×

設計キットと評価基板

MSP430FR4133 LaunchPad開発キット

MSP-EXP430FR4133 LaunchPad開発キットは、MSP430FR4133マイクロコントローラ用の使いやすい評価基板(EVM)です。プログラミング、デバッグ、電力測定を行うためのオンボード・エミュレーションなど、超低消費電力(ULP)のMSP430 FRAM搭載マイクロコントローラ(MCU)プラットフォームの開発に必要なすべての機能を備えています。

MSP430FR2x/4x MCU用のMSP-TS430PM64Dターゲット開発ボード

MSP-TS430PM64D はスタンドアロンの 64 ピン ZIF ソケット・ターゲット・ボードで、これによりJTAGインターフェイスまたはSpy Bi-Wire (2線式JTAG)プロトコルを使用してMSP430 MCUをインシステムでプログラミングおよびデバッグできます。

MSP430FR2x/4x MCU用のMSP-FET430U64Dターゲット開発ボード(64ピン)とMSP-FETプログラマ・バンドル

MSP-FET430U64DはMSP-FETエミュレータとMSP-TS430PM64D 64ピンZIFソケット・ターゲット・ボードを含むバンドルで、これによりJTAGインターフェイスまたはSpy Bi-Wire (2線式JTAG)プロトコルを使用してMSP430 MCUをインシステムでプログラミングおよびデバッグできます。

ソフトウェア

MSP430Ware™ソフトウェア

MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存の MSP430 MCU 設計リソースの完全なコレクションに加えて、MSP430Ware ソフトウェアには、MSP ドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430Wareソフトウェアは CCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

MSP430FR413x/MSP430FR203xのサンプル・コード

すべてのMSPデバイス用に、内蔵する各ペリフェラルをさまざまな用途のニーズに合わせて構成するためのCコード・サンプルが用意されています。

MSP超低消費電力マイクロコントローラ用FRAM組み込みソフトウェア・ユーティリティ

TI FRAMユーティリティ・ソフトウェアは、組み込みソフトウェア・ユーティリティのコレクションとして成長するように設計されており、超低消費電力と、ほぼ無限のFRAM書き込み耐性を活用できます。このユーティリティは MSP430FRxx FRAMマイクロコントローラで利用でき、アプリケーション開発を始めるために役立つコード例が用意されています。

MSP430 Touch Pro GUI

MSP430 Touch Pro Tool は、静電容量式タッチ・ボタン、スライダ、およびホイールの設計を検証するために使用できる、PCベースのツールです。このツールでは、CapTouchセンサ・データを受信して視覚化することで、ユーザーはボタン、スライダ、およびホイールの設計を迅速かつ簡単に評価、診断、およびチューニングできるようになります。

MSP430 Touch Power Designer GUI

MSP430 Capacitive Touch Power Designerを使用すると、与えられたMSP430容量性タッチ・システムの平均消費電流の推定値を計算できます。動作電圧、周波数、ボタン数、ボタン・ゲート時間といったシステム・パラメータを入力することで、特定のデバイス・ファミリの特定の静電容量式タッチ構成の消費電力を数分で推定できます。

MSPマイクロコントローラ用のデジタル信号処理(DSP)ライブラリ

TIのデジタル信号処理ライブラリは、MSP430およびMSP432マイクロコントローラで固定小数点数に対して多くの一般的な信号処理操作を実行するための、高度に最適化された関数のセットです。この関数セットは一般に、高い処理能力を必要とする変換を最小の消費電力、超高精度、リアルタイムで実行するアプリケーション向けに使用されます。このライブラリは、MSP固有のハードウェアを最適に使用して固定小数点演算を行い、大幅な性能向上を実現します。

MSP ドライバ・ライブラリ

MSPドライバ・ライブラリの抽象化されたAPIには、使いやすい関数呼び出しが含まれているため、MSP430ハードウェアのビットやバイトを直接操作する煩雑さから解放されます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTraceテクノロジ

MSP430 マイコン向け EnergyTrace テクノロジはエネルギー・ベースのコード分析ツールで、アプリケーションのエネルギー・プロファイルの測定と表示を行うとともに、消費電力の大幅な低減のための最適化も可能です。

ULP (超低消費電力) Advisor

ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラの超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorはマイクロコントローラに熟練した開発者と、新しい開発者の両方を対象としており、包括的なULPチェックリストを使用してコードをチェックし、アプリケーションのエネルギー消費を最小化するため役立ちます。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

MSP 用の固定小数点算術ライブラリ

MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

MSP430用の浮動小数点算術ライブラリ

低消費電力で低コストのマイクロコントローラ分野にさらなる革新を引き起こすため、TIはMSPMATHLIBを提供します。この浮動小数点算術ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、標準のMSP430算術関数よりも最高で26倍も高速なスカラー関数です。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio IDEとIAR Embedded Workbench IDEの両方に組み込まれています。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境

Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。CCSには、最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。

コマンドライン・プログラマ

MSP Flasher は、FET プログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

MSP MCU プログラマおよびデバッガ

MSP-FETは強力なエミュレーション開発ツールで、多くの場合にデバッグ・プローブと呼ばれます。ユーザーはこのツールを使用して、MSP低消費電力MCUのアプリケーション開発をすぐに始めることができます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。

MSP-GANG量産プログラマ

MSP Gang プログラマは MSP430 または MSP432 用のデバイス・プログラマで、8つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang プログラマは、標準の RS-232 または USB 接続を使用してホスト PC と接続し、柔軟なプログラミング・オプションが用意されているため、ユーザーはプロセスを完全にカスタマイズ可能です。

8.4 ドキュメントのサポート

以下のドキュメントはMSP430FR203xマイクロコントローラについて記載したものです。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでご利用の製品のフォルダへ移動します(製品フォルダへのリンクについては、 8.5を参照してください)。右上の「アラートを受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430FR2033 デバイス正誤表』

このデバイスにおけるすべてのシリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

『MSP430FR2032 デバイス正誤表』

このデバイスにおけるすべてのシリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

ユーザー・ガイド

『MSP430FR4xxおよびMSP430FR2xxファミリ ユーザー・ガイド』

このデバイス・ファミリで利用可能なすべてのモジュールとペリフェラルについての詳細情報です。

『MSP430 FRAMデバイス・ブートローダ(BSL) ユーザー・ガイド』

MSP430 MCUに搭載されたブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430 MCUの組み込みメモリと通信できます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。

『JTAGインターフェイスによるMSP430のプログラミング』

このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』

このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

アプリケーション・レポート

『MSP430 FRAMテクノロジ - ハウツーとベスト・プラクティス』

FRAMは不揮発性メモリ・テクノロジで、SRAMと同様に動作し、多くの新しいアプリケーションを可能にすると同時に、ファームウェアの設計方法に変革をもたらすものです。このアプリケーション・レポートでは、組み込みソフトウェア開発の観点から、MSP430のFRAMテクノロジを使用する方法と、そのベスト・プラクティスについて概説しています。特定用途向けのコード、定数、データ容量の制限、FRAMの使用に従って、アプリケーションのエネルギー消費を最適化するようメモリ・レイアウトを実装する方法について解説します。

『MSP430 32kHz水晶発振器』

適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430 システム・レベルESDの考慮事項』

シリコン・テクノロジのスケーリングによる低電圧化の進行と、コスト効率の優れた超低消費電力コンポーネントを設計する必要性の高まりにより、システム・レベルの ESD の要求はますます高まっています。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。

8.5 関連リンク

表 8-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430FR2033	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR2032	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 商標

MSP430, MSP430Ware, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

8.8 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

8.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR2032IG48	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2032	Samples
MSP430FR2032IG48R	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2032	Samples
MSP430FR2032IG56	ACTIVE	TSSOP	DGG	56	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2032	Samples
MSP430FR2032IG56R	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2032	Samples
MSP430FR2032IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2032	Samples
MSP430FR2033IG48	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2033	Samples
MSP430FR2033IG48R	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2033	Samples
MSP430FR2033IG56	ACTIVE	TSSOP	DGG	56	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2033	Samples
MSP430FR2033IG56R	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2033	Samples
MSP430FR2033IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2033	Samples
MSP430FR2033IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR2033	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

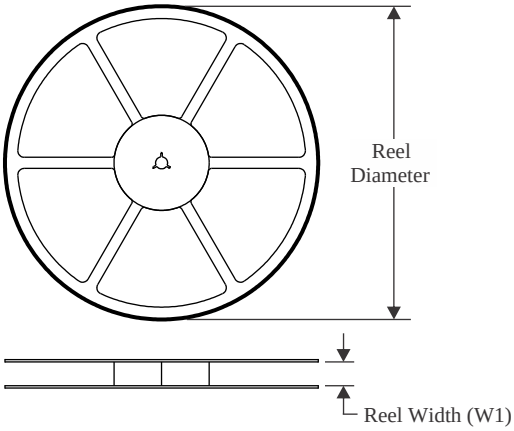
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

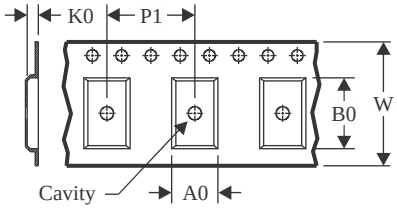
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

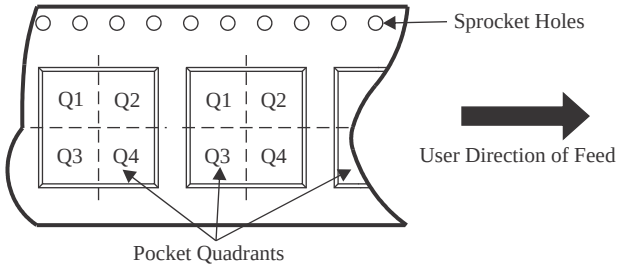


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

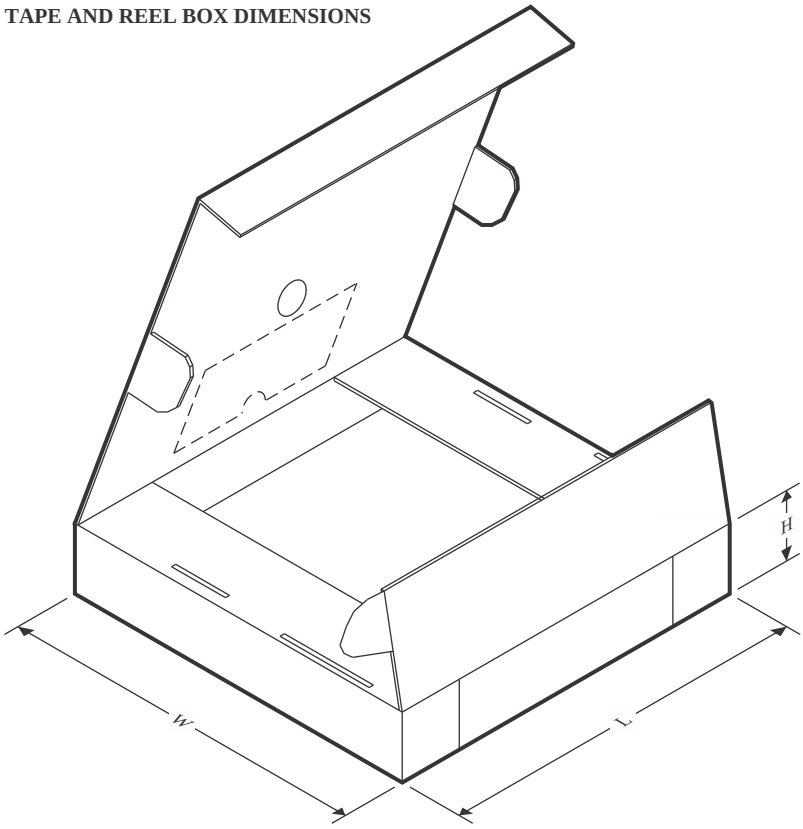
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR2032IG48R	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR2032IG56R	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
MSP430FR2032IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR2033IG48R	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR2033IG56R	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
MSP430FR2033IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

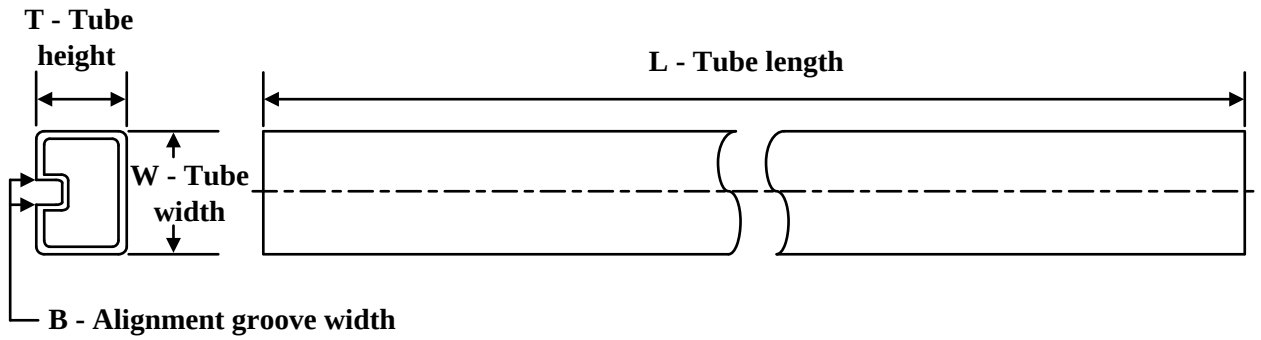
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR2032IG48R	TSSOP	DGG	48	2000	350.0	350.0	43.0
MSP430FR2032IG56R	TSSOP	DGG	56	2000	350.0	350.0	43.0
MSP430FR2032IPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430FR2033IG48R	TSSOP	DGG	48	2000	350.0	350.0	43.0
MSP430FR2033IG56R	TSSOP	DGG	56	2000	350.0	350.0	43.0
MSP430FR2033IPMR	LQFP	PM	64	1000	350.0	350.0	43.0

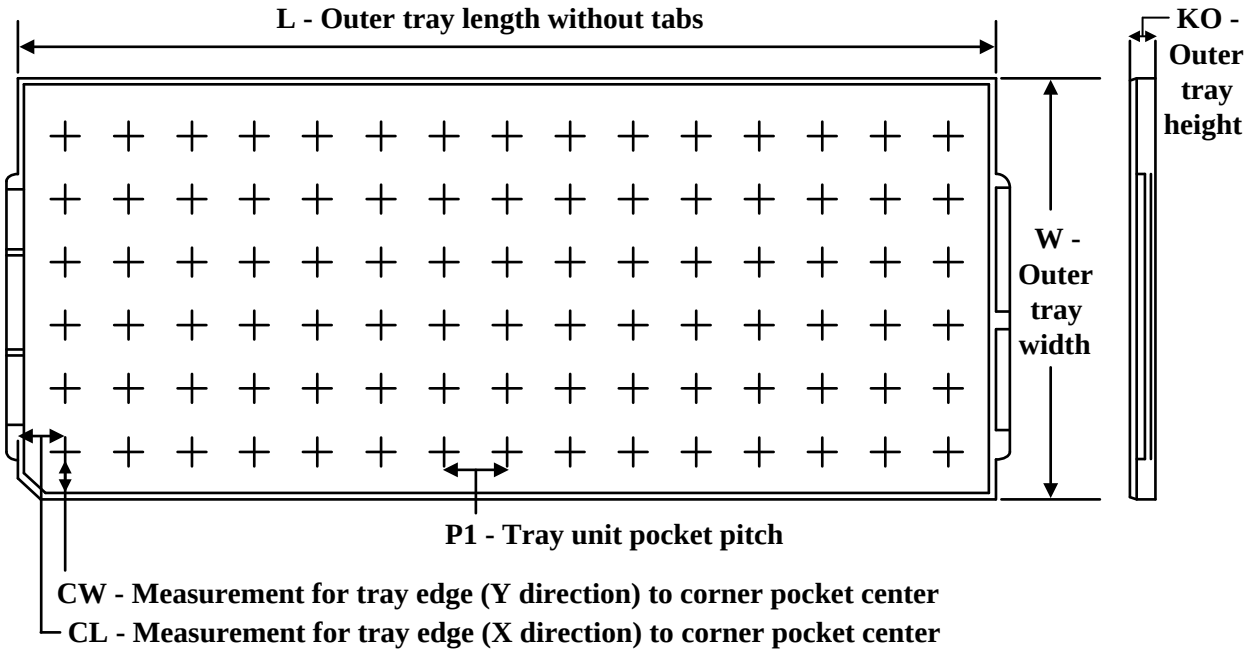
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430FR2032IG48	DGG	TSSOP	48	40	530	11.89	3600	4.9
MSP430FR2032IG56	DGG	TSSOP	56	35	530	11.89	3600	4.9
MSP430FR2033IG48	DGG	TSSOP	48	40	530	11.89	3600	4.9
MSP430FR2033IG56	DGG	TSSOP	56	35	530	11.89	3600	4.9

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

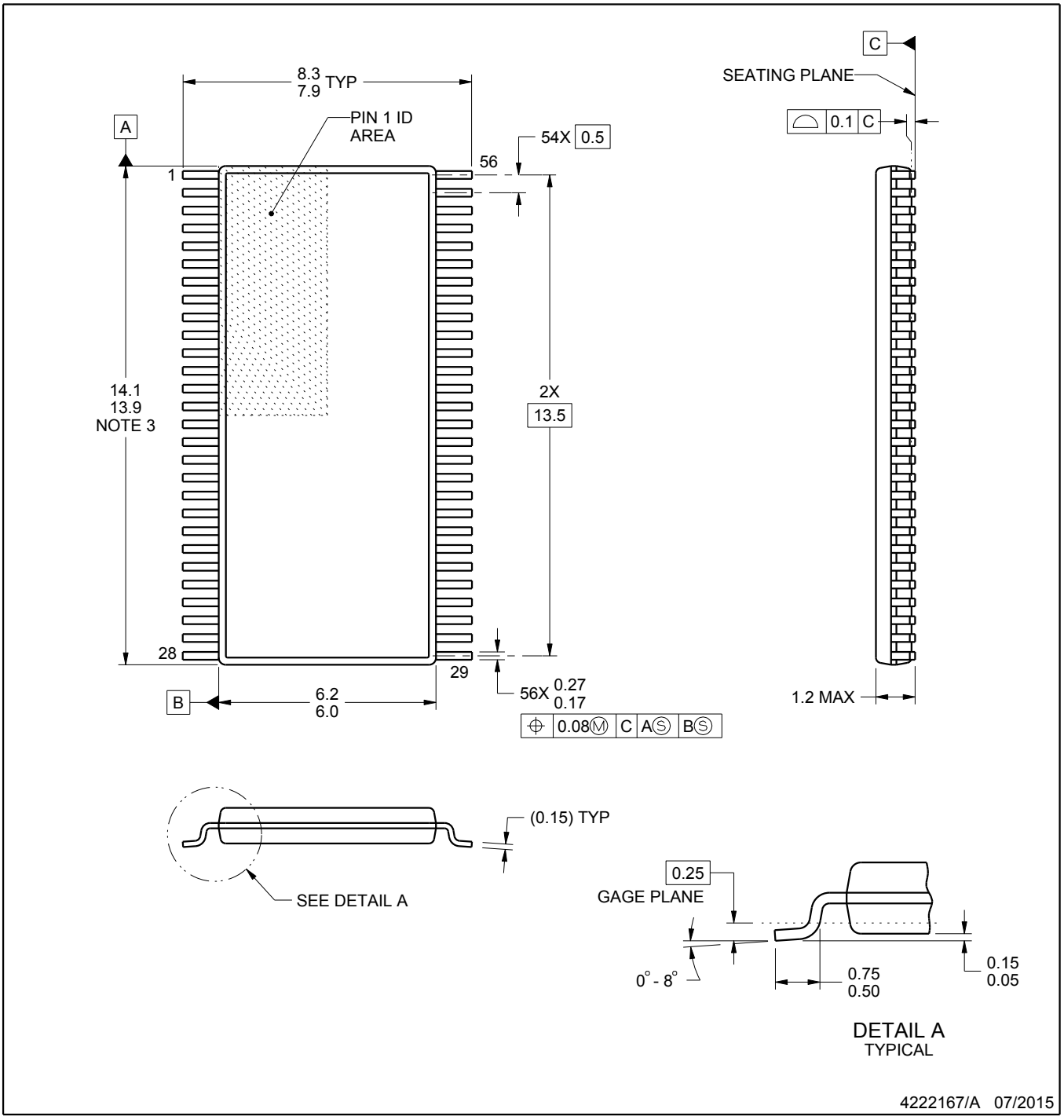
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430FR2033IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

PACKAGE OUTLINE

DGG0056A

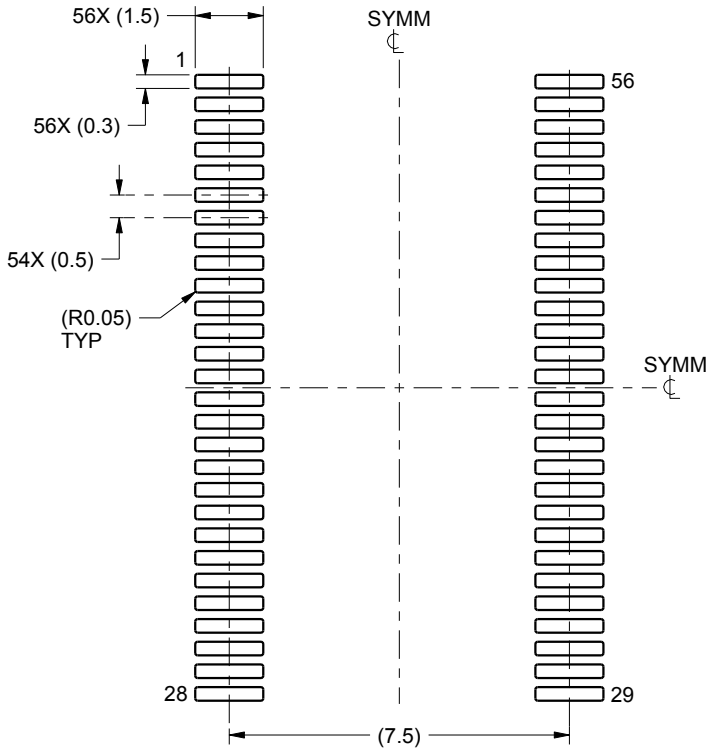
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

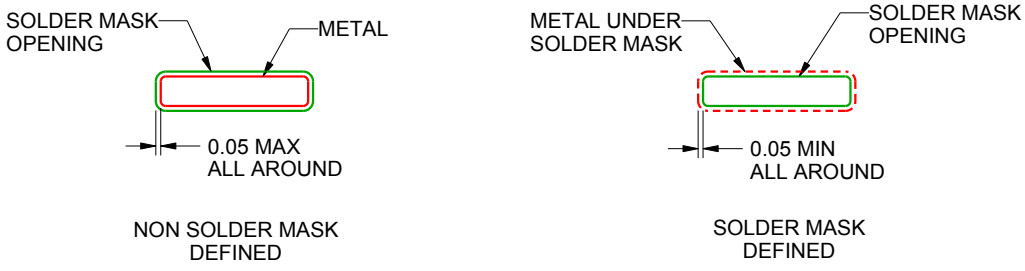


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

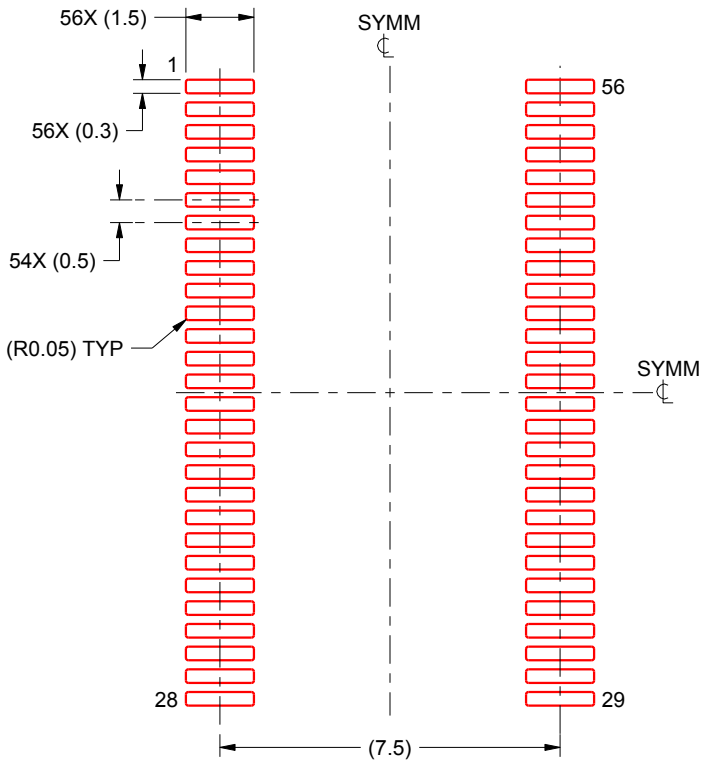


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

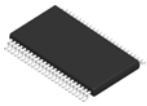


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

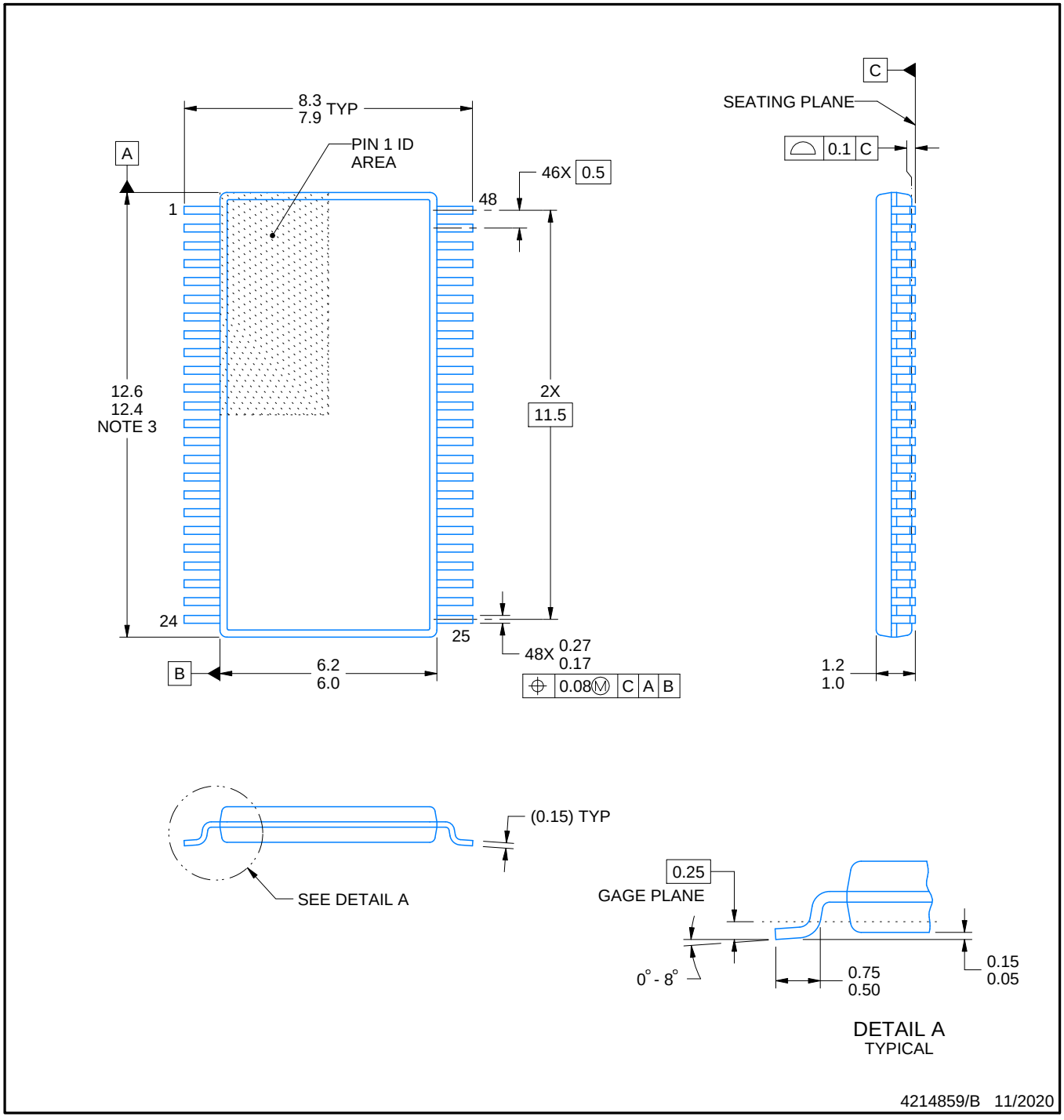


PACKAGE OUTLINE

DGG0048A

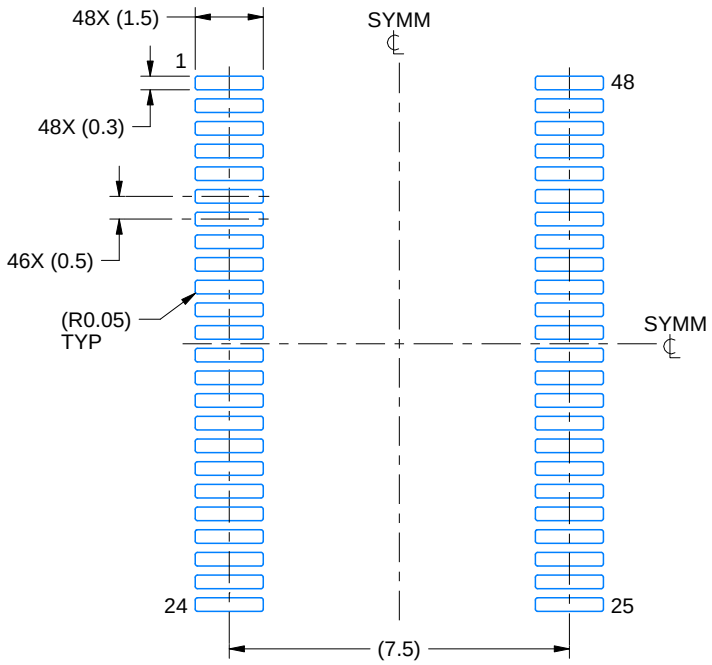
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

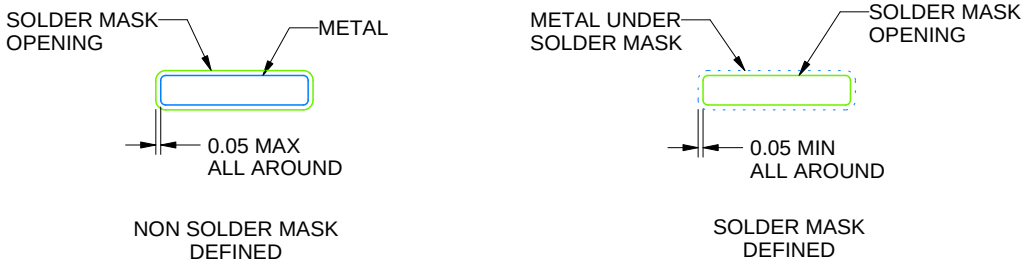


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

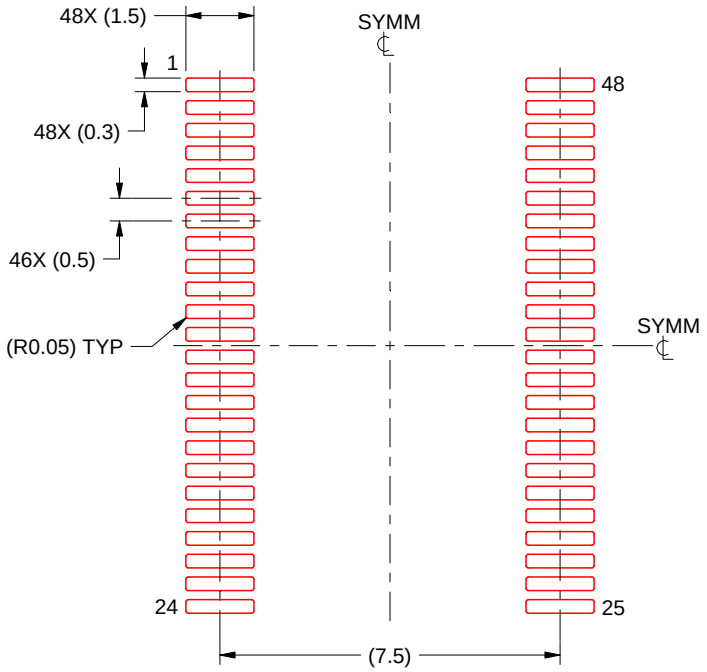


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

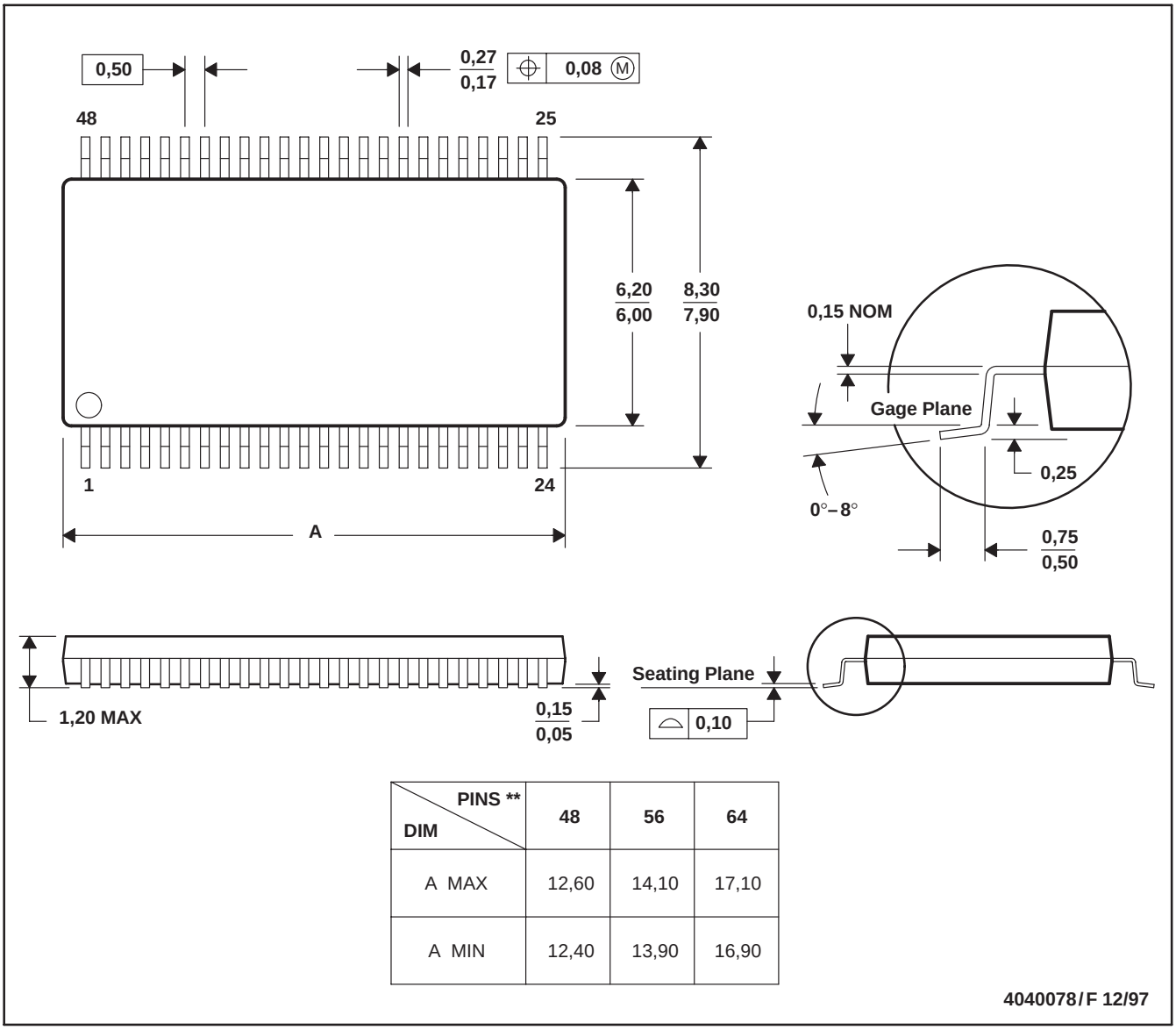
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

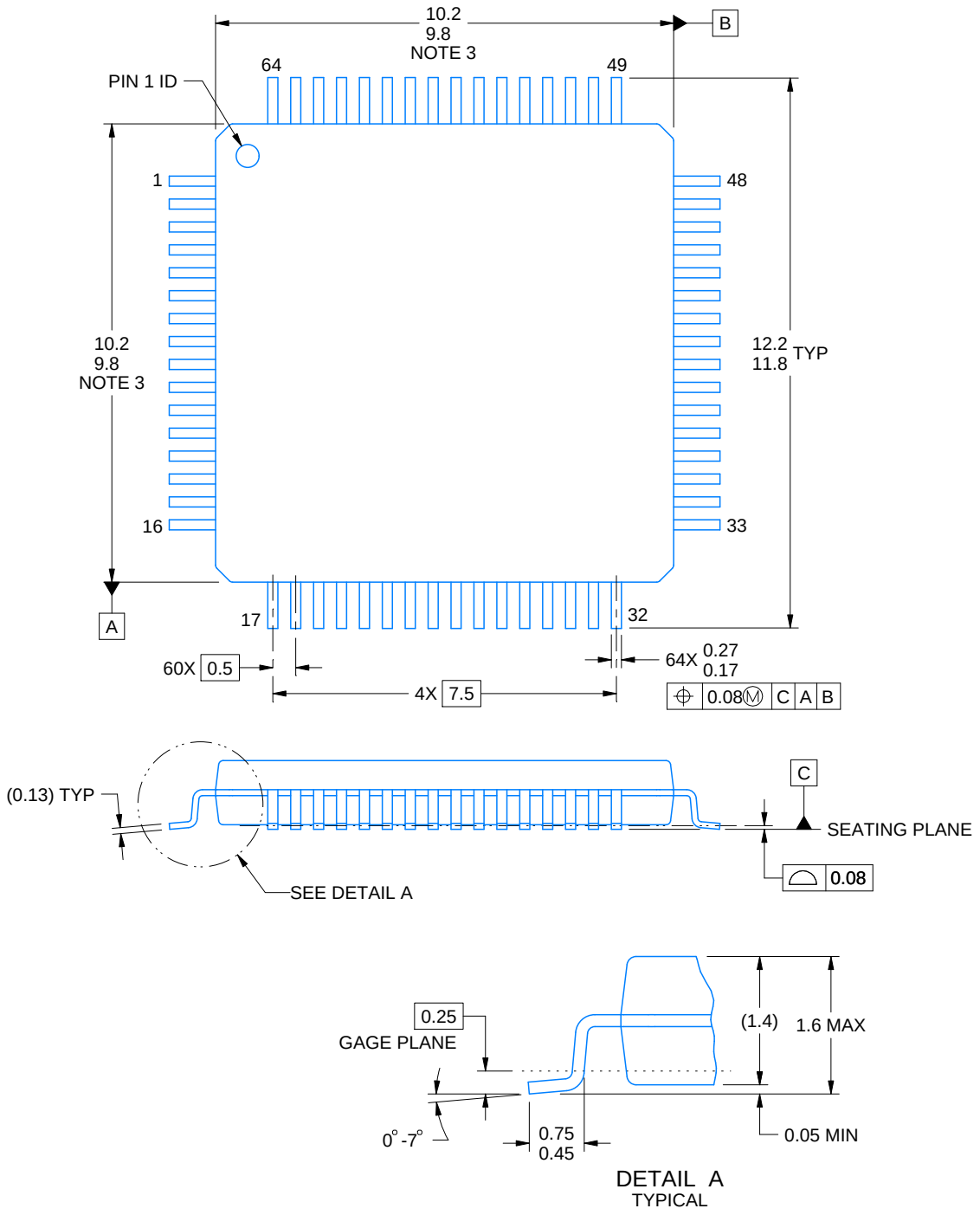
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

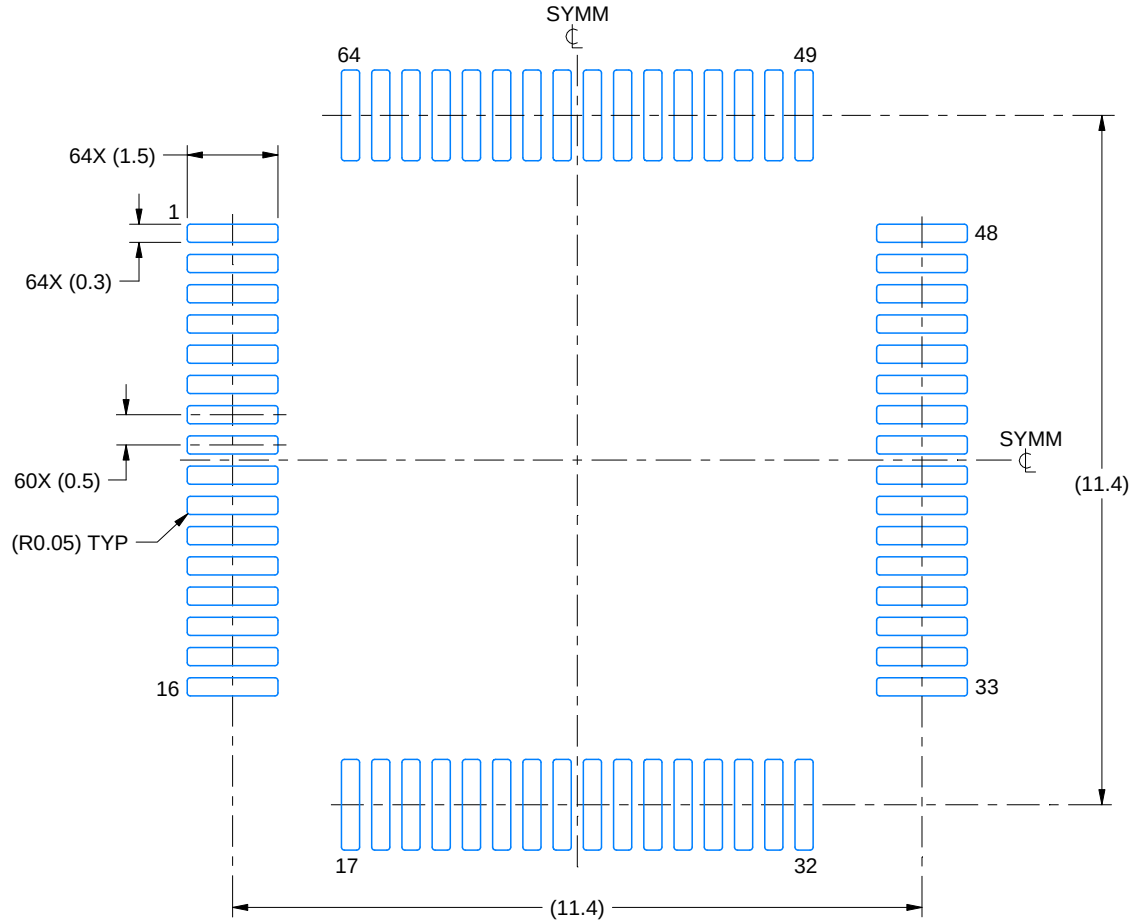
PLASTIC QUAD FLATPACK



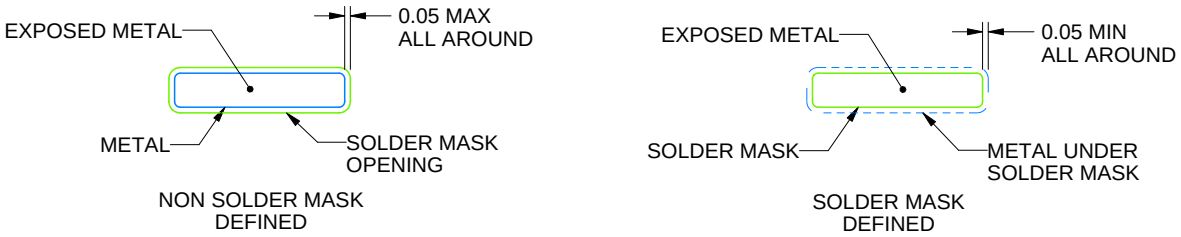
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

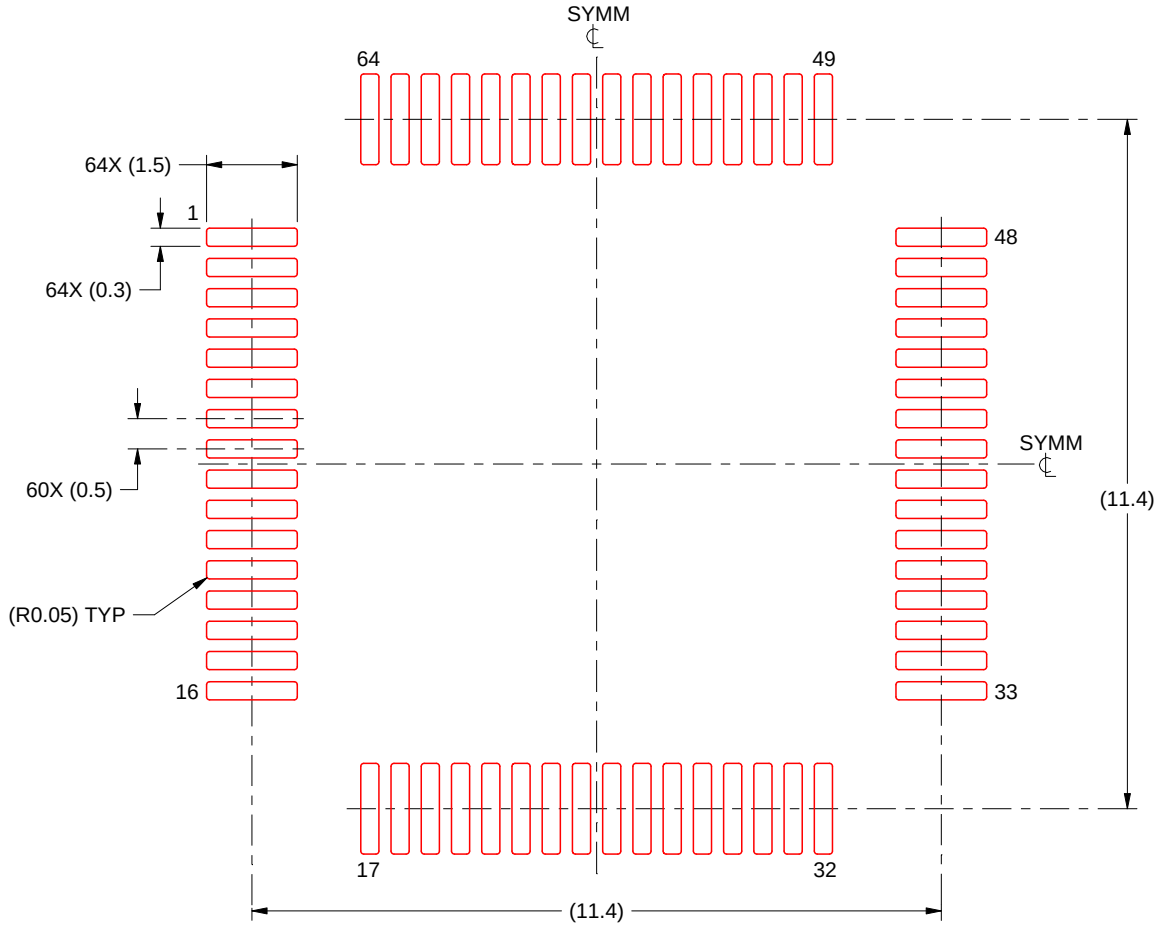


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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