TEXAS INSTRUMENTS
OPA170-Q1, OPA2170-Q1, OPA4170-Q1
JAJSCO9B – DECEMBER 2016 – REVISED NOVEMBER 2017

OPAx170-Q1 36V、単一電源、低消費電力、車載グレード・オペアンプ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
  - デバイスHBM ESD分類レベル3A
  - デバイスCDM ESD分類レベルC5
- 電源電圧範囲: 2.7V～36V、±1.35V～±18V
- 低ノイズ: 19nV/√Hz
- RFI フィルタ付きの入力
- 入力範囲は負の電源電圧にも対応
- 入力範囲は正の電源電圧まで動作
- レール・ツー・レール出力
- ゲイン帯域幅: 1.2MHz
- 低い静止電流: アンプごとに110µA
- 高い同相除去: 120dB
- 低い入力バイアス電流: 15pA (最大)
- チャネル数:
  - OPA170-Q1: 1
  - OPA2170-Q1: 2
  - OPA4170-Q1: 4
- 業界標準パッケージ

2 アプリケーション

- 車載用
- HEVおよびEVパワートレイン
- 先進運転支援システム（ADAS）
- 空調の自動制御
- 温度測定
- ひずみゲージ・アンプ
- 高精度積分器

3 概要

OPA170-Q1、OPA2170-Q1、OPA4170-Q1デバイス(OPAx170-Q1)は、小型パッケージで2.7V (±1.35V) ～36V (±18V)で動作可能な36V単電源低ノイズ・オペアンプのファミリです。低い静止電流で優れたオフセット、ドリフト、帯域幅を提供します。

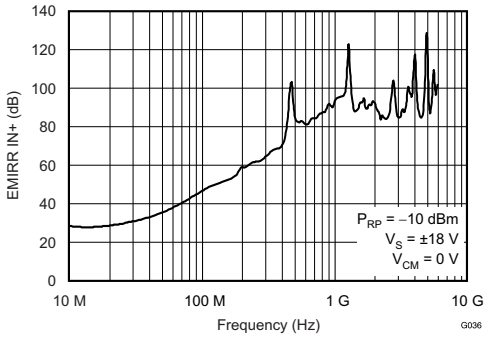
ほとんどのオペアンプでは1つの電源電圧でしか動作が規定されていないのに対して、OPAx170-Q1ファミリは2.7V～36Vでの動作が規定されています。電源レールの範囲外の入力信号が位相反転を起こすことはありません。OPAx170-Q1ファミリは、最大300pFの容量性負荷で安定です。通常の動作時に、入力は負のレールより100mV下、および正のレールから2V以内で動作できます。これらのデバイスは完全なレール・ツー・レール入力で、正のレールを100mV超えて動作しますが、正のレールから2V以内ではパフォーマンスが低下することに注意してください。OPAx170-Q1オペアンプは、-40℃～+125℃での動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA170-Q1	SOT-23 (5)	2.90mm×1.60mm
OPA2170-Q1	VSSOP (8)	3.00mm×3.00mm
OPA4170-Q1	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

EMIRR IN+と周波数との関係



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4 改訂履歴

Revision A (March 2017) から **Revision B** に変更 **Page**

- 「*製品情報*」表から8ピンSOIC、5ピンSOT、8ピンVSSOP、14ピンSOICパッケージを 削除 ... 1
- 表紙のグラフィック 変更 ... 1
- Deleted OPA170-Q1 D (SOIC) and DRL (SOT) pinout drawings and pinout table information ... 3
- Deleted OPA2170-Q1 D (SOIC) and DCU (VSSOP *Micro* size packages ... 4
- Deleted OPA170-Q1 D (SOIC) pinout drawing ... 5
- Deleted D (SOIC) and DRL (SOT) thermal information from OPA170-Q1 *Thermal Information* table ... 7
- Deleted D (SOIC) and DCU (VSSOP) thermal information from OPA2170-Q1 *Thermal Information* table ... 7
- Deleted D (SOIC) thermal information from OPA4170-Q1 *Thermal Information* table ... 7
- 変更 values in 図 38 from 250 Ω to 2.5 kΩ ... 19

2016年12月発行のものから更新 **Page**

- 「*概要*」の最初の段落から、最後の文章を 削除 ... 1
- Deleted static literature number in *Thermal Information: OPA170-Q1* table note ... 7
- Separated the IB and IOS test conditions for the OPA4170 in *Electrical Characteristics* table ... 8
- 追加 additional text to Figure 8 title ... 12
- 変更 "many specifications apply from –40°C to +125°C" to "many specifications apply from –40°C to +85°C" to correct typo ... 24

5 Pin Configuration and Functions

OPA170-Q1 DBV Package
5-Pin SOT-23
Top View

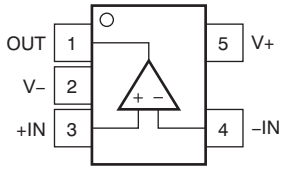

Table 1. Pin Functions: OPA170-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN– (–IN)	4	I	Negative (inverting) input
IN+ (+IN)	3	I	Positive (noninverting) input
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

OPA2170-Q1 DGK Package
8-Pin VSSOP
Top View

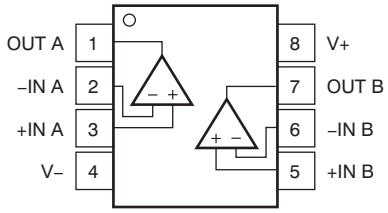

Table 2. Pin Functions: OPA2170-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4170-Q1 PW Package
14-Pin TSSOP
Top View

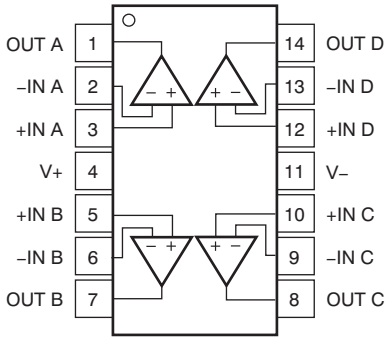

Table 3. Pin Functions: OPA4170-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage	–20	20	V
Single supply voltage		40	V
Signal input pin voltage	(V–) – 0.5	(V+) + 0.5	V
Signal input pin current	–10	10	mA
Output short-circuit current(2)	Continuous		
Operating ambient temperature, T_A	–55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V+ – V–)	2.7	36	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information: OPA170-Q1

THERMAL METRIC(1)		OPA170-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	245.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	133.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2170-Q1

THERMAL METRIC(1)		OPA2170-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4170-Q1

THERMAL METRIC(1)		OPA4170-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C		0.25	±1.8	mV
		T_A = –40°C to 125°C			±2	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		±0.3	±2	µV/°C
PSRR	Input offset voltage vs power supply	V_S = 4 V to 36 V T_A = –40°C to 125°C		1	±5	µV/V
	Channel separation, dc			5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		±8	±15	pA
		T_A = –40°C to 125°C (OPA170-Q1 and OPA2170-Q1)			±3.5	nA
		T_A = –40°C to 125°C (OPA4170-Q1)			±16	
I_{OS}	Input offset current	T_A = 25°C		±4	±15	pA
		T_A = –40°C to 125°C (OPA170-Q1 and OPA2170-Q1)			±3.5	nA
		T_A = –40°C to 125°C (OPA4170-Q1)			±16	
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		22		$nV/\sqrt{Hz}$
		f = 1 kHz		19		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range (1)		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±2 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to 125°C	90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to 125°C	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 4 V to 36 V (V–) + 0.35 V < V_O < (V+) – 0.35 V T_A = –40°C to 125°C	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			1.2		MHz
SR	Slew rate	G = 1		0.4		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = 1 10-V step		20		µs
		To 0.01% (12-bit), V_S = ±18 V, G = 1 10-V step		28		µs
	Overload recovery time	V_{IN} × Gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}		0.0002%		

(1) The input range can be extended beyond (V+) – 2 V up to V+. For additional information, see *Typical Characteristics* and *Application and Implementation*.

Electrical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from positive rail	I_L = 0 mA V_S = 4 V to 36 V	10			mV
		I_L sourcing 1 mA V_S = 4 V to 36 V	115			mV
V_O	Voltage output swing from negative rail	I_L = 0 mA V_S = 4 V to 36 V			8	mV
		I_L sinking 1 mA V_S = 4 V to 36 V			70	mV
V_O	Voltage output swing from rail	V_S = 5 V R_L = 10 kΩ T_A = –40°C to 125°C	(V–) + 0.03		(V+) – 0.05	V
		R_L = 10 kΩ A_{OL} ≥ 110 dB T_A = –40°C to 125°C	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current		–20		17	mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			pF
R_O	Open-loop output resistance	f = 1 MHz I_O = 0 A		900		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A T_A = 25°C		110	145	µA
		I_O = 0 A T_A = –40°C to 125°C			155	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–55		150	°C

6.8 Typical Characteristics: Table of Graphs

表 4. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	図 1
Offset Voltage Drift Distribution	図 2
Offset Voltage vs Temperature	図 3
Offset Voltage vs Common-Mode Voltage	図 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	図 5
Offset Voltage vs Power Supply	図 6
I_B and I_{OS} vs Common-Mode Voltage	図 7
Input Bias Current vs Temperature	図 8
Output Voltage Swing vs Output Current (Maximum Supply)	図 9
CMRR and PSRR vs Frequency (Referred-to-Input)	図 10
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Short-Circuit Current vs Temperature	図 34
Maximum Output Voltage vs Frequency	図 35
EMIRR IN+ vs Frequency	図 36

6.9 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

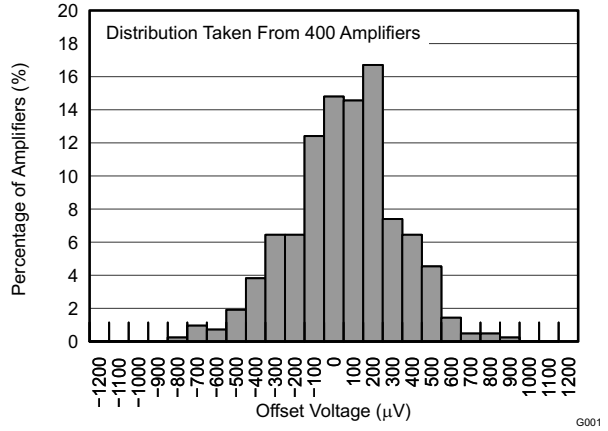


図 1. Offset Voltage Production Distribution

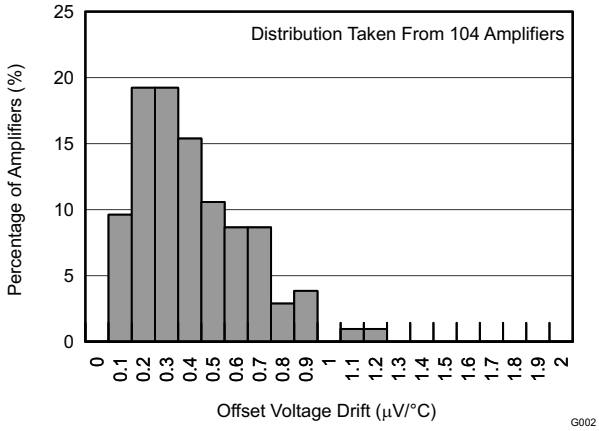


図 2. Offset Voltage Drift Distribution

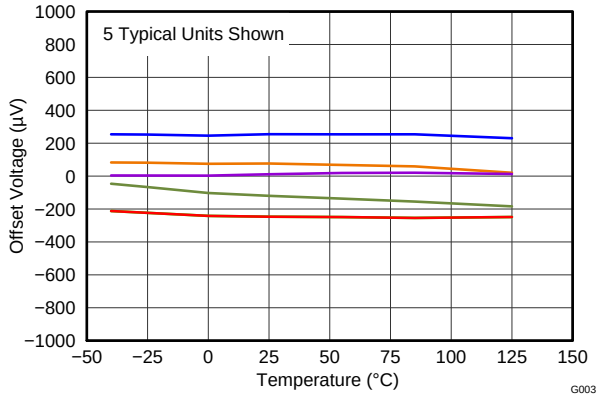


図 3. Offset Voltage vs Temperature

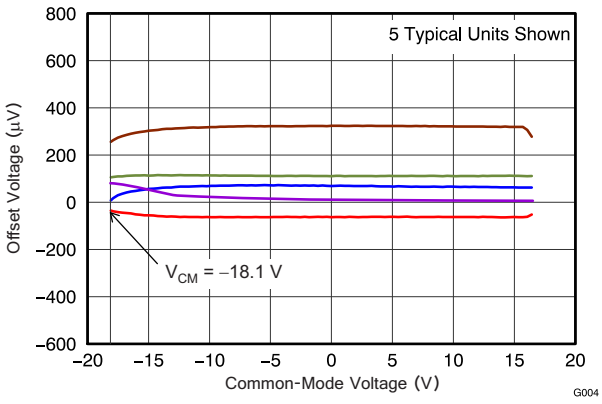


図 4. Offset Voltage vs Common-Mode Voltage

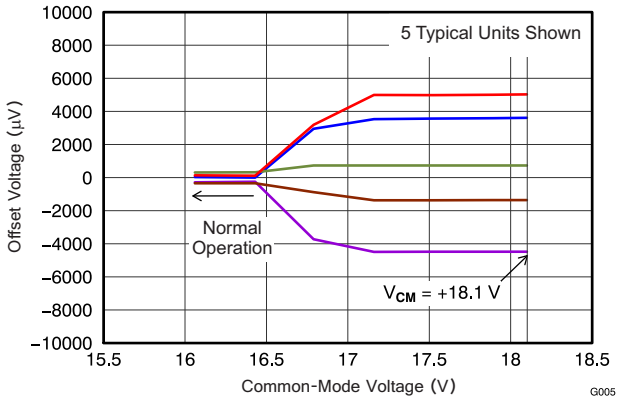


図 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

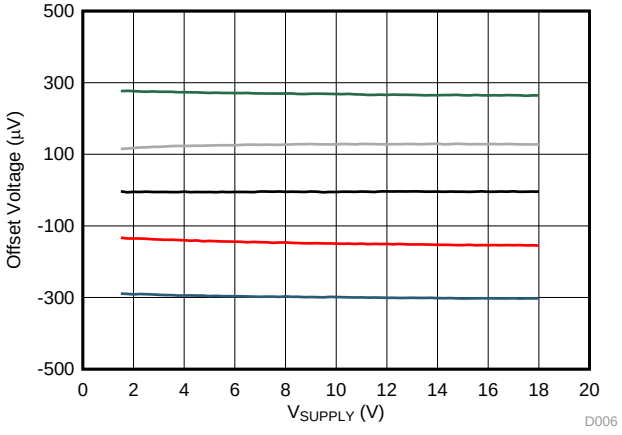


図 6. Offset Voltage vs Power Supply

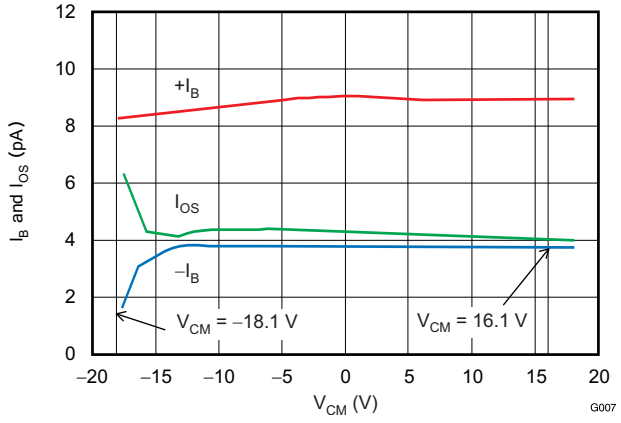


図 7. I_B and I_{OS} vs Common-Mode Voltage

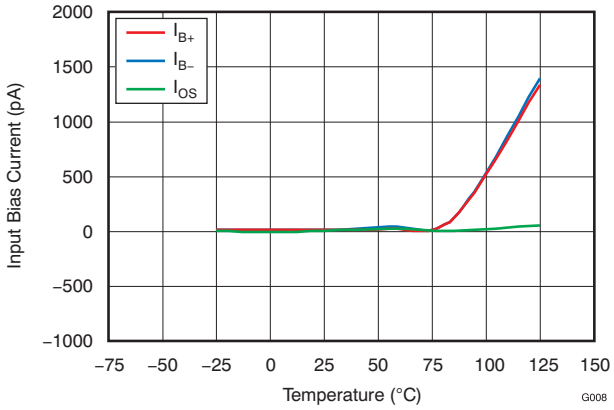


図 8. Input Bias Current vs Temperature for Single and Dual Versions

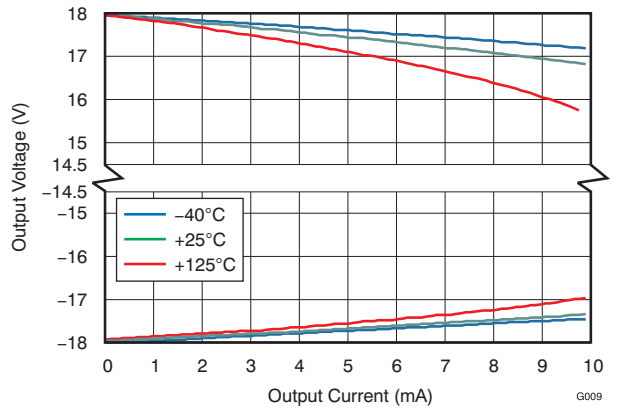


図 9. Output Voltage Swing vs Output Current (Maximum Supply)

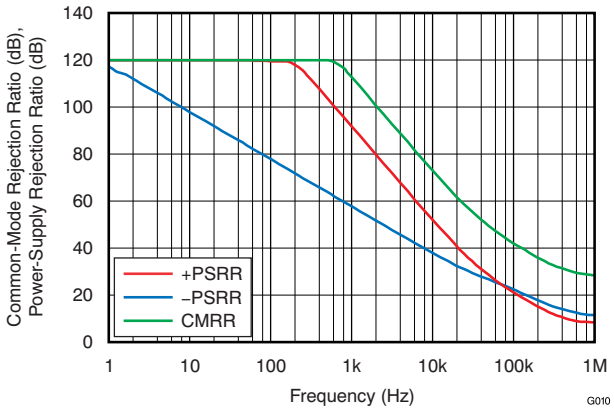


図 10. CMRR and PSRR vs Frequency (Referred to Input)

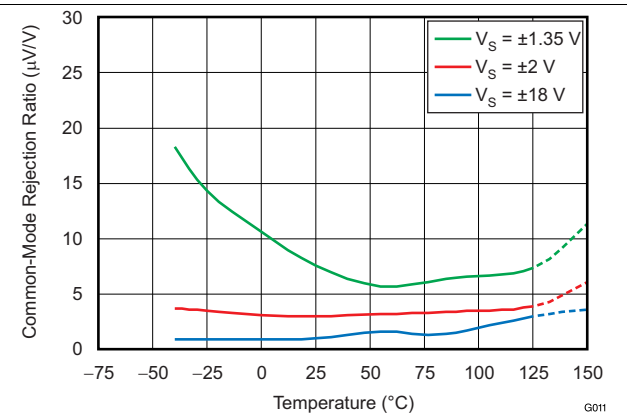


図 11. CMRR vs Temperature

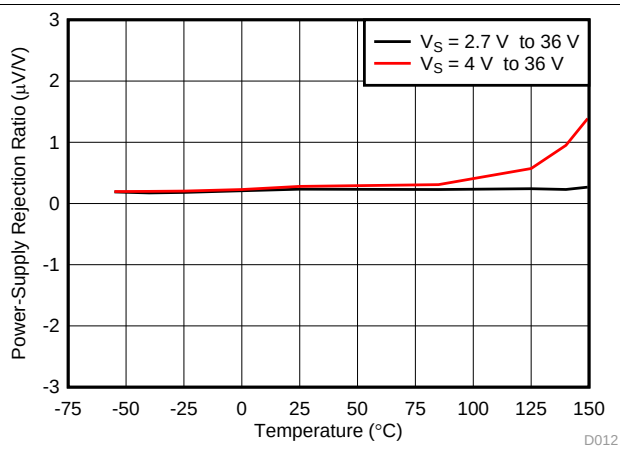


図 12. PSRR vs Temperature

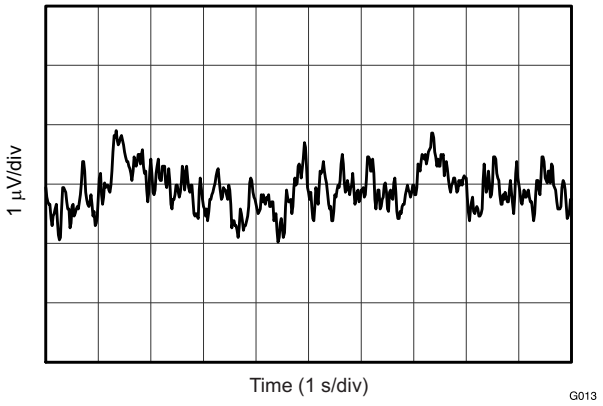


図 13. 0.1-Hz to 10-Hz Noise

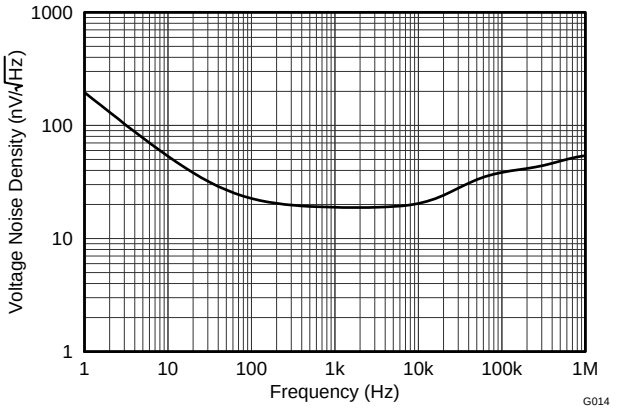


図 14. Input Voltage Noise Spectral Density vs Frequency

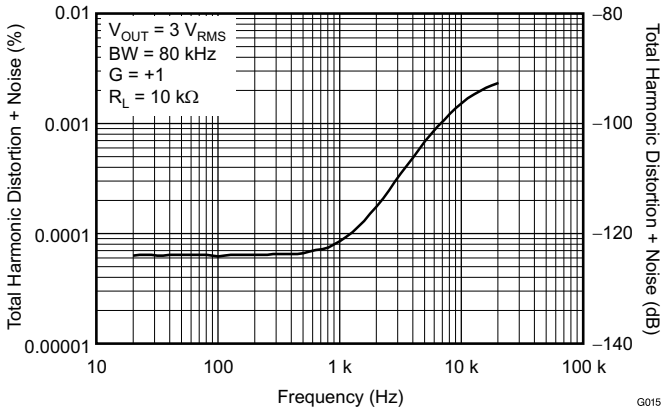


図 15. THD + N Ratio vs Frequency

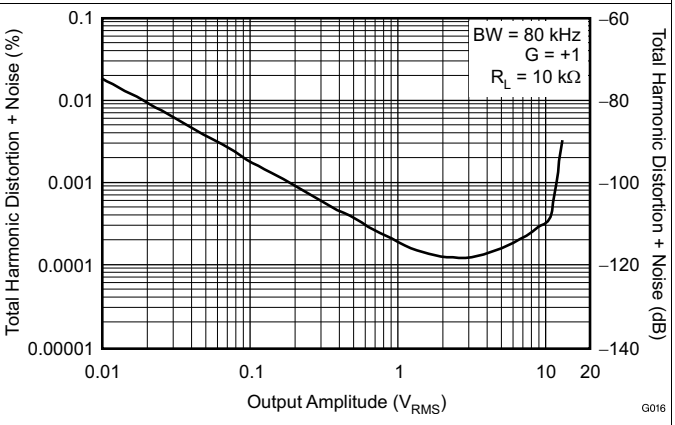


図 16. THD + N vs Output Amplitude

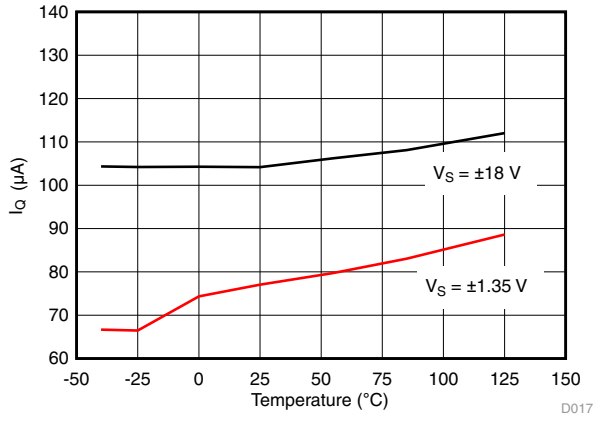


図 17. Quiescent Current vs Temperature

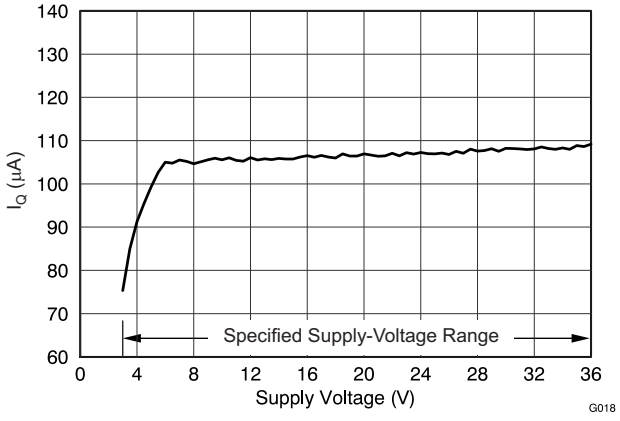


図 18. Quiescent Current vs Supply Voltage

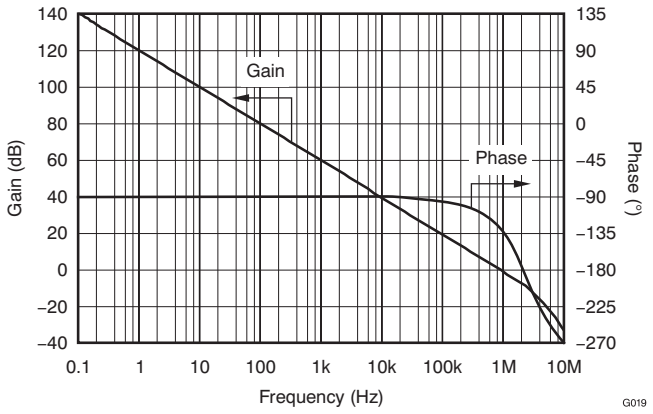


図 19. Open-Loop Gain and Phase vs Frequency

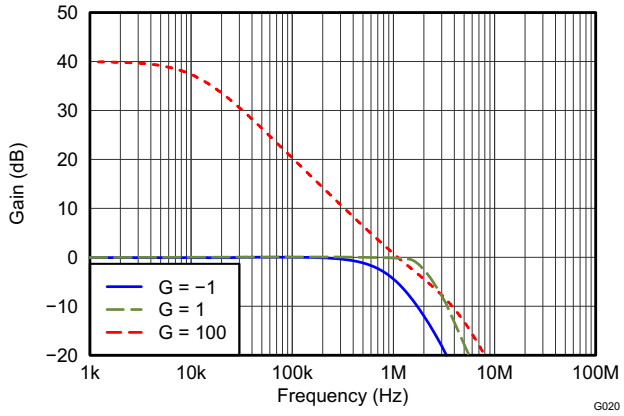


図 20. Closed-Loop Gain vs Frequency

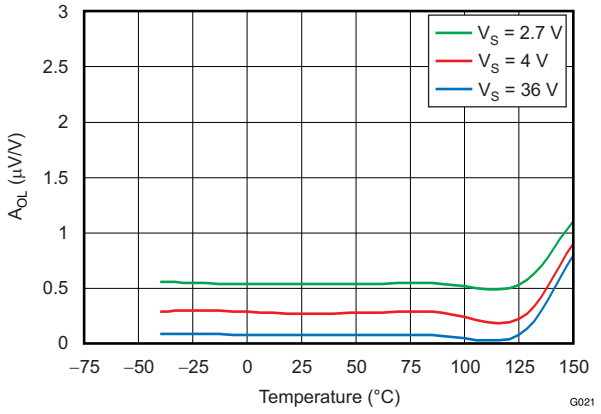


図 21. Open-Loop Gain vs Temperature

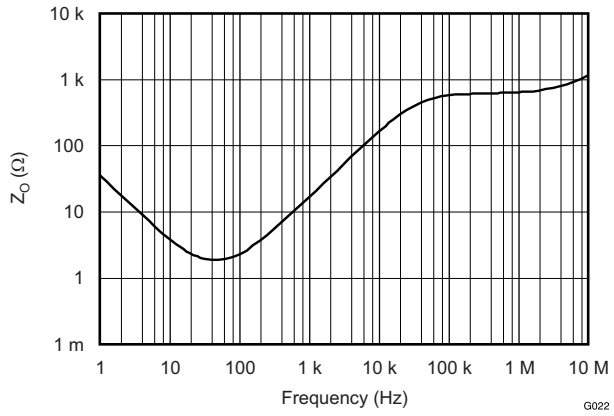
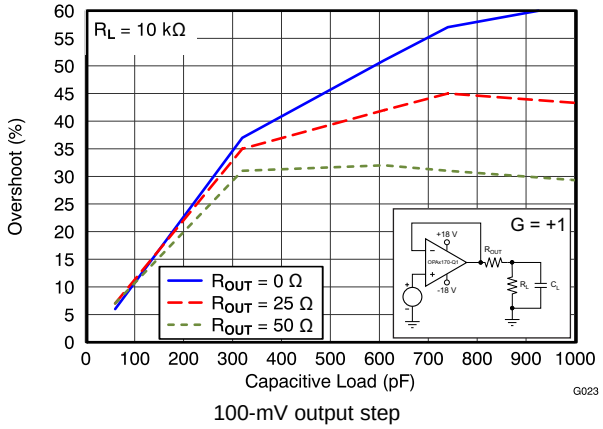
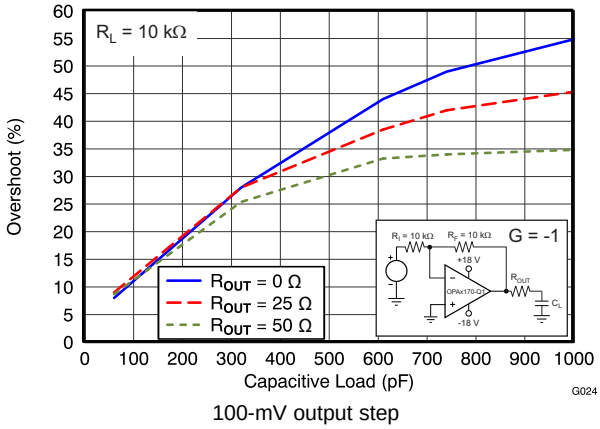


図 22. Open-Loop Output Impedance vs Frequency



100-mV output step

図 23. Small-Signal Overshoot vs Capacitive Load



100-mV output step

図 24. Small-Signal Overshoot vs Capacitive Load

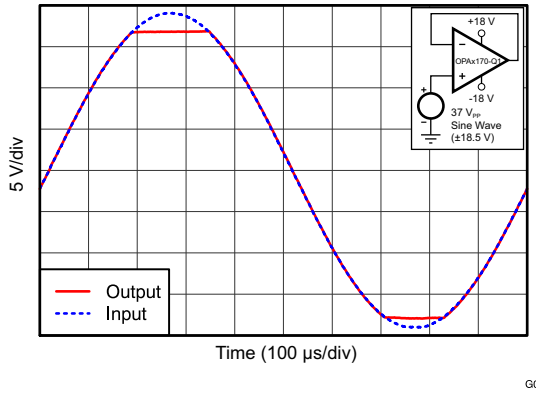


図 25. No Phase Reversal

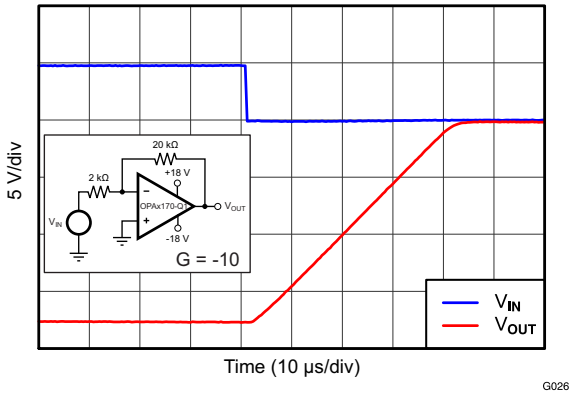


図 26. Positive Overload Recovery

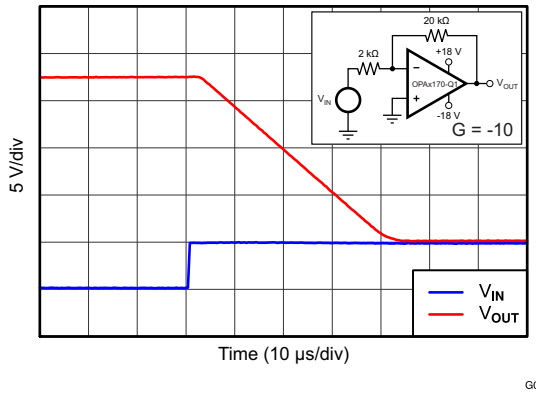


図 27. Negative Overload Recovery

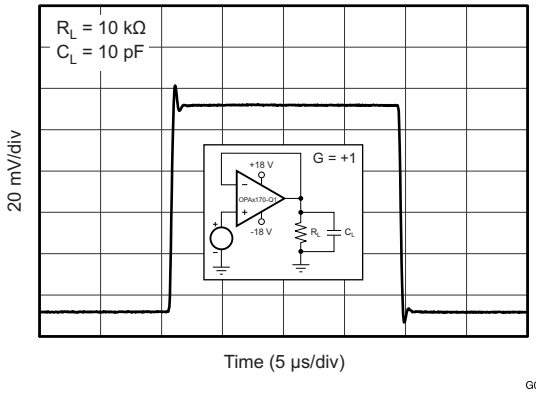


図 28. Small-Signal Step Response (100-mV)

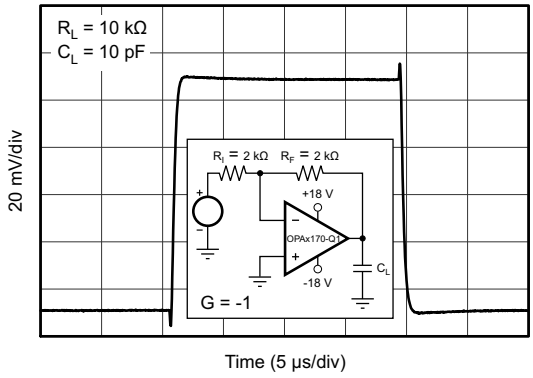


図 29. Small-Signal Step Response (100-mV)

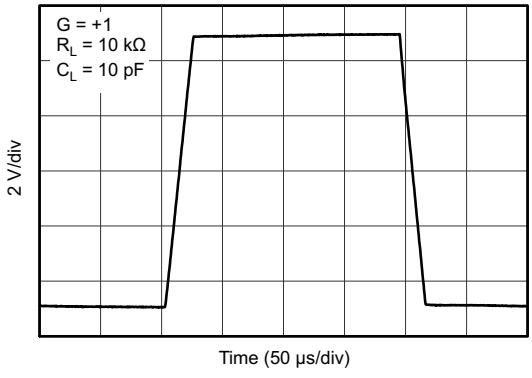


図 30. Large-Signal Step Response

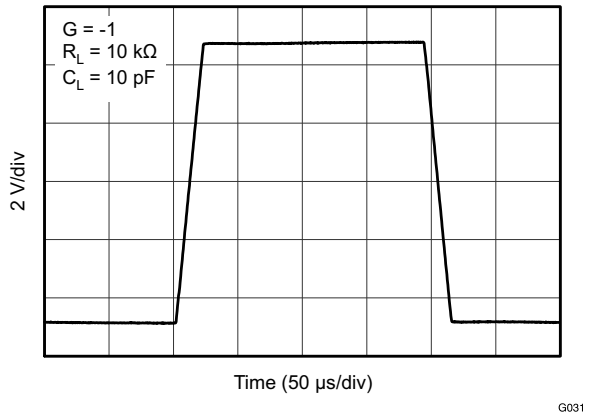
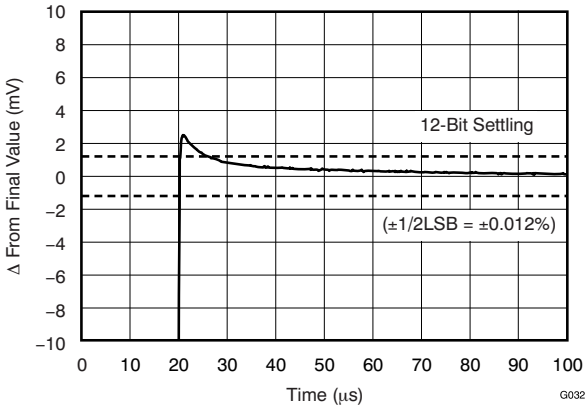
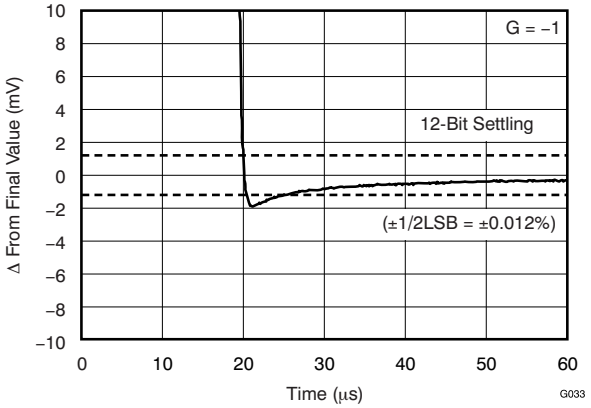


図 31. Large-Signal Step Response



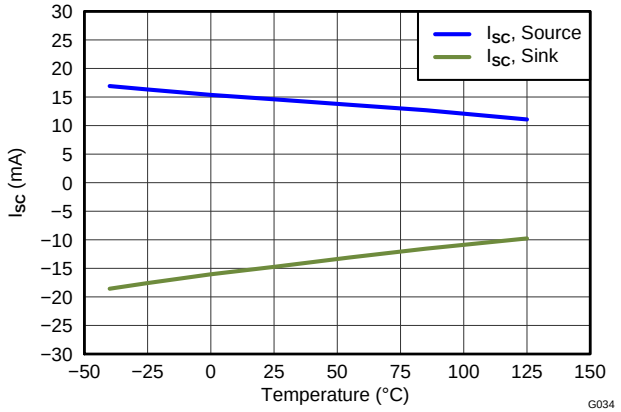
10-V positive step

図 32. Large-Signal Settling Time



10-V negative step

図 33. Large-Signal Settling Time



10-V negative step

図 34. Short-Circuit Current vs Temperature

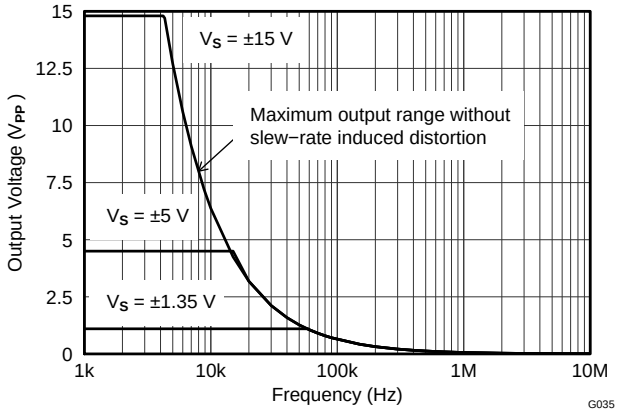


図 35. Maximum Output Voltage vs Frequency

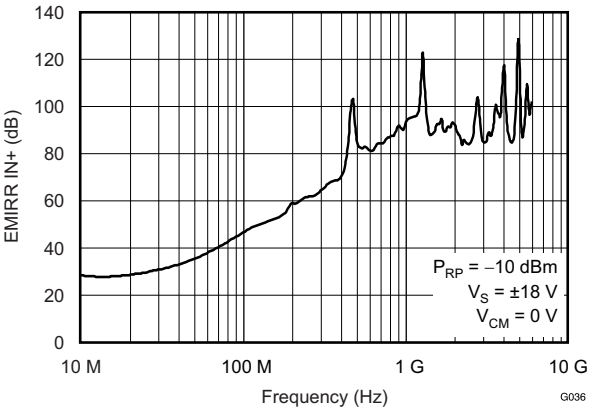


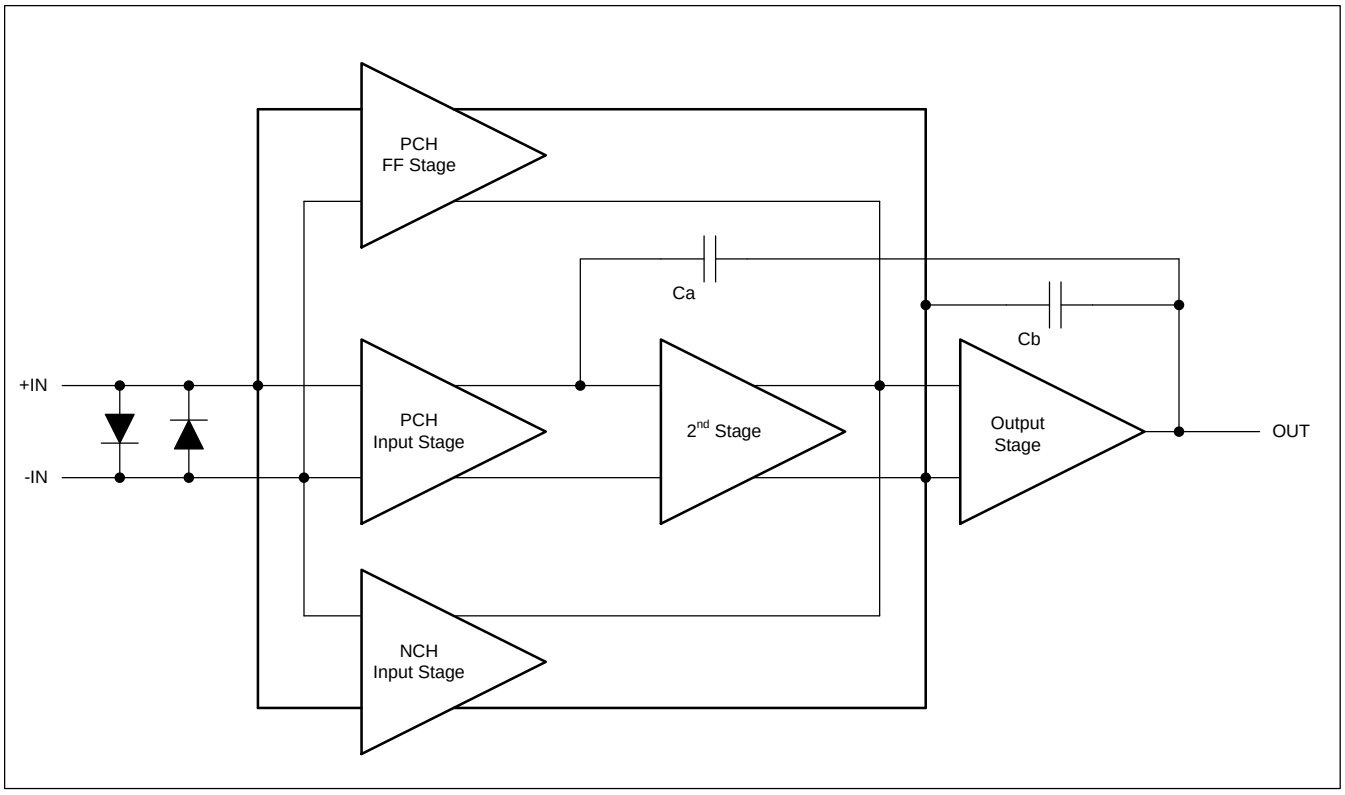
図 36. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The OPAx170-Q1 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 2 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx170-Q1 family of amplifiers is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are listed in *表 4*.

Feature Description (continued)

7.3.2 Phase-Reversal Protection

The OPAx170-Q1 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx170-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. 図 37 shows this performance.

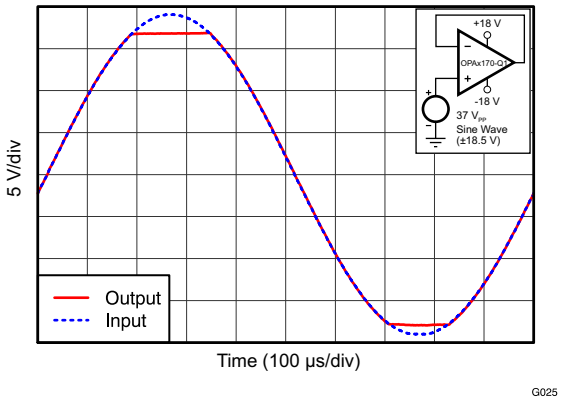


図 37. No Phase Reversal

7.3.3 Electrical Overstress

Designers typically ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions typically focus on the device inputs, but may involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of basic ESD circuitry and the relevance of the circuitry to an electrical overstress event is helpful. 図 38 shows the ESD circuits (indicated by the dashed line area) in the OPAx170-Q1. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)

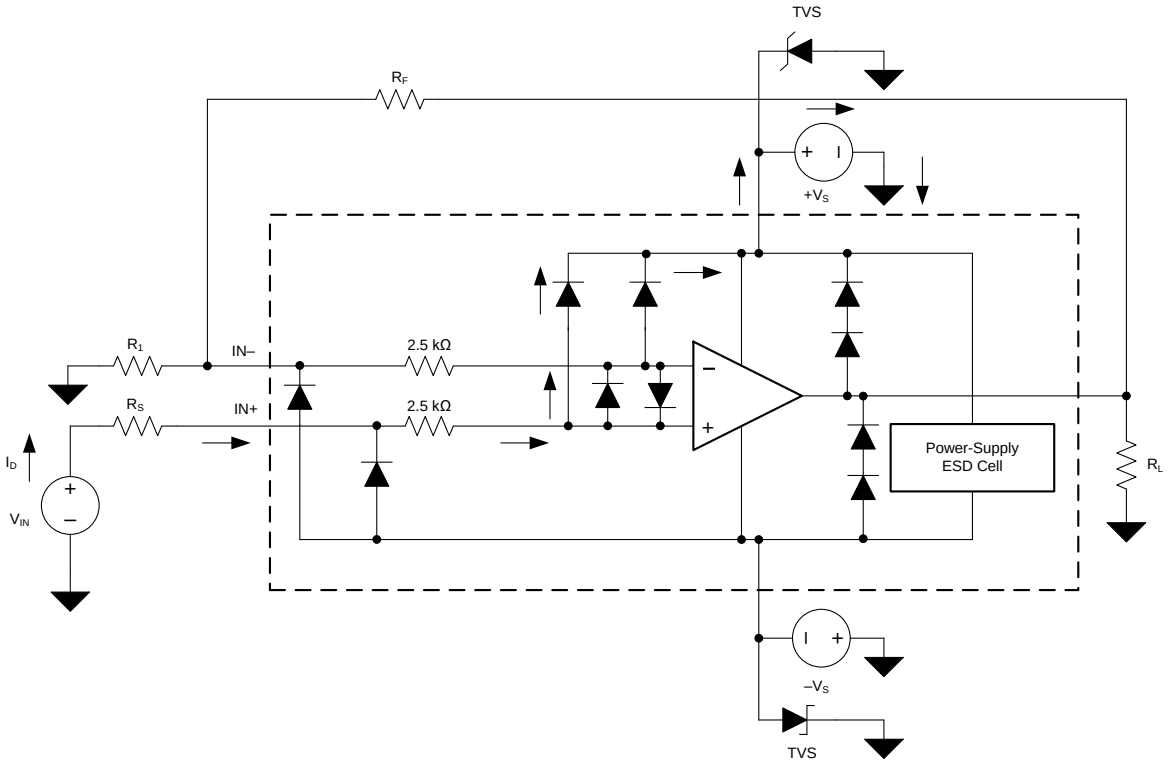


図 38. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. The absorption device can activate depending on the path of the current. The absorption device has a trigger (or threshold voltage) that is above the normal operating voltage of the OPAx170-Q1, but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see 図 38), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 38 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (continued)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 図 38. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAx170-Q1 input pins are protected from excessive differential voltage with back-to-back diodes, as shown in 図 38. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx170-Q1. 図 38 is an example configuration that implements a current-limiting feedback resistor.

7.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx170-Q1 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 図 39 and 図 40 are graphs showing small-signal overshoot versus capacitive load for several values of R_{OUT}. See *Feedback Plots Define Op Amp AC Performance* for details of analysis techniques and application circuits.

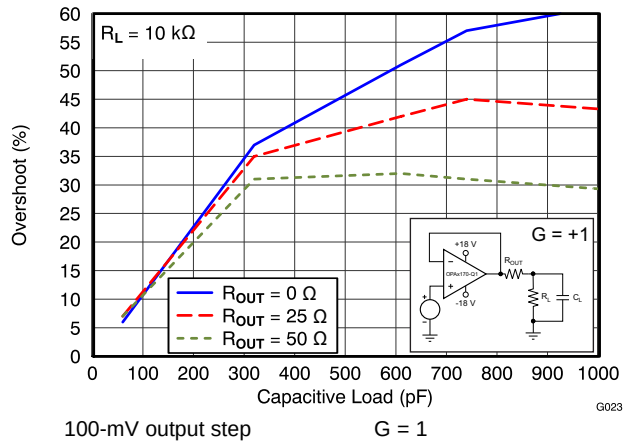


図 39. Small-Signal Overshoot vs Capacitive Load

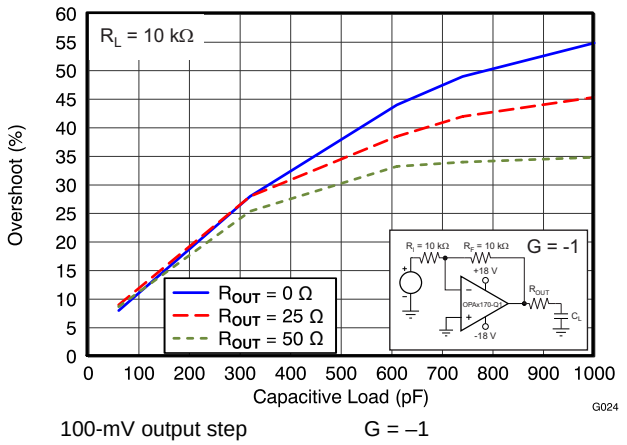


図 40. Small-Signal Overshoot vs Capacitive Load

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx170-Q1 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 5.

表 5. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER		MIN	TYP	MAX	UNIT
Input common-mode voltage		(V+) – 2		(V+) + 0.1	V
Offset voltage			7		mV
	vs temperature		12		µV/°C
Common-mode rejection			65		dB
Open-loop gain			60		dB
Gain-bandwidth product			0.3		MHz
Slew rate			0.3		V/µs

7.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx170-Q1 is approximately 2 µs.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx170-Q1 family of operational amplifiers provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, capacitors with a value of 0.1 µF are adequate. Follow the additional recommendations in the *Layout Guidelines* section to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier that may cause instability. Adding an isolation resistor between the amplifier output and the capacitive load stabilizes the amplifier. The design process for selecting this resistor is shown in the *Typical Application* section.

8.2 Typical Application

This circuit can drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an operational amplifier. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

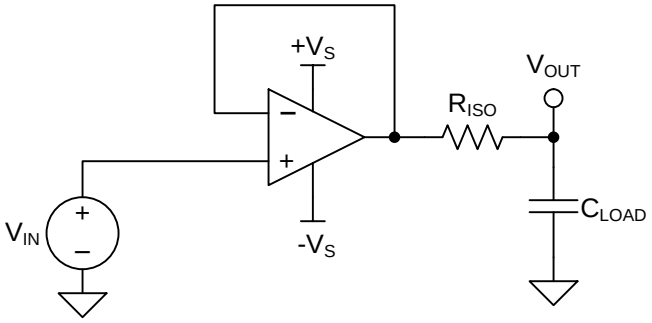


図 41. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100-pF, 1000-pF, 0.01-µF, 0.1-µF, and 1-µF
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

図 41 shows a unity-gain buffer driving a capacitive load. 式 1 shows the transfer function for the circuit in 図 41. Not shown in 図 41 is the open-loop output resistance of the operational amplifier, R_O.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 式 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_O + R_{ISO}) and C_{LOAD}. R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO}, so the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB / decade. 図 42 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Typical Application (continued)

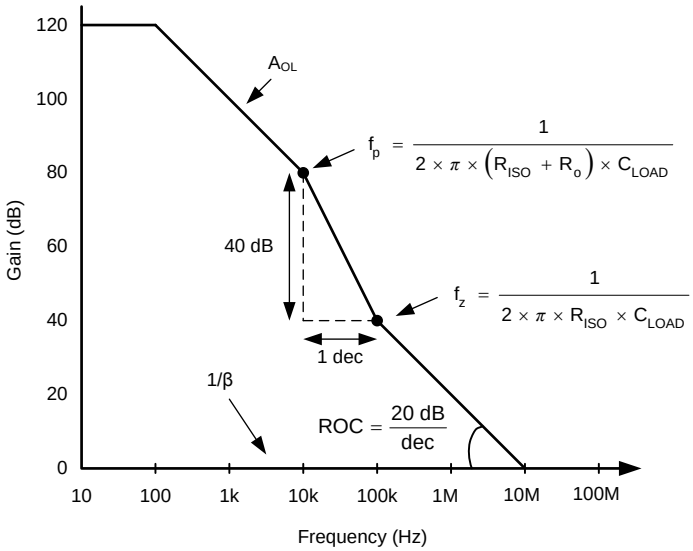


図 42. Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_O. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 6 shows the overshoot percentage and ac gain peaking that correspond to 45° and 60° phase margins. For more details on this design and other alternative devices that can be used in place of the OPAx170-Q1 family, see *Capacitive Load Drive Solution Using an Isolation Resistor*.

表 6. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.3 Application Curve

Using the described methodology, the values of R_{ISO} that yield phase margins of 45º and 60º for various capacitive loads were determined. 図 43 shows the results.

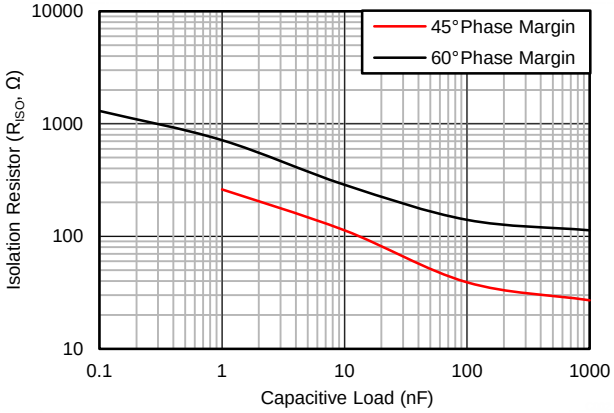


図 43. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

9 Power Supply Recommendations

The OPAx170-Q1 family is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *表 4*.

注意

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in 図 45, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

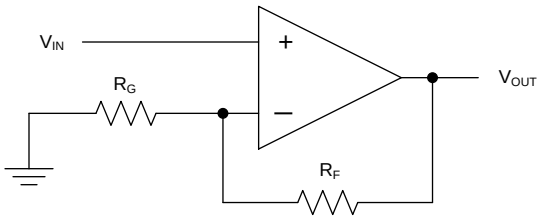


図 44. Schematic Representation of a Noninverting Configuration

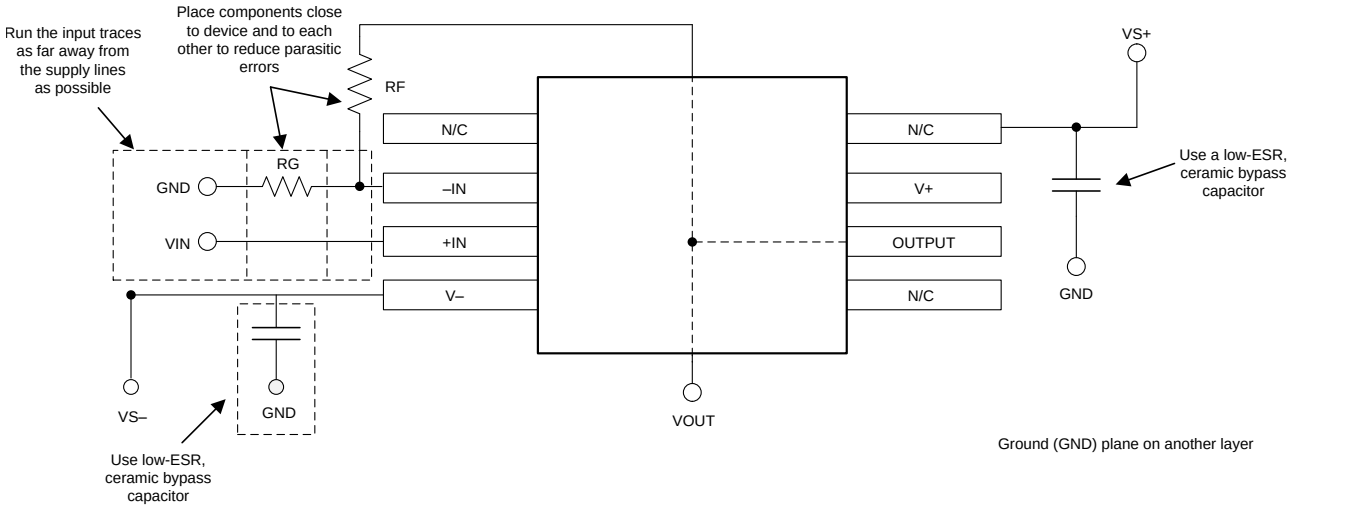


図 45. Operational Amplifier Board Layout for a Noninverting Configuration

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはWEBENCH® Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

11.1.1.2 DIPアダプタ評価モジュール

DIPアダプタ評価モジュール・ツールを使用すると、小さな表面実装ICのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU (SOIC-8)、PW (TSSOP-8)、DGK (MSOP-8)、DBV (SOT-23-6、SOT-23-5、およびSOT-23-3)、DCK (SC70-6およびSC70-5)、およびDRL (SOT563-6)のTIパッケージに対応しています。DIPアダプタ評価モジュールは、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

11.1.1.3 ユニバーサル・オペアンプ評価モジュール

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のデバイス・パッケージ・タイプ向け回路のプロトタイプ作成を容易にします。この評価モジュール基板は、多くの異なる回路を簡単かつ迅速に構築できるように設計されています。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、SOT-23のすべてのパッケージがサポートされています。

注

これらの基板には部品が搭載されていないため、ユーザーが独自のデバイスを実装する必要があります。ユニバーサル・オペアンプ評価モジュールを注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

11.1.1.4 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

デバイス・サポート (continued)

11.1.1.5 WEBENCH®Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH® Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

11.2 ドキュメントのサポート

11.2.1 関連資料

参照資料については、以下をご覧ください(www.ti.comからダウンロードできます)。

- 『フィードバック・プロットによるオペアンプAC性能の定義』
- 『絶縁抵抗の使用による容量性負荷駆動のソリューション』

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 7. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA170-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2170-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4170-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA170AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	170Q	Samples
OPA2170AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2170	Samples
OPA4170AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4170Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

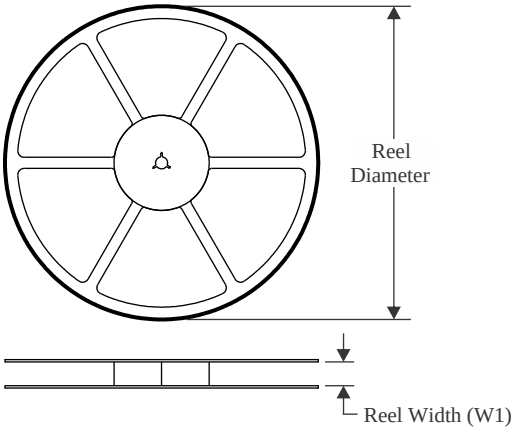
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

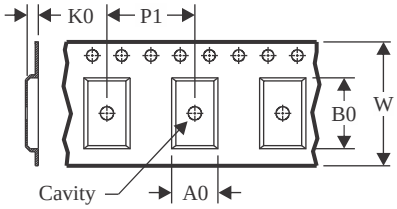
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

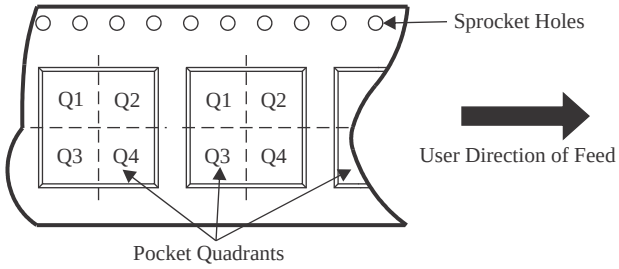


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

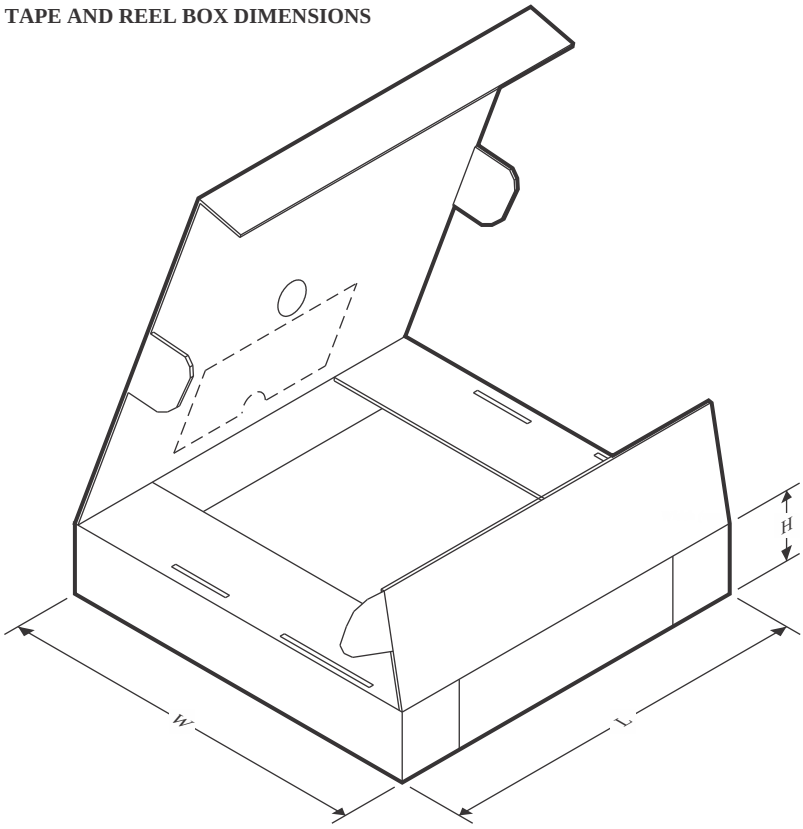
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA170AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA2170AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA4170AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

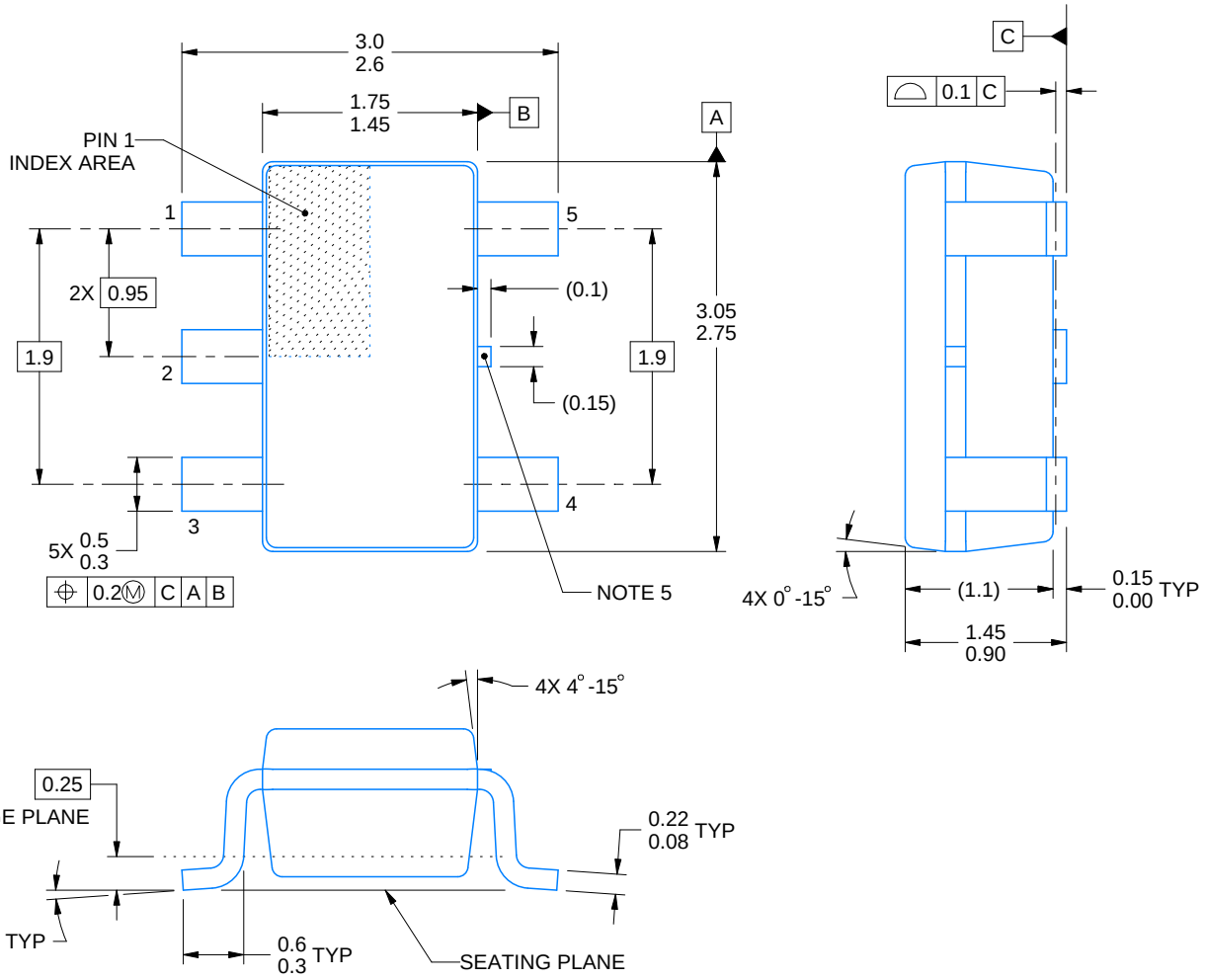
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA170AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA2170AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA4170AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

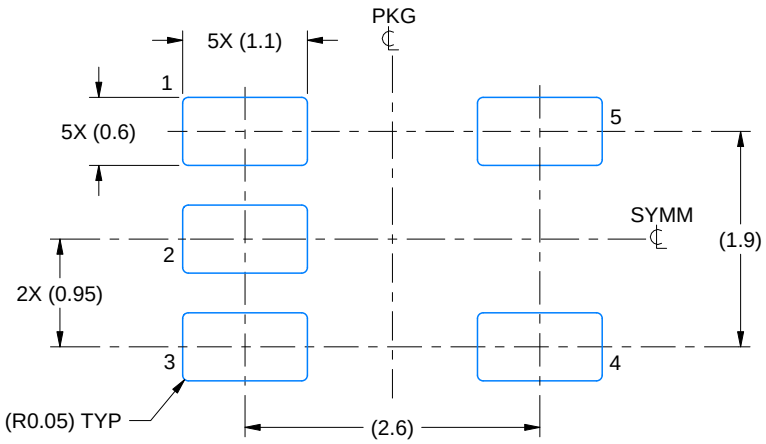
SMALL OUTLINE TRANSISTOR



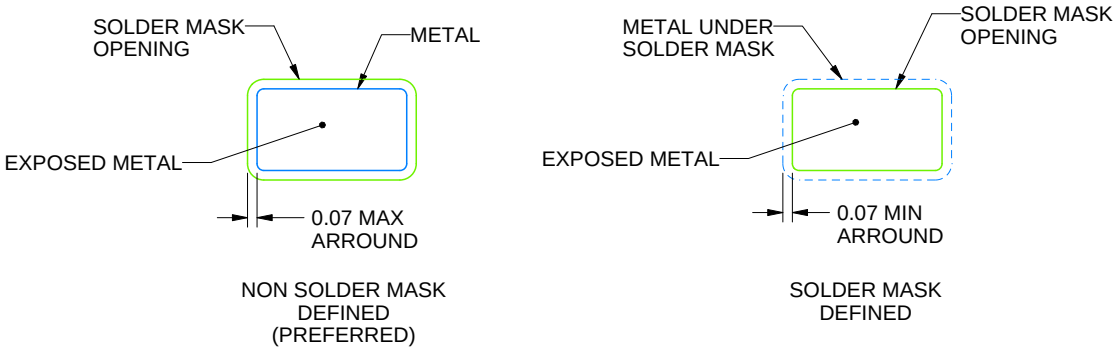
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

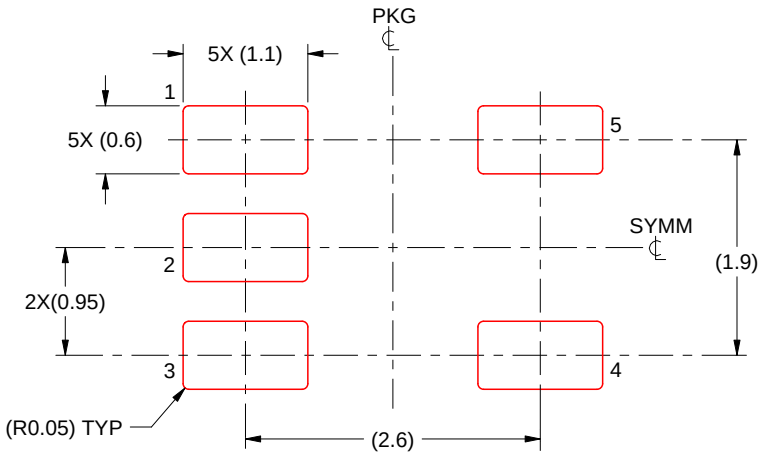


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

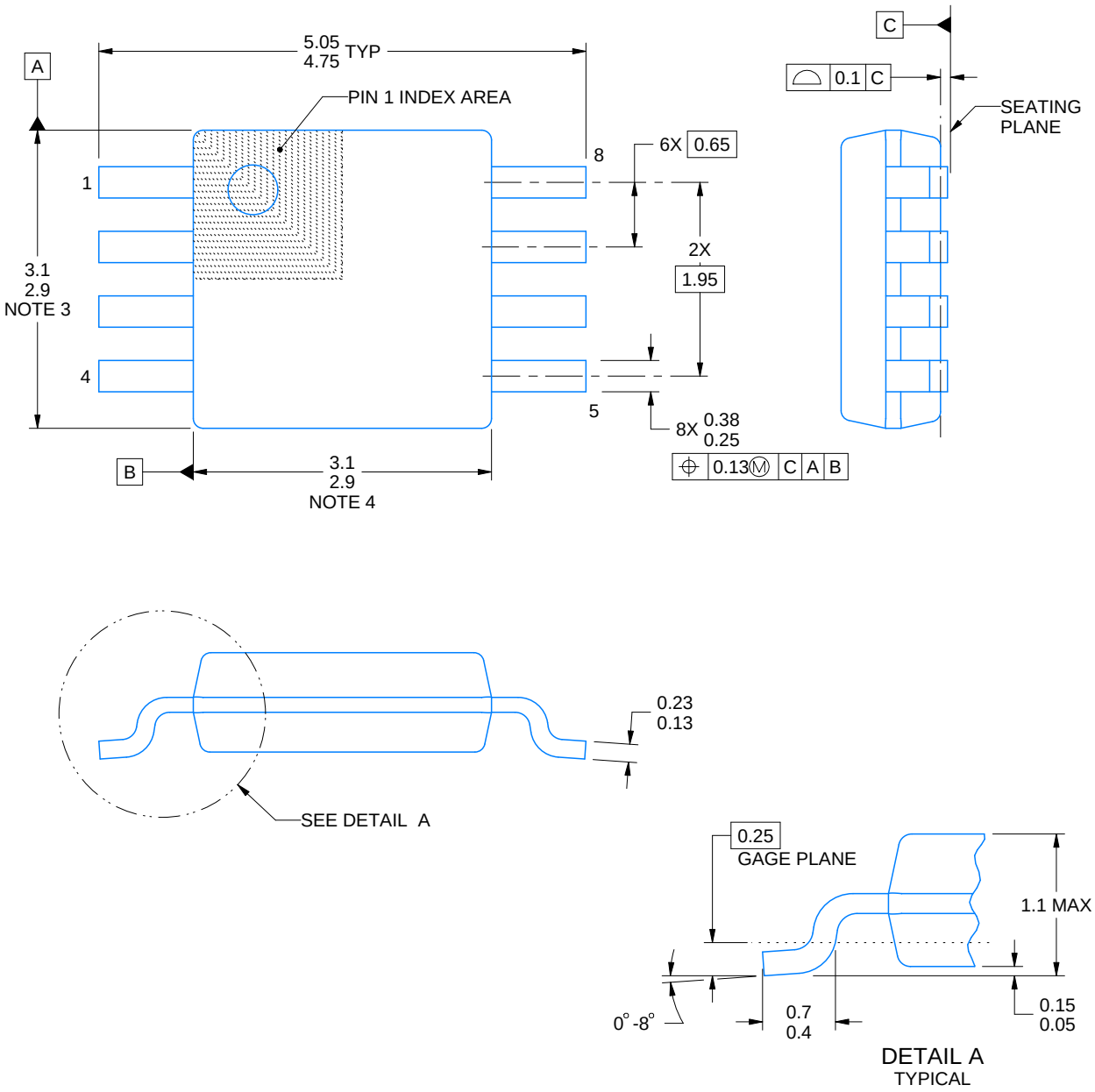
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

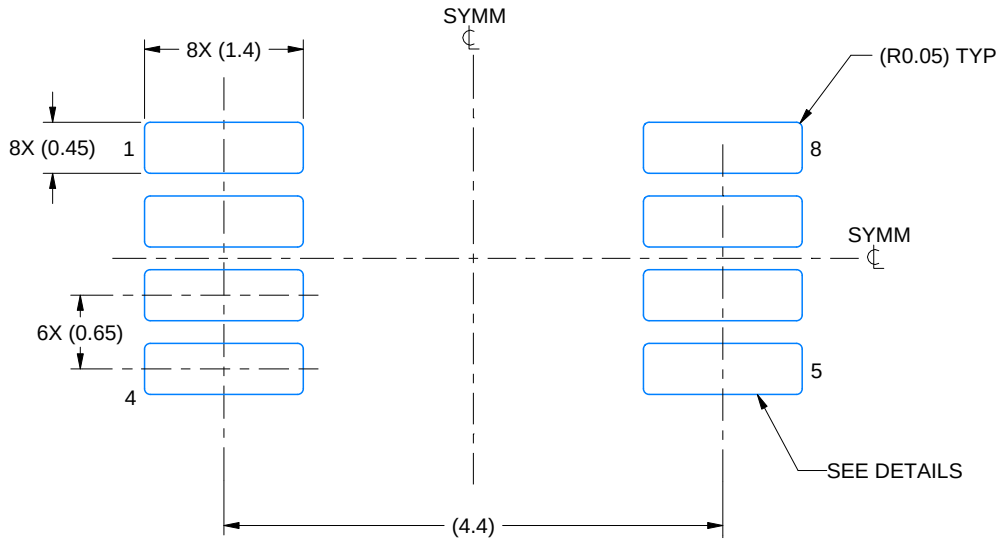
SMALL OUTLINE PACKAGE



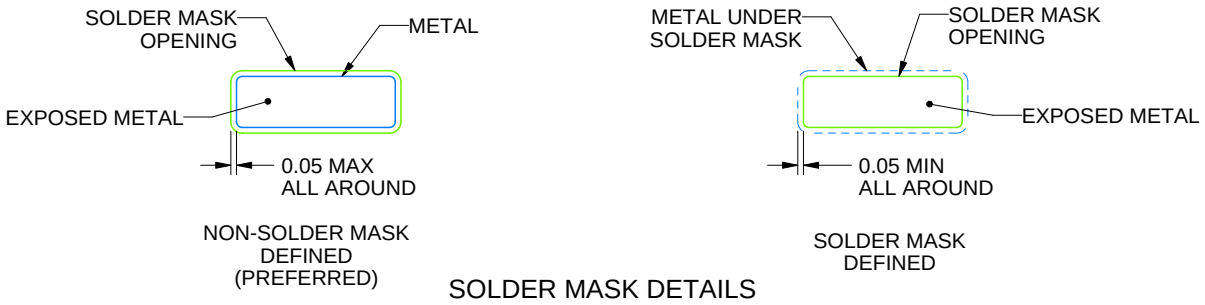
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

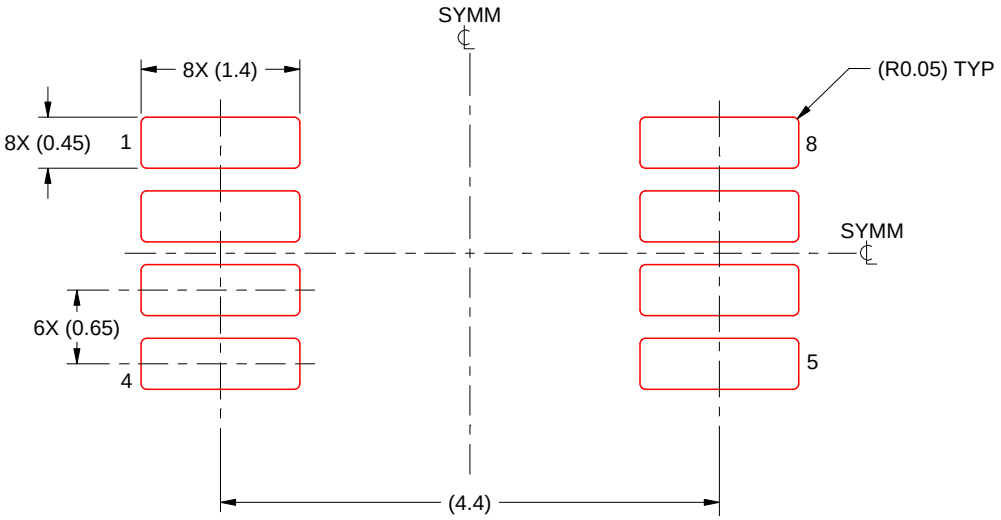


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

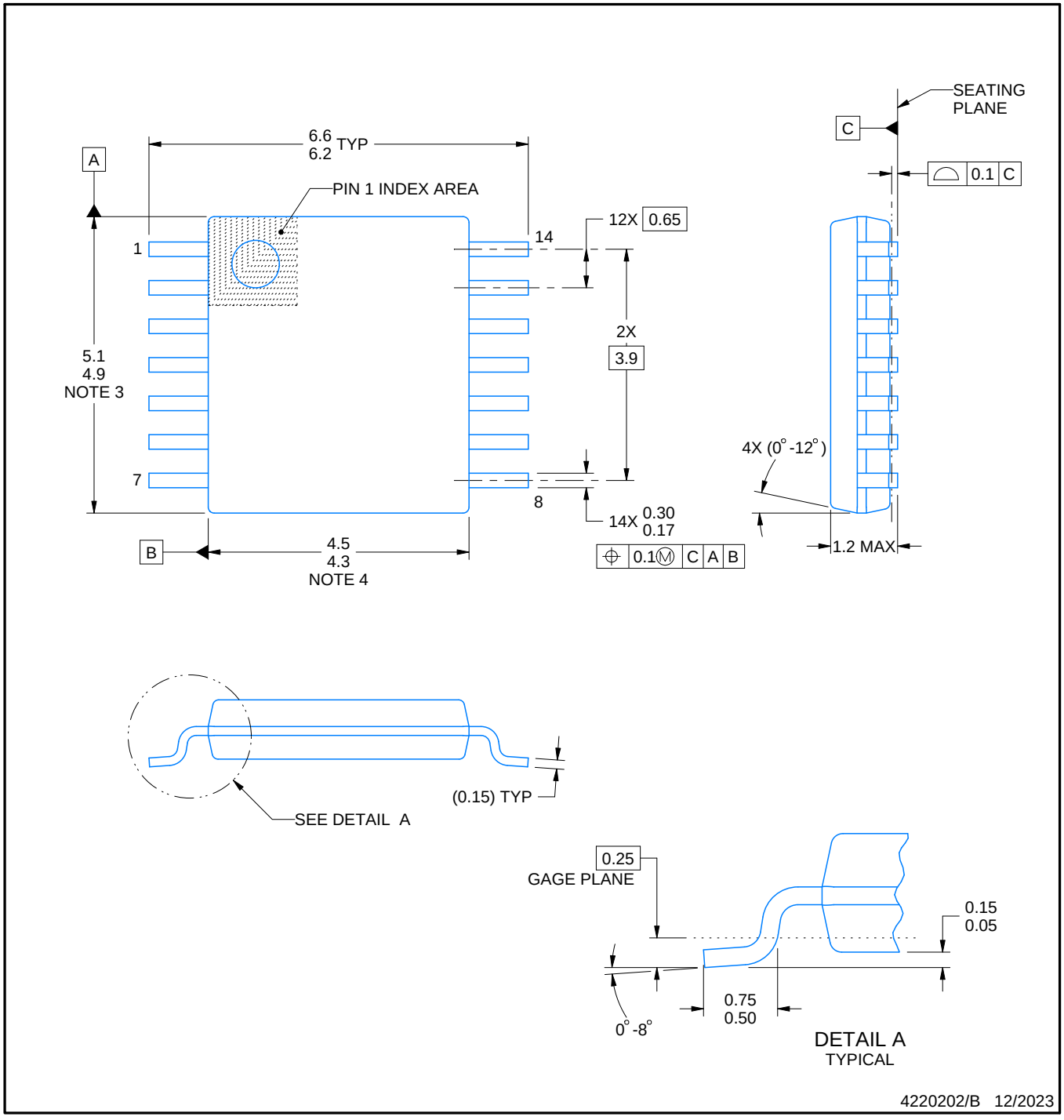
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

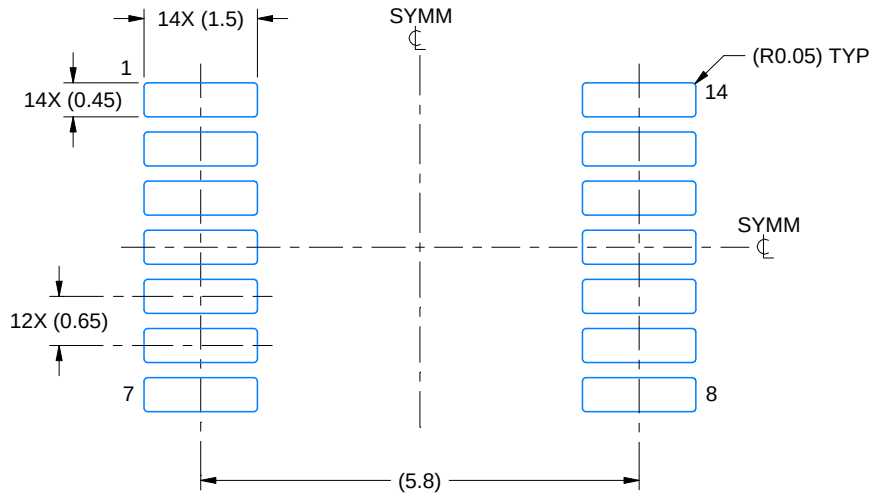
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

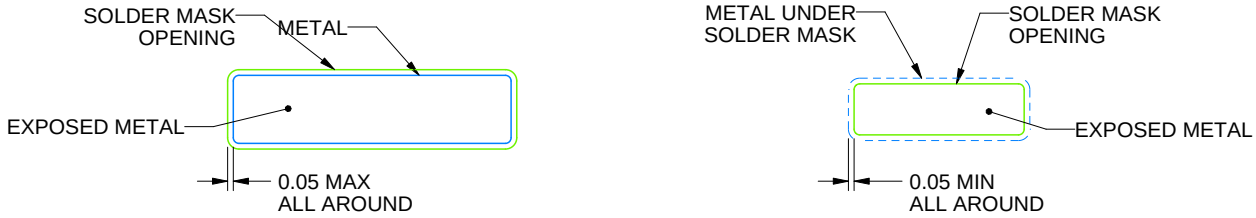


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

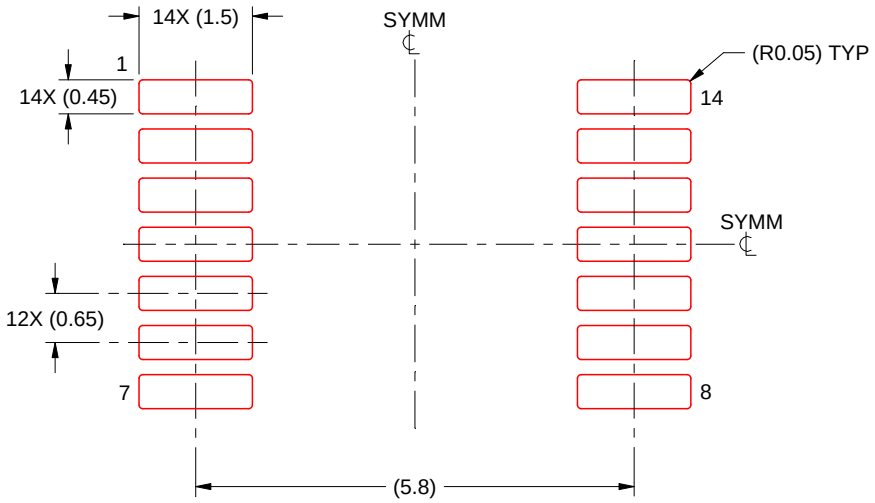


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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