

OPAx170 36V、単一電源、SOT553、低消費電力オペアンプのバリュー・ライン・シリーズ

1 特長

- 電源電圧範囲: 2.7V~36V、 $\pm 1.35V \sim \pm 18V$
- 低ノイズ: $19nV/\sqrt{Hz}$
- RFI フィルタ付きの入力
- 入力範囲は負の電源電圧にも対応
- 入力範囲は正の電源電圧まで動作
- レール・ツー・レール出力
- ゲイン帯域幅: 1.2MHz
- 低い静止電流: アンプごとに110 μ A
- 高い同相除去: 120dB
- 低い入力バイアス電流: 15pA (最大)
- 業界標準のパッケージとMicroパッケージで供給
- WEBENCH® Power Designerにより、OPAx170を使用するカスタム設計を作成

2 アプリケーション

- 電源モジュールのトラッキング・アンプ
- 商業施設の電源
- トランスデューサ・アンプ
- ブリッジ・アンプ
- 温度計測
- ひずみゲージ・アンプ
- 高精度積分器
- バッテリー駆動計測器
- 試験用機器

3 概要

OPA170、OPA2170、OPA4170デバイス(OPAx170)は36V、単一電源、低ノイズのオペアンプ・ファミリで、Microパッケージで供給され、2.7V ($\pm 1.35V$)から36V ($\pm 18V$)までの範囲の電源電圧で動作できます。低い静止電流で優れたオフセット、ドリフト、帯域幅を提供します。シングル、デュアル、クアッドの各製品で同一の仕様を備え、設計の柔軟性を高めています。

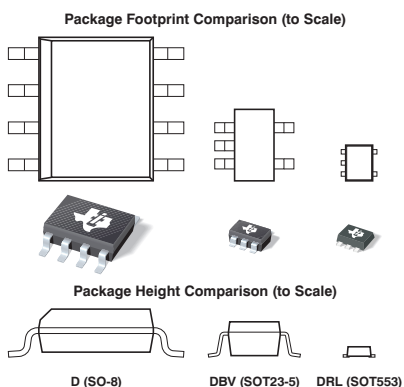
ほとんどのオペアンプでは1つの電源電圧でのみ動作が規定されているのに対して、OPAx170ファミリのオペアンプは2.7V~36Vで動作が規定されています。入力信号が電源レールを超えていても、位相反転は発生しません。OPAx170ファミリは、最大300pFの容量性負荷で安定です。通常の動作時に、入力は負のレールより100mV下、および正のレールから2V以内で動作できます。これらのデバイスは完全なレール・ツー・レール入力で、正のレールを100mV超えて動作しますが、正のレールから2V以内ではパフォーマンスが低下することに注意してください。OPAx170オペアンプは-40°C~+125°Cで動作が規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
OPA170	SOIC (8)	4.90mmx3.91mm
	SOT (5)	1.60mmx1.20mm
	SOT-23 (5)	2.90mmx1.60mm
OPA2170	SOIC (8)	4.90mmx3.91mm
	VSSOP (8)	3.00mmx3.00mm
	VSSOP (8)、microサイズ	2.30mmx2.00mm
	WSO (8)	2.00mmx2.00mm
OPA4170	SOIC (14)	8.65mmx3.91mm
	TSSOP (14)	5.00mmx4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

36Vオペアンプの最小パッケージ



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (December 2017) から Revision E に変更		Page
•	Changed minimum supply voltage from –20 V to 0 V in <i>Absolute Maximum Ratings</i> table	7
•	Changed maximum supply voltage from 20 V to 40 V in <i>Absolute Maximum Ratings</i> table	7

Revision C (March 2016) から Revision D に変更		Page
•	<i>WEBENCH</i> のリンクとセクションおよび「ドキュメントについての通知を受け取る方法」の更新 追加	1
•	8ピンDSG (WSON)パッケージ 追加	1
•	変更 values in <i>Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application</i> from: 250 Ω to: 2.5 Ω	20

Revision B (September 2012) から Revision C に変更		Page
•	「特長」一覧と「概要」セクションの最後の段落に最新のパッケージ指定子を 追加	1
•	「ピンの機能」表、「ESD定格」表、「推奨動作条件」表、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1

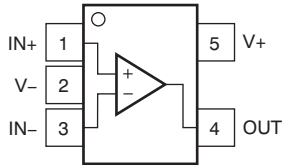
Revision A (September 2011) から Revision B に変更		Page
•	ドキュメントのタイトルに「バリュー・ライン・シリーズ」を 追加	1

5 Device Comparison Table

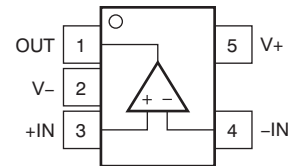
DEVICE	NO OF CHANNELS	PACKAGE-LEAD						
		SOT	SOT23-5	D	DSG	VSSOP	VSSOP (micro size)	TSSOP
OPA170	1	5	5	8	—	—	—	—
OPA2170	2	—	—	8	8	8	8	—
OPA4170	4	—	—	14	—	—	—	14

6 Pin Configuration and Functions

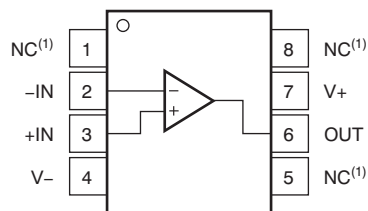
**OPA170 DRL Package
5-Pin SOT
Top View**



**OPA170 DBV Package
5-Pin SOT-23
Top View**



**OPA170 D Package
8-Pin SOIC
Top View**

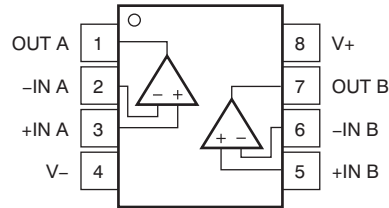


Pin Functions: OPA170

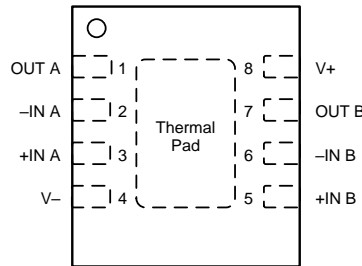
NAME	PIN			I/O	DESCRIPTION
	SOT	SOT-23	D		
IN- (-IN)	3	4	2	I	Negative (inverting) input
IN+ (+IN)	1	3	3	I	Positive (noninverting) input
NC ⁽¹⁾	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	4	1	6	O	Output
V+	5	5	7	—	Positive (highest) power supply
V-	2	2	4	—	Negative (lowest) power supply

(1) NC indicates no internal connection.

OPA2170 D, DGK, and DCU Packages
8-Pin VSSOP, SOIC, and VSSOP (micro size)
Top View



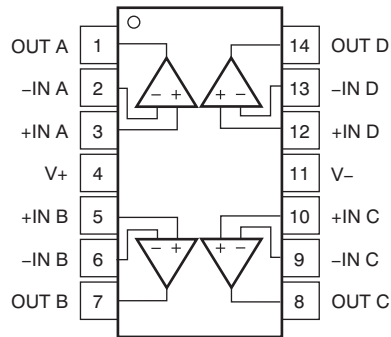
OPA2170 DSG Package
8-Pin WSON
Top View



Pin Functions: OPA2170

NAME	PIN				I/O	DESCRIPTION
	SOIC	VSSOP	VSSOP (micro size)	WSON		
-IN A	2	2	2	2	I	Inverting input, channel A
-IN B	6	6	6	6	I	Inverting input, channel B
+IN A	3	3	3	3	I	Noninverting input, channel A
+IN B	5	5	5	5	I	Noninverting input, channel B
OUT A	1	1	1	1	O	Output, channel A
OUT B	7	7	7	7	O	Output, channel B
V-	4	4	4	4	—	Negative (lowest) power supply
V+	8	8	8	8	—	Positive (highest) power supply

**OPA4170 D and PW Packages
14-Pin SOIC and TSSOP
Top View**



Pin Functions: OPA4170

NAME	PIN		I/O	DESCRIPTION
	SOIC	TSSOP		
-IN A	2	2	I	Inverting input, channel A
-IN B	6	6	I	Inverting input, channel B
-IN C	9	9	I	Inverting input, channel C
-IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V-	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.⁽¹⁾

	MIN	MAX	UNIT
Supply voltage	0	40	V
Single supply voltage		40	V
Signal input pin voltage	(V ₋) – 0.5	(V ₊) + 0.5	V
Signal input pin current	–10	10	mA
Output short-circuit current ⁽²⁾	Continuous		
Operating ambient temperature, T _A	–55	150	°C
Junction temperature, T _J		150	°C
Storage temperature, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _S	Supply voltage (V ₊ – V ₋)	2.7	36	V
T _A	Operating temperature	–40	125	°C

7.4 Thermal Information: OPA170

THERMAL METRIC ⁽¹⁾		OPA170			UNIT
		D (SOIC)	DBV (SOT-23)	DRL (SOT)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.9	133.9	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	42.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information: OPA2170

THERMAL METRIC ⁽¹⁾		OPA2170				UNIT
		D (SOIC)	DCU (VSSOP, micro size)	DGK (VSSOP)	DSG (WSON)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	175.2	180	71.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.1	74.9	55	89.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	22.2	130	38.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.2	1.6	5.3	3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.8	22.8	120	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	13	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Thermal Information: OPA4170

THERMAL METRIC ⁽¹⁾		OPA4170		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.7 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$T_A = 25^\circ\text{C}$		0.25	± 1.8	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 2	mV
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 0.3	± 2	$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage vs power supply	$V_S = 4\text{ V}$ to 36 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1	± 5	$\mu\text{V}/\text{V}$
	Channel separation, dc			5		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
I_B	Input bias current	$T_A = 25^\circ\text{C}$		± 8	± 15	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 3.5	nA
I_{OS}	Input offset current	$T_A = 25^\circ\text{C}$		± 4	± 15	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 3.5	nA
NOISE						
	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		2		μV_{PP}
e_n	Input voltage noise density	$f = 100\text{ Hz}$		22		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		19		$\text{nV}/\sqrt{\text{Hz}}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range ⁽¹⁾		$(V-) - 0.1$		$(V+) - 2$	V
CMRR	Common-mode rejection ratio	$V_S = \pm 2\text{ V}$, $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	90	104		dB
		$V_S = \pm 18\text{ V}$, $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	104	120		dB
INPUT IMPEDANCE						
	Differential			$100 \parallel 3$		$\text{M}\Omega \parallel \text{pF}$
	Common-mode			$6 \parallel 3$		$10^{12}\ \Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_S = 4\text{ V}$ to 36 V , $(V-) + 0.35\text{ V} < V_O < (V+) - 0.35\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			1.2		MHz
SR	Slew rate	$G = +1$		0.4		$\text{V}/\mu\text{s}$
t_s	Settling time	To 0.1%, $V_S = \pm 18\text{ V}$, $G = +1$, 10-V step		20		μs
		To 0.01% (12-bit), $V_S = \pm 18\text{ V}$, $G = +1$, 10-V step		28		μs
	Overload recovery time	$V_{IN} \times \text{Gain} > V_S$		2		μs
THD+N	Total harmonic distortion + noise	$G = +1$, $f = 1\text{ kHz}$, $V_O = 3\text{ V}_{RMS}$		0.0002%		

- (1) The input range can be extended beyond $(V+) - 2\text{ V}$ up to $V+$. See the [Typical Characteristics](#) and [Application and Implementation](#) sections for additional information.

Electrical Characteristics (continued)

 at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from positive rail	$I_L = 0\text{ mA}$, $V_S = 4\text{ V to }36\text{ V}$	10			mV
		I_L sourcing 1 mA , $V_S = 4\text{ V to }36\text{ V}$	115			mV
V_O	Voltage output swing from negative rail	$I_L = 0\text{ mA}$, $V_S = 4\text{ V to }36\text{ V}$			8	mV
		I_L sinking 1 mA , $V_S = 4\text{ V to }36\text{ V}$			70	mV
V_O	Voltage output swing from rail	$V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$; $T_A = -40^\circ\text{C to }+125^\circ\text{C}$	(V-) + 0.03		(V+) – 0.05	V
		$R_L = 10\text{ k}\Omega$, $A_{OL} \geq 110\text{ dB}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$	(V-) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current		–20		17	mA
C_{LOAD}	Capacitive load drive		See Typical Characteristics			pF
R_O	Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0\text{ A}$		900		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	$I_O = 0\text{ A}$; $T_A = 25^\circ\text{C}$		110	145	μA
		$I_O = 0\text{ A}$; $T_A = -40^\circ\text{C to }+125^\circ\text{C}$			155	μA
TEMPERATURE						
	Specified range		–40		125	$^\circ\text{C}$
	Operating range		–55		150	$^\circ\text{C}$

7.8 Typical Characteristics

$V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, (unless otherwise noted)

表 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3
Offset Voltage vs Common-Mode Voltage	图 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	图 5
Offset Voltage vs Power Supply	图 6
I_B and I_{OS} vs Common-Mode Voltage	图 7
Input Bias Current vs Temperature	图 8
Output Voltage Swing vs Output Current (Maximum Supply)	图 9
CMRR and PSRR vs Frequency (Referred-to-Input)	图 10
CMRR vs Temperature	图 11
PSRR vs Temperature	图 12
0.1-Hz to 10-Hz Noise	图 13
Input Voltage Noise Spectral Density vs Frequency	图 14
THD+N Ratio vs Frequency	图 15
THD+N vs Output Amplitude	图 16
Quiescent Current vs Temperature	图 17
Quiescent Current vs Supply Voltage	图 18
Open-Loop Gain and Phase vs Frequency	图 19
Closed-Loop Gain vs Frequency	图 20
Open-Loop Gain vs Temperature	图 21
Open-Loop Output Impedance vs Frequency	图 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	图 23 , 图 24
No Phase Reversal	图 25
Positive Overload Recovery	图 26
Negative Overload Recovery	图 27
Small-Signal Step Response (100 mV)	图 28 , 图 29
Large-Signal Step Response	图 30 , 图 31
Large-Signal Settling Time (10-V Positive Step)	图 32
Large-Signal Settling Time (10-V Negative Step)	图 33
Short-Circuit Current vs Temperature	图 34
Maximum Output Voltage vs Frequency	图 35
EMIRR IN+ vs Frequency	图 36

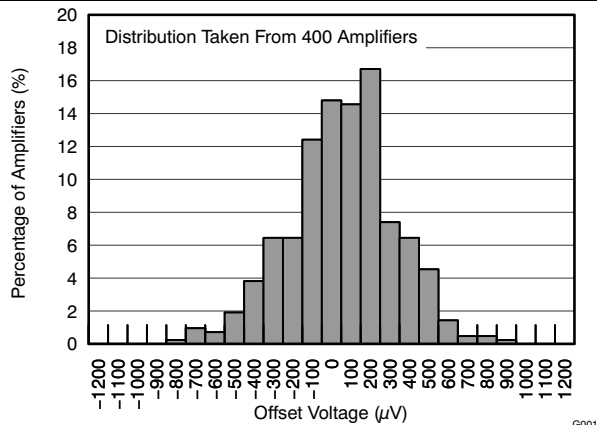


FIG 1. Offset Voltage Production Distribution

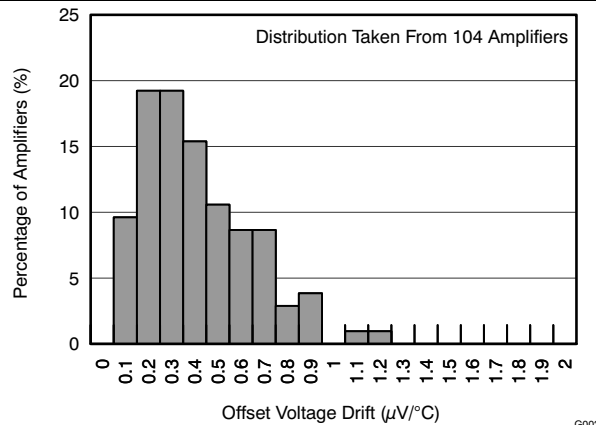


FIG 2. Offset Voltage Drift Distribution

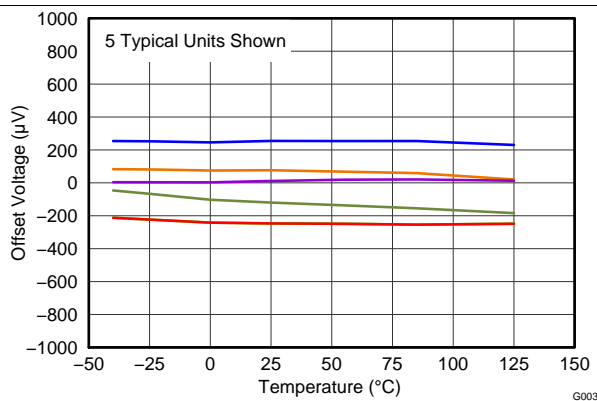


FIG 3. Offset Voltage vs Temperature

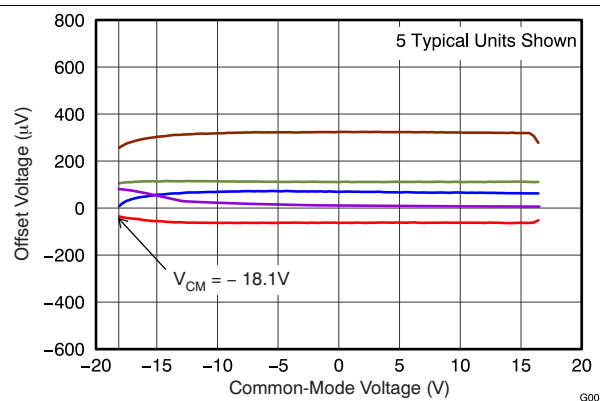


FIG 4. Offset Voltage vs Common-Mode Voltage

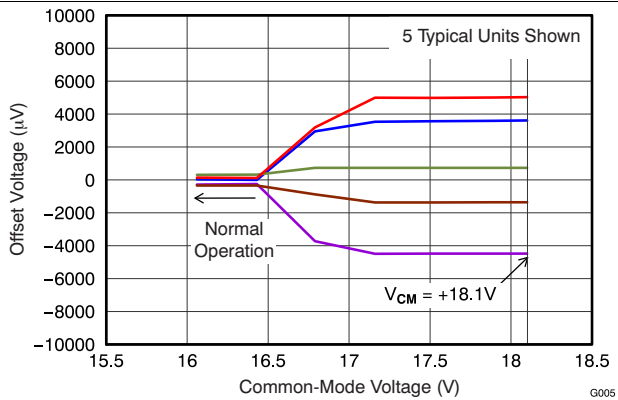


FIG 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

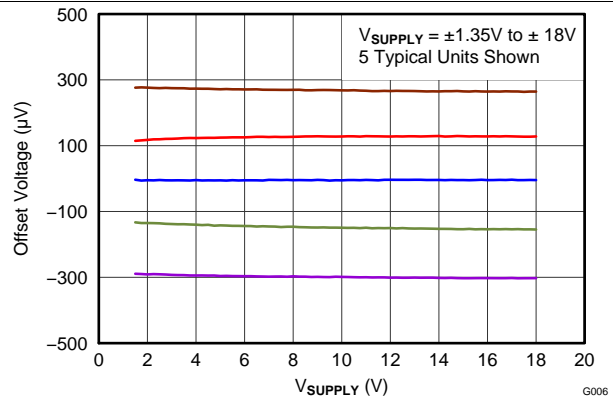


FIG 6. Offset Voltage vs Power Supply

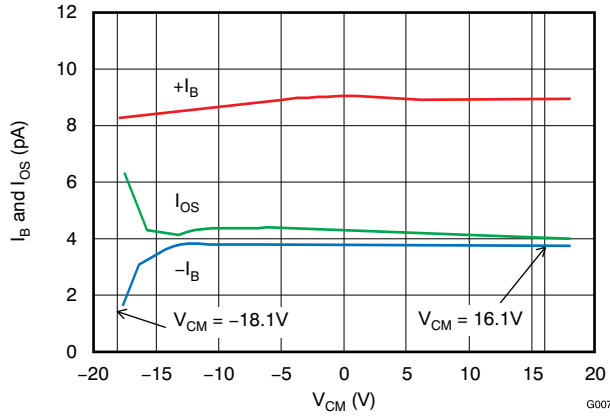


图 7. I_B and I_{OS} vs Common-Mode Voltage

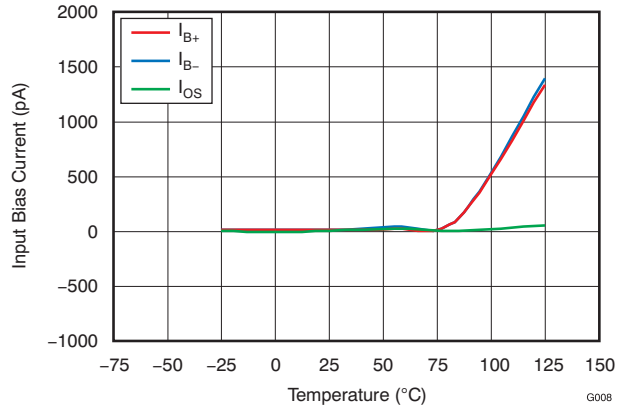


图 8. Input Bias Current vs Temperature

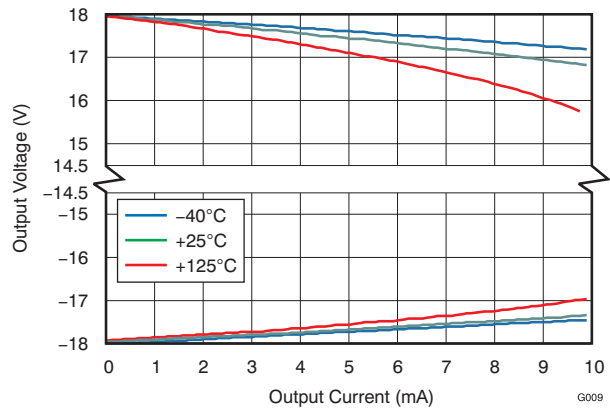


图 9. Output Voltage Swing vs Output Current (Maximum Supply)

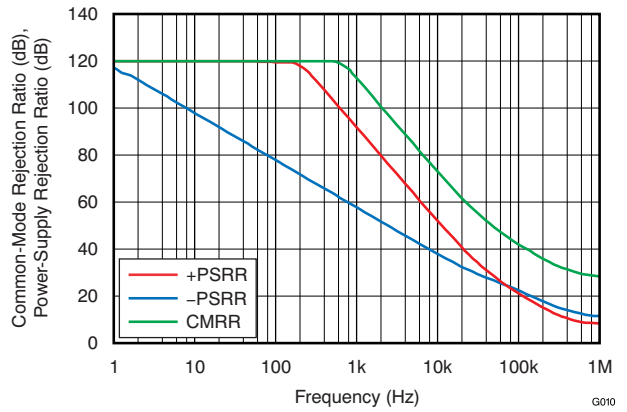


图 10. CMRR and PSRR vs Frequency (Referred-to Input)

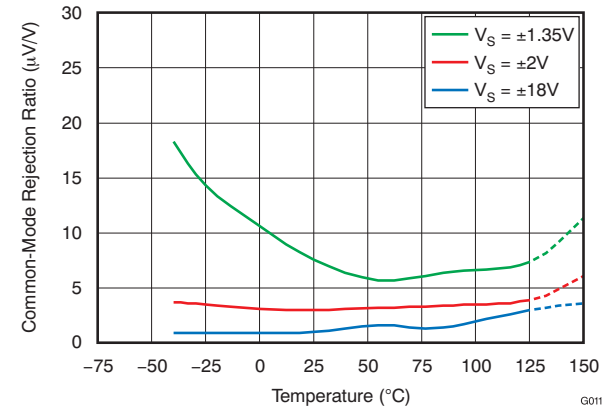


图 11. CMRR vs Temperature

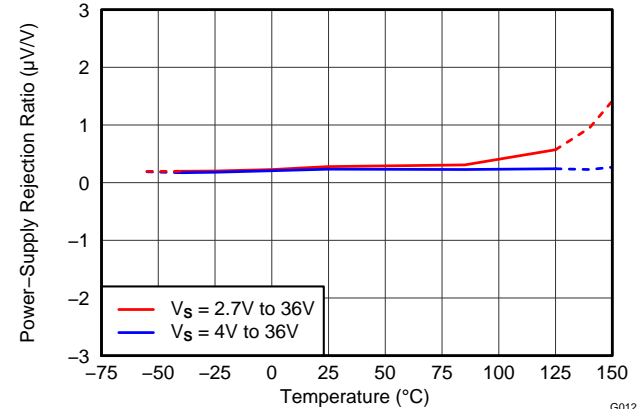


图 12. PSRR vs Temperature

OPA170, OPA2170, OPA4170

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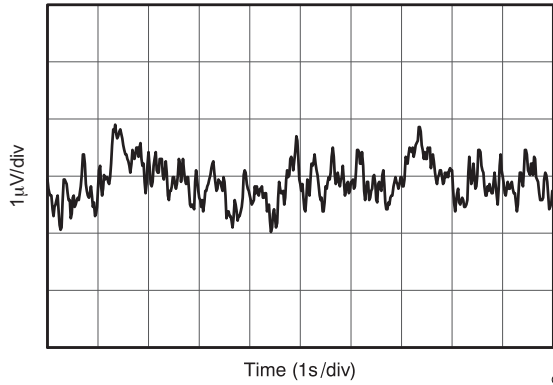


Figure 13. 0.1-Hz to 10-Hz Noise

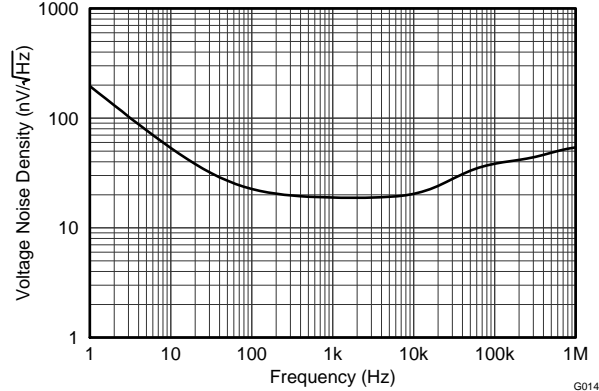


Figure 14. Input Voltage Noise Spectral Density vs Frequency

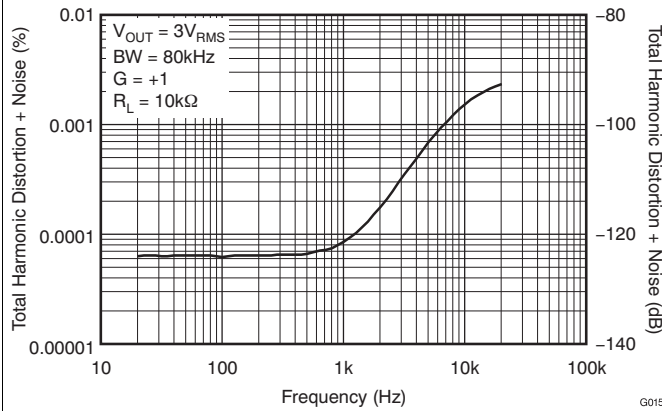


Figure 15. THD+N Ratio vs Frequency

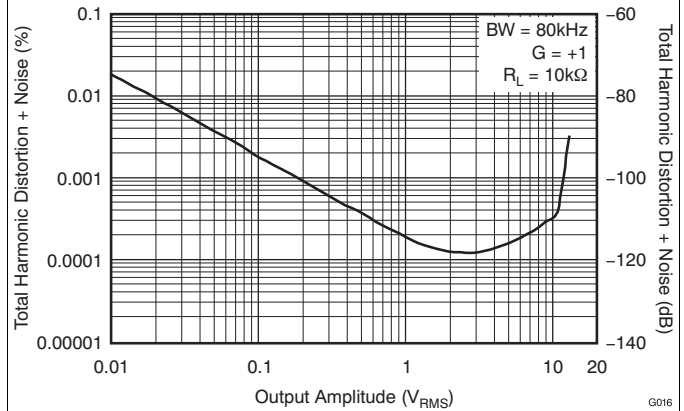


Figure 16. THD+N vs Output Amplitude

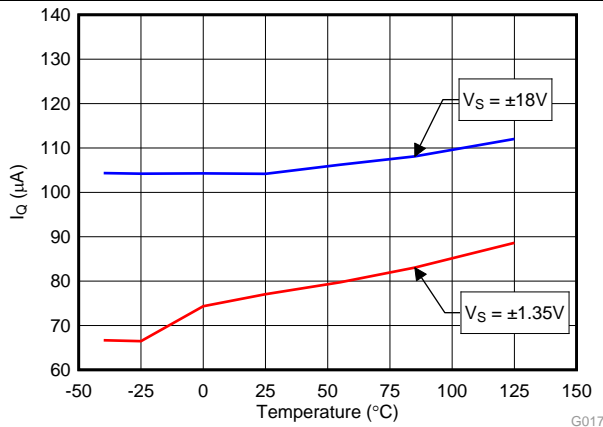


Figure 17. Quiescent Current vs Temperature

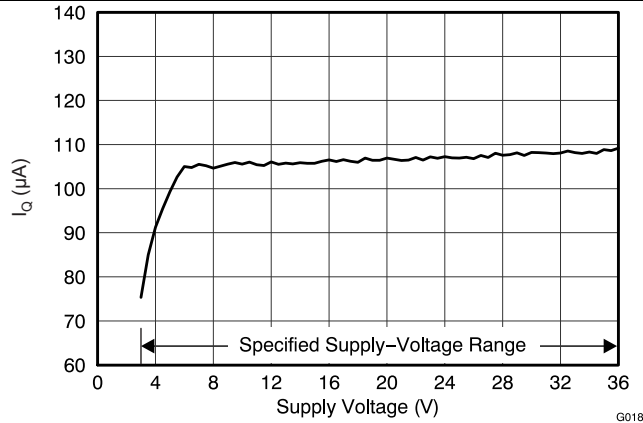


Figure 18. Quiescent Current vs Supply Voltage

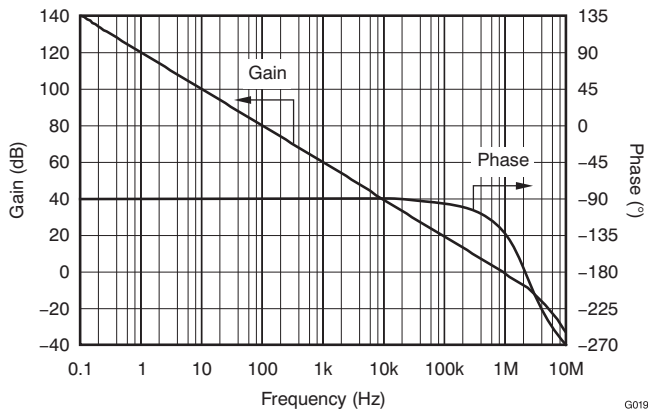


Figure 19. Open-Loop Gain and Phase vs Frequency

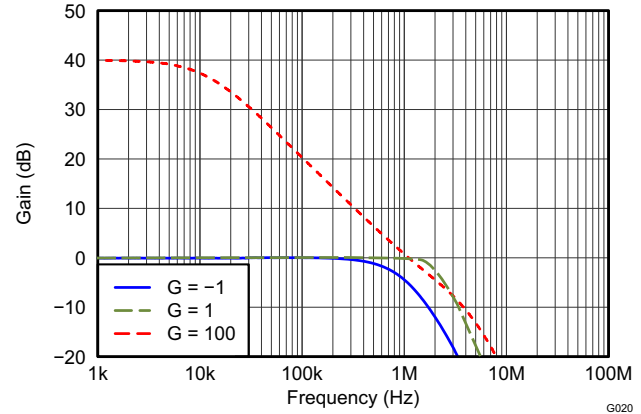


Figure 20. Closed-Loop Gain vs Frequency

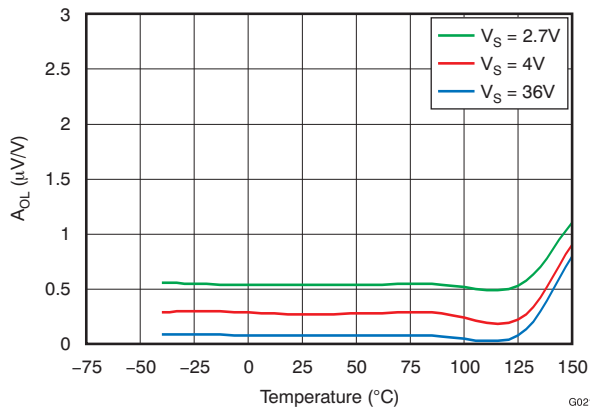


Figure 21. Open-Loop Gain vs Temperature

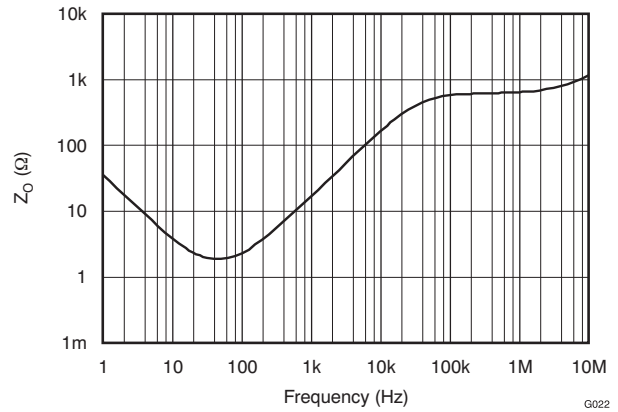


Figure 22. Open-Loop Output Impedance vs Frequency

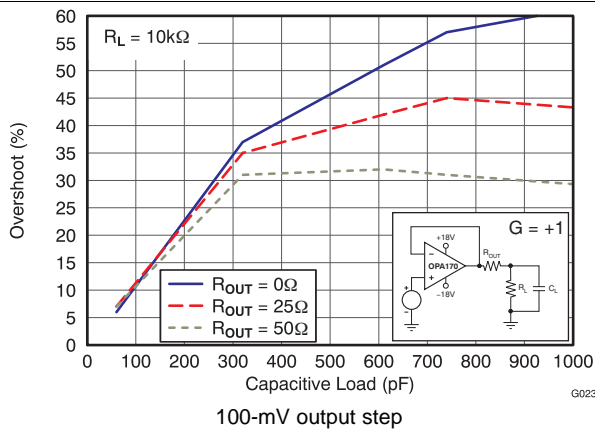


Figure 23. Small-Signal Overshoot vs Capacitive Load

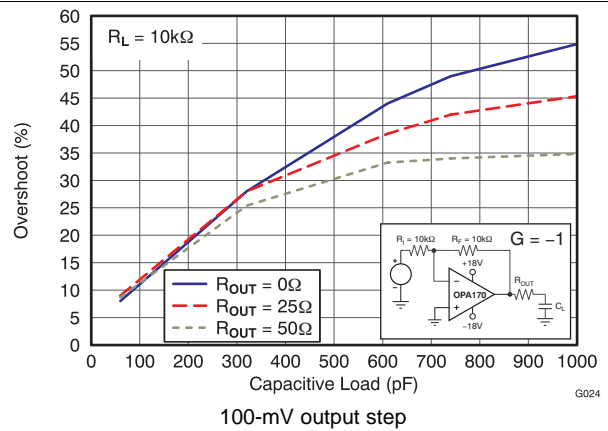


Figure 24. Small-Signal Overshoot vs Capacitive Load

OPA170, OPA2170, OPA4170

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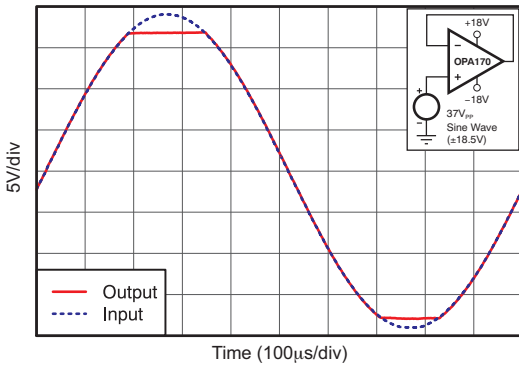


Figure 25. No Phase Reversal

G025

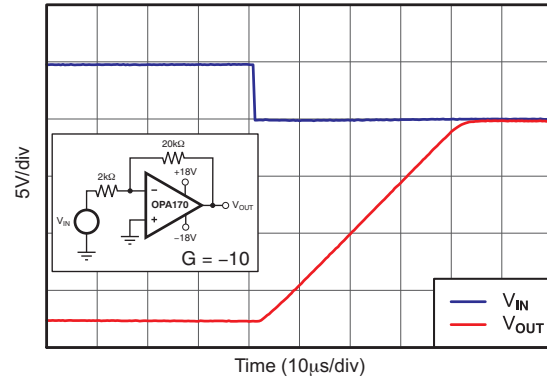


Figure 26. Positive Overload Recovery

G026

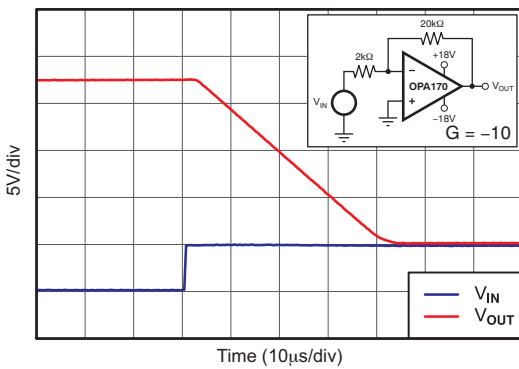


Figure 27. Negative Overload Recovery

G027

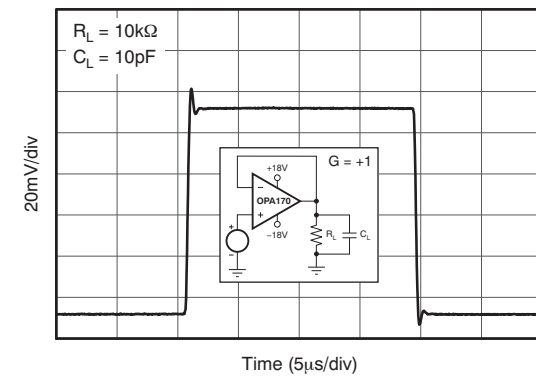


Figure 28. Small-Signal Step Response (100 mV)

G028

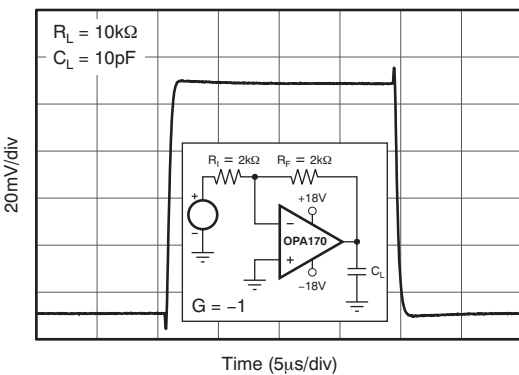


Figure 29. Small-Signal Step Response (100 mV)

G029

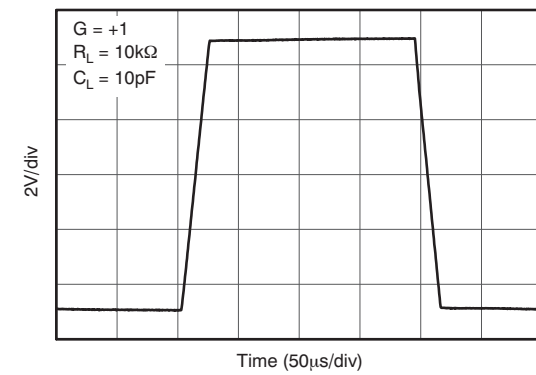
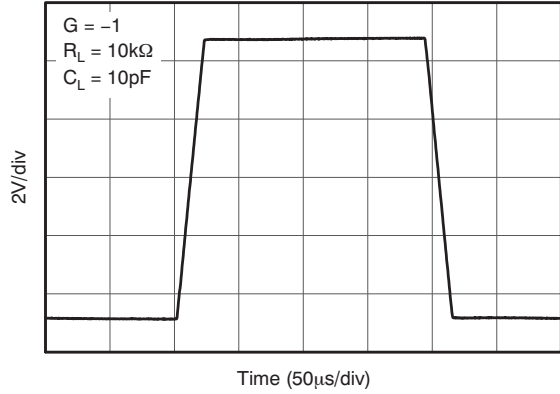


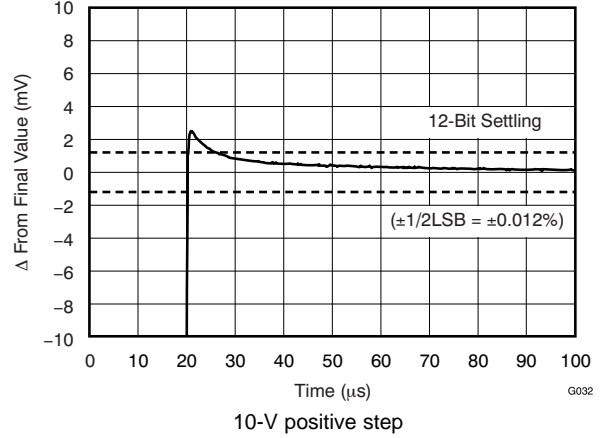
Figure 30. Large-Signal Step Response

G030



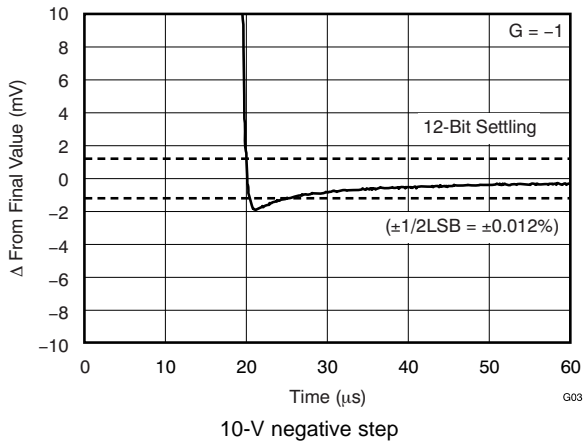
G031

31. Large-Signal Step Response



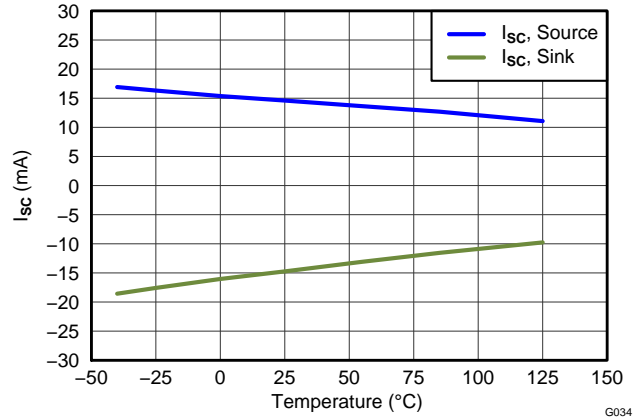
G032

32. Large-Signal Settling Time



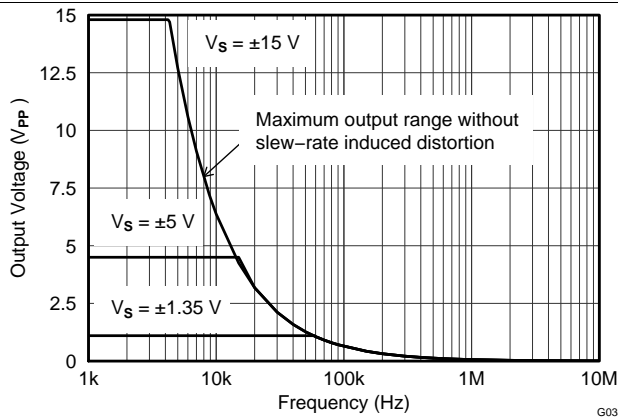
G033

33. Large-Signal Settling Time



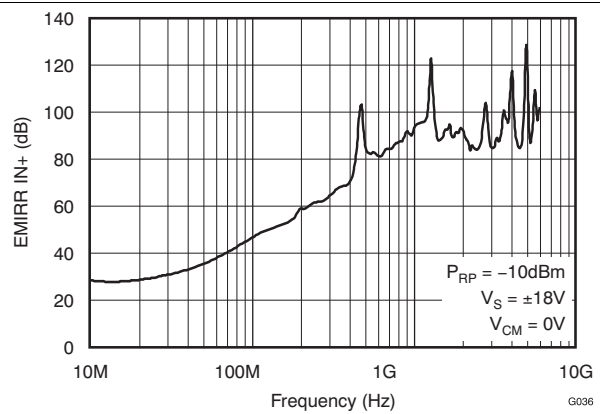
G034

34. Short-Circuit Current vs Temperature



G035

35. Maximum Output Voltage vs Frequency



G036

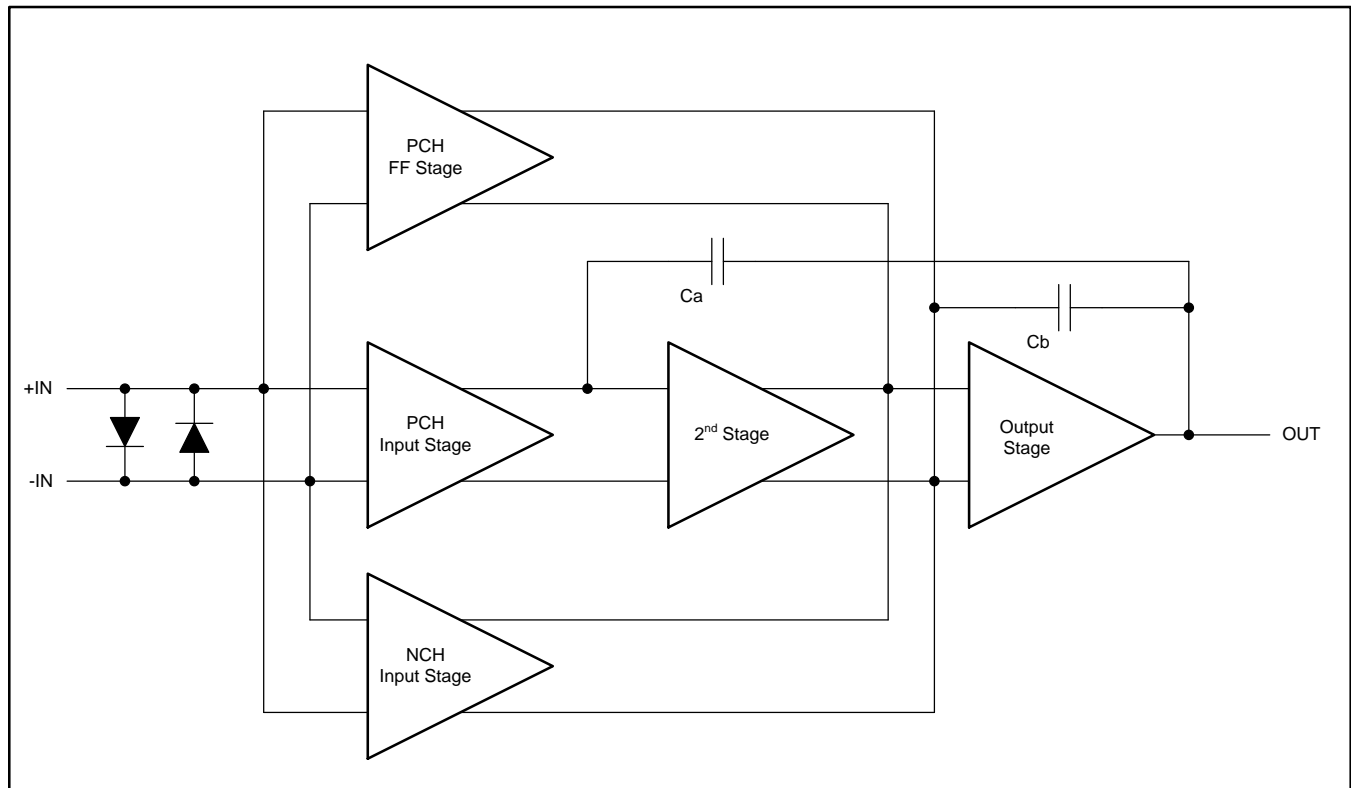
36. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The OPAx170 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only $2 \mu\text{V}/^\circ\text{C}$ provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL} .

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The OPAx170 family of amplifiers is specified for operation from 2.7 V to 36 V ($\pm 1.35 \text{ V}$ to $\pm 18 \text{ V}$). Many of the specifications apply from -40°C to $+125^\circ\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

Feature Description (continued)

8.3.2 Phase-Reversal Protection

The OPAx170 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx170 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in [Figure 37](#).

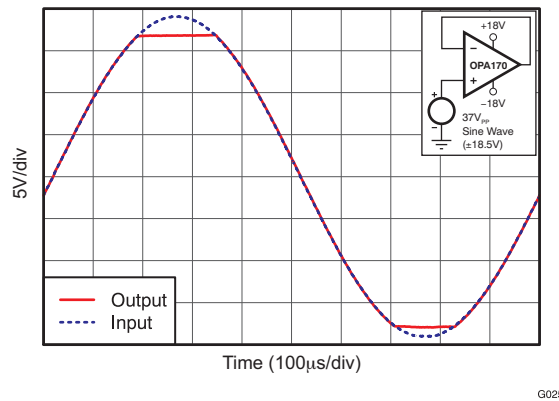


Figure 37. No Phase Reversal

8.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. [Figure 38](#) illustrates the ESD circuits contained in the OPAx170 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

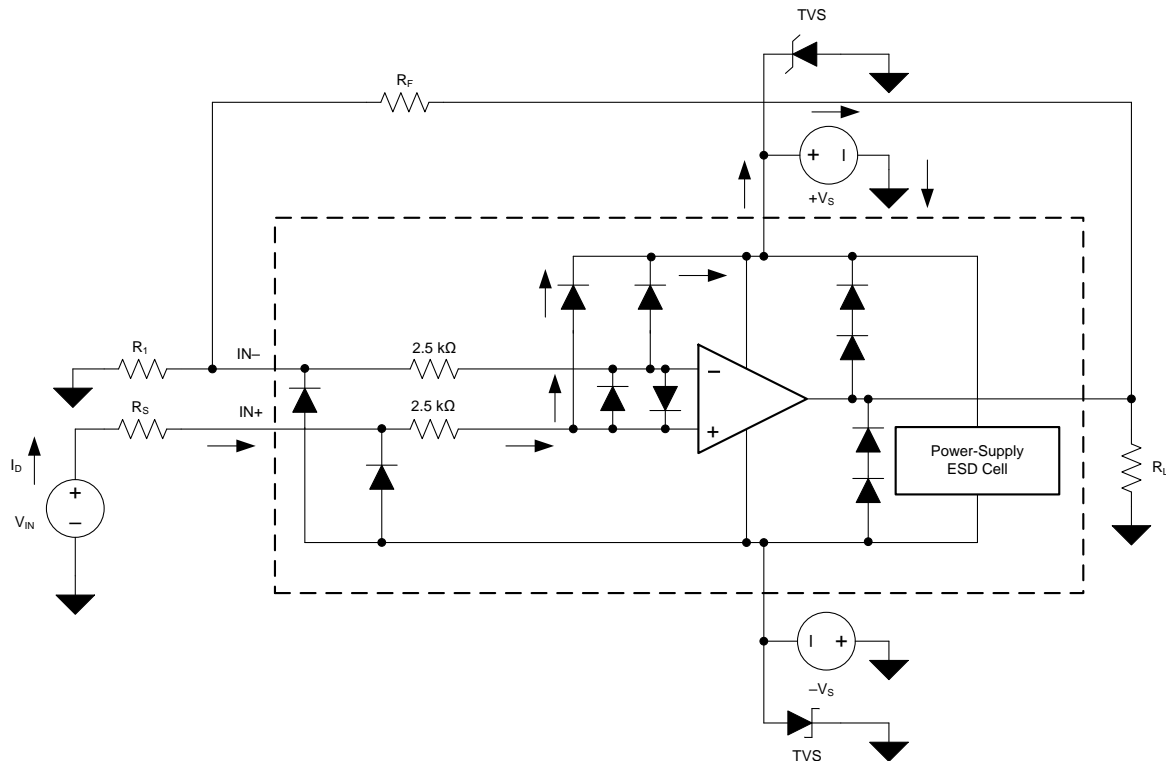
Feature Description (continued)


FIG 38. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx170 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (refer to FIG 38), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

FIG 38 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($V+$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $V+$ can sink the current, one of the upper input steering diodes conducts and directs current to $V+$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (continued)

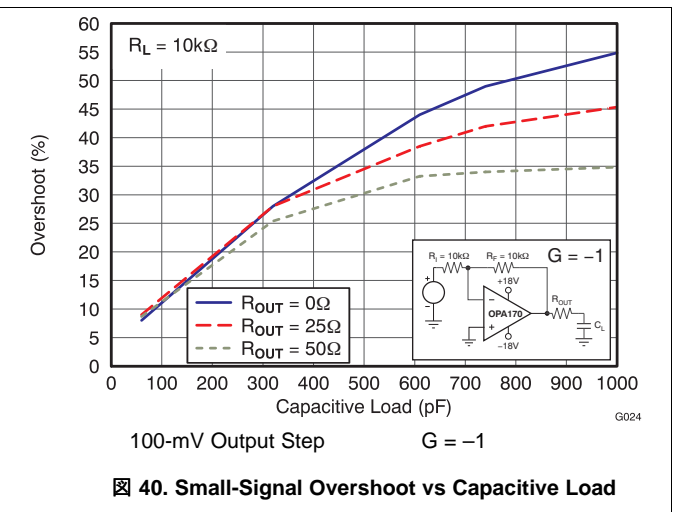
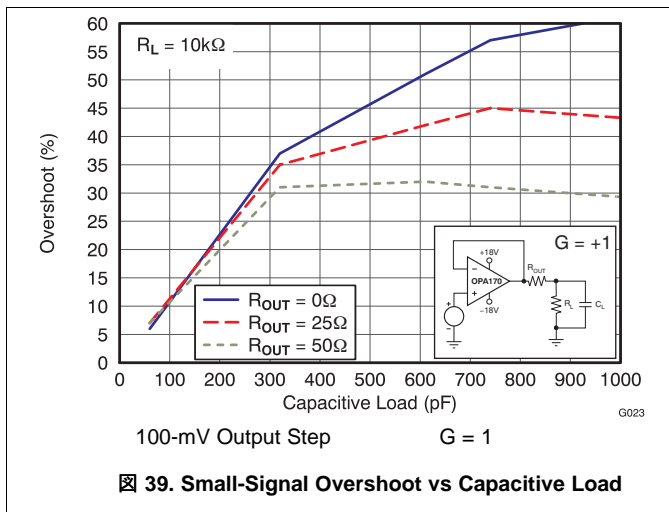
Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ($V+$ or $V-$) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see [Figure 38](#). Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAx170 input pins are protected from excessive differential voltage with back-to-back diodes; see [Figure 38](#). In most circuit applications, the input protection circuitry has no effect. However, in low-gain or $G = 1$ circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx170. [Figure 38](#) illustrates an example configuration that implements a current-limiting feedback resistor.

8.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx170 have been optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Refer to [Figure 39](#) and [Figure 40](#) illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT} . Also, refer to applications bulletin AB-028, *Feedback Plots Define Op Amp AC Performance*, for details of analysis techniques and application circuits.



8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAX170 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in [表 2](#).

表 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
	vs temperature	12		μV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
Gain-bandwidth product		0.3		MHz
Slew rate		0.3		V/μs

8.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAX170 is approximately 2 μs.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx170 family of operational amplifiers provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1- μ F capacitors are adequate. Follow the additional recommendations in [Layout Guidelines](#) in order to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier (potentially causing instability). One method of stabilizing the amplifier in such applications is to add an isolation resistor between the amplifier output and the capacitive load. The design process for selecting this resistor is given in [Typical Application](#).

9.2 Typical Application

This circuit can be used to drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an operational amplifier. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

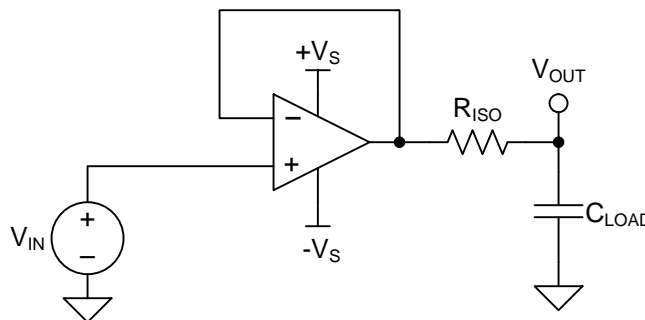


图 41. Unity-Gain Buffer With R_{ISO} Stability Compensation

9.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (± 15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μ F, 0.1 μ F, and 1 μ F
- Phase margin: 45° and 60°

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the OPAx170 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance

Typical Application (continued)

- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Unity-Gain Buffer

Figure 41 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 41. Not shown in Figure 41 is the open-loop output resistance of the operational amplifier, R_o .

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \tag{1}$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by $(R_o + R_{ISO})$ and C_{LOAD} . Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and $1/\beta$ is 20 dB/decade. Figure 42 depicts the concept. The $1/\beta$ curve for a unity-gain buffer is 0 dB.

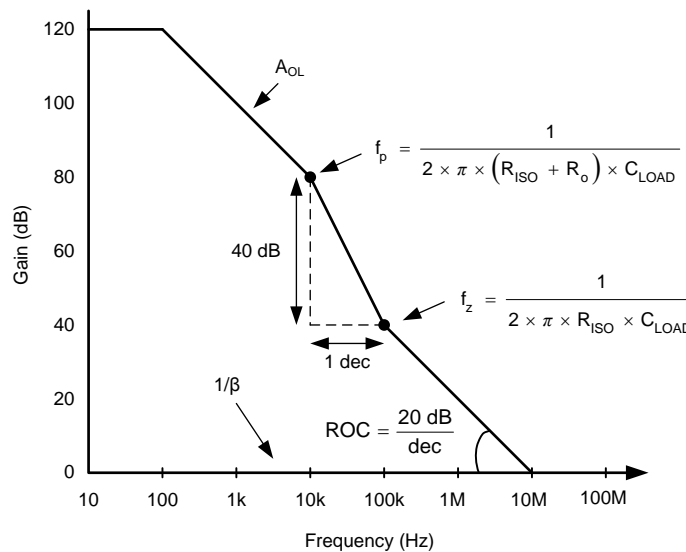


Figure 42. Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o . In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA170, see the Precision Design, [Capacitive Load Drive Solution Using an Isolation Resistor](#).

Table 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.3 Application Curve

Using the described methodology, the values of R_{ISO} that yield phase margins of 45° and 60° for various capacitive loads were determined. The results are shown in [Figure 43](#).

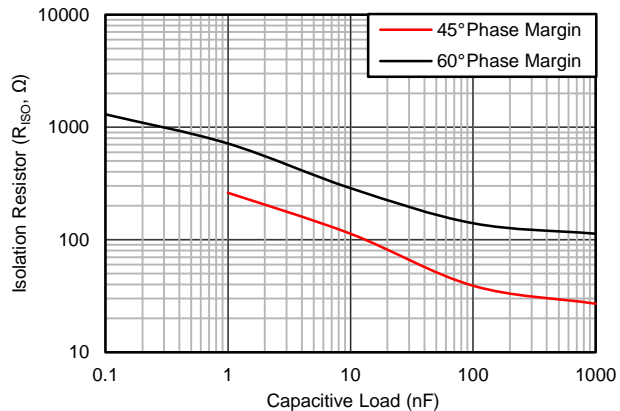


Figure 43. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

10 Power Supply Recommendations

The OPAx170 is specified for operation from 2.7 V to 36 V (± 1.35 V to ± 18 V); many specifications apply from -40°C to 85°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

注意

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see application report [SLOA089, Circuit Board Layout Techniques](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 45](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

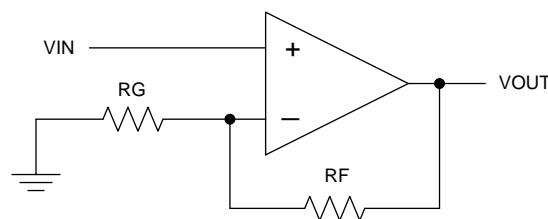
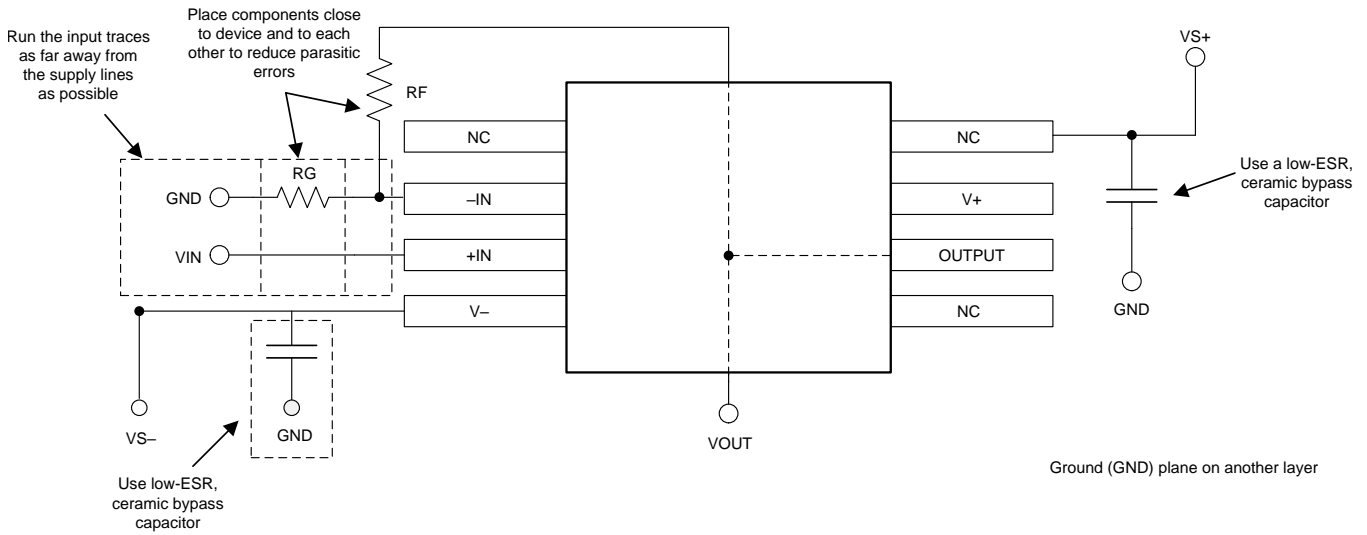


Figure 44. Schematic Representation

Layout Example (continued)



45. Operational Amplifier Board Layout for a Noninverting Configuration

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

12.1.2 開発サポート

12.1.2.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

12.1.2.2 DIPアダプタ評価モジュール

DIPアダプタ評価モジュール・ツールを使用すると、小さな表面実装ICのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU(SOIC-8)、PW(TSSOP-8)、DGK(MSOP-8)、DBV(SOT23-6、SOT23-5、およびSOT23-3)、DCK(SC70-6およびSC70-5)、およびDRL(SOT563-6)のTIパッケージに対応しています。DIPアダプタ評価モジュールは、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

12.1.2.3 ユニバーサル・オペアンプ評価モジュール

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のICパッケージ・タイプ向けの回路のプロトタイプ作成を容易にします。この評価モジュール基板は、多くの異なる回路を簡単かつ迅速に構築できるように設計されています。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、およびSOT23のパッケージがすべてサポートされています。

注

これらの基板には部品が搭載されていないため、ユーザーが独自のICを供給する必要があります。ユニバーサル・オペアンプ評価モジュールを注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

12.1.2.4 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、<http://www.ti.com/ww/en/analog/precision-designs/>からオンラインで入手できます。

デバイス・サポート (continued)

12.1.2.5 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

12.1.2.6 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designerにより、OPAx170デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WBENCHでご覧になれます。

12.2 ドキュメントのサポート

12.2.1 関連資料

参照資料については、以下をご覧ください(www.ti.comからダウンロードできます)。

- 『フィードバック・プロットによるオペアンプAC性能の定義』
- 『絶縁抵抗の使用による容量性負荷駆動のソリューション』
- 『基板のレイアウト技法』

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA170	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2170	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4170	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

コミュニティ・リソース (continued)

TI E2E™オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.6 商標

TINA-TI, E2E are trademarks of Texas Instruments.
 WEBENCH is a registered trademark of Texas Instruments.
 TINA, DesignSoft are trademarks of DesignSoft, Inc.
 All other trademarks are the property of their respective owners.

12.7 静電気放電に関する注意事項



これらのデバイスは、限定的なESD (静電破壊) 保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA170AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A	Samples
OPA170AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI	Samples
OPA170AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI	Samples
OPA170AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A	Samples
OPA170AIDRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAQ	Samples
OPA170AIDRLT	ACTIVE	SOT-5X3	DRL	5	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAQ	Samples
OPA2170AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A	Samples
OPA2170AIDCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC	Samples
OPA2170AIDCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC	Samples
OPA2170AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPNI	Samples
OPA2170AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPNI	Samples
OPA2170AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A	Samples
OPA2170AIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U	Samples
OPA2170AIDSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U	Samples
OPA4170AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170	Samples
OPA4170AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170	Samples
OPA4170AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170	Samples
OPA4170AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA170, OPA2170, OPA4170 :

● Automotive : [OPA170-Q1](#), [OPA2170-Q1](#), [OPA4170-Q1](#)

● Enhanced Product : [OPA170-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA170AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA170AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA170AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA170AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA170AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA170AIDRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA170AIDRLT	SOT-5X3	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA2170AIDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2170AIDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2170AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2170AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2170AIDSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2170AIDSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA4170AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4170AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

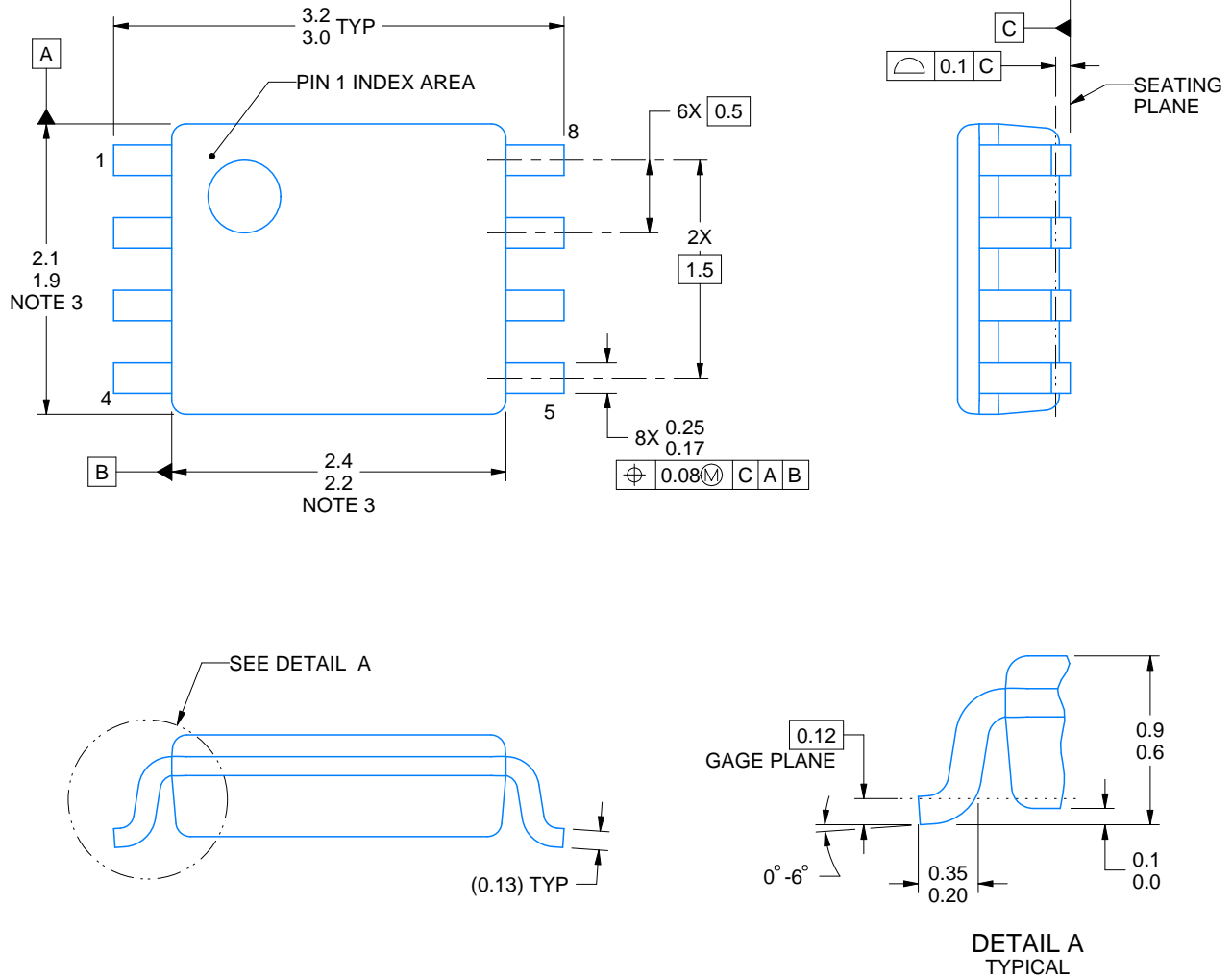

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA170AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA170AIDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA170AIDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA170AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA170AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA170AIDRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
OPA170AIDRLT	SOT-5X3	DRL	5	250	202.0	201.0	28.0
OPA2170AIDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
OPA2170AIDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
OPA2170AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2170AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2170AIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2170AIDSGT	WSON	DSG	8	250	210.0	185.0	35.0
OPA4170AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4170AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA170AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2170AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2170AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4170AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4170AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5



4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

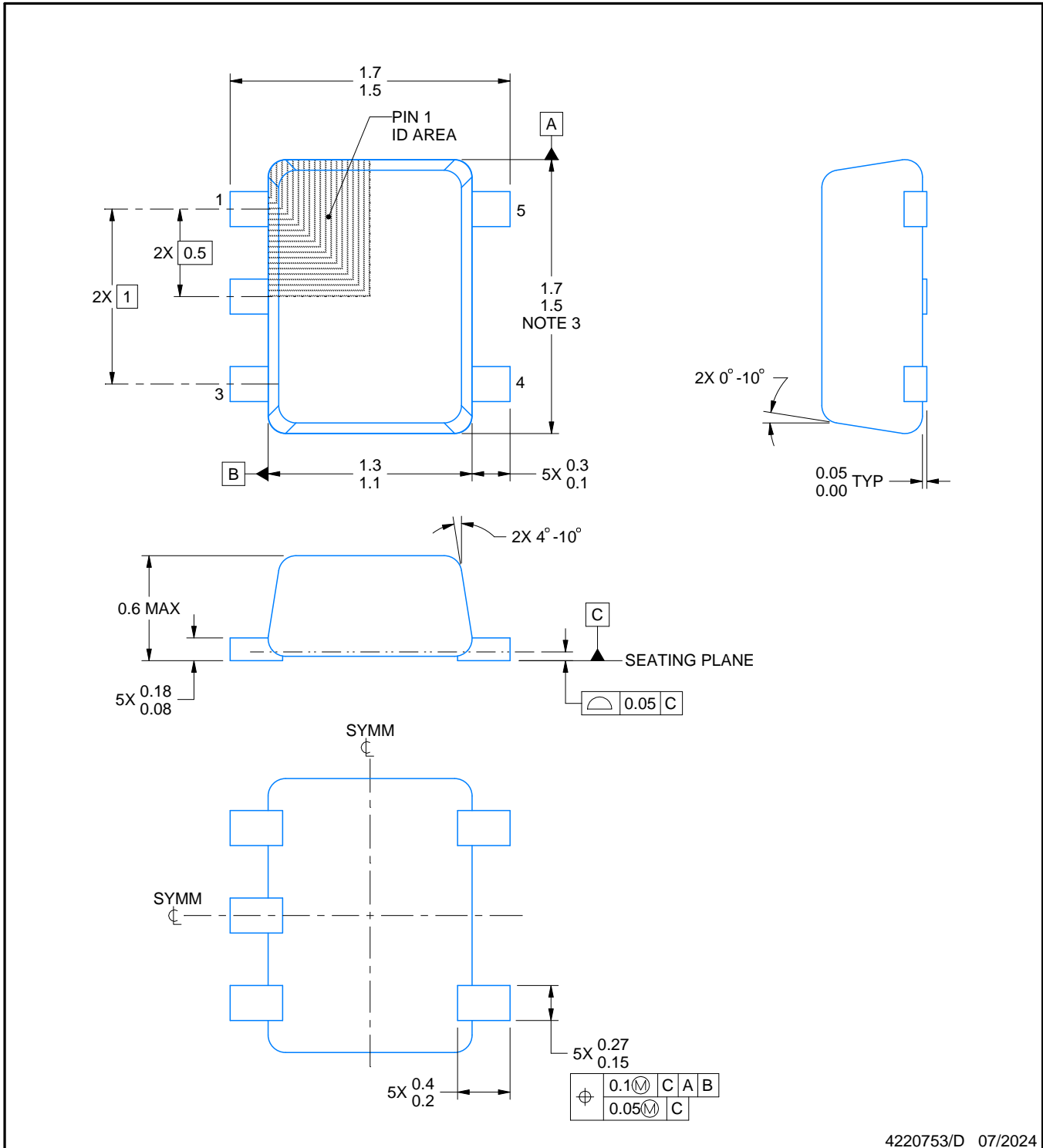
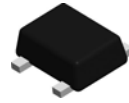


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220753/D 07/2024

NOTES:

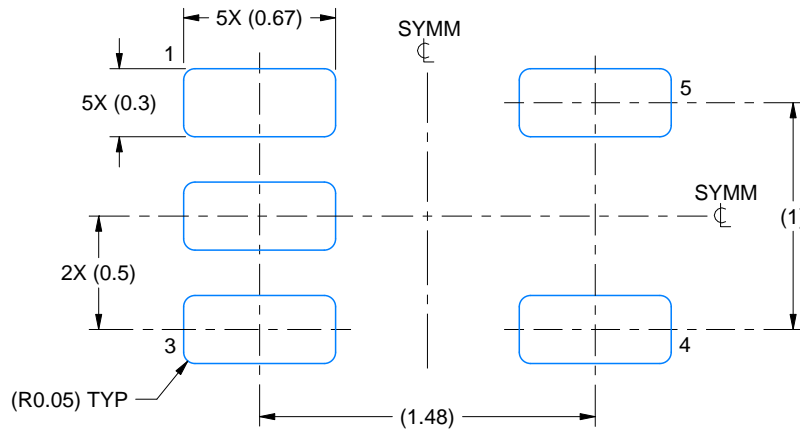
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

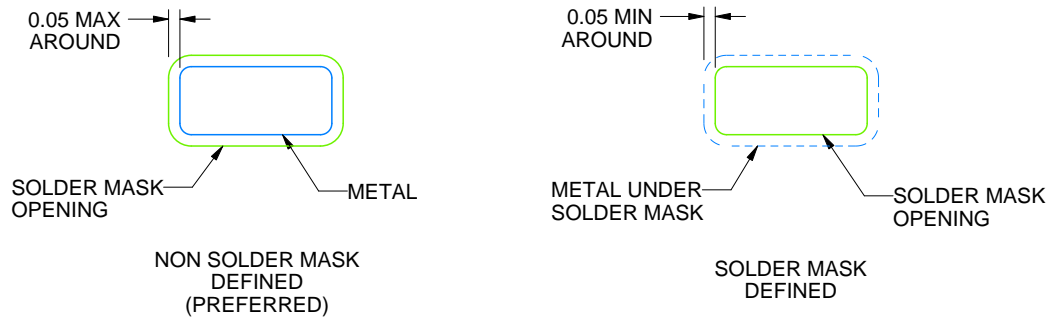
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/D 07/2024

NOTES: (continued)

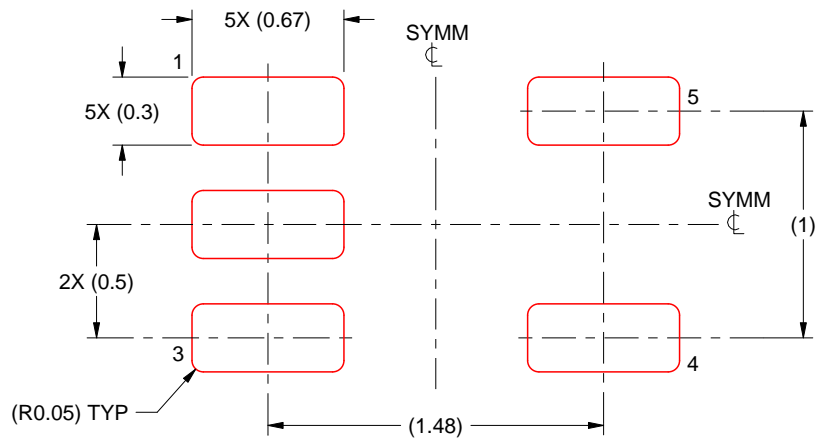
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/D 07/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

DSG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

NOTES:

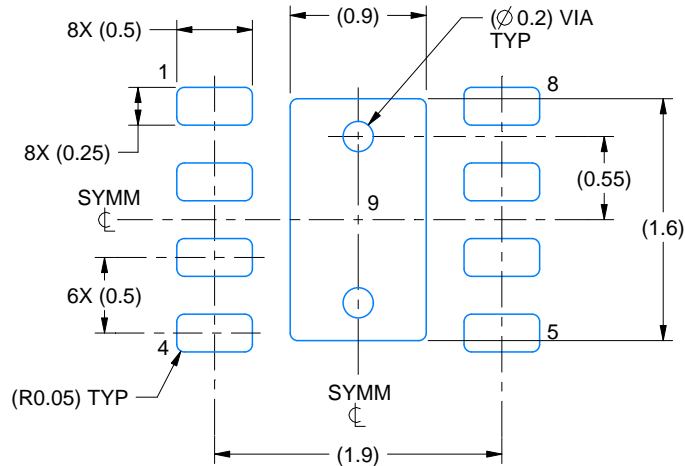
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

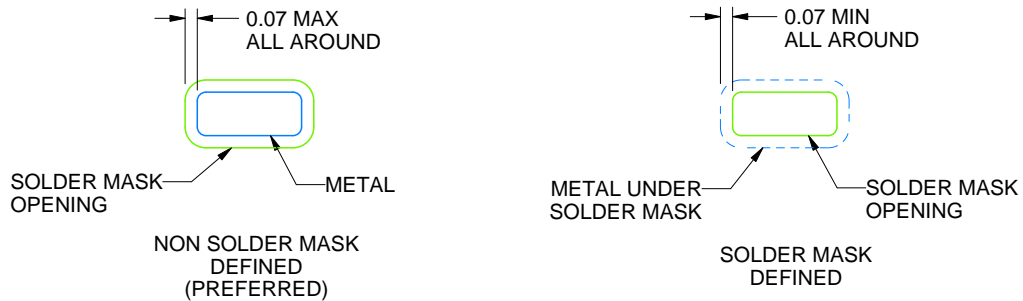
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

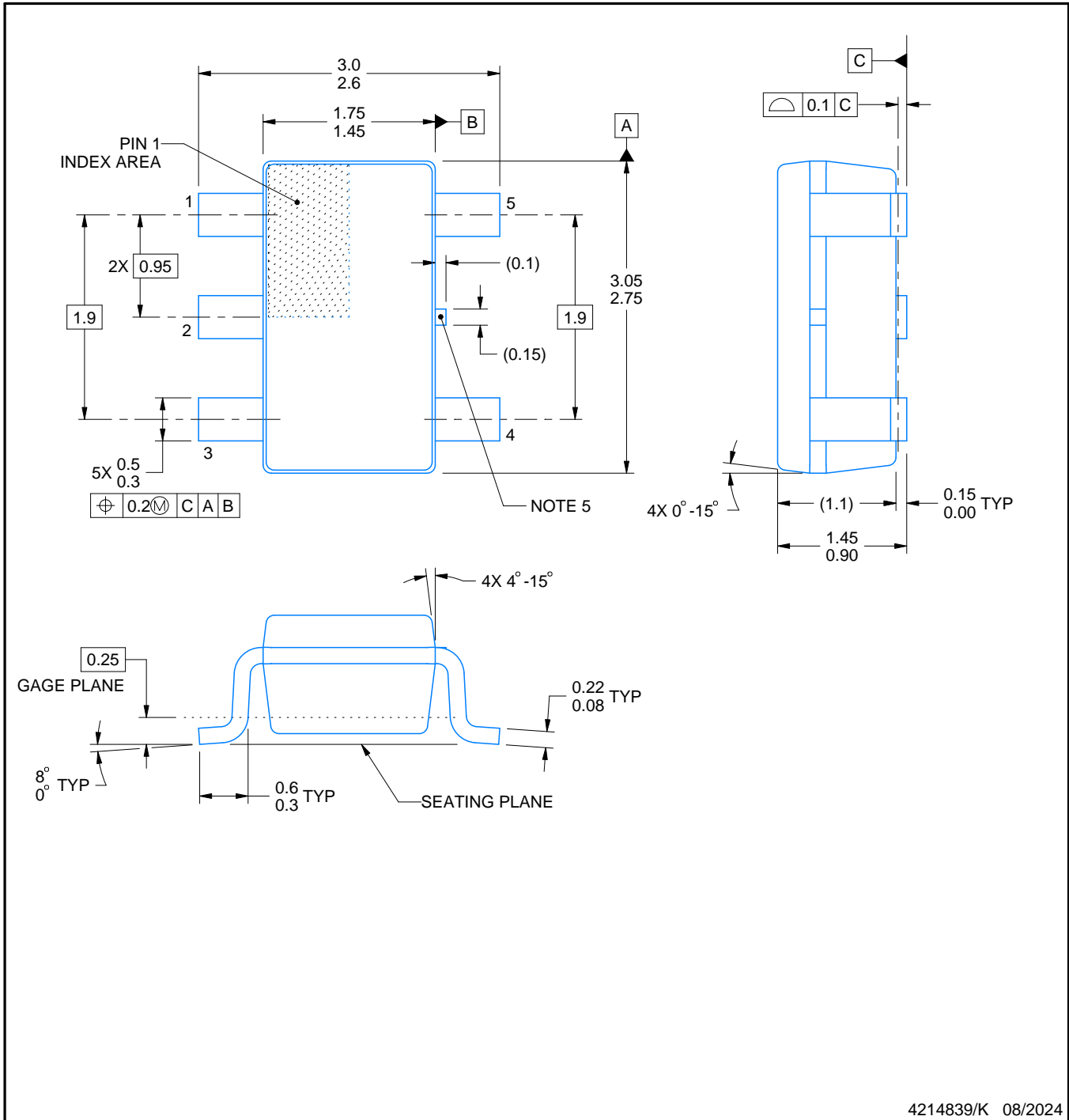
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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