Texas Instruments

OPA188-Q1, OPA2188-Q1

JAJSD37 – APRIL 2017

OPAx188-Q1高精度、低ノイズ、レール・ツー・レール出力、36V、ゼロドリフト、車載用グレード・オペアンプ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - OPA188-Q1デバイス温度グレード1: -40℃～+125℃
  - OPA2188-Q1デバイス温度グレード2: -40℃～+105℃
  - デバイスHBM ESD分類レベル1C
  - デバイスCDM ESD分類レベルC5
- 広い電源電圧範囲: ±2V～±18V
- 低いオフセット電圧: 25μV (最大値)
- ゼロドリフト: 0.03μV/℃
- 低ノイズ: 8.8nV/√Hz
  - 0.1Hz～10Hzのノイズ: 0.25μV$_{PP}$
- 非常に優れたDC精度
  - PSRR: 142dB
  - CMRR: 146dB
  - オープンループ・ゲイン: 136dB
- ゲイン帯域幅: 2MHz
- 静止電流: 510μA (最大値)
- 広い電源電圧範囲: ±2V～±18V
- レール・ツー・レール出力
- 入力に負のレールも含む
- RFIフィルタ付きの入力

2 アプリケーション

- HEV/EVのパワートレイン
  - DC/DCコンバータ
  - トラクション・インバータ
- 高精度の安全性とセンシング: (ブレーキ、位置、乗客の在席の検出)
- 高精度の監督と監視

3 概要

OPAx188-Q1オペアンプ・ファミリは、TI独自のゼロ・ドリフト技術により、低いオフセット電圧(最大値25μV)と、時間や温度に対してほぼゼロのドリフト係数を実現しています。この小型で高精度、低静止電流のアンプ・ファミリは入力インピーダンスが高く、レールから15mV以内のレール・ツー・レール出力を提供します。入力同相範囲には、負のレールも含まれます。4V～36V (±2 V～±18 V)の単電源またはデュアル電源を使用できます。

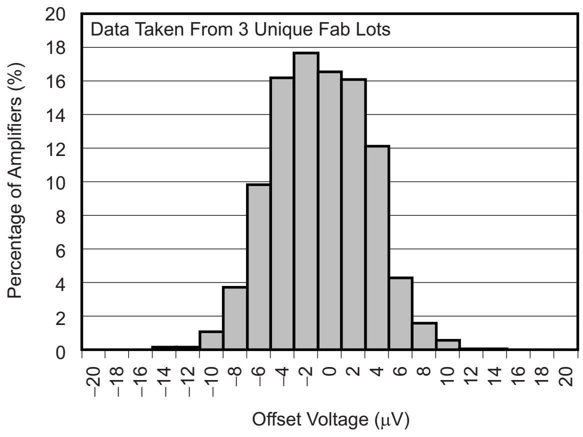
OPA188-Q1とOPA2188-Q1は、いずれもVSSOP-8で供給されます。単一チャネル・バージョン(OPA188-Q1)は-40℃～+125℃、デュアル・チャネル・バージョン(OPA2188-Q1)は-40℃～+105℃で完全に動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(typ)
OPA188-Q1	VSSOP (8)	3.00mm×3.00mm
OPA2188-Q1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

オフセット電圧の製造分布



English Data Sheet: SBOS860

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4 改訂履歴

日付	改訂内容	注
2017年4月	*	初版

5 Device Comparison Table

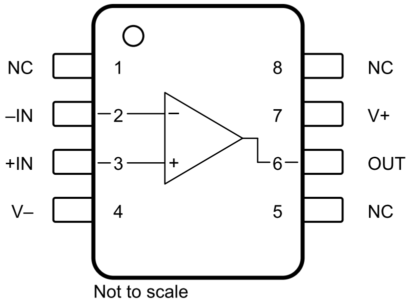
5.1 Portfolio Comparison

Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (μV, maximum)	OFFSET VOLTAGE DRIFT (μV/°C, maximum)	BANDWIDTH (MHz)	INPUT VOLTAGE NOISE (μV_{PP}, f = 0.1 Hz to 10 Hz)
Single	OPA188-Q1 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA333 (5 V)	±10	±0.05	0.35	1.1
	OPA378 (5 V)	±50	±0.25	0.9	0.4
	OPA735 (12 V)	±5	±0.05	1.6	2.5
Dual	OPA2188-Q1 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA2333 (5 V)	±10	±0.05	0.35	1.1
	OPA2378 (5 V)	±50	±0.25	0.9	0.4
	OPA2735 (12 V)	±5	±0.05	1.6	2.5
Quad	OPA4330 (5 V)	±50	±0.25	0.35	1.1

6 Pin Configuration and Functions

OPA188-Q1 DGK Package
8-Pin VSSOP
Top View

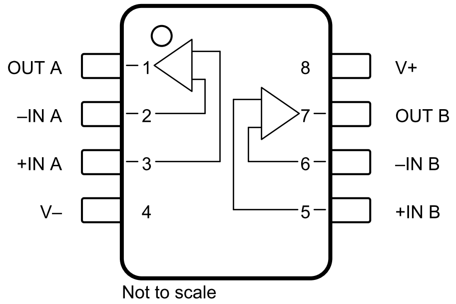


(1) NC = no connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	2	I	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

OPA2188-Q1 DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply	Split-supply		±20	V
		Single-supply		40	
	Signal input pins(2)		(V–) – 0.5	(V+) + 0.5	
		Differential		±0.7	
Current	Signal input pins(2)			±10	mA
	Output short-circuit(3)		Continuous		
Temperature	OPA188-Q1, T_J			150	°C
	OPA2188-Q1, T_J			125	°C
	Storage, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, V– or V+.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1500	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) R_L = 10 kΩ connected to V_S / 2 (1), and V_{CM} = V_{OUT} = V_S / 2(1)

			MIN	NOM	MAX	UNIT
V_S	Operating voltage range	Split–supply	±2		±18	V
		Single–supply	4		36	
T_A	OPA188-Q1 Temperature Grade 1: Specified temperature range		–40		125	°C
	OPA2188-Q1 Temperature Grade 2: Specified temperature range		–40		105	

(1) V_S / 2 = midsupply.

7.4 Thermal Information

THERMAL METRIC(1)		OPA188-Q1	OPA2188-Q1	UNIT
		DGK (VSSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.7	163.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	57.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.0	83.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.0	6.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.4	82.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: High-Voltage Operation

at T_A = 25°C, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V), R_L = 10 kΩ connected to V_S / 2 (1), and $V_{CM} = V_{OUT} = V_S$ / 2(1) (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±6	±25	µV
dV_{IO}/dT	Input offset voltage drift	OPA188-Q1 T_A = –40°C to 125°C		±0.03	±0.085	µV/°C
		OPA2188-Q1 T_A = –40°C to 105°C		±0.03	±0.085	µV/°C
PSRR	Power-supply rejection ratio	OPA188-Q1 V_S = 4 V to 36 V T_A = –40°C to 125°C		±0.075	±0.3	µV/V
		OPA2188-Q1 V_S = 4 V to 36 V T_A = –40°C to 105°C		±0.075	±0.3	µV/V
	Long-term stability(2)			4		µV
INPUT BIAS CURRENT						
I_B	Input bias current	$V_{CM} = V_S$ / 2		±160	±1400	pA
		OPA188-Q1 T_A = –40°C to 125°C			±18	nA
		OPA2188-Q1 T_A = –40°C to 105°C			±18	nA
I_{OS}	Input offset current	$V_{CM} = V_S$ / 2		±320	±2800	pA
		OPA188-Q1 T_A = –40°C to 125°C			±6	nA
		OPA2188-Q1 T_A = –40°C to 105°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		250		nV_{PP}
		f = 0.1 Hz to 10 Hz		40		nVrms
	Input voltage noise density	f = 1 kHz		8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	OPA188-Q1 T_A = –40°C to 125°C	V–		(V+) – 1.5	V
		OPA2188-Q1 T_A = –40°C to 105°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	$(V–) < V_{CM} < (V+) – 1.5$ V	120	134		dB
		$(V–) + 0.5$ V $< V_{CM} < (V+) – 1.5$ V V_S = ±18 V	130	146		dB
		OPA188-Q1 $(V–) + 0.5$ V $< V_{CM} < (V+) – 1.5$ V V_S = ±18 V, T_A = –40°C to 125°C	120	126		dB
		OPA2188-Q1 $(V–) + 0.5$ V $< V_{CM} < (V+) – 1.5$ V V_S = ±18 V, T_A = –40°C to 105°C	120	126		dB
INPUT IMPEDANCE						
Z_{ID}	Differential			100 || 6		MΩ || pF
Z_{IC}	Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$(V–) + 0.5$ V $< V_O < (V+) – 0.5$ V	130	136		dB
		OPA188-Q1 $(V–) + 0.5$ V $< V_O < (V+) – 0.5$ V T_A = –40°C to 125°C	120	126		dB
		OPA2188-Q1 $(V–) + 0.5$ V $< V_O < (V+) – 0.5$ V T_A = –40°C to 105°C	120	126		dB
FREQUENCY RESPONSE						

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(1) V_S / 2 = midsupply.
(2) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits at approximately 4 µV.

Electrical Characteristics: High-Voltage Operation (continued)

at T_A = 25°C, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V), R_L = 10 kΩ connected to V_S / 2 (1), and V_{CM} = V_{OUT} = V_S / 2(1) (unless otherwise noted)

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
GBW	Gain-bandwidth product				2		MHz
SR	Slew rate		G = 1		0.8		V/µs
t_S	Settling time	0.1%	V_S = ±18 V, G = 1, 10-V step		20		µs
		0.01%	V_S = ±18 V, G = 1, 10-V step		27		µs
t_{OR}	Overload recovery time		V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise		1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001%		
OUTPUT							
	Voltage output swing from rail		No load		6	15	mV
			R_L = 10 kΩ		220	250	mV
			OPA188-Q1 R_L = 10 kΩ, T_A = –40°C to 125°C		310	350	mV
			OPA2188-Q1 R_L = 10 kΩ, T_A = –40°C to 105°C		310	350	mV
I_{SC}	Short-circuit current		Sinking		–18		mA
			Sourcing		16		mA
R_O	Open-loop output resistance		f = 1 MHz, I_O = 0 mA		120		Ω
C_{LOAD}	Capacitive load drive				1		nF
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)		V_S = ±4 V to V_S = ±18 V		450	510	µA
			OPA188-Q1 I_O = 0 mA T_A = –40°C to 125°C			600	µA
			OPA2188-Q1 I_O = 0 mA T_A = –40°C to 105°C			600	µA

7.6 Electrical Characteristics: Low-Voltage Operation

at T_A = 25°C, V_S = ±2 V to < ±4 V (V_S = 4 V to < 8 V), R_L = 10 kΩ connected to V_S / 2(1), and V_{CM} = V_{OUT} = V_S / 2(1) (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±6	±25	µV
dV_{IO}/dT	Input offset voltage drift	OPA188-Q1 T_A = –40°C to 125°C		±0.03	±0.085	µV/°C
		OPA2188-Q1 T_A = –40°C to 105°C		±0.03	±0.085	µV/°C
PSRR	Power-supply rejection ratio	OPA188-Q1 V_S = 4 V to 36 V T_A = –40°C to 125°C		0.075	0.3	µV/V
		OPA2188-Q1 V_S = 4 V to 36 V T_A = –40°C to 105°C		0.075	0.3	µV/V
	Long-term stability(2)			4		µV
INPUT BIAS CURRENT						
I_B	Input bias current			±160	±1400	pA
		OPA188-Q1 T_A = –40°C to 125°C			±18	nA
		OPA2188-Q1 T_A = –40°C to 105°C			±18	nA
I_{OS}	Input offset current			±320	±2800	pA
		OPA188-Q1 T_A = –40°C to 125°C			±6	nA
		OPA2188-Q1 T_A = –40°C to 105°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		250		nV_{PP}
		f = 0.1 Hz to 10 Hz		40		nVrms
	Input voltage noise density	f = 1 kHz		8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	OPA188-Q1 T_A = –40°C to 125°C	V–		(V+) – 1.5	V
		OPA2188-Q1 T_A = –40°C to 105°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	106	114		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V V_S = ±2 V	114	120		dB
		OPA188-Q1 (V–) + 0.5 V < V_{CM} < (V+) – 1.5 V V_S = ±2 V, T_A = –40°C to 125°C	110	120		dB
		OPA2188-Q1 (V–) + 0.5 V < V_{CM} < (V+) – 1.5 V V_S = ±2 V, T_A = –40°C to 105°C	110	120		dB
INPUT IMPEDANCE						
Z_{ID}	Differential			100 || 6		MΩ || pF
Z_{IC}	Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN						

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(1) V_S / 2 = midsupply.
(2) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits at approximately 4 µV.

Electrical Characteristics: Low-Voltage Operation (continued)

at T_A = 25°C, V_S = ±2 V to < ±4 V (V_S = 4 V to < 8 V), R_L = 10 kΩ connected to V_S / 2(1), and V_{CM} = V_{OUT} = V_S / 2(1) (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
A_{OL}	Open-loop voltage gain	(V–) + 0.5 V < V_O < (V+) – 0.5 V R_L = 5 kΩ	110	120		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V	120	130		dB
		OPA188-Q1 (V–) + 0.5 V < V_O < (V+) – 0.5 V T_A = –40°C to 125°C	110	120		dB
		OPA2188-Q1 (V–) + 0.5 V < V_O < (V+) – 0.5 V T_A = –40°C to 105°C	110	120		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = 1		0.8		V/µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001%		
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		OPA188-Q1 R_L = 10 kΩ, T_A = –40°C to 125°C		310	350	mV
		OPA2188-Q1 R_L = 10 kΩ, T_A = –40°C to 105°C		310	350	mV
I_{SC}	Short-circuit current	Sinking		–18		mA
		Sourcing		16		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 mA		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)	V_S = ±2 V to V_S = ±4 V		425	485	µA
		OPA188-Q1 I_O = 0 mA T_A = –40°C to 125°C			575	µA
		OPA2188-Q1 I_O = 0 mA T_A = –40°C to 105°C			575	µA

7.7 Typical Characteristics: Table of Graphs

7.7.1 Table of Graphs

表 1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	図 1
Offset Voltage Drift Distribution	図 2
Offset Voltage vs Temperature	図 3
Offset Voltage vs Common-Mode Voltage	図 4, 図 5
Offset Voltage vs Power Supply	図 6
Open-Loop Gain and Phase vs Frequency	図 7
Closed-Loop Gain vs Frequency	図 8
I_B and I_{OS} vs Common-Mode Voltage	図 9
Input Bias Current vs Temperature	図 10
Output Voltage Swing vs Output Current (Maximum Supply)	図 11
CMRR and PSRR vs Frequency (Referred-to-Input)	図 12
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Large-Signal Settling Time (10-V Positive Step)	図 33
Large-Signal Settling Time (10-V Negative Step)	図 34
Short-Circuit Current vs Temperature	
Maximum Output Voltage vs Frequency	図 35
EMIRR IN+ vs Frequency	図 36

7.8 Typical Characteristics

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

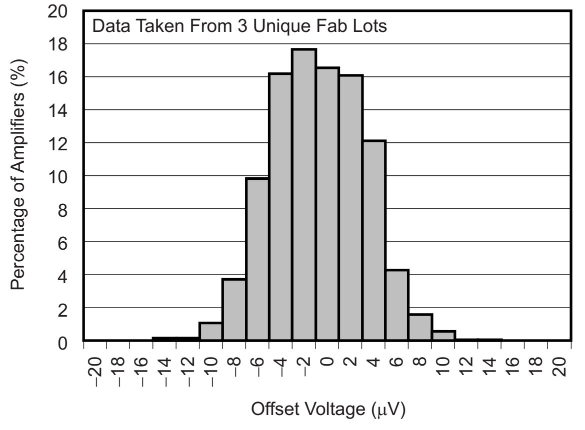


図 1. Offset Voltage Production Distribution

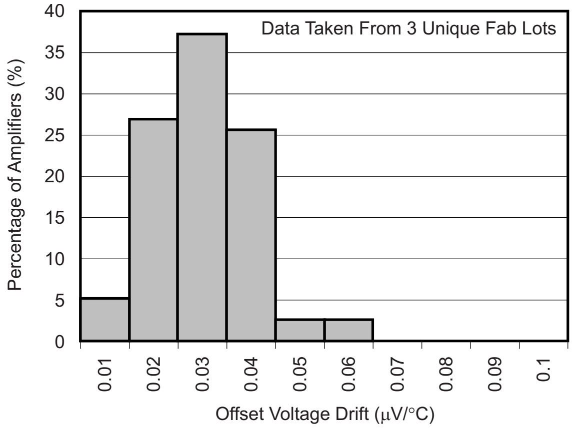
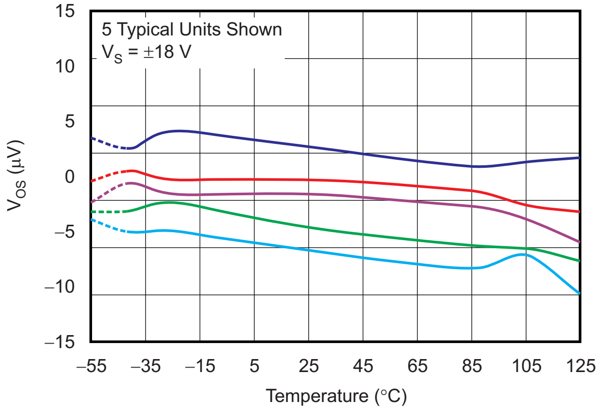


図 2. Offset Voltage Drift Distribution



OPA188-Q1 is specified from T_A = –40°C to +125°C
OPA2188-Q1 is specified from T_A = –40°C to +105°C

図 3. Offset Voltage vs Temperature

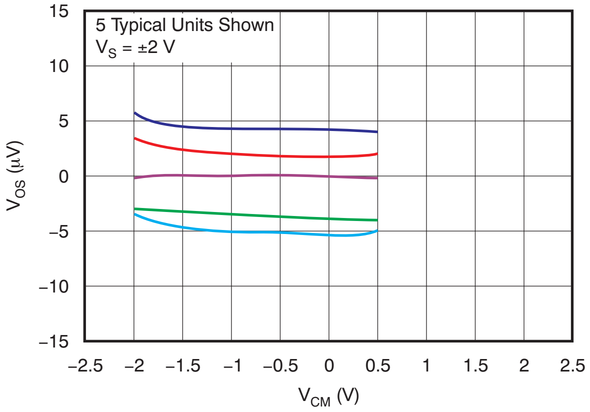


図 4. Offset Voltage vs Common-Mode Voltage

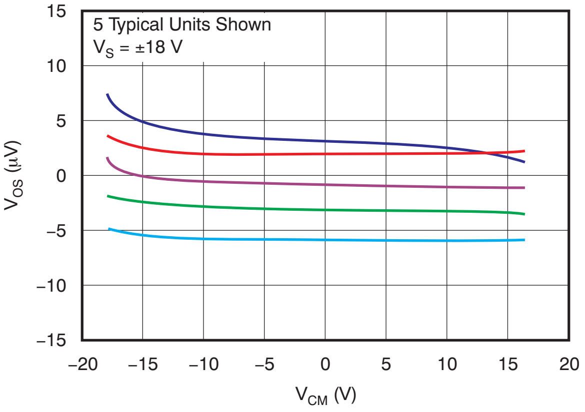


図 5. Offset Voltage vs Common-Mode Voltage

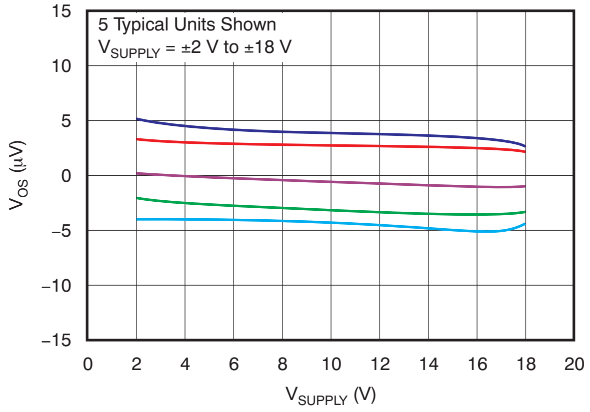


図 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

at $V_S = \pm 18$ V, $V_{CM} = V_S / 2$, $R_{LOAD} = 10$ kΩ connected to $V_S / 2$, and $C_L = 100$ pF (unless otherwise noted)

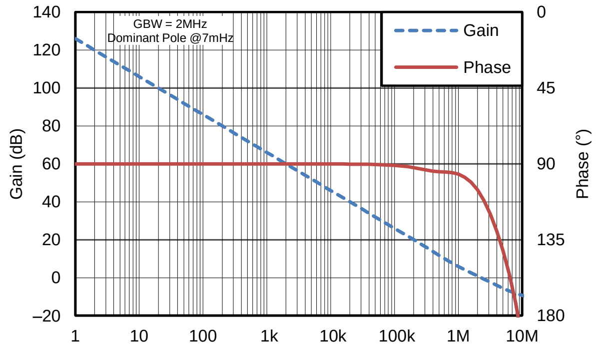


図 7. Open-Loop Gain and Phase vs Frequency

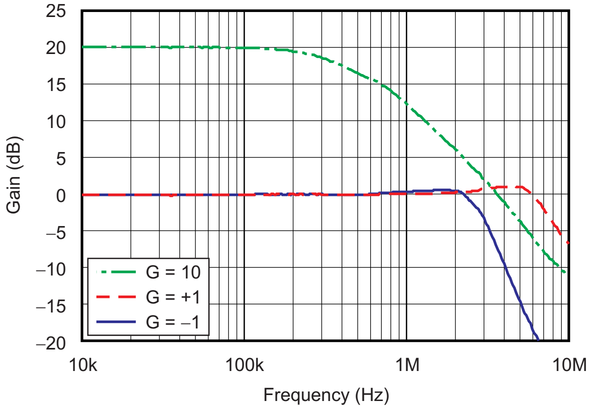


図 8. Closed-Loop Gain vs Frequency

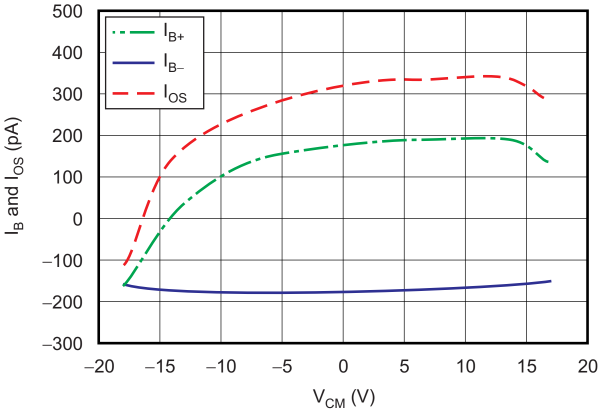
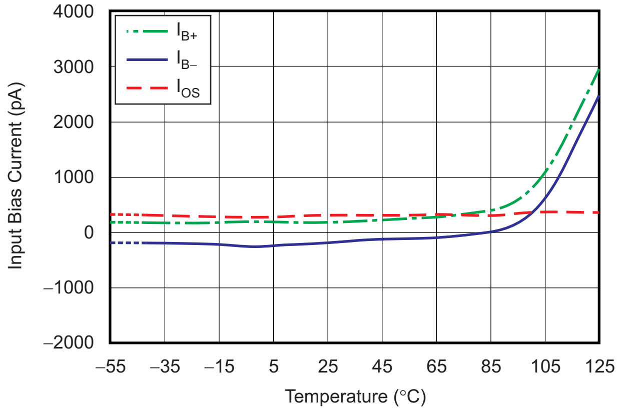


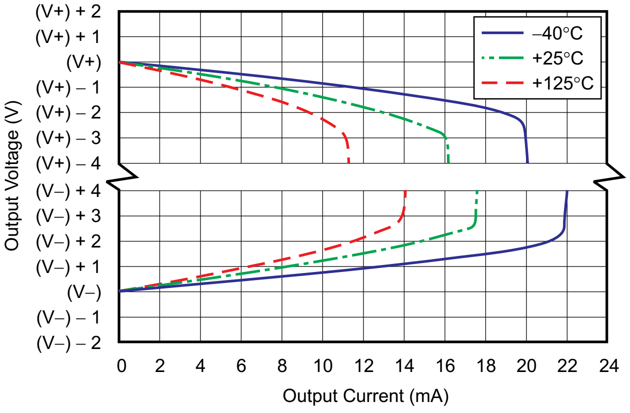
図 9. I_B and I_{OS} vs Common-Mode Voltage



OPA188-Q1 is specified from T_A = –40°C to +125°C

OPA2188-Q1 is specified from T_A = –40°C to +105°C

図 10. Input Bias Current vs Temperature



OPA188-Q1 is specified from T_A = –40°C to +125°C

OPA2188-Q1 is specified from T_A = –40°C to +105°C

図 11. Output Voltage Swing vs Output Current (Maximum Supply)

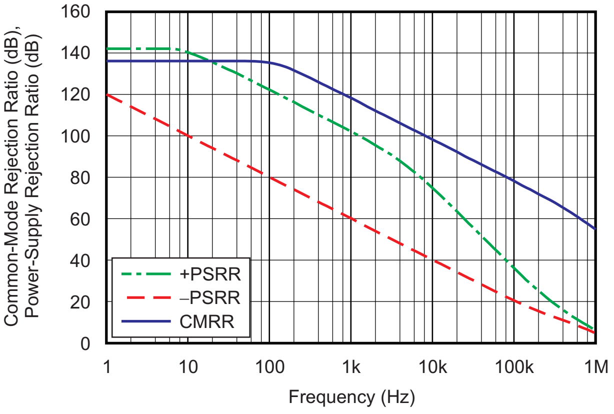
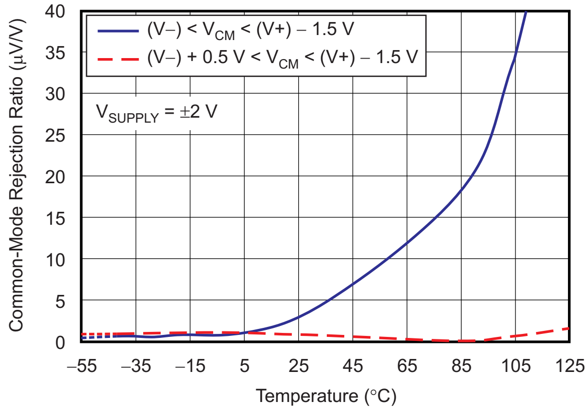


図 12. CMRR and PSRR vs Frequency (Referred-to-Input)

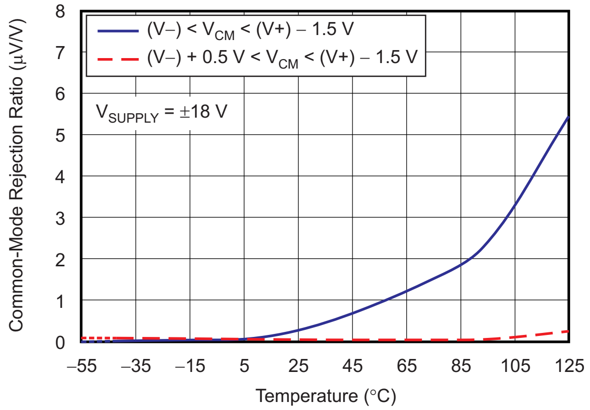
Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



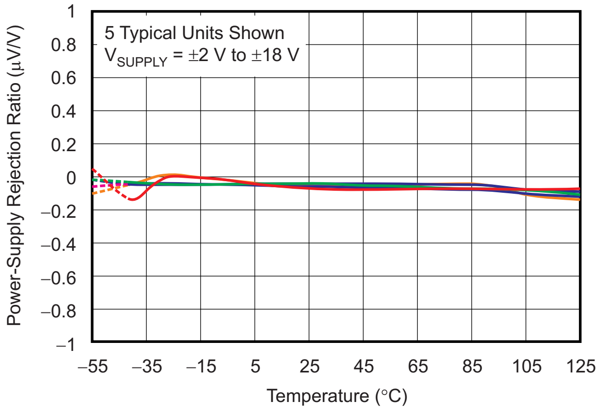
OPA188-Q1 is specified from T_A = –40°C to +125°C
OPA2188-Q1 is specified from T_A = –40°C to +105°C

図 13. CMRR vs Temperature



OPA188-Q1 is specified from T_A = –40°C to +125°C
OPA2188-Q1 is specified from T_A =–40°C to +105°C

図 14. CMRR vs Temperature



OPA188-Q1 is specified from T_A = –40°C to +125°C
OPA2188-Q1 is specified from T_A = –40°C to +105°C

図 15. PSRR vs Temperature

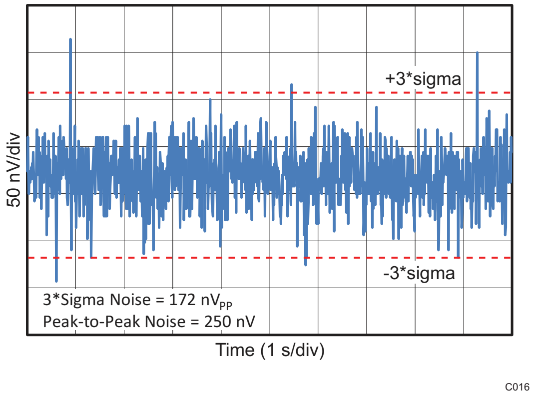


図 16. 0.1-Hz to 10-Hz Noise

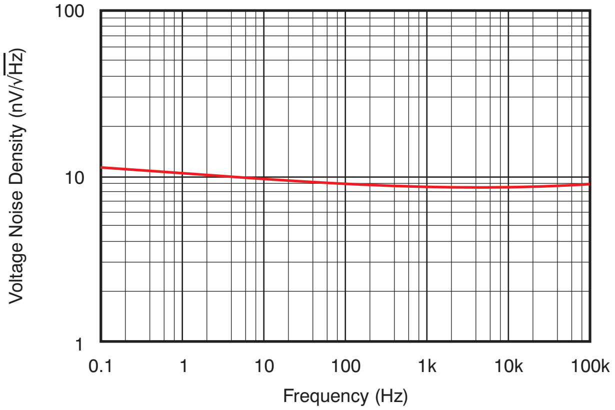


図 17. Input Voltage Noise Spectral Density vs Frequency

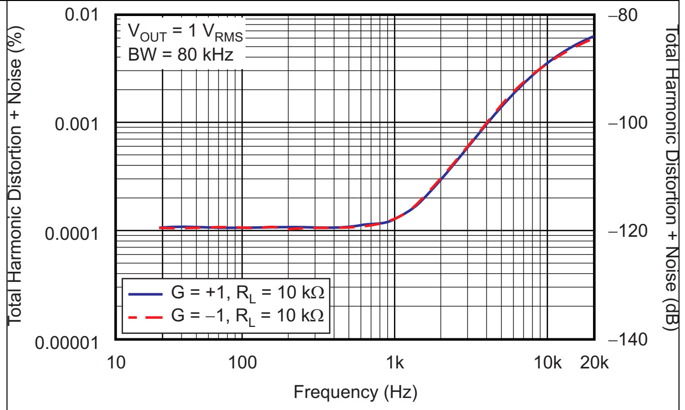


図 18. THD+N Ratio vs Frequency

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

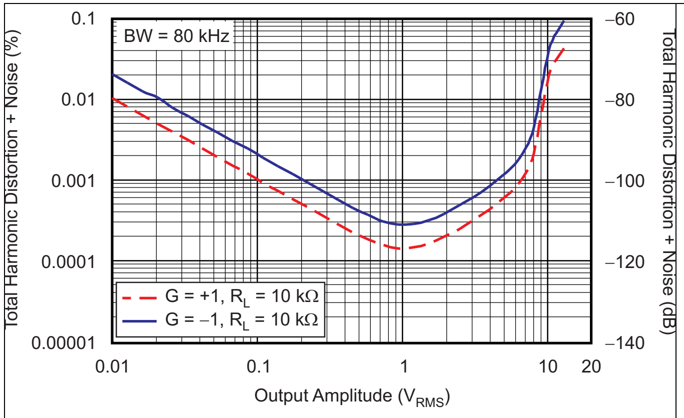


図 19. THD+N vs Output Amplitude

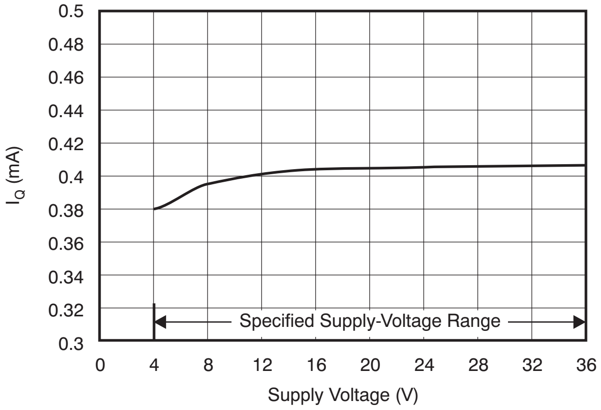
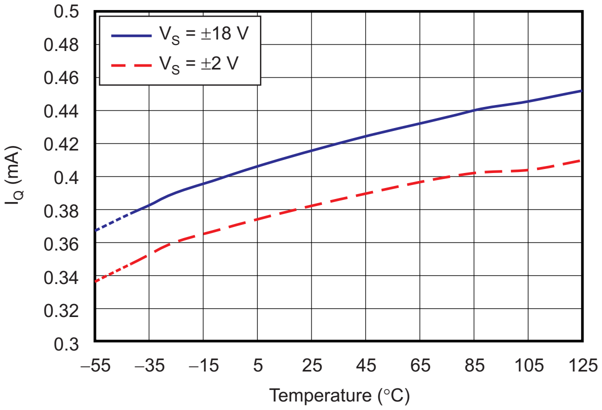
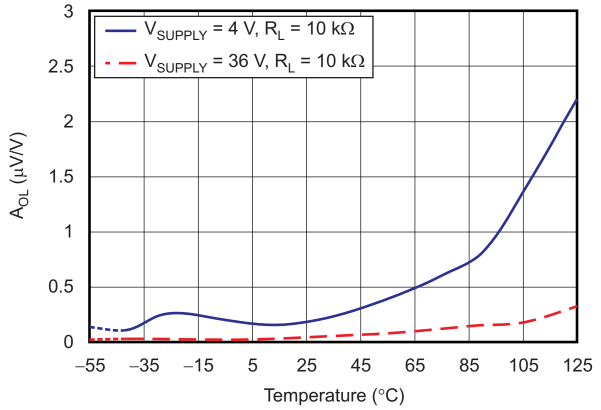


図 20. Quiescent Current vs Supply Voltage



OPA188-Q1 is specified from T_A = –40°C to +125°C
OPA2188-Q1 is specified from T_A = –40°C to +105°C

図 21. Quiescent Current vs Temperature



OPA188-Q1 is specified from T_A = –40°C to +125°C
OPA2188-Q1 is specified from T_A = –40°C to +105°C

図 22. Open-Loop Gain vs Temperature

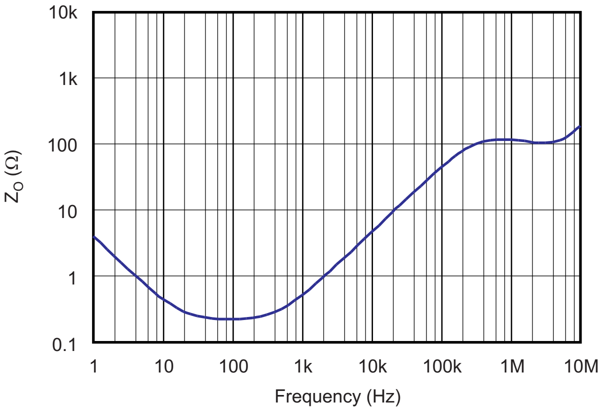


図 23. Open-Loop Output Impedance vs Frequency

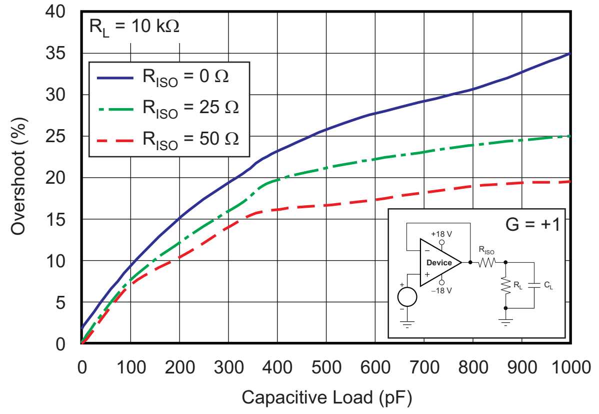


図 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

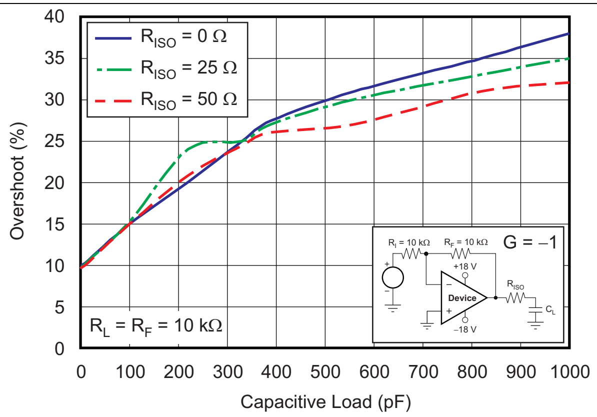


図 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

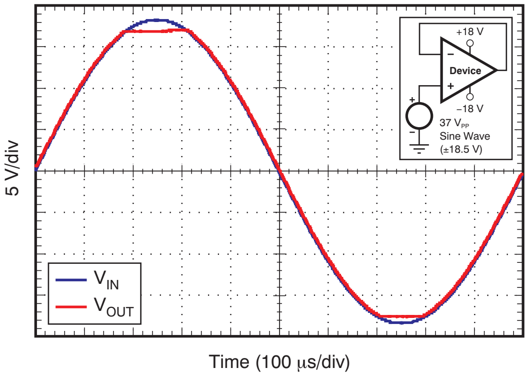


図 26. No Phase Reversal

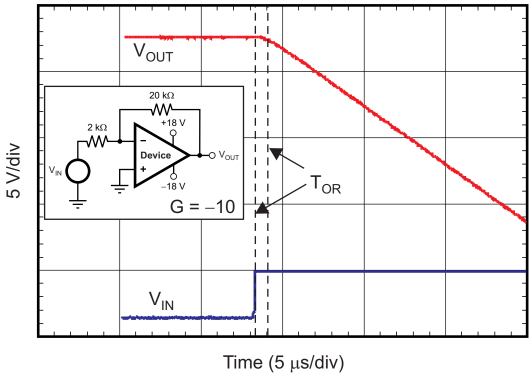


図 27. Positive Overload Recovery

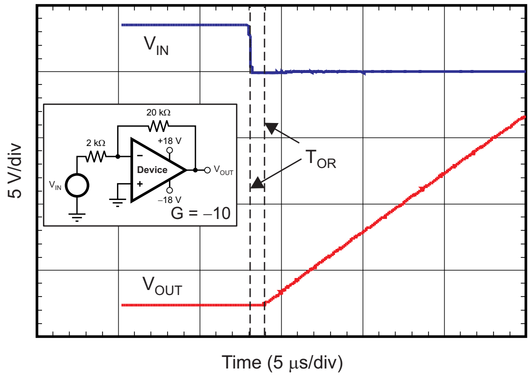


図 28. Negative Overload Recovery

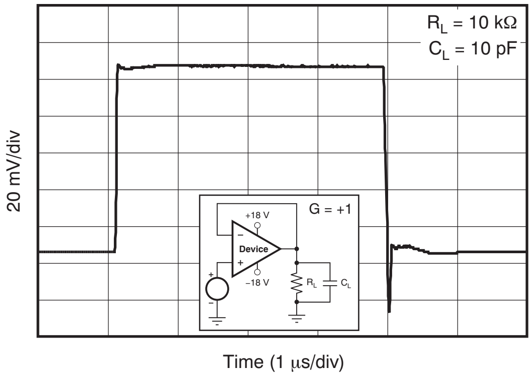


図 29. Small-Signal Step Response (100 mV)

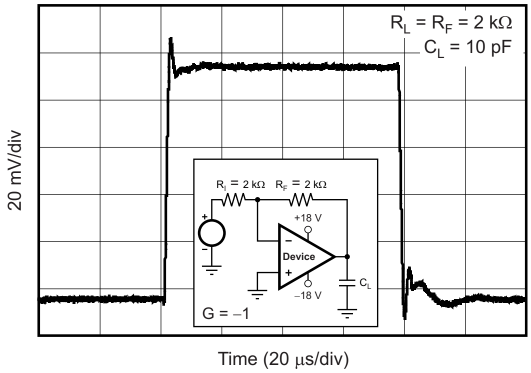


図 30. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

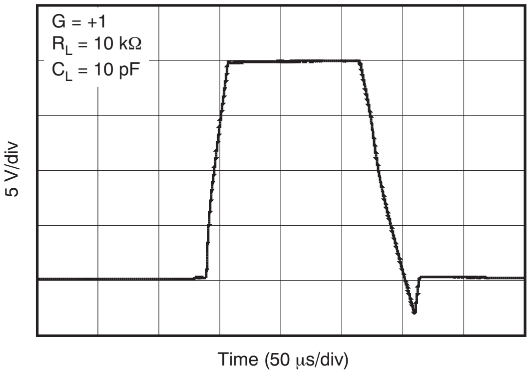


図 31. Large-Signal Step Response

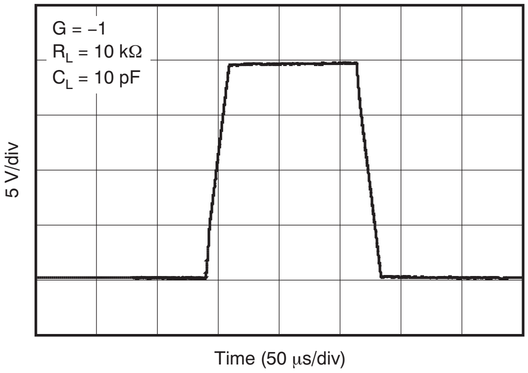


図 32. Large-Signal Step Response

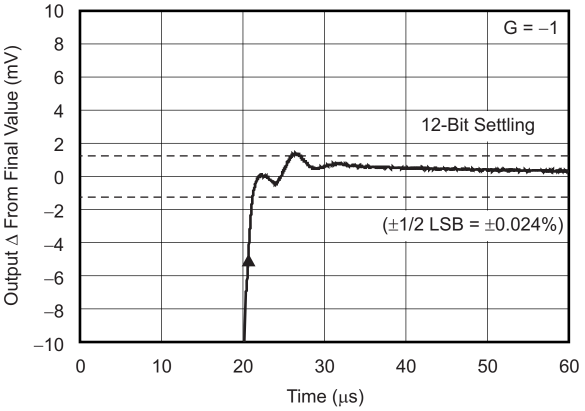


図 33. Large-Signal Settling Time (10-V Positive Step)

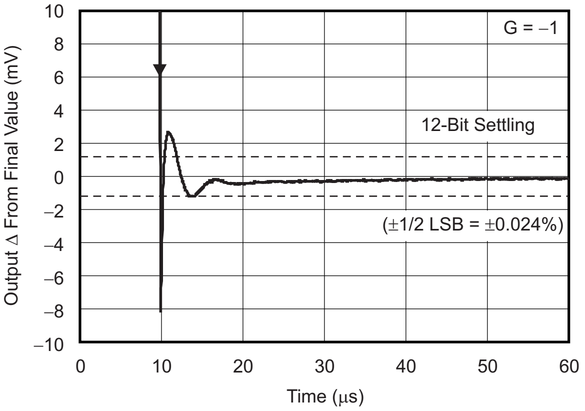


図 34. Large-Signal Settling Time (10-V Negative Step)

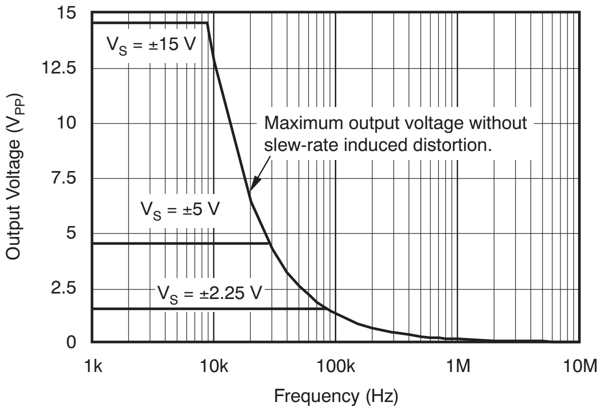


図 35. Maximum Output Voltage vs Frequency

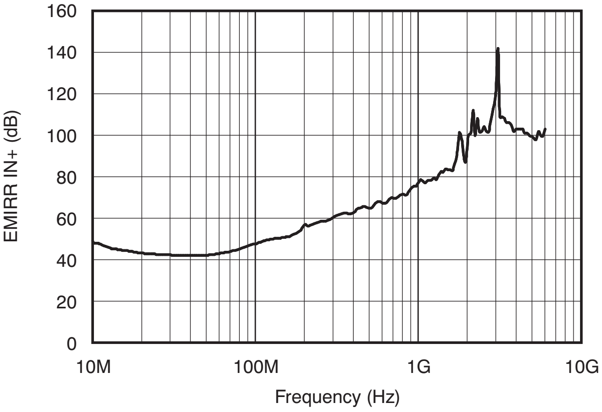


図 36. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The OPAx188-Q1 operational amplifier series combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.085 µV/°C provides stability over the entire temperature range. In addition, this device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The OPAx188-Q1 device is part of a family of zero-drift, low-power, rail-to-rail output operational amplifiers. These devices operate from 4 V to 36 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise and zero flicker noise.

8.2 Functional Block Diagram

図 37 shows a representation of the proprietary OPAx188-Q1 architecture. 表 2 lists the active and passive component counts for this device. The component count allows for accurate reliability calculations.

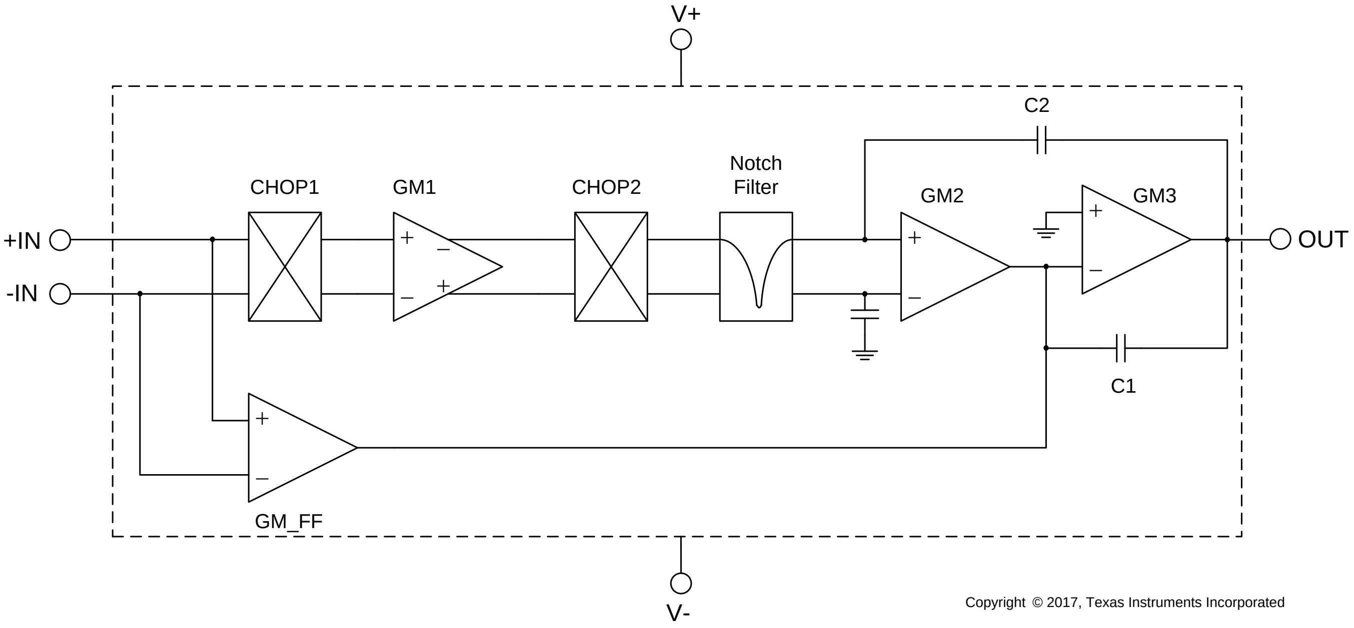


図 37. Functional Block Diagram

表 2. Component Count

COMPONENT	COUNT
Transistors	636
Diodes	5
Resistors	41
Capacitors	72

8.3 Feature Description

The OPAx188-Q1 series is unity-gain stable and free from unexpected output phase reversal. This device series uses a proprietary, periodic zero-drift technique to provide low input offset voltage and very low input offset voltage drift over temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by ensuring the potentials are equal on both input pins. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield the operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1 μV/°C or higher, depending on the materials used.

8.3.1 Operating Characteristics

The OPAx188-Q1 is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

8.3.2 Phase-Reversal Protection

The OPAx188-Q1 series has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx188-Q1 series input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail; 図 38 shows this performance.

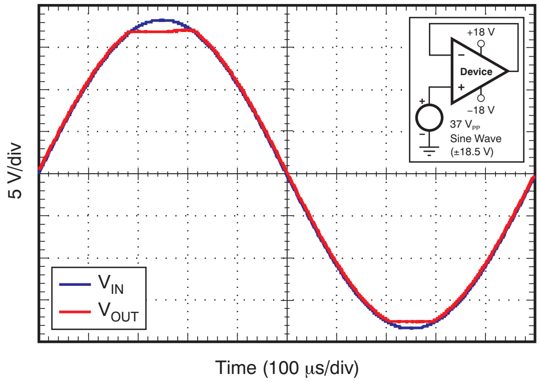


図 38. No Phase Reversal

8.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers (such as the OPAx188-Q1 series) use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the devices from being amplified. However, the devices may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

8.3.4 Internal Offset Correction

The OPAx188-Q1 op amp series uses an auto-calibration technique with a time-continuous 750-kHz op amp in the signal path. This amplifier is zero-corrected every 3 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Feature Description (continued)

8.3.5 EMI Rejection

The OPAx188-Q1 series uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx188-Q1 series benefits from these design improvements. Texas Instruments™ has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 図 39 shows the results of this testing on the OPAx188-Q1. 表 3 lists the EMIRR IN+ values for the OPAx188-Q1 devices at particular frequencies commonly encountered in real-world applications. Applications listed in 表 3 may be centered on or operated near the particular frequency shown. Detailed information can also be found in *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

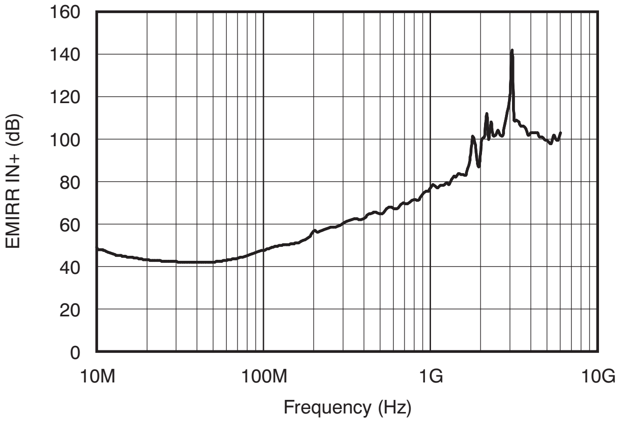


図 39. EMIRR Testing

表 3. OPAx188-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	62.2 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	74.7 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	100.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, *Bluetooth*®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	102.4 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	104.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	100.3 dB

8.3.6 Capacitive Load and Stability

The device dynamic characteristics are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 図 40 and 図 41 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. For details of analysis techniques and application circuits, see *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com.

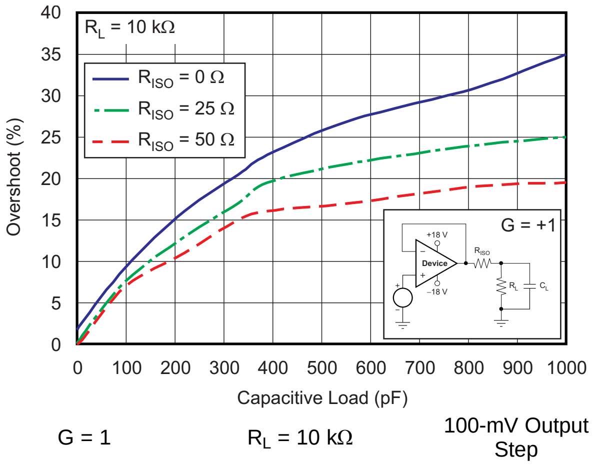


図 40. Small-Signal Overshoot Versus Capacitive Load

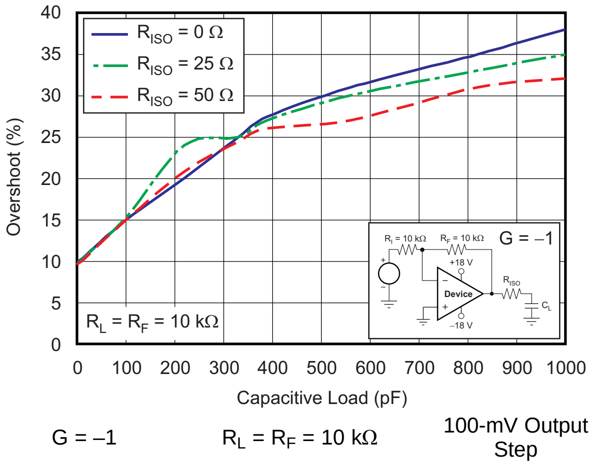


図 41. Small-Signal Overshoot Versus Capacitive Load

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See 図 42 for an illustration of the ESD circuits contained in the OPAx188-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an internal absorption device of the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx188-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

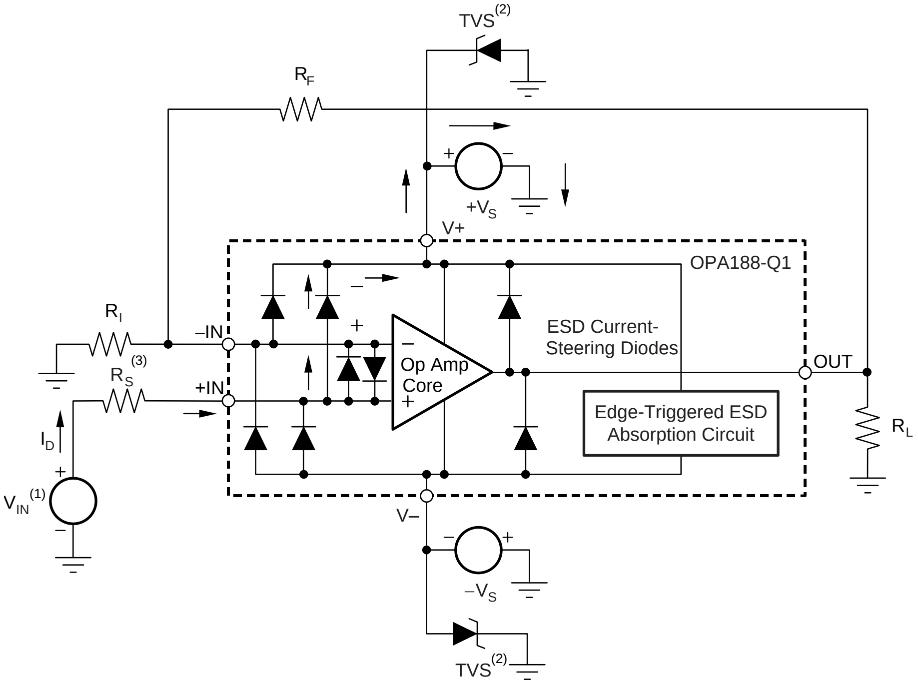
When the operational amplifier connects into a circuit (such as 図 42 shows), the ESD protection components are intended to remain inactive and do not become involved in the operation of the application circuit. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits may be biased on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 42 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper-input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the absolute maximum ratings of the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies (+V_S or –V_S) are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins, as shown in 図 42. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



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(1) $V_{IN} = +V_S + 500$ mV.
(2) TVS: $+V_{S(max)} > V_{TVSBR(min)} > +V_S$.
(3) Suggested value is approximately 1 kΩ.

図 42. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

The OPAx188-Q1 series input terminals are protected from excessive differential voltage with back-to-back diodes, as shown in 図 42. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain and G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPAx188-Q1 series. 図 42 shows an example configuration that implements a current-limiting feedback resistor.

8.4 Device Functional Modes

The OPAx188-Q1 series has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx188-Q1 family is 36 V (±18 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx188-Q1 operational amplifiers combine precision offset and drift with excellent overall performance, making the series ideal for many precision applications. The precision offset drift of only 0.085 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPAx188-Q1 series can be used.

9.2 Typical Applications

9.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in 図 43 is a high-side voltage-to-current (V-I) converter. The converter translates an input voltage of 0 V to 2 V to an output current of 0 mA to 100 mA. 図 44 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2188-Q1 facilitate excellent dc accuracy for the circuit.

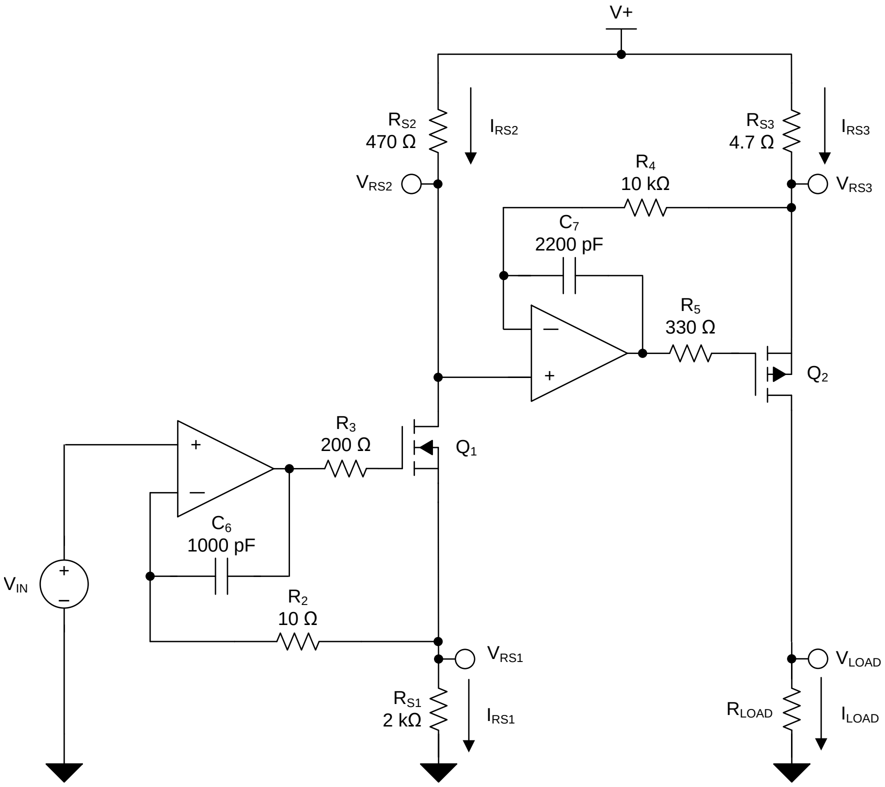


図 43. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 5 V dc
- Input: 0 V to 2 V dc
- Output: 0 mA to 100 mA dc

9.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPAx188-Q1 CMOS operational amplifier is a high-precision, ultra-low offset, ultra-low drift amplifier, optimized for low-voltage, single-supply operation, with an output swing to within 15 mV of the positive rail. The devices in the OPAx188-Q1 family use chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making this device appropriate for precise dc control. The rail-to-rail output stage of the OPAx188-Q1 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in reference design TIPD102, a step-by-step process to design a *High-Side Voltage-to-Current (V-I) Converter*.

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD102, *High-Side Voltage-to-Current (V-I) Converter* (SLAU502).

9.2.1.3 Application Curves

図 44 shows the measured transfer function for the high-side voltage-to-current converter shown in 図 43 .

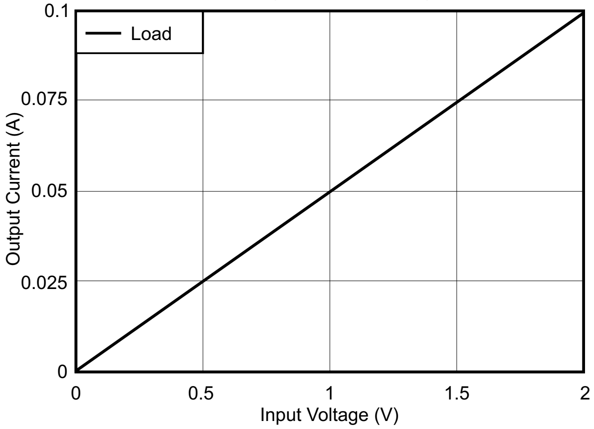


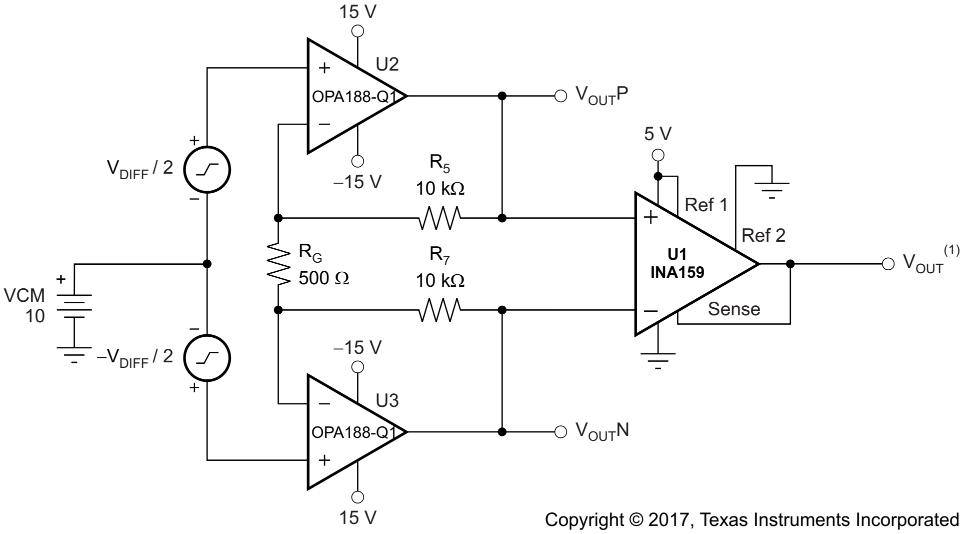
図 44. Measured Transfer Function for High-Side V-I Converter

9.2.2 Discrete INA + Attenuation for ADC With 3.3-V Supply

注

The TINA-TI files shown in the following sections require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

図 45 shows an example of how the OPA188-Q1 series is used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link to download the TINA-TI file: Discrete INA.



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(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (\text{Ref } 1) / 2$.

図 45. Discrete INA + Attenuation for ADC With 3.3-V Supply

9.2.3 Bridge Amplifier

図 46 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: Bridge Amplifier Circuit.

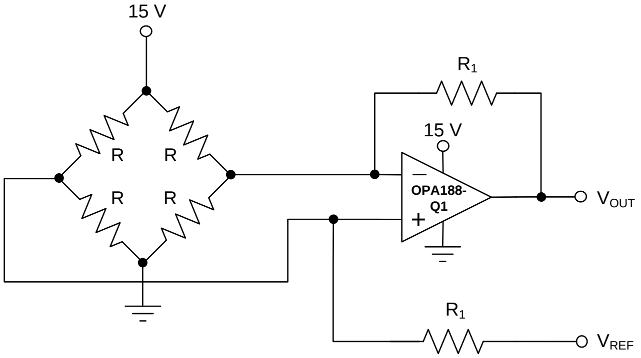

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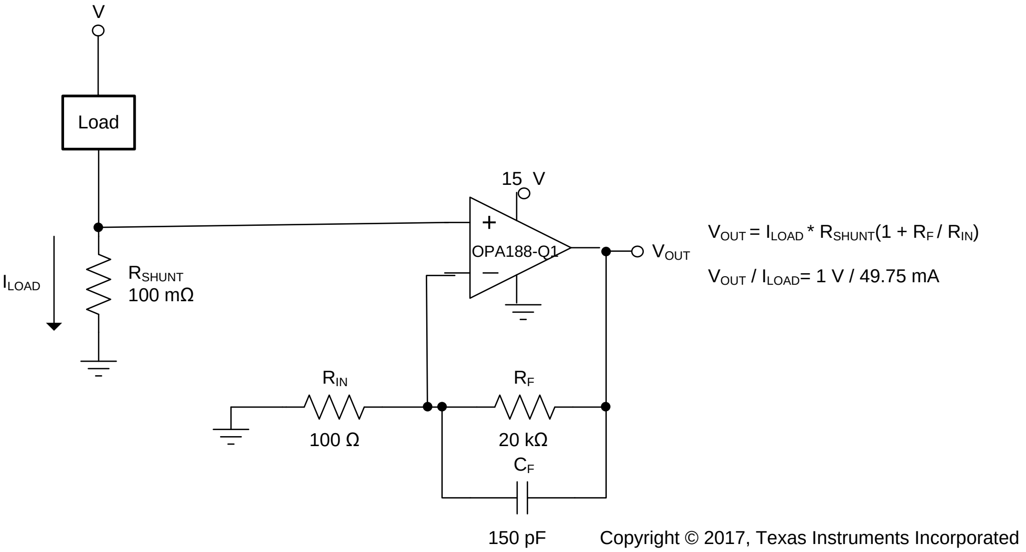
図 46. Bridge Amplifier

9.2.4 Low-Side Current Monitor

図 47 shows the OPAx188-Q1 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPAx188-Q1, with a gain of 201. The load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: Current-Sensing Circuit.



$V_{OUT} = I_{LOAD} * R_{SHUNT}(1 + R_F / R_{IN})$

$V_{OUT} / I_{LOAD} = 1\ V / 49.75\ mA$

図 47. Low-Side Current Monitor

9.2.5 Programmable Power Supply

図 48 shows the OPA188-Q1 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPA188-Q1 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: Programmable Power-Supply Circuit.

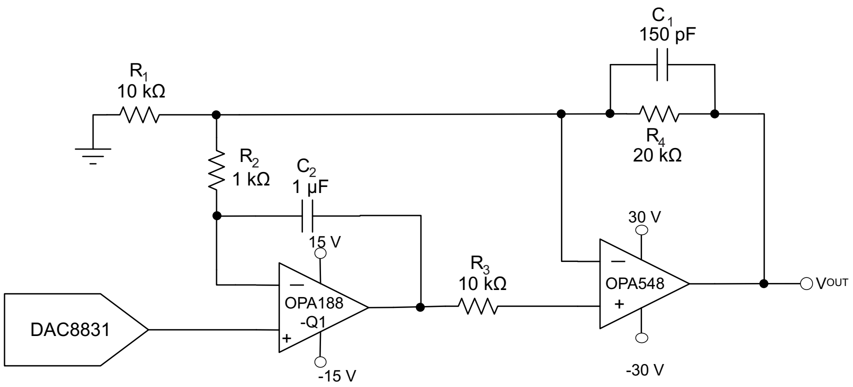
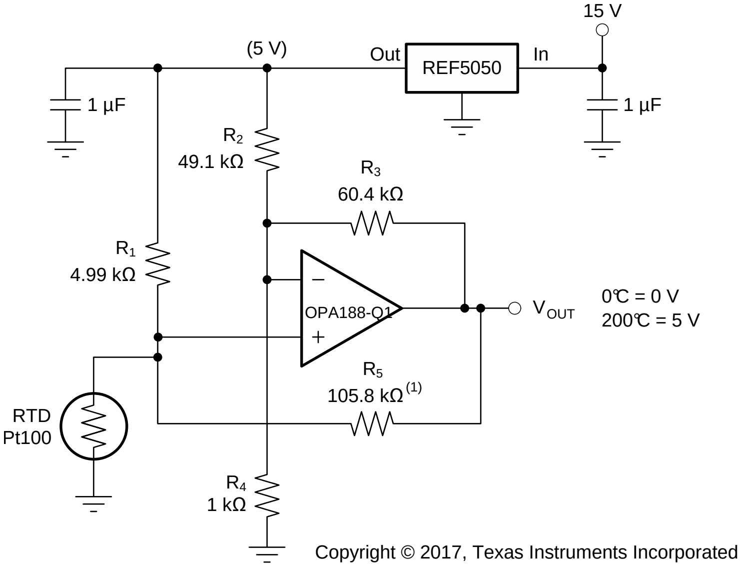


図 48. Programmable Power Supply

9.2.6 RTD Amplifier With Linearization

See *Analog Linearization Of Resistance Temperature Detectors* for an in-depth analysis of 図 49. Click the following link to download the TINA-TI file: RTD Amplifier with Linearization.



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(1) R_5 provides positive-varying excitation to linearize output.

図 49. RTD Amplifier With Linearization

10 Power Supply Recommendations

The OPAx188-Q1 series is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to +125°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

> **注意**
>
> Supply voltages larger than 40 V can permanently damage the device (see the Absolute Maximum Ratings).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

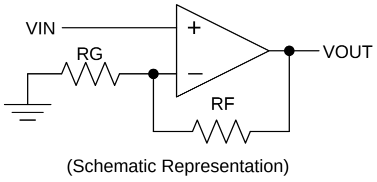
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Low-ESR, 0.1-µF ceramic bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example



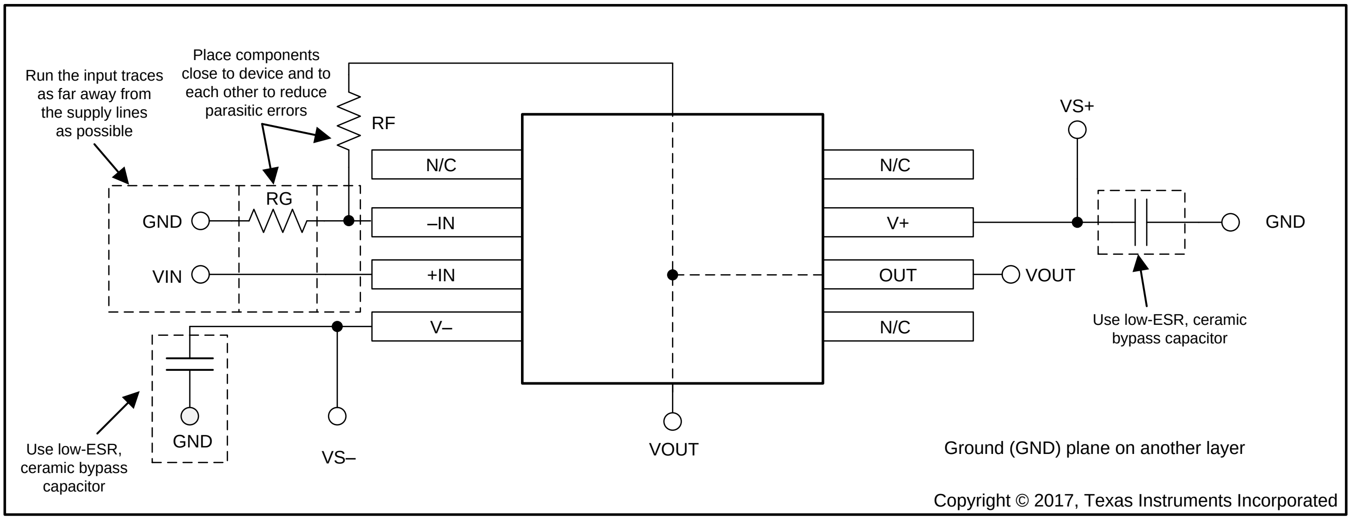


図 50. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 TINA-TI™(無償のダウンロード・ソフトウェア)

TINA™ は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINA-TIソフトウェアのフル機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

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12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください：

- *『オペアンプのEMI除去率』*(SBOA128)
- *『フィードバック・プロットによるオペアンプAC性能の定義』*(SBOA015)
- *『抵抗温度検出器のアナログ線形化』*(SLYT442)
- *『ハイサイドの電圧/電流(V-I)コンバータ』*(SLAU502)

12.3 関連リンク

表 4 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA188-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2188-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

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12.5 コミュニティ・リソース

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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12.7 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA188AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	188	Samples
OPA2188AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2188	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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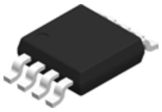
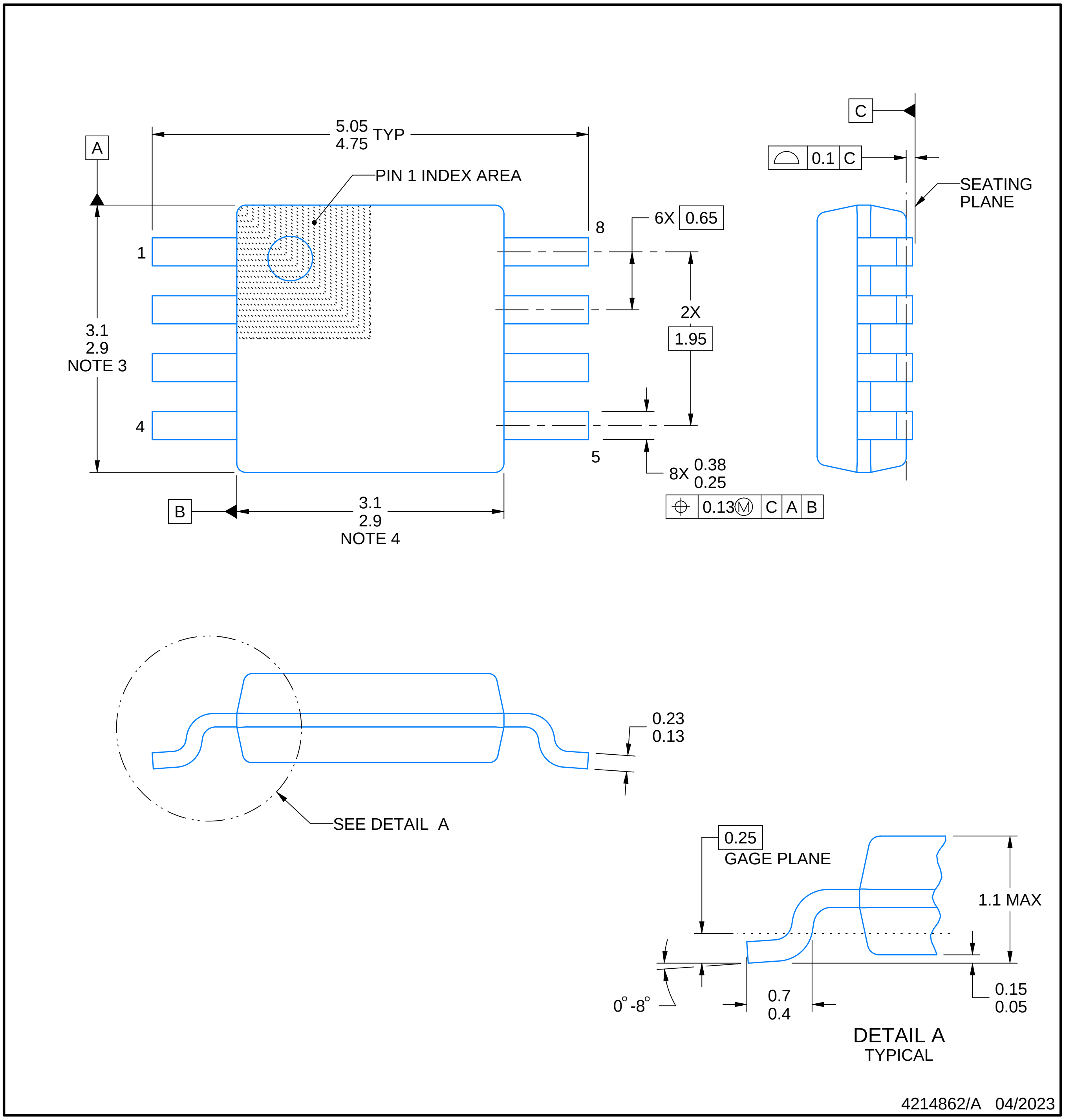
PACKAGE OUTLINE



DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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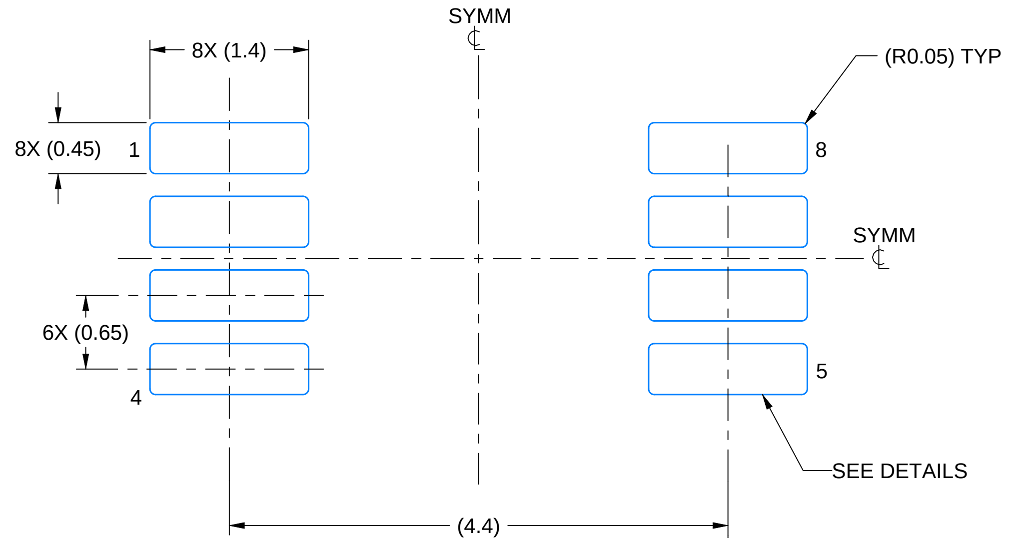
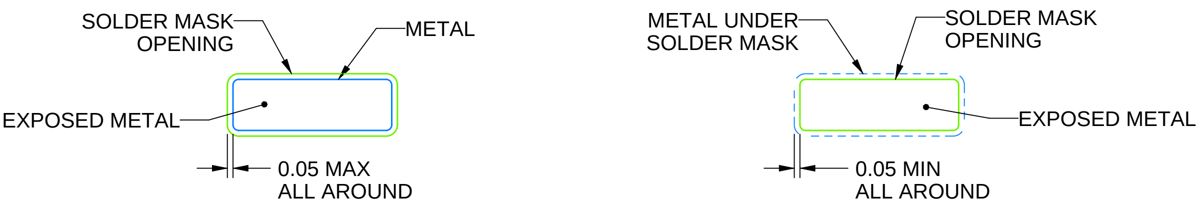
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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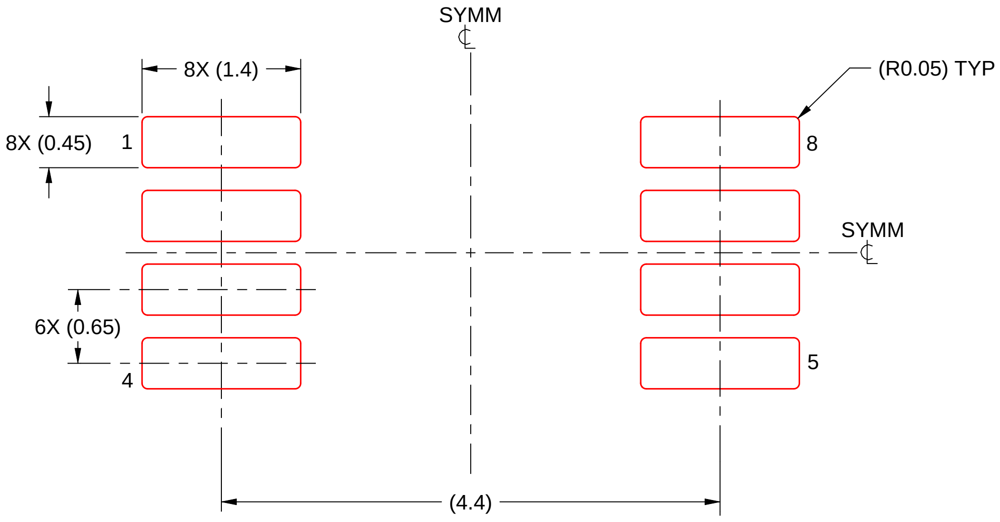
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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