TEXAS INSTRUMENTS

OPA322, OPA322S
OPA2322, OPA2322S
OPA4322, OPA4322S

SBOS538F – JANUARY 2011 – REVISED DECEMBER 2016

OPAx322x 20-MHz, Low-Noise, 1.8-V, RRI/O, CMOS Operational Amplifier With Shutdown

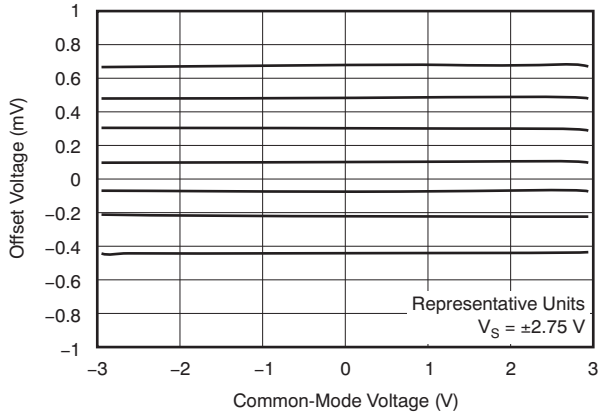
1 Features

- Gain Bandwidth: 20 MHz
- Low Noise: 8.5 nV/√Hz at 1 kHz
- Slew Rate: 10 V/μs
- Low THD+N: 0.0005%
- Rail-to-Rail I/O
- Offset Voltage: 2 mV (maximum)
- Supply Voltage: 1.8 V to 5.5 V
- Supply Current: 1.5 mA/ch
  - Shutdown: 0.1 μA/ch
- Unity-Gain Stable
- Small Packages:
  - SOT-23, SON, VSSOP, TSSOP

2 Applications

- Sensor Signal Conditioning
- Consumer Audio
- Multi-Pole Active Filters
- Control-Loop Amplifiers
- Communications
- Security
- Scanners

Zero-Crossover Rail-to-Rail Input Stage Eliminates Distortion



3 Description

The OPAx322x series consists of single, dual, and quad-channel CMOS operational amplifiers featuring low noise and rail-to-rail inputs and outputs optimized for low-power, single-supply applications. Specified over a wide supply range of 1.8 V to 5.5 V, the low quiescent current of only 1.5 mA per channel makes these devices well-suited for power-sensitive applications.

The combination of very low noise (8.5 nV/√Hz at 1 kHz), high-gain bandwidth (20 MHz), and fast slew rate (10 V/μs) make the OPAx322x family ideal for a wide range of applications, including signal conditioning and sensor amplification requiring high gains. Featuring low THD+N, the OPAx322x series is also excellent for consumer audio applications, particularly for single-supply systems.

The OPAx322S models include a shutdown mode that allow the amplifiers to be switched from normal operation to a standby current that is typically less than 0.1 μA.

The OPA322 (single version) is available in 5-pin SOT-23 and 6-pin SOT-23, while the OPA2322 (dual version) is offered in 8-pin VSSOP, 10-pin VSSOP, 8-pin SOIC, and 8-pin SON packages. The quad version OPA4322 comes in 14-pin TSSOP and 16-pin TSSOP packages. All versions are specified for operation from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA322	SOT-23 (5)	2.90 mm × 1.60 mm
OPA322S	SOT-23 (6)	2.90 mm × 1.60 mm
OPA2322	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SON (8)	3.00 mm × 3.00 mm
OPA2322S	VSSOP (10)	3.00 mm × 3.00 mm
OPA4322	TSSOP (14)	5.00 mm × 4.40 mm
OPA4322S	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2012) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed device package descriptions to current standards ... 1
- Deleted *Package/Ordering Information* table; see *Package Option Addendum* at the end of this data sheet ... 7

Changes from Revision D (March 2012) to Revision E — **Page**

- Changed product status from Production Data to Mixed Status ... 1
- Updated D and DGK pinout drawing ... 5
- Added Figure 26 to Figure 29 ... 15
- Added *Shutdown Function* section ... 20

Changes from Revision C (November 2011) to Revision D — **Page**

- Changed product status from Mixed Status to Production Data ... 1
- Added OPA4322, OPA4322S to the Input Bias Current, *Input bias current, Over temperature* parameter in Electrical Characteristics table ... 9
- Changed Power Supply, OPA4322, OPA4322S *Over temperature* parameter maximum specification in the Electrical Characteristics table ... 10

Changes from Revision B (July 2011) to Revision C — **Page**

- Changed status of OPA2322 SO-8 (D) to production data from product preview ... 1

Changes from Revision A (May 2011) to Revision B **Page**

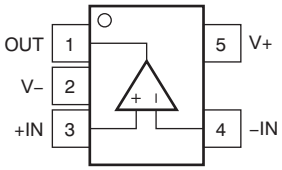
- Added OPA322S thermal information to *OPA322 Thermal Information* table ... 8
- Added OPA2322S thermal information to *OPA2322 Thermal Information* table ... 8
- Added OPA4322S thermal information to *OPA4322 Thermal Information* table ... 8
- Changed Input Bias Current *Input bias current, Over temperature* parameter in Electrical Characteristics table ... 9
- Changed Open-Loop Gain, *Open-loop voltage gain* parameter typical specification in the Electrical Characteristics table ... 9
- Changed Open-Loop Gain, *Phase margin* parameter test conditions in the Electrical Characteristics table ... 9
- Changed Power Supply, Quiescent current per amplifier OPA322/S parameter maximum specification in the Electrical Characteristics ... 10
- Changed Power Supply, OPA322 *Over temperature* parameter maximum specification in the Electrical Characteristics table ... 10
- Changed Power Supply, Quiescent current per amplifier OPA4322/S parameter typical specification in the Electrical Characteristics ... 10
- Added test conditions to *Power Supply* section in Electrical Characteristics table ... 10
- Changed Shutdown, *Quiescent current, per amplifier* parameter maximum specification in Electrical Characteristics table ... 10
- Updated Figure 1 ... 11
- Added Figure 25 ... 15
- Changed *Overload Recovery Time* section ... 19

Changes from Original (January 2011) to Revision A **Page**

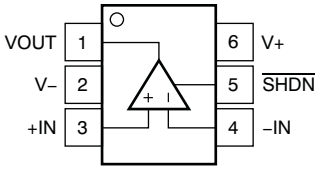
- Changed document status to *Production Data* ... 1

5 Pin Configuration and Functions

OPA322: DBV Package
5-Pin SOT-23
Top View



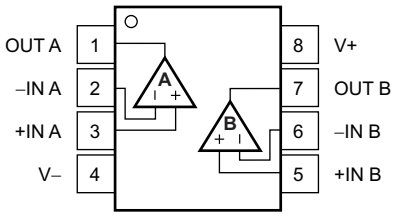
OPA322S: DBV Package
6-Pin SOT-23
Top View



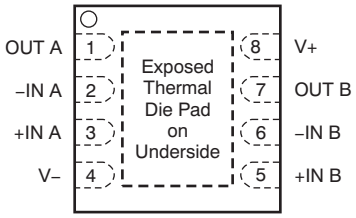
Pin Functions: OPA322, OPA322S

PIN			I/O	DESCRIPTION
NAME	OPA322 SOT-23	OPA322S SOT-23		
–IN	4	4	I	Inverting input
+IN	3	3	I	Noninverting input
OUT	1	1	O	Output
$\overline{\text{SHDN}}$	—	5	I	Shutdown control (active low)
V–	2	2	—	Negative (lowest) power supply
V+	5	6	—	Positive (highest) power supply

OPA2322: D and DGK Packages
8-Pin SOIC and VSSOP
Top View

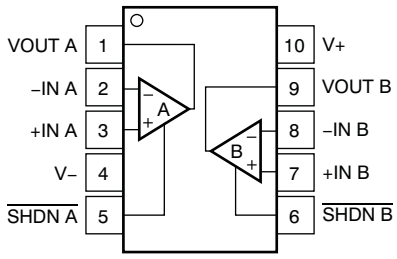


OPA2322: DRG Package
8-Pin SON
Top View



(1) Connect thermal pad to V–.
(2) Pad size: 2 mm × 1.2 mm.

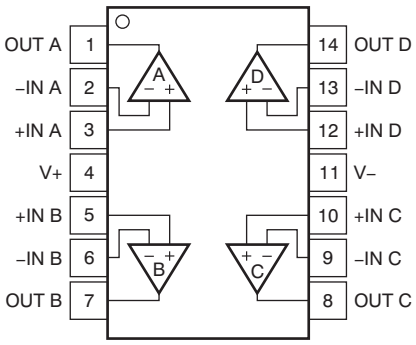
OPA2322S: DGS Package
10-Pin VSSOP
Top View



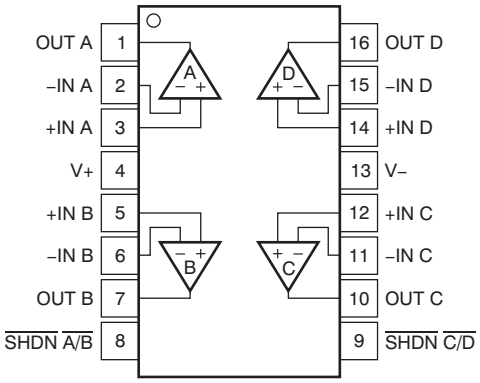
Pin Functions: OPA2322, OPA2322S

PIN				I/O	DESCRIPTION
NAME	OPA2322		OPA2322S		
	SOIC, VSSOP	SON	VSSOP		
–IN A	2	2	2	I	Inverting input, channel A
+IN A	3	3	3	I	Noninverting input, channel A
–IN B	6	6	8	I	Inverting input, channel B
+IN B	5	5	7	I	Noninverting input, channel B
OUT A	1	1	—	O	Output, channel A
OUT B	7	7	—	O	Output, channel B
$\overline{\text{SHDN A}}$	—	—	5	I	Shutdown control, channel A (active low)
$\overline{\text{SHDN B}}$	—	—	6	I	Shutdown control, channel B (active low)
V–	4	4	4	—	Negative (lowest) power supply
V+	8	8	10	—	Positive (highest) power supply
VOUT A	—	—	1	O	Output, channel A
VOUT B	—	—	9	O	Output, channel B

PW Package
14-Pin TSSOP
Top View



PW Package
16-Pin TSSOP
Top View



Pin Functions: OPA4322, OPA4322S

PIN			I/O	DESCRIPTION
NAME	OPA4322	OPA4322S		
	TSSOP	TSSOP		
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
–IN C	9	11	I	Inverting input, channel C
+IN C	10	12	I	Noninverting input, channel C
–IN D	13	15	I	Inverting input, channel D
+IN D	12	14	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	10	O	Output, channel C
OUT D	14	16	O	Output, channel D
$\overline{\text{SHDN A/B}}$	—	8	I	Shutdown control, channels A and B (active low)
$\overline{\text{SHDN C/D}}$		9	I	Shutdown control, channels C and D (active low)
V–	11	13	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		6	V
	Signal input pins(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input pins(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Operating, T_A	–40	150	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Specified voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information: OPA322, OPA322S

THERMAL METRIC(1)		OPA322 DBV (SOT-23) 5 PINS	OPA322S DBV (SOT-23) 6 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	219.3	177.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	107.5	108.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	27.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	13.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.9	26.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2322, OPA2322S

THERMAL METRIC(1)		OPA2322 D (SOIC) 8 PINS	OPA2322 DRG (SON) 8 PINS	OPA2322 DGK (VSSOP) 8 PINS	OPA2322S DGS (VSSOP) 10 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.6	50.6	174.8	171.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	67.1	54.9	43.9	43	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64	25.2	95	91.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.2	0.6	2	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.4	25.3	93.5	89.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	—	5.7	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4322, OPA4322S

THERMAL METRIC(1)		OPA4322 PW (TSSOP) 14 PINS	OPA4322S PW (TSSOP) 16 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.8	105.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.9	28.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	51.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.8	50.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

At V_S = 1.8 V to 5.5 V, or ±0.9 V to ±2.75 V, T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and $\overline{SHDN\_x}$ = V_S+ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.5	2	mV
dV_{OS}/dT	vs temperature	V_S = 5.5 V			1.8	6	µV/°C
PSR	vs power supply	V_S = 1.8 V to 5.5 V	T_A = 25°C		10	50	µV/V
			T_A = –40°C to 125°C		20	65	
	Channel separation	At 1 kHz			130		dB
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	T_A = 25°C	90	100		dB
			T_A = –40°C to 125°C	90			
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			±0.2	±10	pA
		T_A = –40°C to 85°C				±50	
		OPA322 and OPA322S, T_A = –40°C to 125°C				±800	
		OPA2322 and OPA2322S, T_A = –40°C to 125°C				±400	
		OPA4322 and OPA4322S, T_A = –40°C to 125°C				±400	
I_{OS}	Input offset current	T_A = 25°C			±0.2	±10	pA
		T_A = –40°C to 85°C				±50	
		T_A = –40°C to 125°C				±400	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.8		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz			8.5		nV/√Hz
		f = 10 kHz			7		
i_n	Input current noise density	f = 1 kHz			0.6		fA/√Hz
INPUT CAPACITANCE							
	Differential				5		pF
	Common-mode				4		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ		100	130		dB
		0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ		94			
PM	Phase margin	V_S = 5 V, C_L = 50 pF			47		°
FREQUENCY RESPONSE							
GBP	Gain bandwidth product	V_S = 5 V, C_L = 50 pF, unity gain			20		MHz
SR	Slew rate	V_S = 5 V, C_L = 50 pF, G = +1			10		V/µs
t_S	Settling time	V_S = 5 V, C_L = 50 pF, to 0.1%, 2-V step, G = +1			0.25		µs
		V_S = 5 V, C_L = 50 pF, to 0.01%, 2-V step, G = +1			0.32		
	Overload recovery time	V_S = 5 V, C_L = 50 pF, V_{IN} × G > V_S			100		ns
THD+N	Total harmonic distortion + noise(1)	V_S = 5 V, C_L = 50 pF, V_O = 4 V_{PP}, G = +1, f = 10 kHz, R_L = 10 kΩ			0.0005%		
		V_S = 5 V, C_L = 50 pF, V_O = 2 V_{PP}, G = +1, f = 10 kHz, R_L = 600 Ω			0.0011%		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB

Electrical Characteristics (continued)

At V_S = 1.8 V to 5.5 V, or ±0.9 V to ±2.75 V, T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and $\overline{SHDN}\_x$ = V_S+ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output (swing from both rails)	R_L = 10 kΩ	T_A = 25°C		10	20	mV
			T_A = –40°C to 125°C			30	
I_{SC}	Short-circuit current	V_S = 5.5 V			±65		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
R_O	Open-loop output resistance	I_O = 0 mA, f = 1 MHz			90		Ω
POWER SUPPLY							
V_S	Specified voltage range			1.8		5.5	V
I_Q	Quiescent current per amplifier	OPA322 and OPA322S, I_O = 0 mA, V_S = 5.5 V	T_A = 25°C		1.6	1.9	mA
			T_A = –40°C to 125°C			2	
		OPA2322 and OPA2322S, I_O = 0 mA, V_S = 5.5 V	T_A = 25°C		1.5	1.75	
			T_A = –40°C to 125°C			1.85	
		OPA4322 and OPA4322S, I_O = 0 mA, V_S = 5.5 V	T_A = 25°C		1.4	1.65	
			T_A = –40°C to 125°C			1.75	
	Power-on time	V_{S+} = 0 V to 5 V, to 90% I_Q level			28		µs
SHUTDOWN(2)							
I_{QSD}	Quiescent current (per amplifier)	V_S = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{SHDN}$ = $V_{S–}$			0.1	0.5	µA
V_{IH}	High voltage (enabled)	V_S = 1.8 V to 5.5 V, amplifier enabled		(V+) – 0.1			V
V_{IL}	Low voltage (disabled)	V_S = 1.8 V to 5.5 V, amplifier disabled				(V–) + 0.1	V
t_{ON}	Amplifier enable time (full shutdown)(3)	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S/2(4)			10		µs
	Amplifier enable time (partial shutdown)(3)	V_S = 1.8 V to 5.5 V, partial shutdown; G = 1, V_{OUT} = 0.9 × V_S/2(4)			6		µs
t_{OFF}	Amplifier disable time(3)	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S/2			3		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V_{IH} = 5 V			0.13		µA
		V_S = 1.8 V to 5.5 V, V_{IL} = 0 V			0.04		

(2) Ensured by design and characterization; not production tested.
(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(4) Full shutdown refers to the dual OPA2322S having both channels A and B disabled ($\overline{SHDN\_A}$ = $\overline{SHDN\_B}$ = $V_{S–}$) and the quad OPA4322S having all channels A to D disabled ($\overline{SHDN\_A/B}$ = $\overline{SHDN\_C/D}$ = $V_{S–}$). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

6.8 Typical Characteristics

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted).

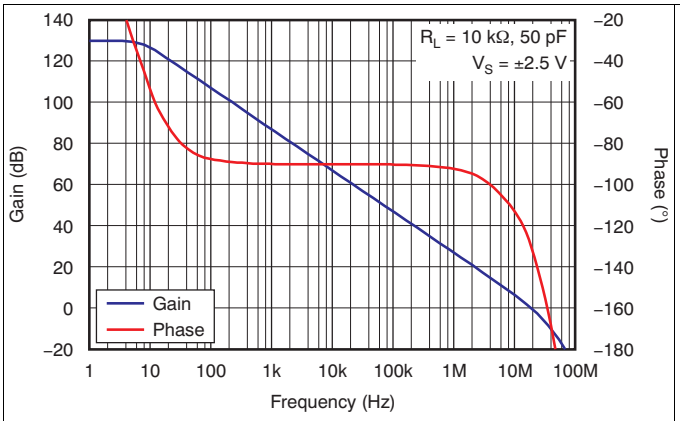


Figure 1. Open-Loop Gain and Phase vs Frequency

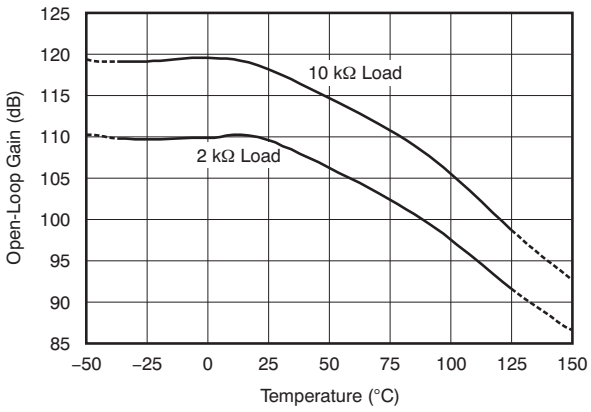


Figure 2. Open-Loop Gain vs Temperature

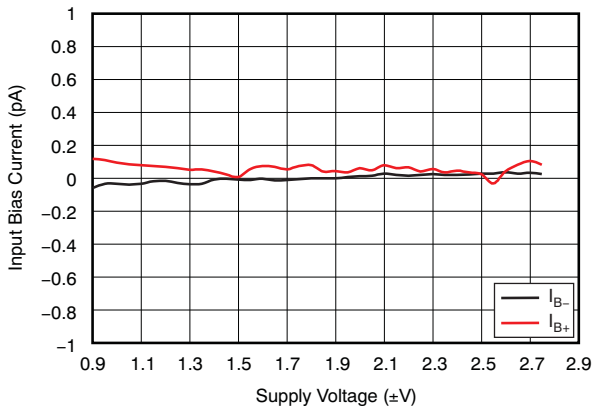


Figure 3. Input Bias Current vs Supply Voltage

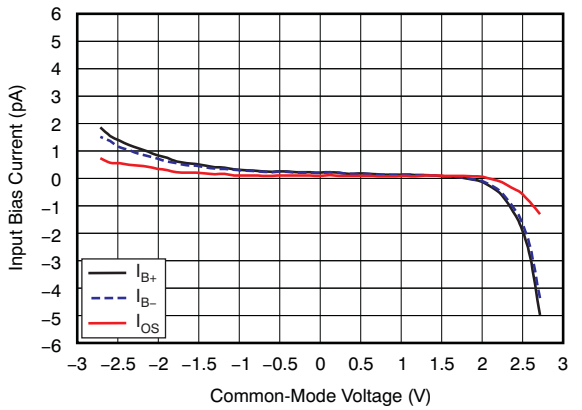


Figure 4. Input Bias Current vs Common-Mode Voltage

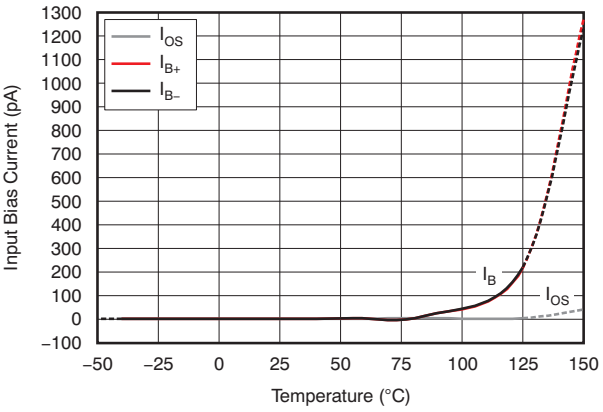


Figure 5. Input Bias Current vs Temperature

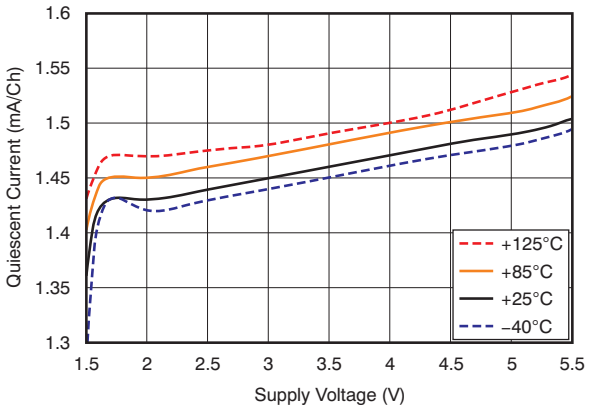


Figure 6. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted).

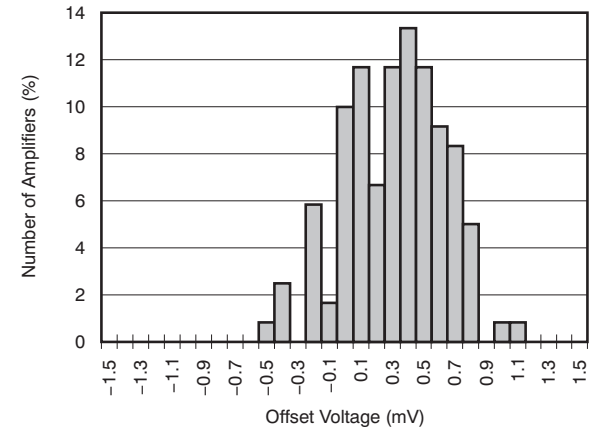


Figure 7. Offset Voltage Production Histogram

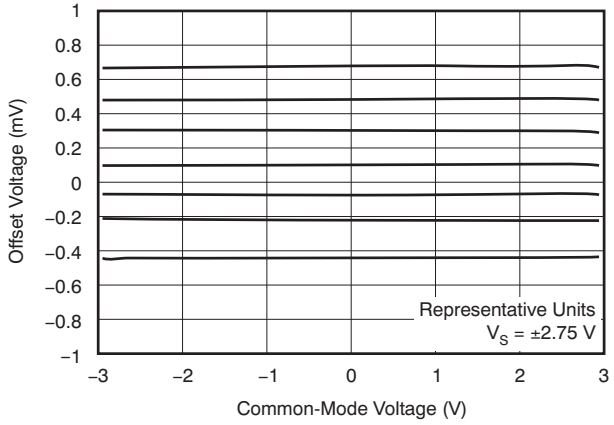


Figure 8. Offset Voltage vs Common-Mode Voltage

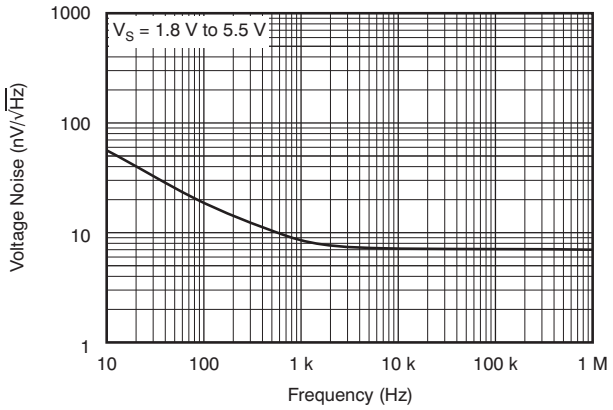


Figure 9. Input Voltage Noise Spectral Density vs Frequency

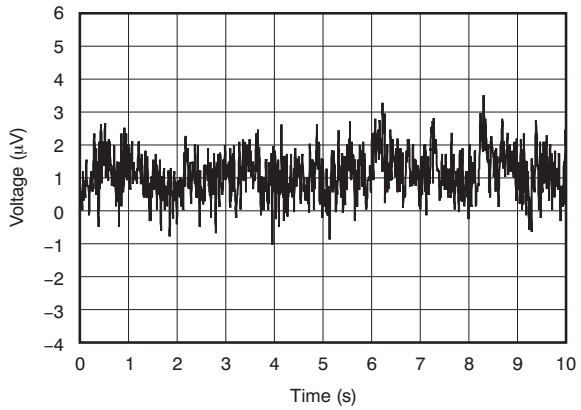


Figure 10. 0.1-Hz to 10-Hz Input Voltage Noise

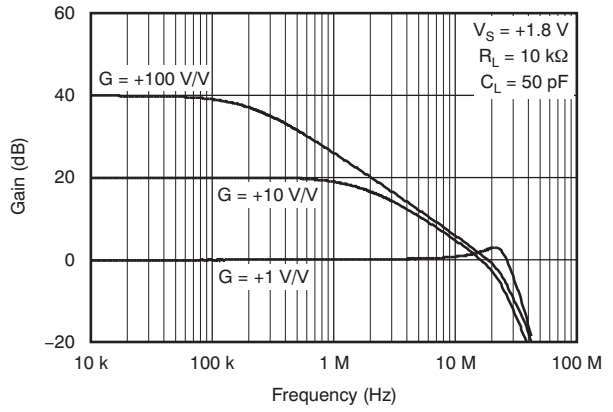


Figure 11. Closed-Loop Gain vs Frequency

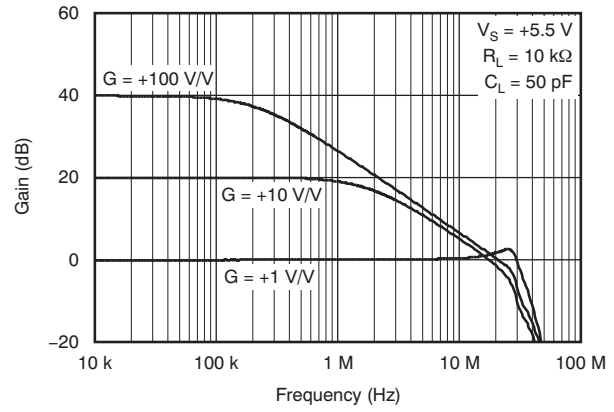


Figure 12. Closed-Loop Gain vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted).

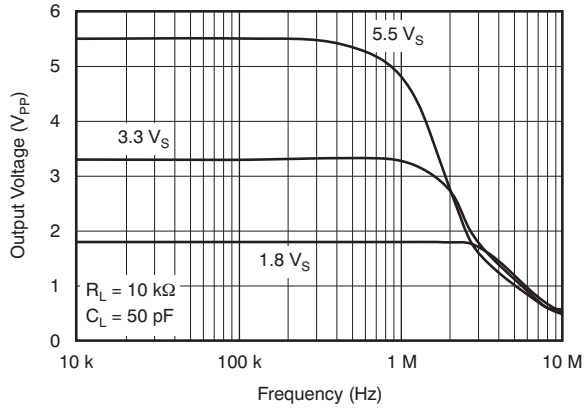


Figure 13. Maximum Output Voltage vs Frequency

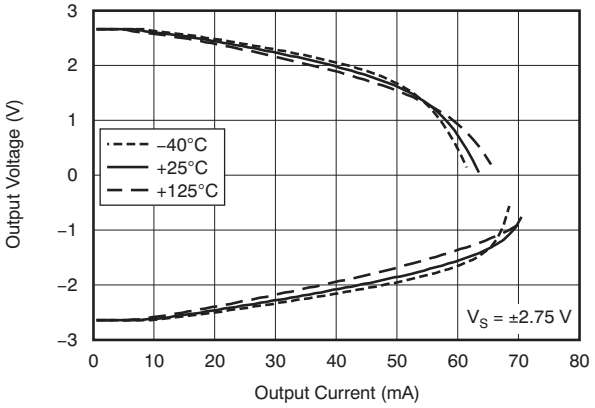


Figure 14. Output Voltage Swing vs Output Current

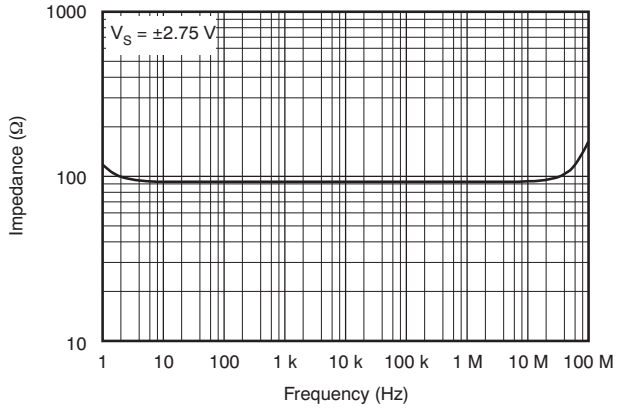


Figure 15. Open-Loop Output Impedance vs Frequency

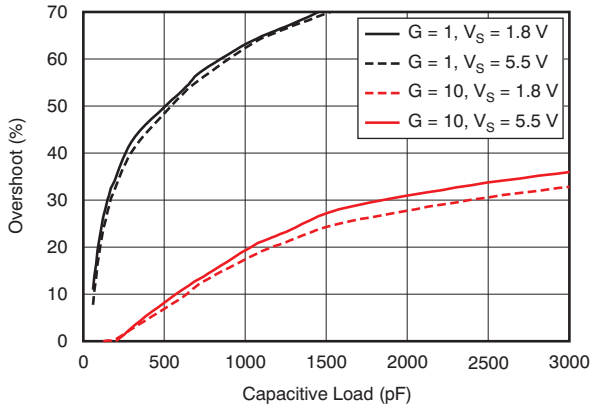


Figure 16. Small-Signal Overshoot vs Load Capacitance

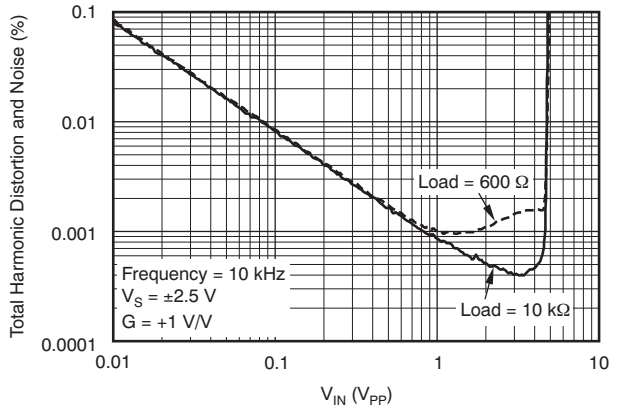


Figure 17. THD+N vs Amplitude

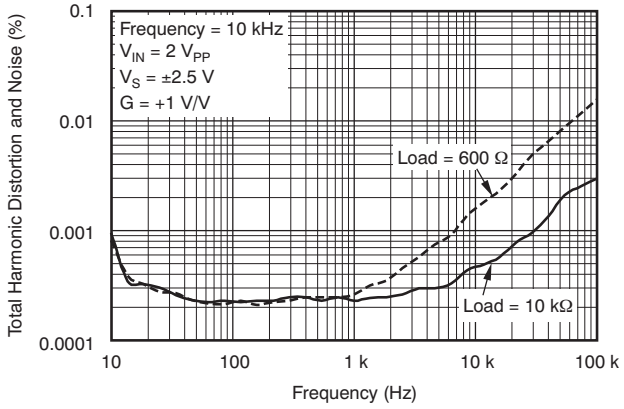


Figure 18. THD+N vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted).

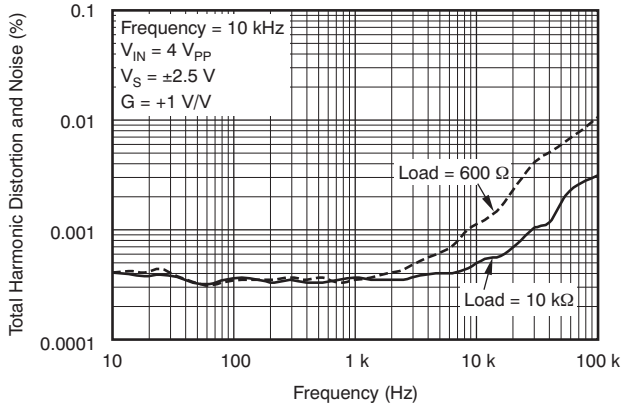


Figure 19. THD+N vs Frequency

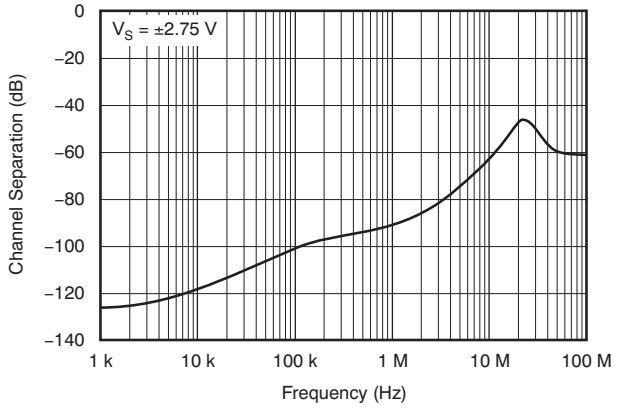


Figure 20. Channel Separation vs Frequency (for Dual)

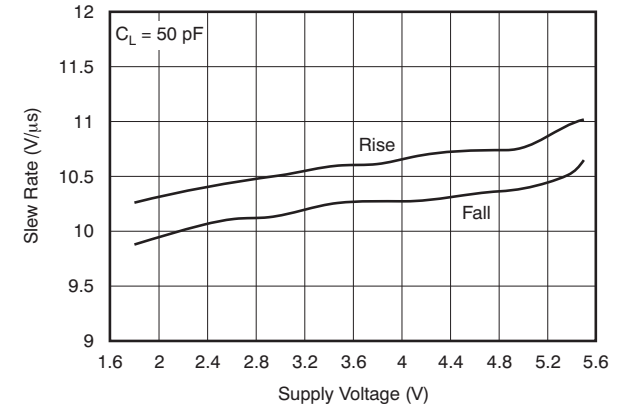


Figure 21. Slew Rate vs Supply Voltage

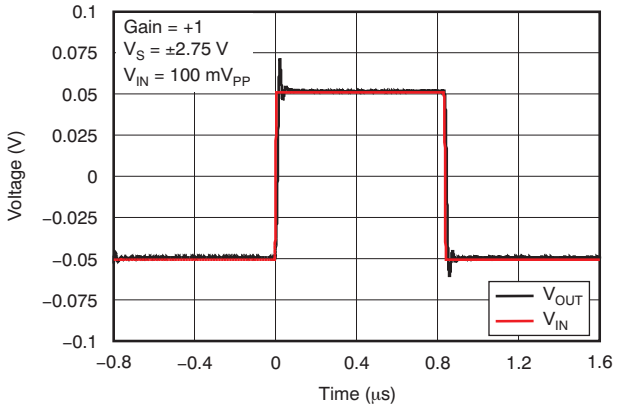


Figure 22. Small-Signal Step Response

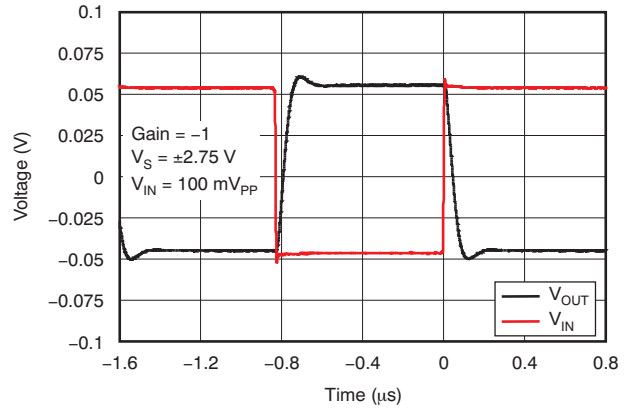


Figure 23. Small-Signal Step Response

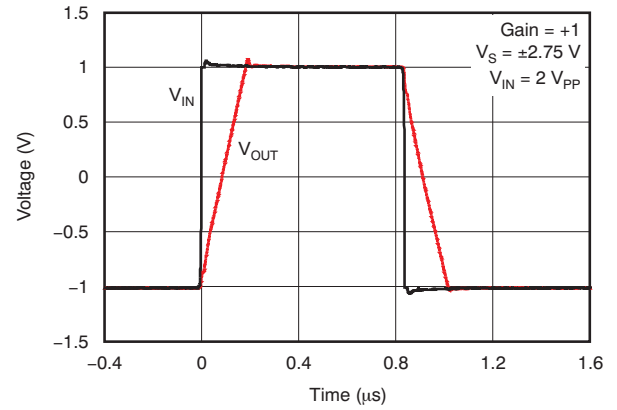


Figure 24. Large-Signal Step Response vs Time

Typical Characteristics (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted).

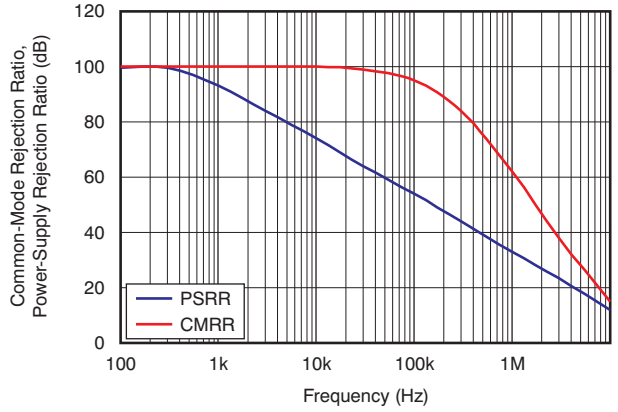


Figure 25. CMRR and PSRR vs Frequency

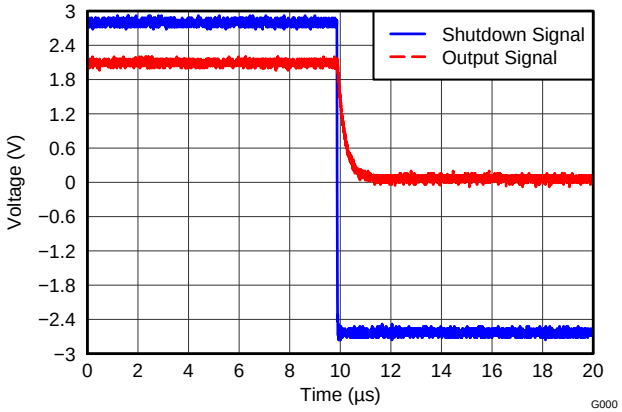


Figure 26. Turnoff Transient

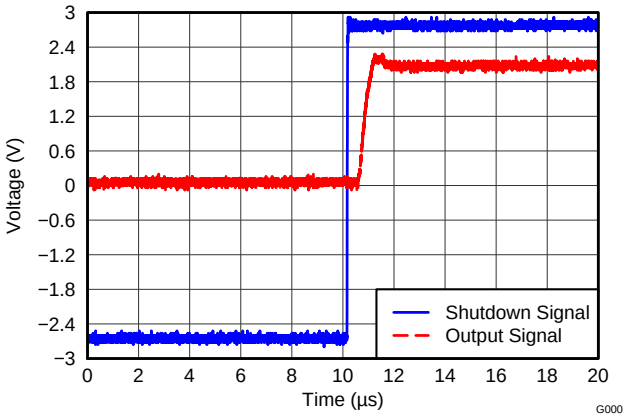
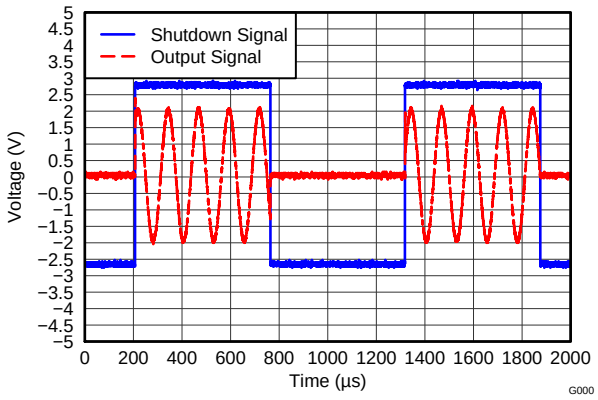
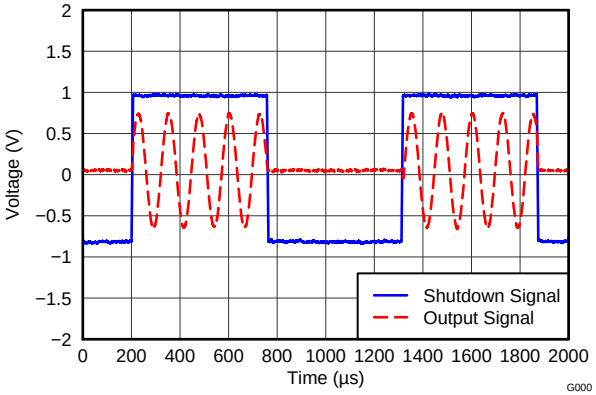


Figure 27. Turnon Transient



5.5 V (High Supply)

Figure 28. Turnon and Turnoff Transient



1.8 V (Low Supply)

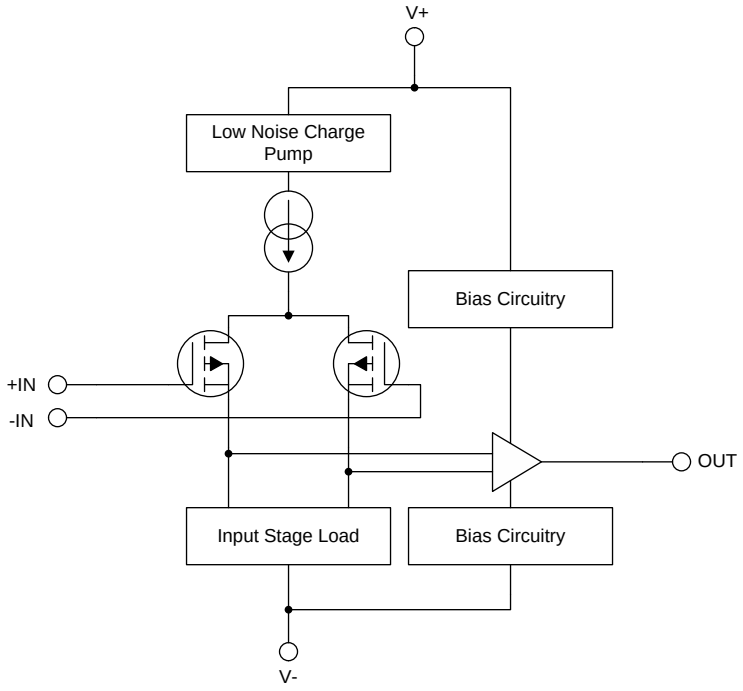
Figure 29. Turnon and Turnoff Transient

7 Detailed Description

7.1 Overview

The OPA322 family of operational amplifiers (op amps) are high-speed, precision amplifiers perfectly suited to drive 12-, 14-, and 16-bit analog-to-digital converters. Low-output impedance with flat frequency characteristics and zero-crossover distortion circuitry enable high linearity over the full input common-mode range, achieving true rail-to-rail input from a 1.8-V to 5.5-V single supply.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA322 series op amps are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (±0.9 V to ±2.75 V), making them highly versatile and easy to use. The power-supply pins must have local bypass ceramic capacitors (typically 0.001 μF to 0.1 μF). These amplifiers are fully specified from 1.8 V to 5.5 V and over the extended temperature range of –40°C to 125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

7.3.2 Input and ESD Protection

The OPA322 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 30 shows how a series input resistor (R_S) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to the minimum in noise-sensitive applications.

Feature Description (continued)

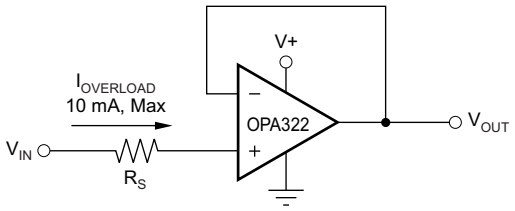


Figure 30. Input Current Protection

7.3.3 Phase Reversal

The OPA322 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 31 shows the input voltage exceeding the supply voltage without any phase reversal.

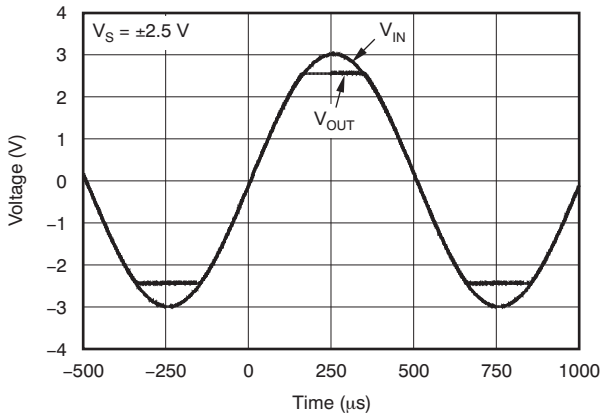
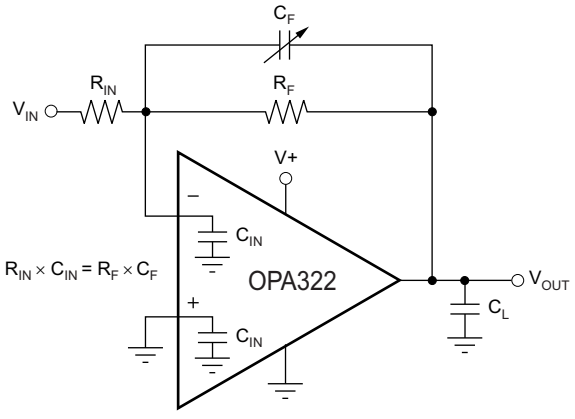


Figure 31. No Phase Reversal

7.3.4 Feedback Capacitor Improves Response

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 32. This capacitor compensates for the zero created by the feedback network impedance and the OPA322 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



NOTE: Where C_{IN} is equal to the OPA322 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 32. Feedback Capacitor Improves Dynamic Performance

Feature Description (continued)

For the circuit shown in Figure 32, the value of the variable feedback capacitor must be chosen so that the input resistance times the input capacitance of the OPA322 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor with Equation 1.

$$R_{IN} \times C_{IN} = R_F \times C_F \quad (1)$$

where

- C_{IN} is equal to the OPA322 input capacitance (sum of differential and common-mode) plus the layout capacitance

The capacitor value can be adjusted until optimum performance is obtained.

7.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA322 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

7.3.6 Output Impedance

The open-loop output impedance of the OPA322 common-source output stage is approximately 90 Ω. When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a tenfold increase in effective output impedance. While the OPA322 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This characteristic, in turn, prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA322 has excellent capacitive load drive capability for an op amp with its bandwidth.

7.3.7 Capacitive Load and Stability

The OPA322 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA322 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA322 remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 33. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S), typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 34.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider, however, may be insignificant. For instance, with a load resistance, R_L = 10 kΩ and R_S = 20 Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600 Ω, which the OPA322 is able to drive, the error increases to 7.5%.

Feature Description (continued)

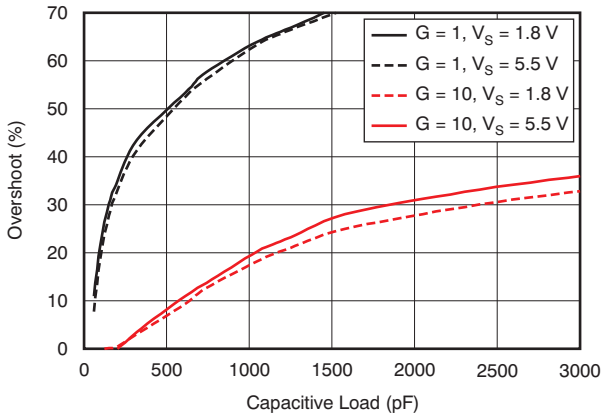


Figure 33. Small-Signal Overshoot vs Capacitive Load (100-mV$_{PP}$ Output Step)

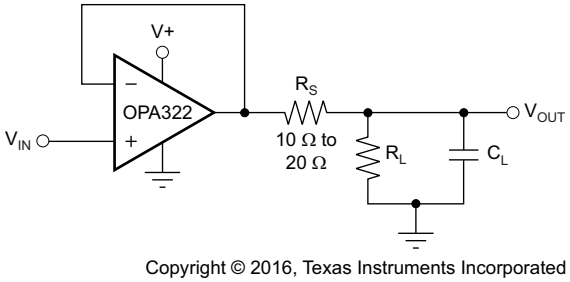


Figure 34. Improving Capacitive Load Drive

7.3.8 Overload Recovery Time

Overload recovery time is the time required for the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 35 and Figure 36 show the positive and negative overload recovery times of the OPA322, respectively. In both cases, the time elapsed before the OPA322 comes out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

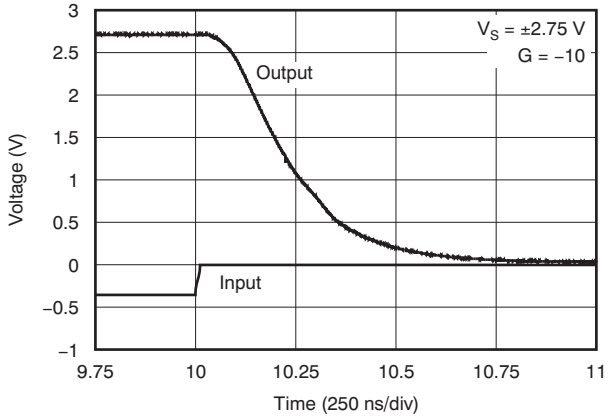


Figure 35. Positive Recovery Time

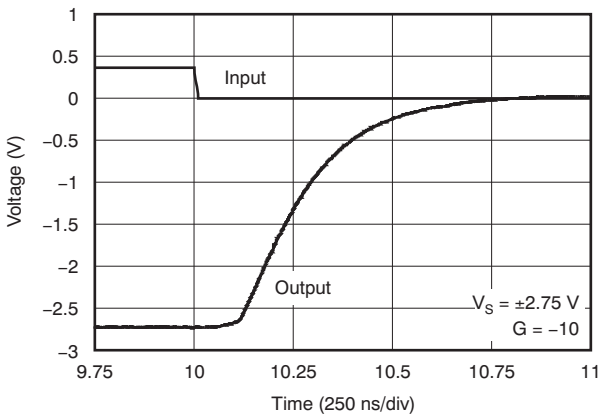


Figure 36. Negative Recovery Time

Feature Description (continued)

7.3.9 Shutdown Function

The SHDN (enable) pin function of the OPAx322S is referenced to the negative supply voltage of the operational amplifier. A logic level high enables the op amp. A valid logic high is defined as voltage [(V+) – 0.1 V], up to (V+), applied to the SHDN pin. A valid logic low is defined as [(V–) + 0.1 V], down to (V–), applied to the enable pin. The maximum allowed voltage applied to SHDN is 5.5 V with respect to the negative supply, independent of the positive supply voltage. This pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit.

The logic input is a high-impedance CMOS input. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx322S to be operated as a *gated* amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases with increased load resistance. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to mid-supply (V_S / 2) is required. If using the OPAx322S without a load, the resulting turnoff time is significantly increased.

7.4 Device Functional Modes

The OPA322 family of operational amplifiers are operational when power-supply voltages between 1.8 V to 5.5 V are applied. Devices with an *S* suffix have a shutdown capability. For a detailed description of the shutdown function, refer to *Shutdown Function*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA322 family offers outstanding DC and AC performance. These devices operate up to a 5.5-V power supply and offer ultra-low input bias current and 20-MHz bandwidth. These features make the OPA322 family a robust operational amplifier for both battery-powered and industrial applications.

8.1.1 Active Filter

The OPA322 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 37 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional second-order MFB stage; or
3. using a noninverting filter topology, such as the Sallen-Key (shown in Figure 38).

MFB, Sallen-Key, low-pass, and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

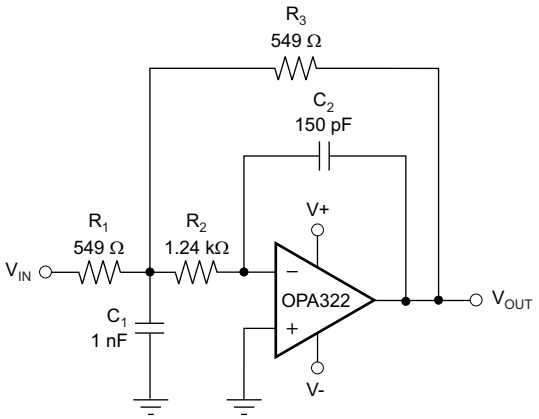


Figure 37. Second-Order, Butterworth, 500-kHz Low-Pass Filter

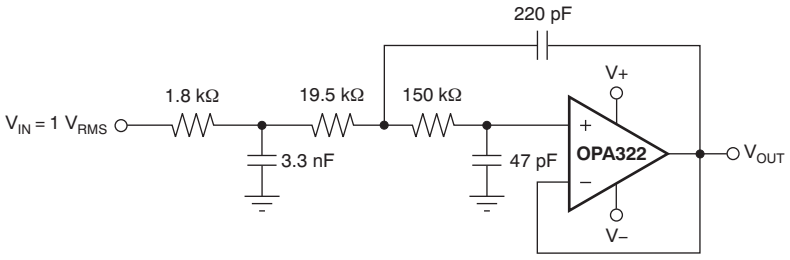


Figure 38. OPA322 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

8.2 Typical Application

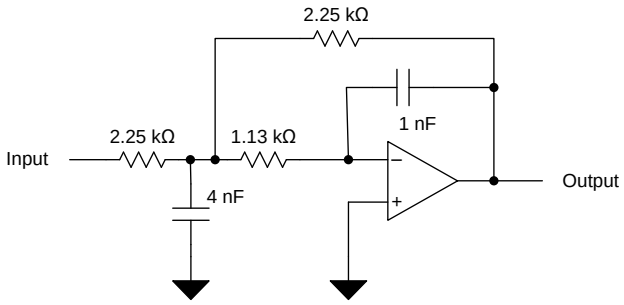


Figure 39. Second-Order, Low-Pass Filter Schematic

8.2.1 Design Requirements

- Gain = 1 V/V
- Low-pass cutoff frequency = 50 kHz
- –40-db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in. Use Equation 2 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \tag{2}$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the lowpass cutoff frequency are calculated by Equation 3.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \tag{3}$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

Typical Application (continued)

8.2.3 Application Curve

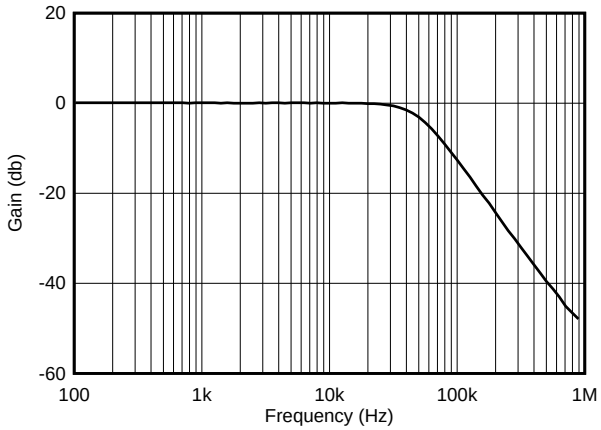


Figure 40. OPA322 Second-Order, 50-kHz, Low-Pass Filter

9 Power Supply Recommendations

The OPA322 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

10 Layout

10.1 Layout Guidelines

The OPA322 is a wideband amplifier. To realize the full operational performance of the device, follow good high-frequency printed-circuit board (PCB) layout practices. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces must be designed for minimum inductance.

10.1.1 Leadless DFN Package

The OPA2322 uses the DFN style package (also known as SON), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes PCB space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low height (0.8 mm).

DFN packages are physically small, and have a smaller routing area. Additionally, they offer improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SOIC and VSSOP). The absence of external leads also eliminates bent-lead issues.

The DFN package can easily be mounted using standard PCB assembly techniques. See the application reports, *QFN/SON PCB Attachment* and *Quad Flatpack No-Lead Logic Packages*. The dimension of the exposed thermal die pad is 2 mm × 1.2 mm and is centered.

NOTE

The exposed leadframe die pad on the bottom of the DFN package must be connected to the most negative potential (V–).

10.2 Layout Example

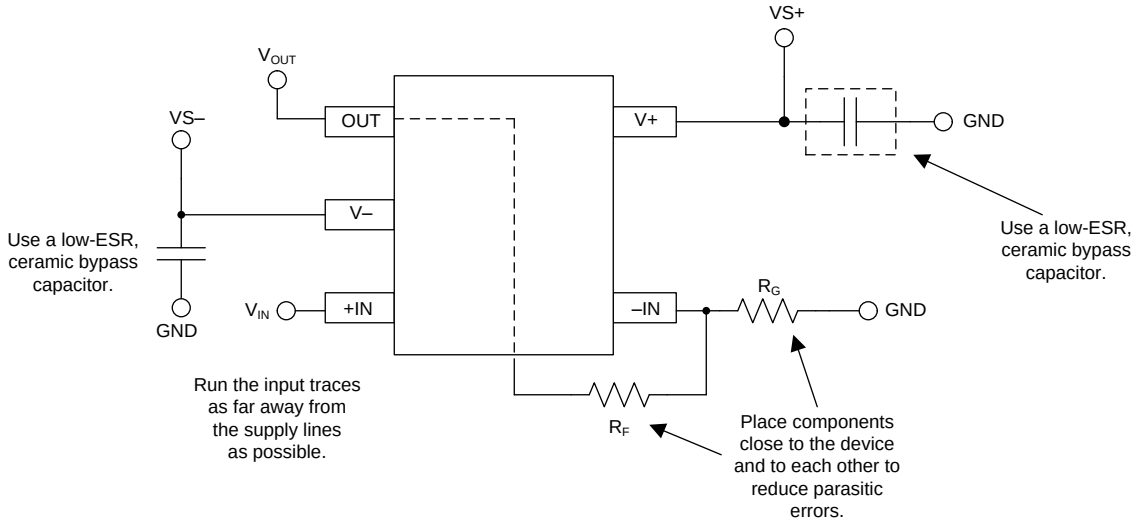


Figure 41. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

11.1.2.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.2.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.2.3 Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.2.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.2.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Device Support (continued)

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPA322x, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *QFN/SON PCB Attachment* (SLUA271)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)
- *OPA322, OPA2322, OPA4322 EMIR Immunity Performance* (SBOT005)
- *FilterPro™ User's Guide* (SBFA001)
- *AFE for Transient Recorder and Digital Fault Recorder Using High-Speed ADCs and Differential Amplifiers* (TIDUAT7)
- *Reference Design for Interfacing Current Output Hall Sensors and CTs With Differential ADCs/MCUs* (TIDUA57)
- *Single-Ended Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors* (TIDU583)
- *Differential Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors* (TIDU569)

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA322	Click here	Click here	Click here	Click here	Click here
OPA322S	Click here	Click here	Click here	Click here	Click here
OPA2322	Click here	Click here	Click here	Click here	Click here
OPA2322S	Click here	Click here	Click here	Click here	Click here
OPA4322	Click here	Click here	Click here	Click here	Click here
OPA4322S	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

FilterPro, TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2322AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2322A	Samples
OPA2322AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOZI	Samples
OPA2322AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOZI	Samples
OPA2322AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2322A	Samples
OPA2322AIDRGR	ACTIVE	SON	DRG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPCI	Samples
OPA2322AIDRGT	ACTIVE	SON	DRG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPCI	Samples
OPA2322SAIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPBI	Samples
OPA2322SAIDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPBI	Samples
OPA322AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAD	Samples
OPA322AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAD	Samples
OPA322SAIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAF	Samples
OPA322SAIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAF	Samples
OPA4322AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322A	Samples
OPA4322AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322A	Samples
OPA4322SAIPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322SA	Samples
OPA4322SAIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322SA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2322, OPA322, OPA4322 :

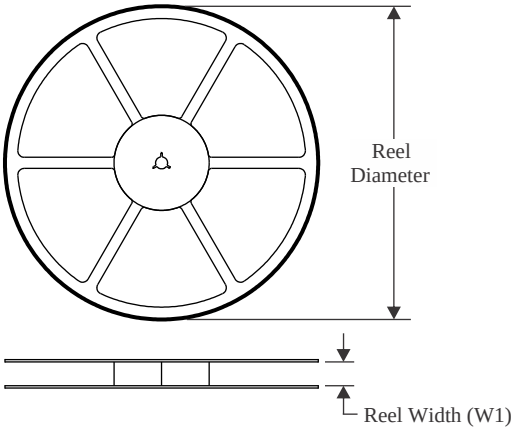
- Automotive : OPA2322-Q1, OPA322-Q1, OPA4322-Q1

NOTE: Qualified Version Definitions:

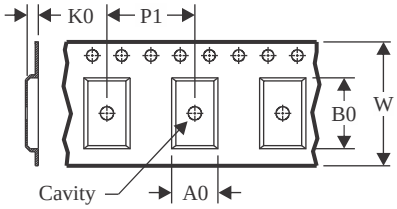
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

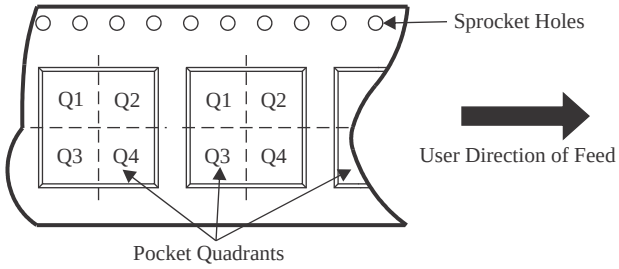


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

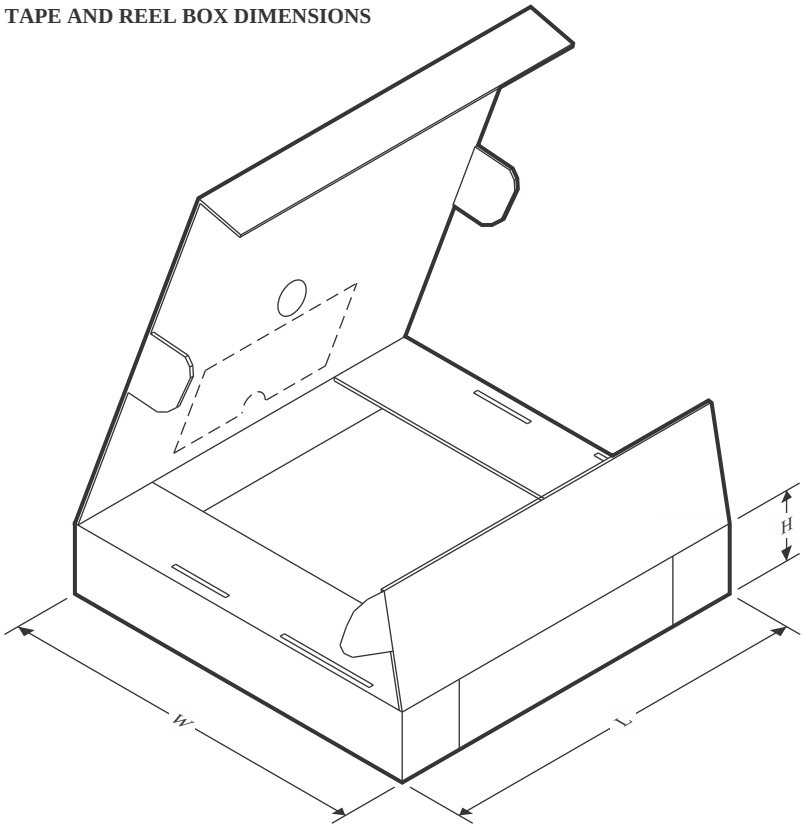
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2322AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2322AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2322AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2322SAIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322SAIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA322AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA322AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA322AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA322SAIDBVT	SOT-23	DBV	6	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA4322AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4322SAIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

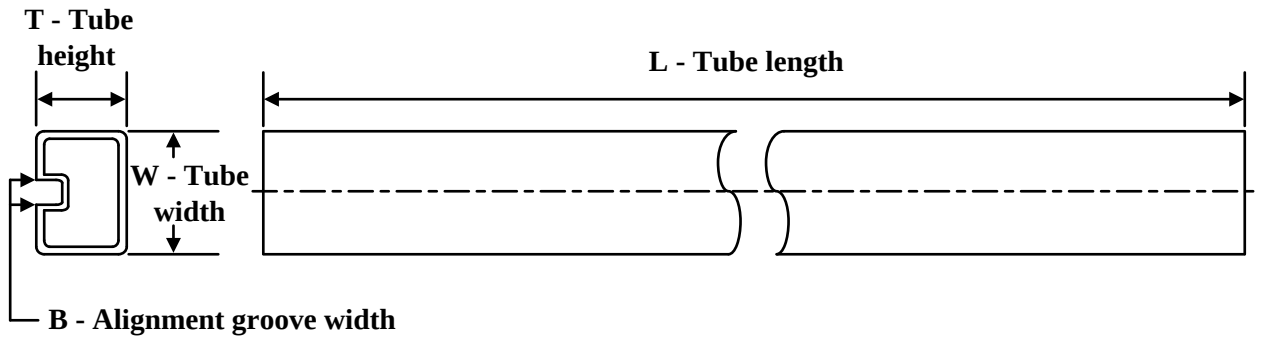
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2322AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2322AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2322AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2322AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2322AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2322AIDRGR	SON	DRG	8	3000	356.0	356.0	35.0
OPA2322AIDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA2322SAIDGSR	VSSOP	DGS	10	2500	356.0	356.0	35.0
OPA2322SAIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA322AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA322AIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA322AIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA322SAIDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
OPA4322AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA4322SAIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

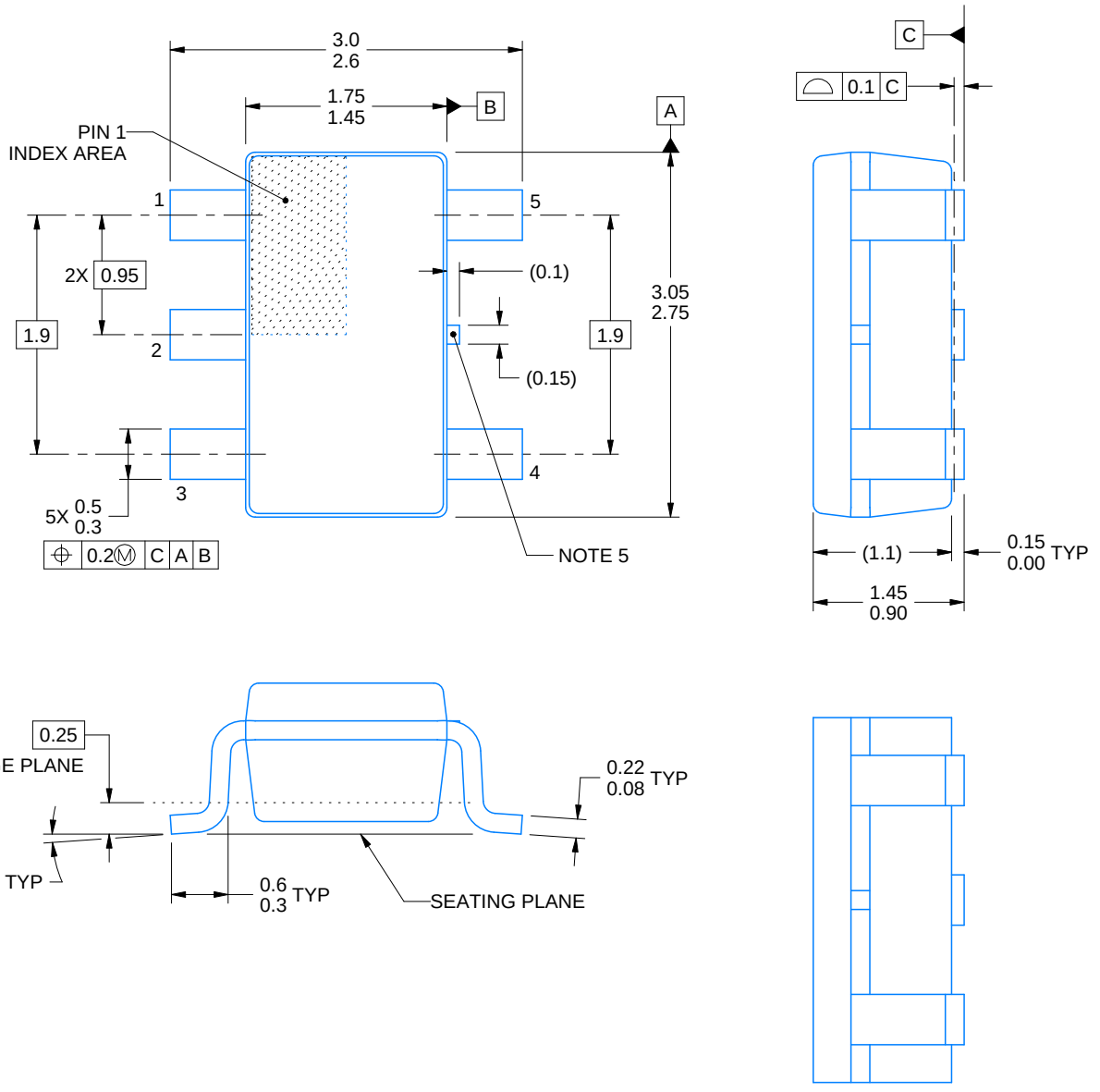
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2322AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4322AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA4322SAIPW	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

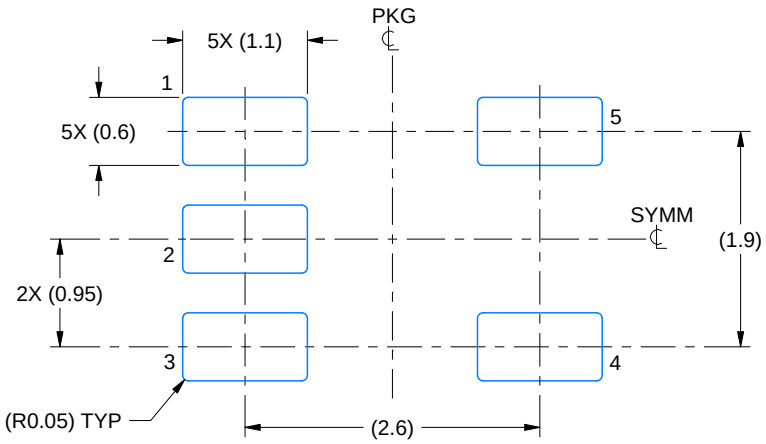


ALTERNATIVE PACKAGE SINGULATION VIEW

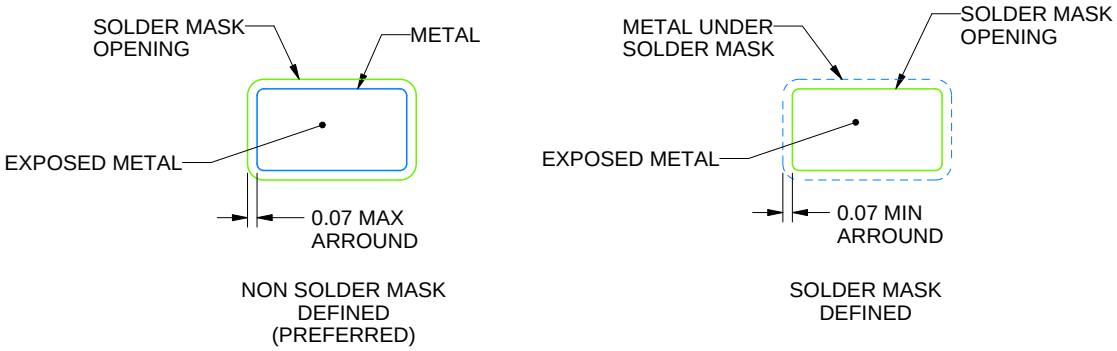
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

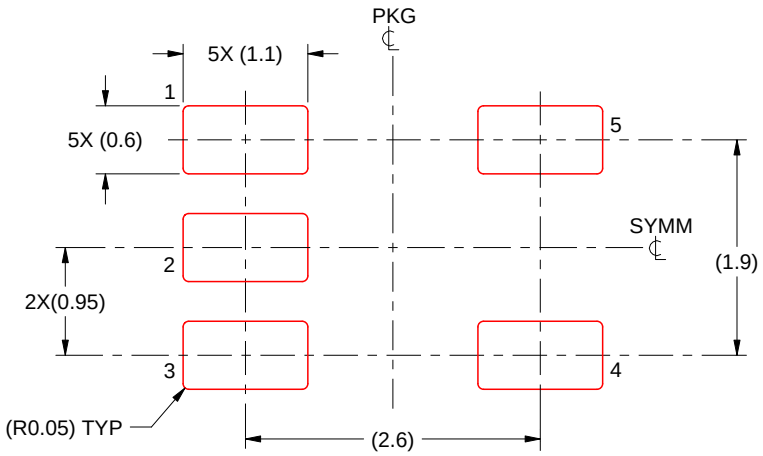


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



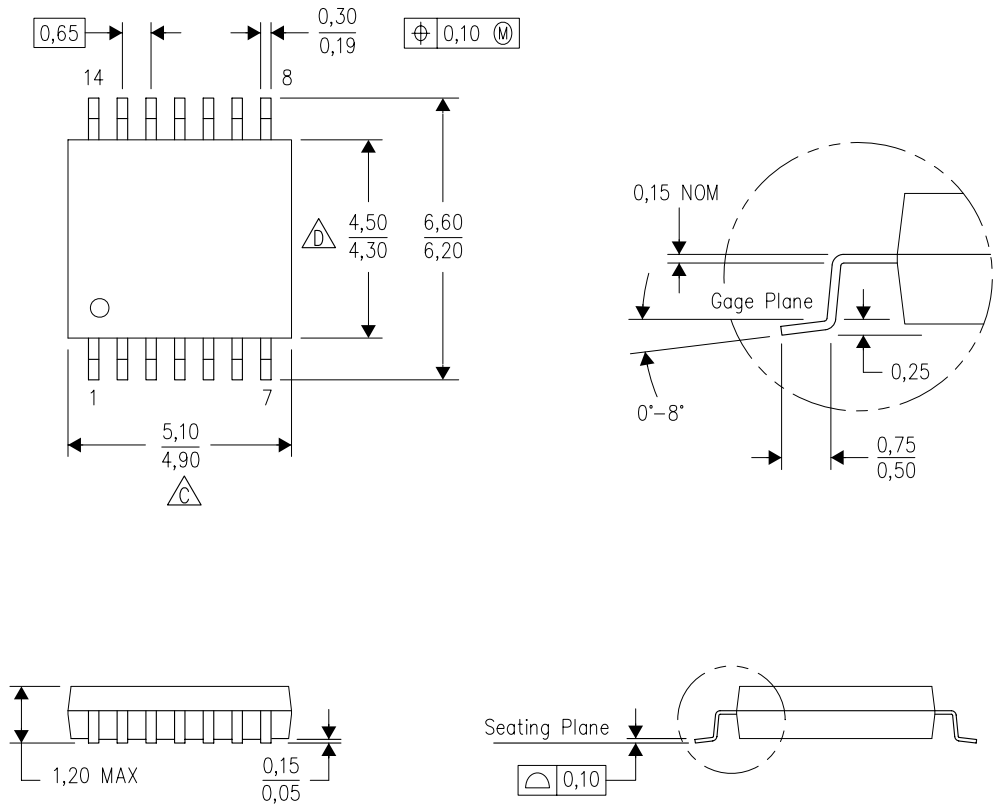
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

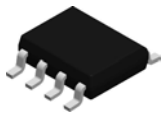
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

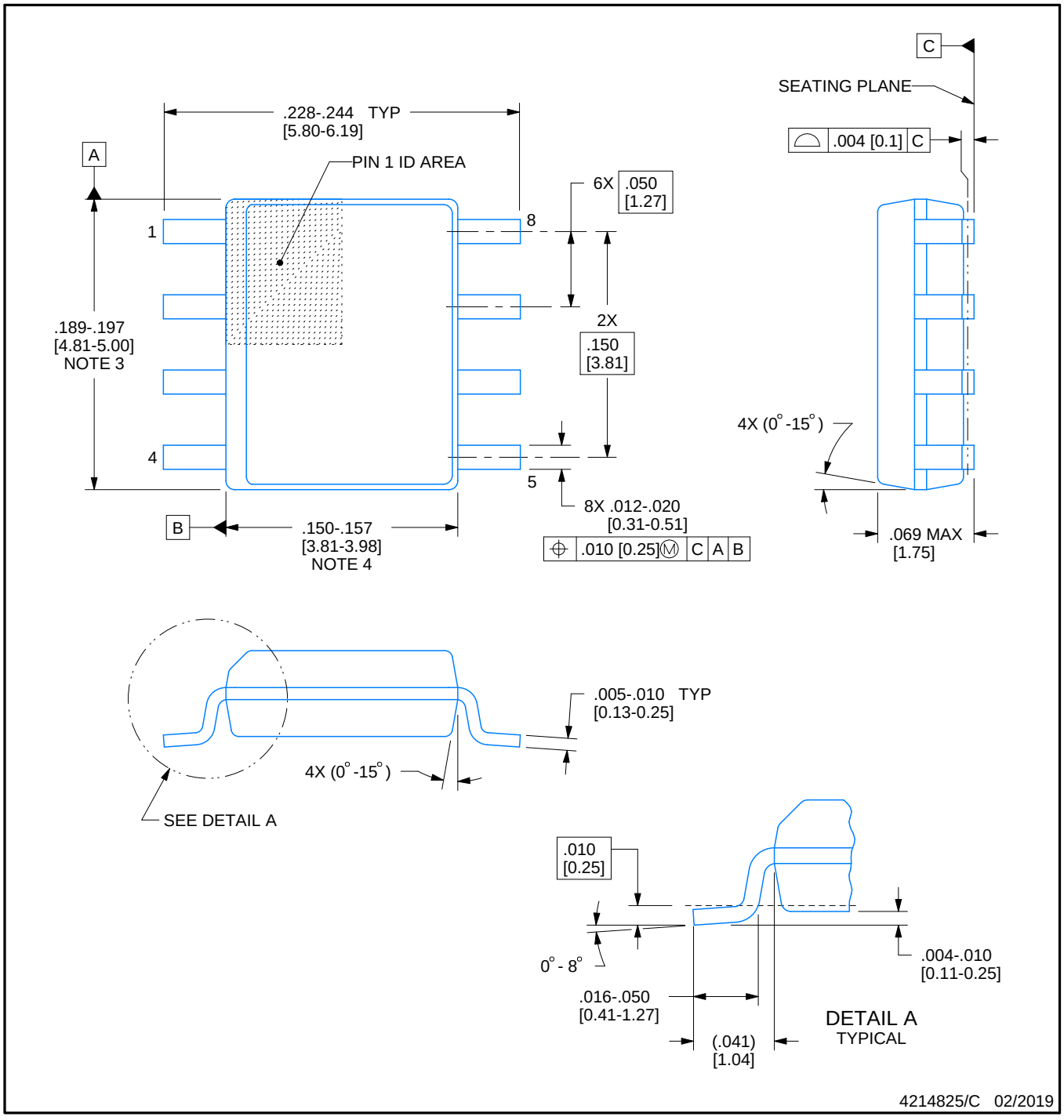


PACKAGE OUTLINE

D0008A

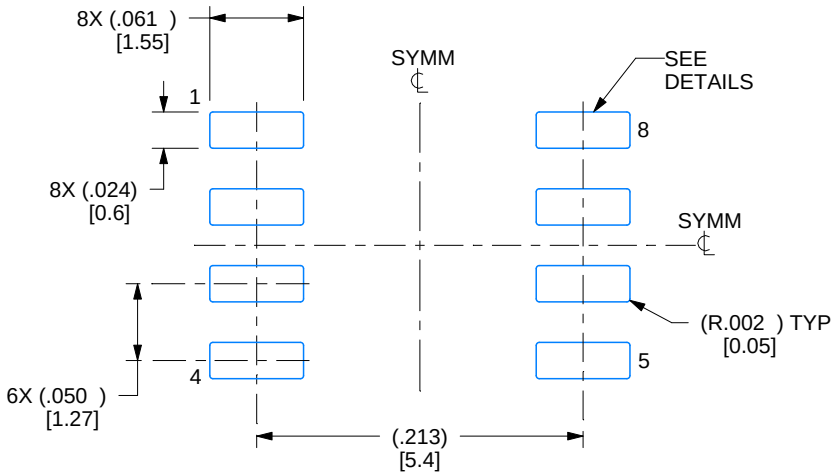
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

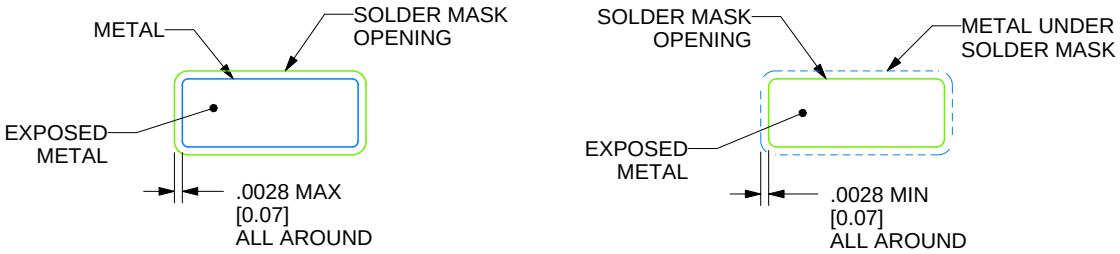


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

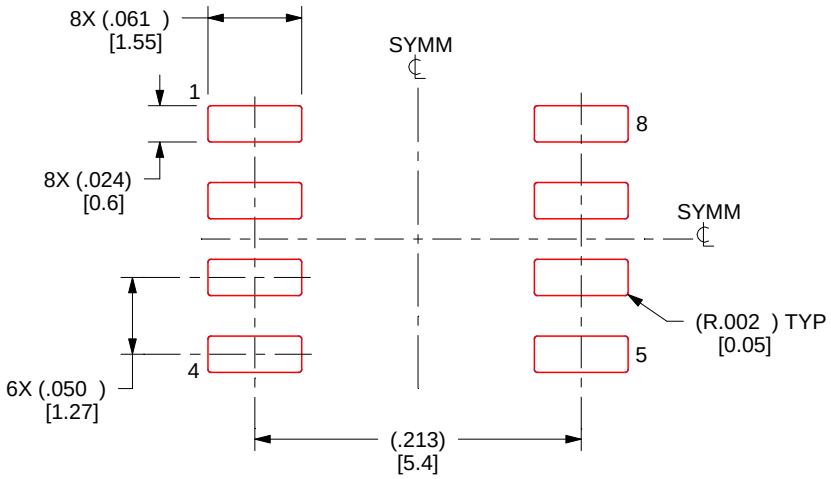
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

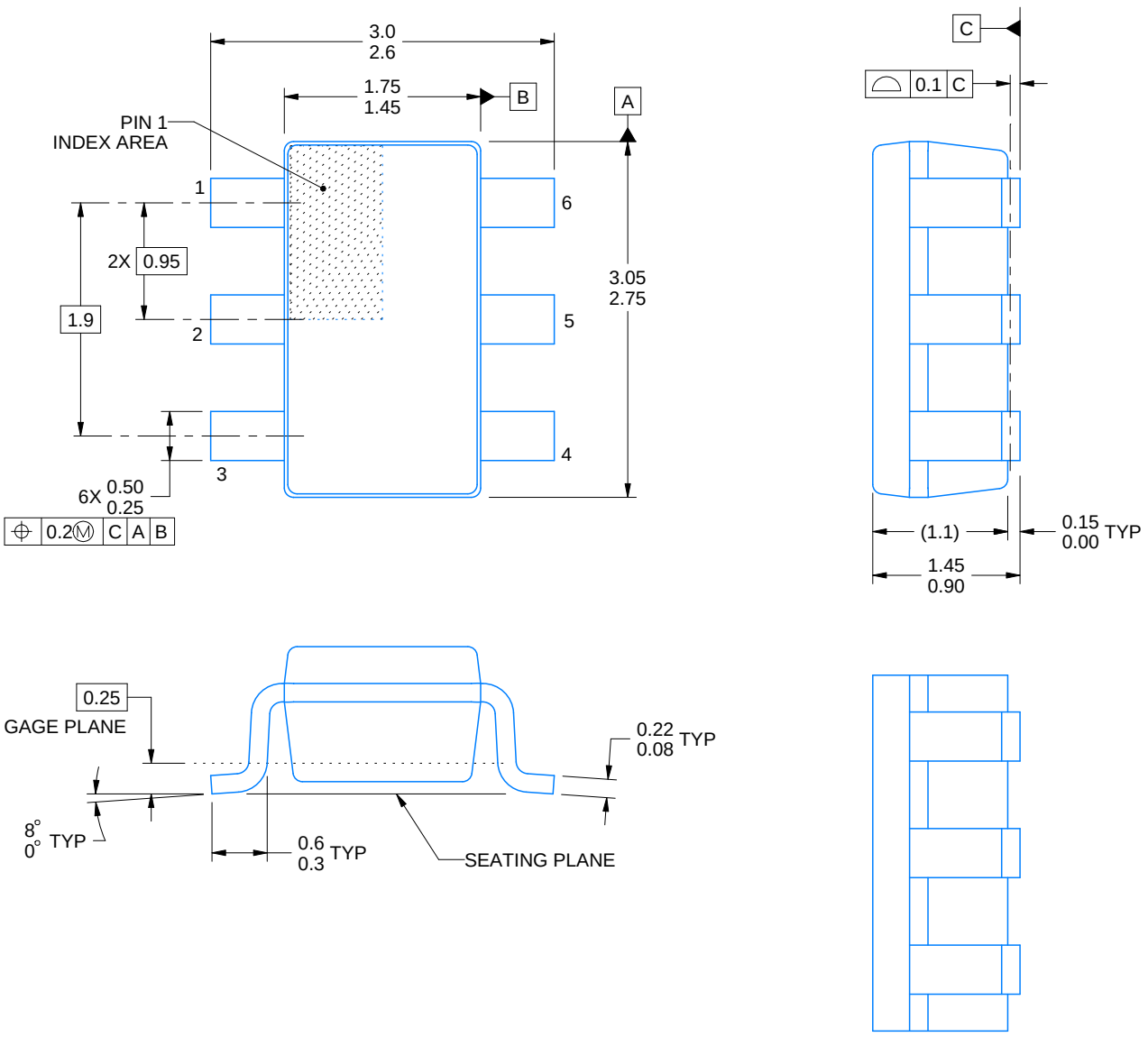
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

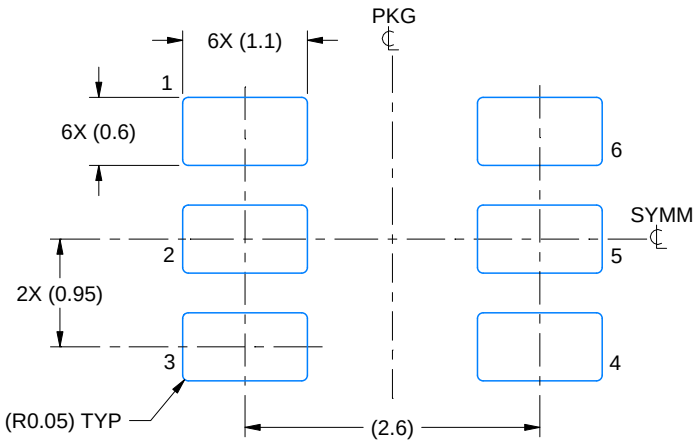


ALTERNATIVE PACKAGE SINGULATION VIEW

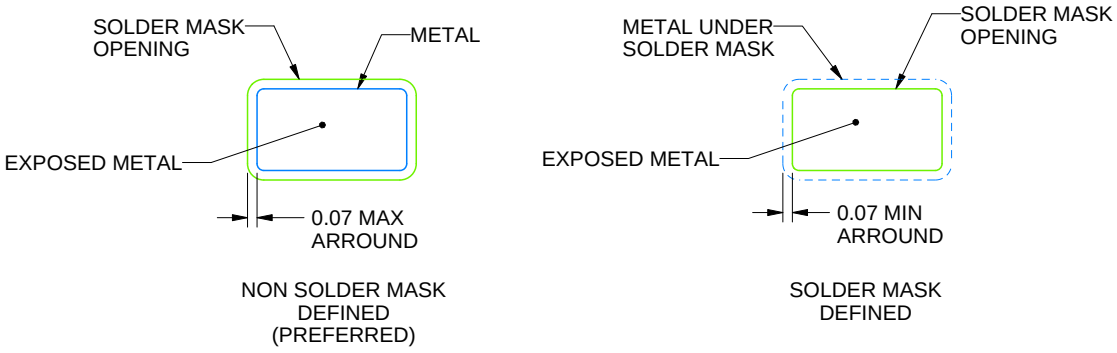
4214840/F 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

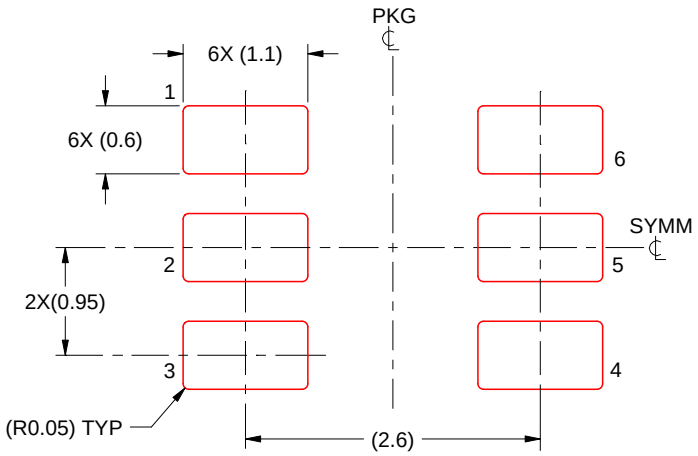


SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



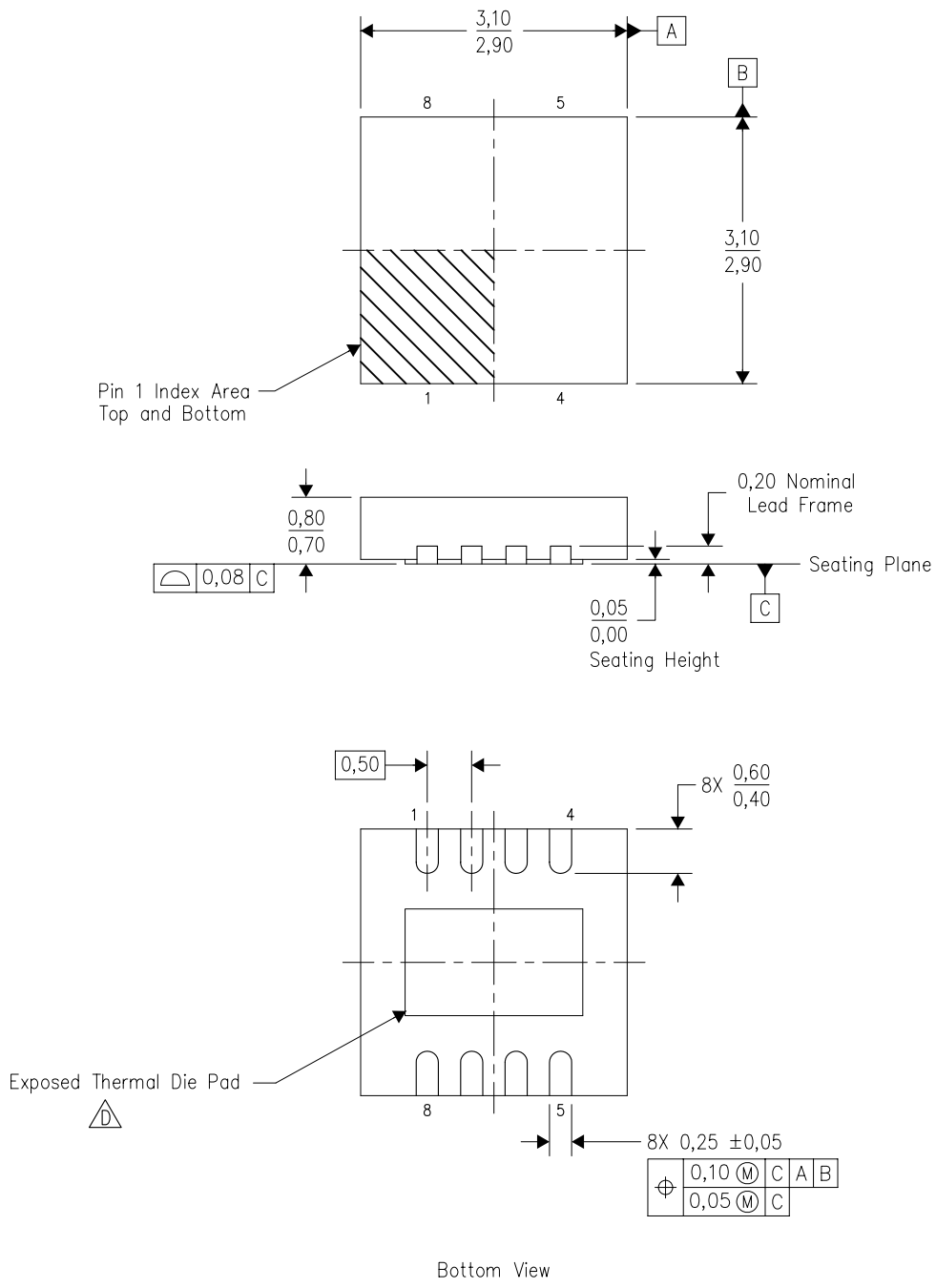
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



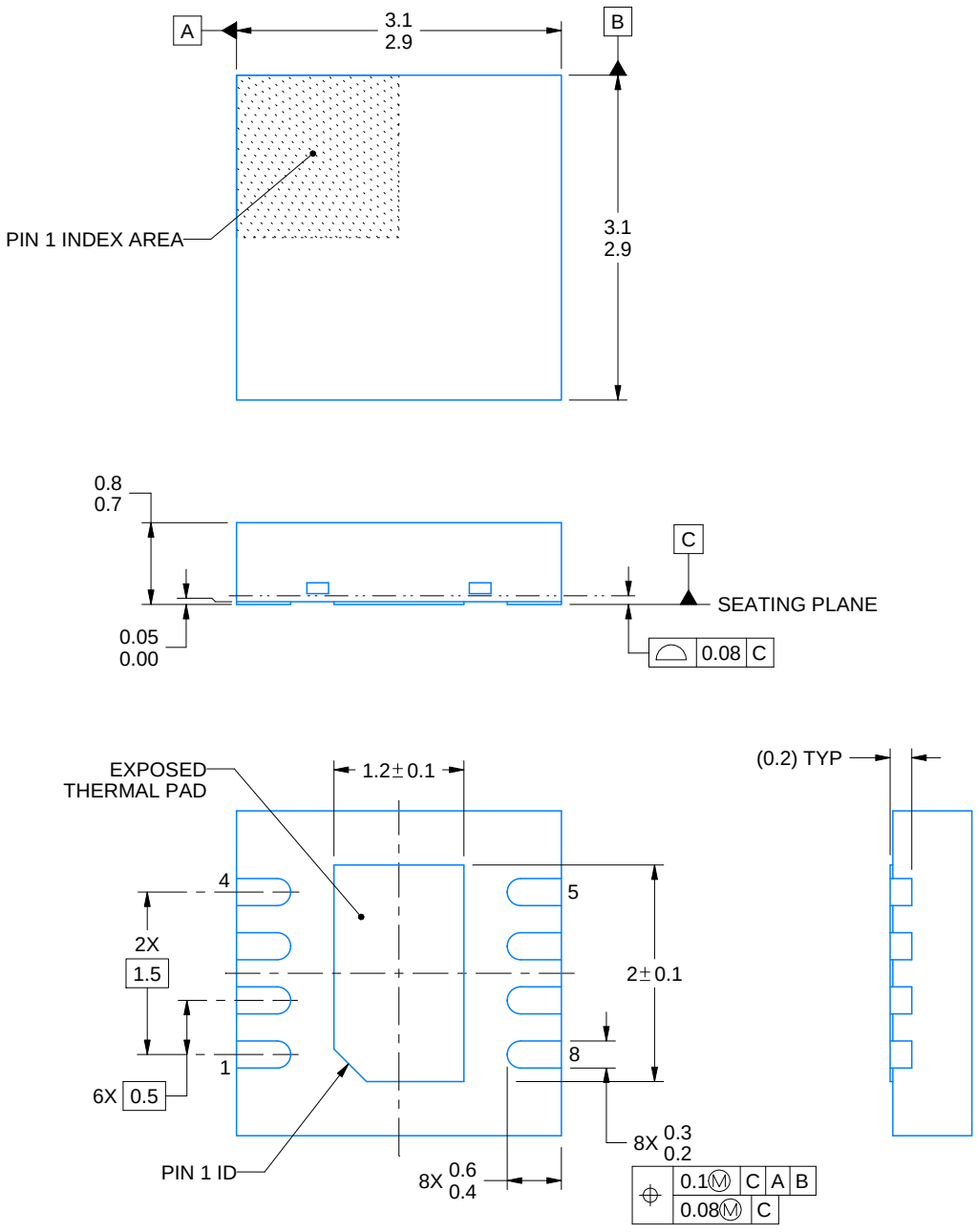
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

PACKAGE OUTLINE

DRG0008A

WSON - 0.8 mm max height

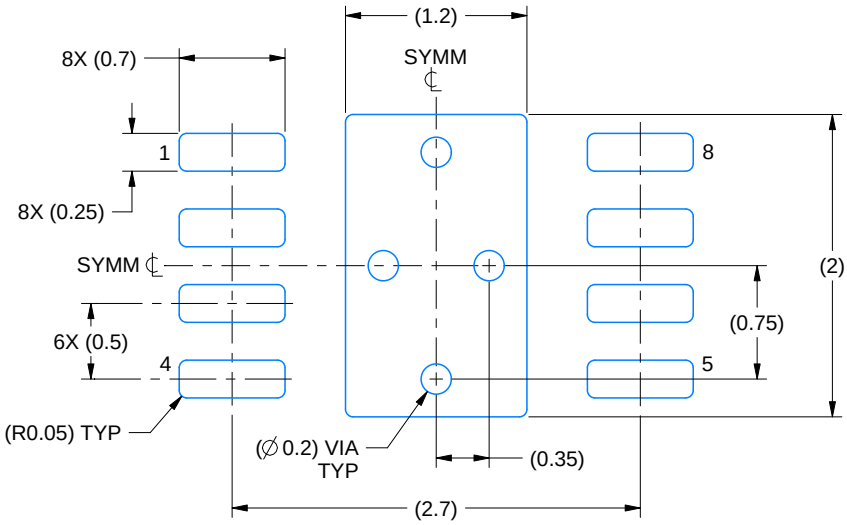
PLASTIC SMALL OUTLINE - NO LEAD



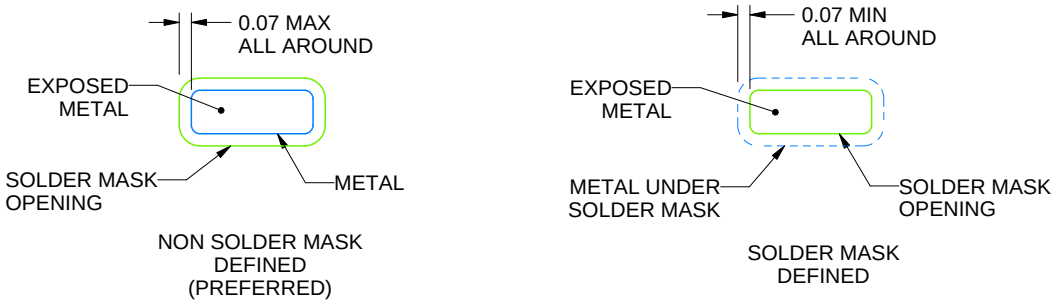
4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

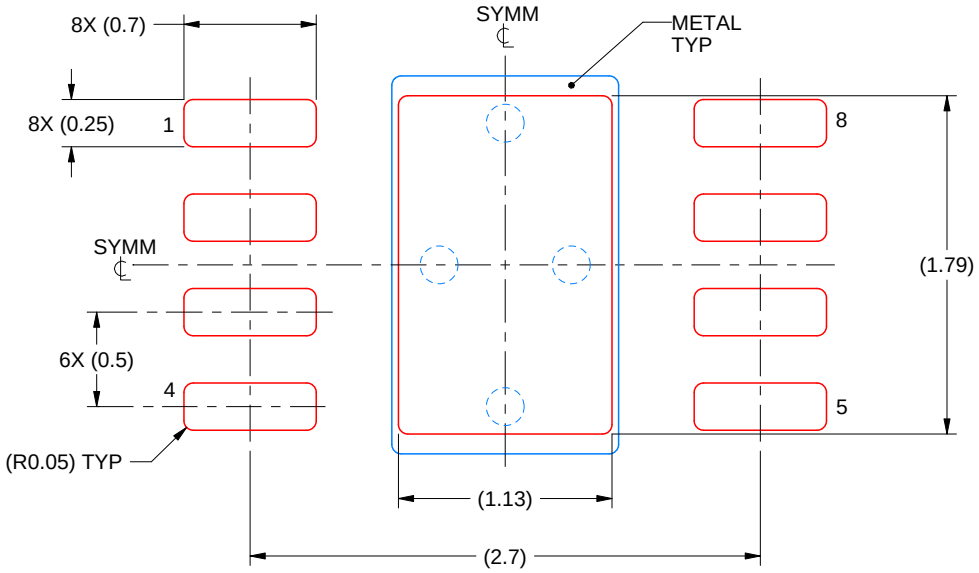


SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

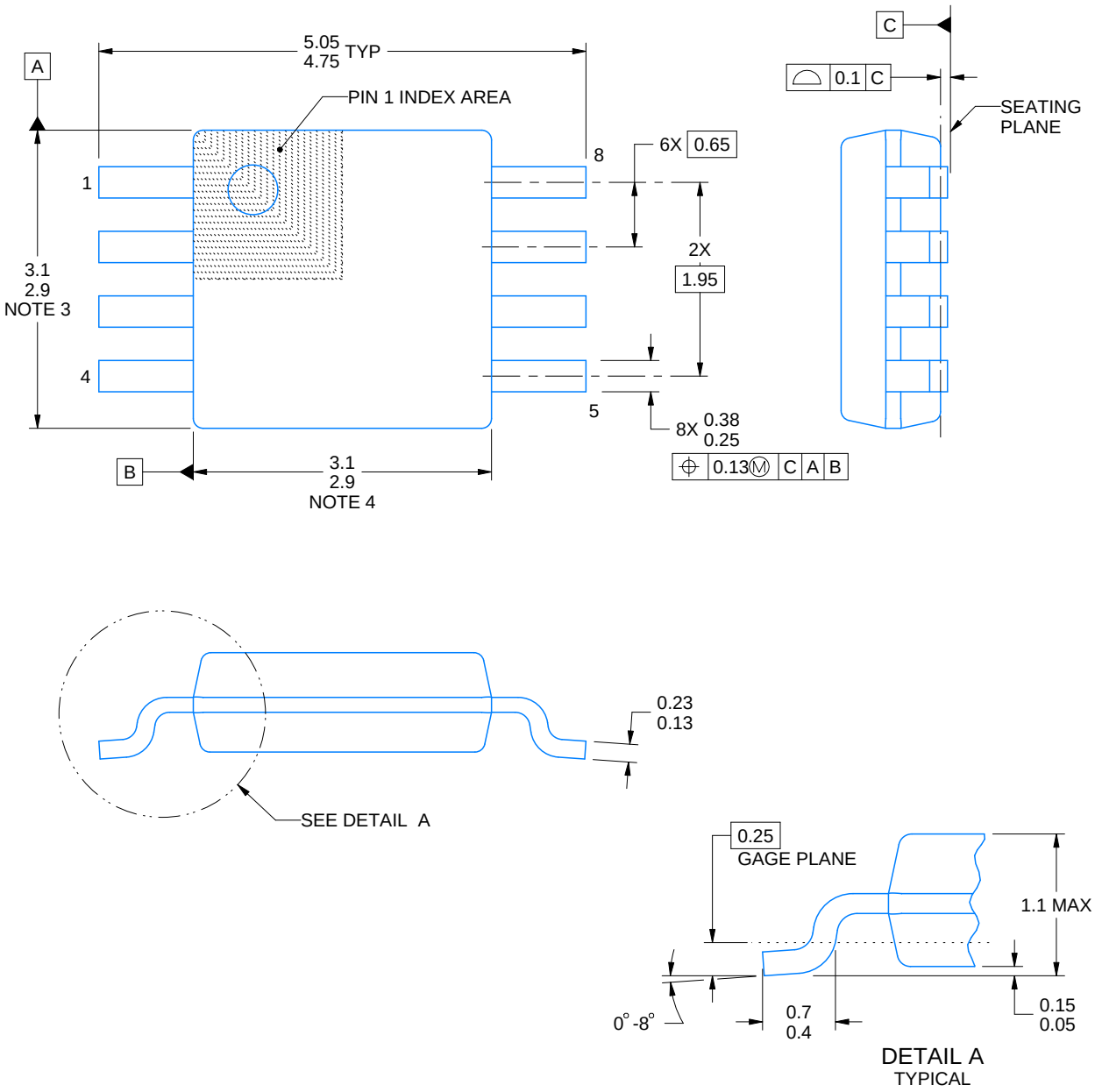
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

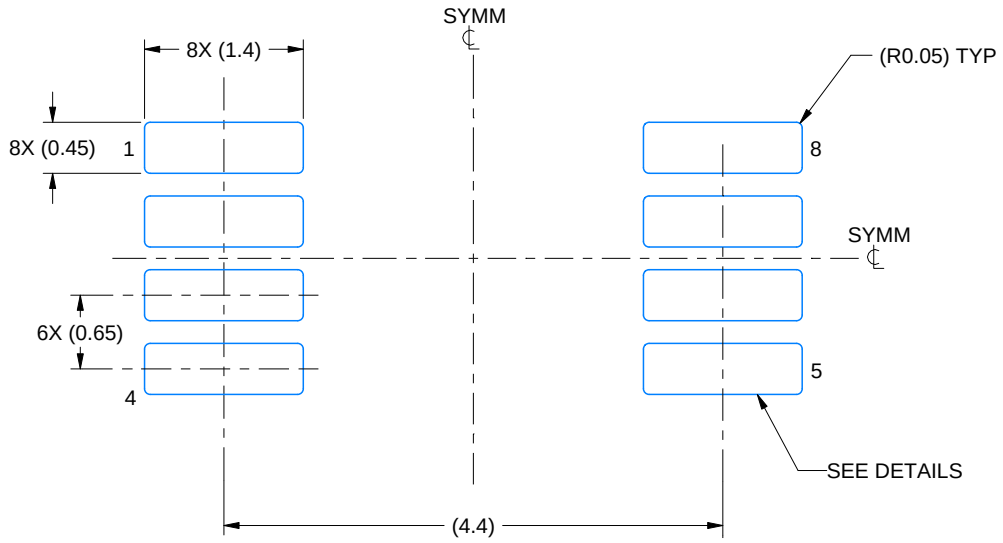
SMALL OUTLINE PACKAGE



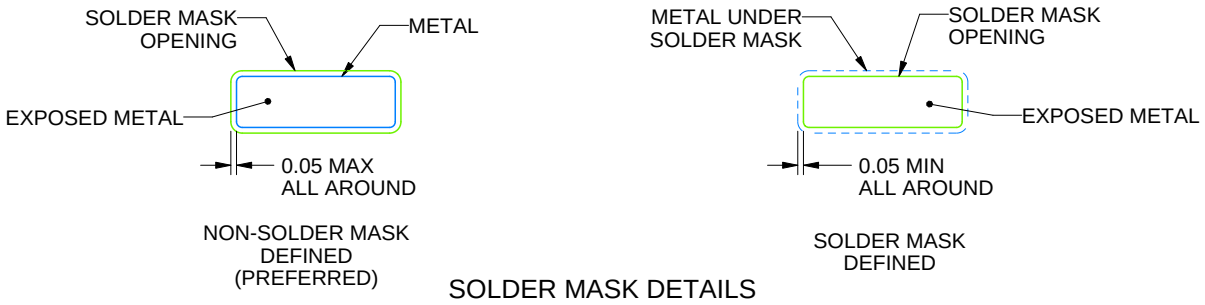
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

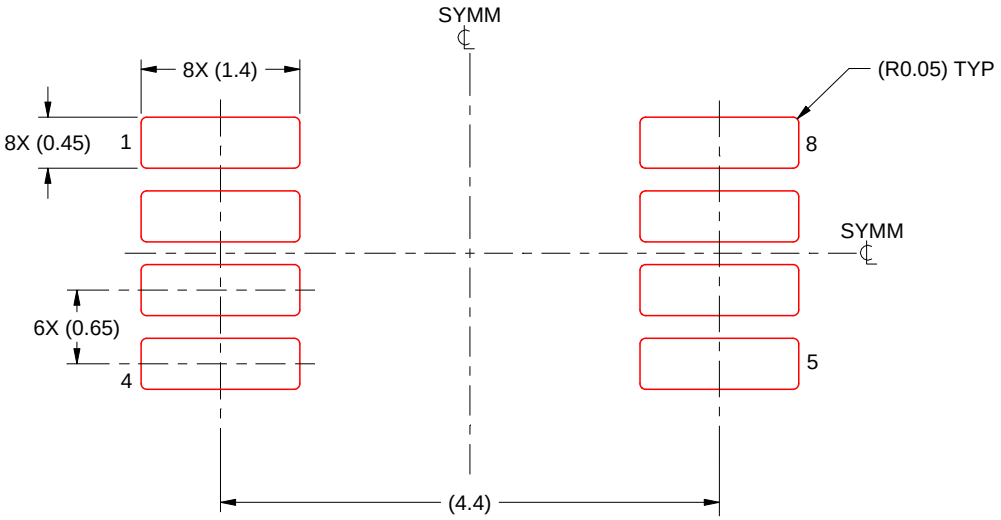


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

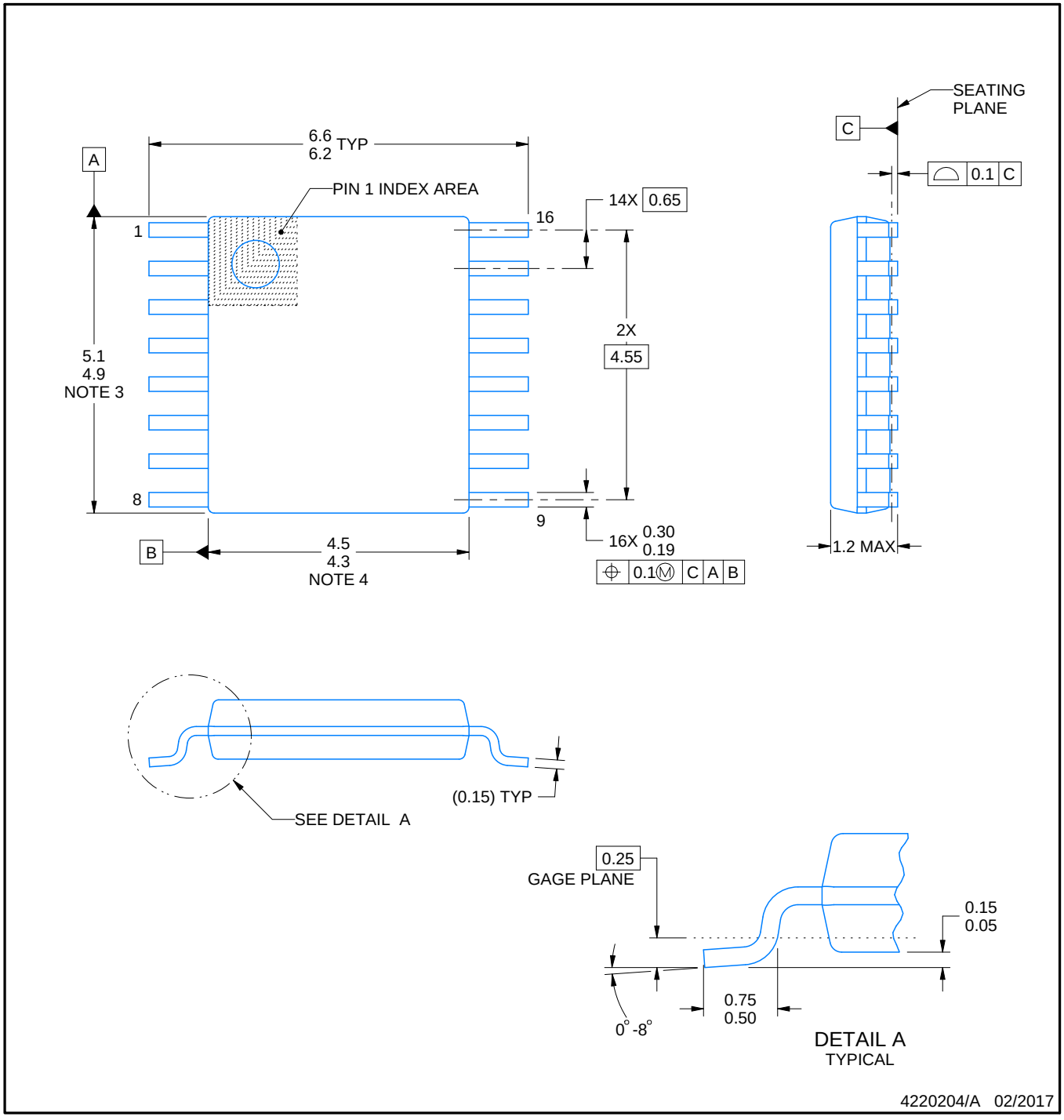
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

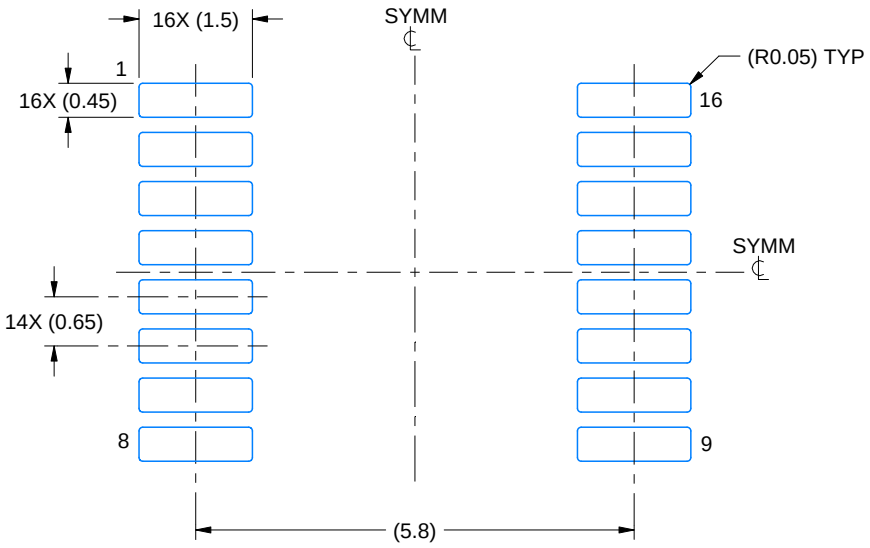
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

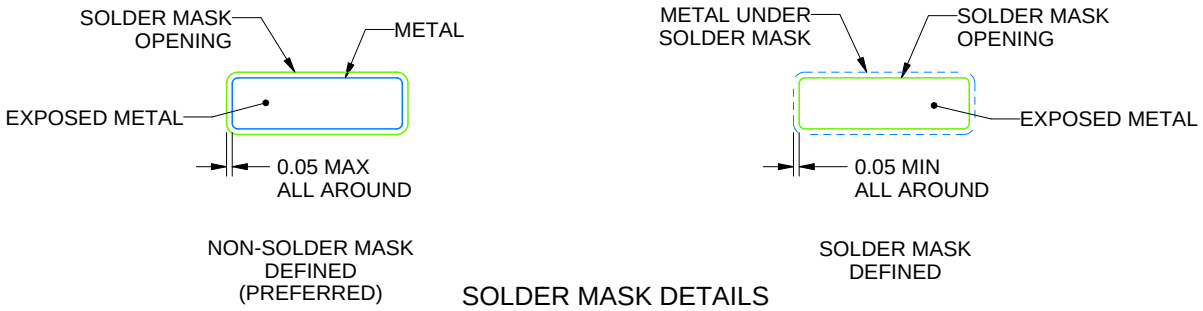


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

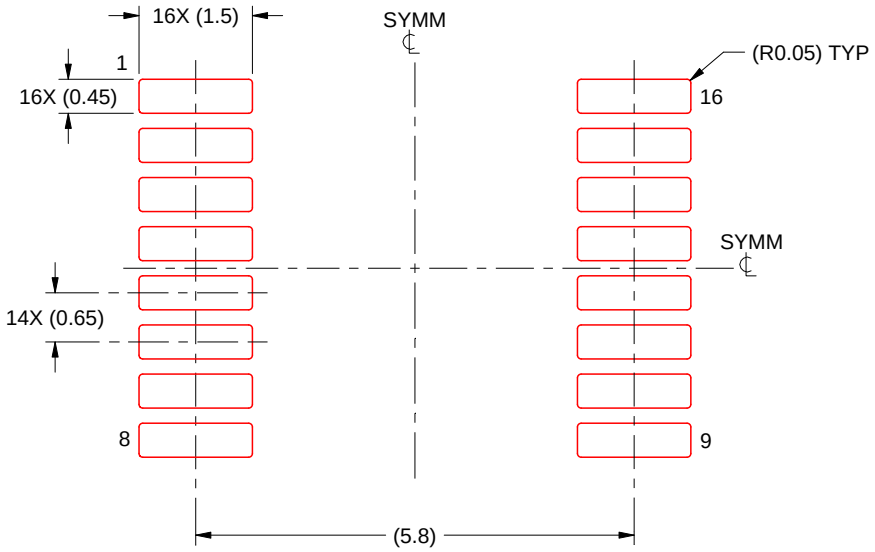


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

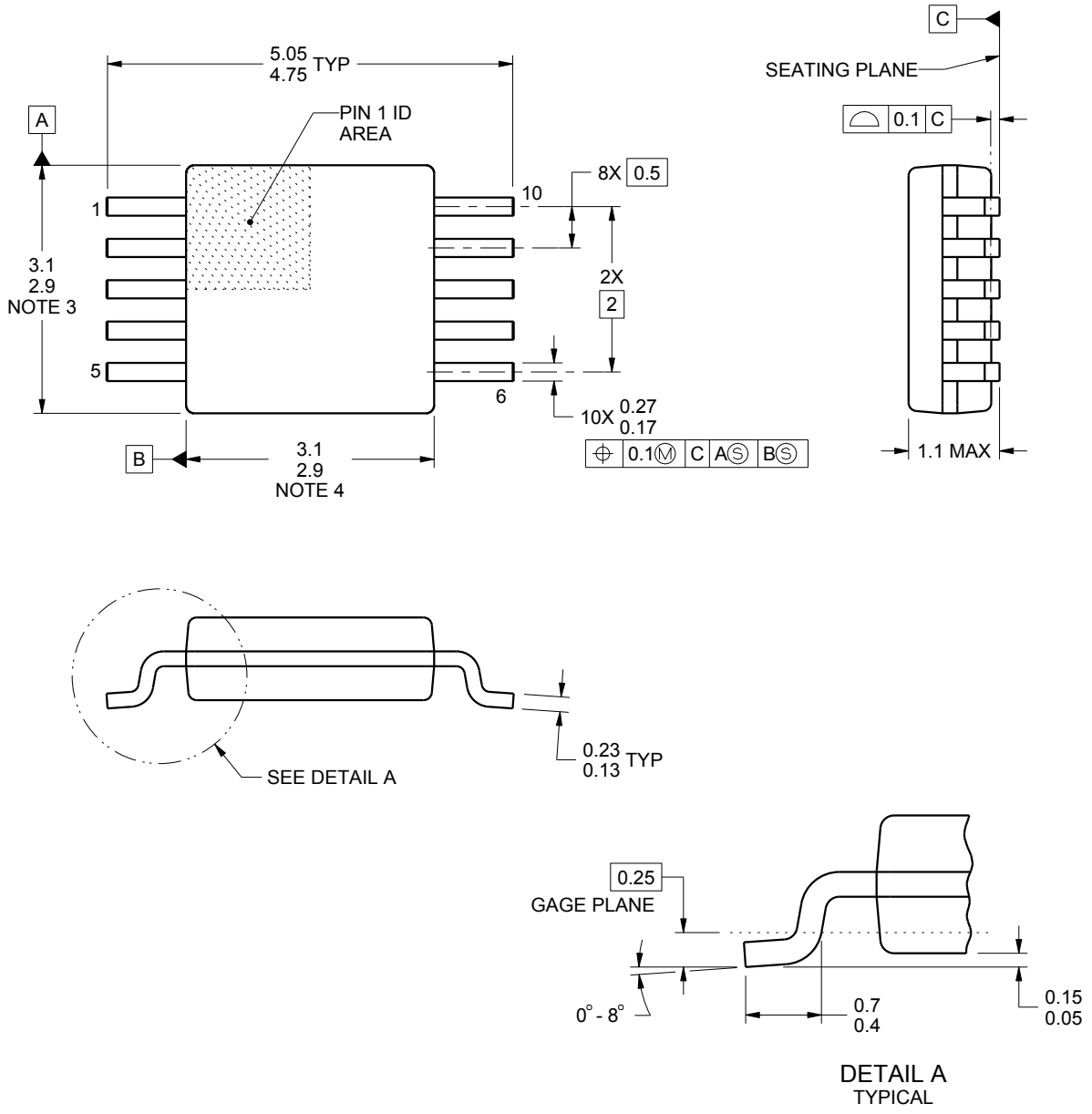
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

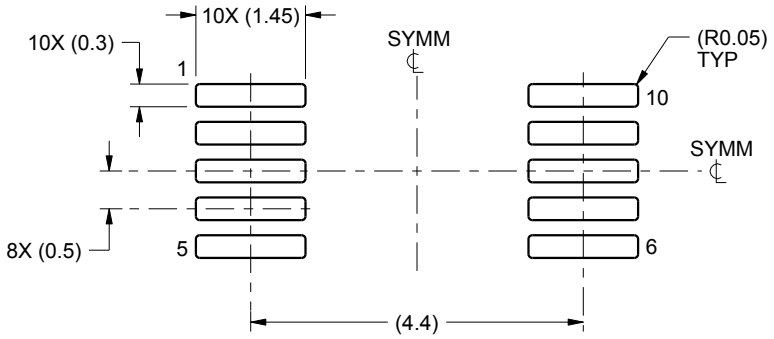
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

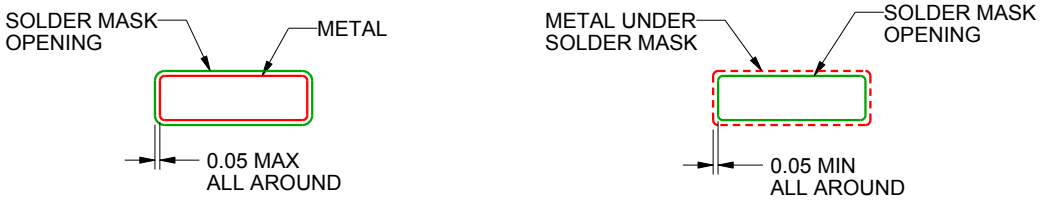


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

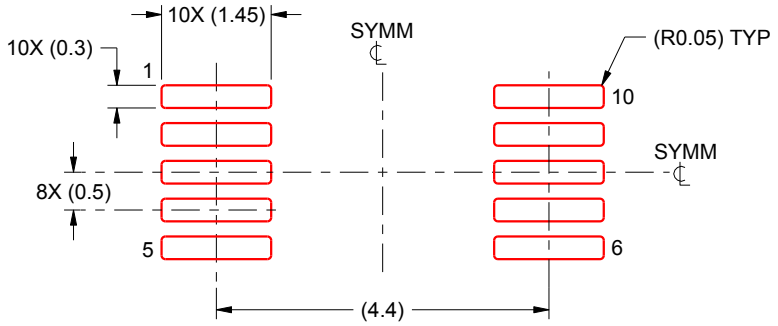


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265