TEXAS INSTRUMENTS
OPA363, OPA2363, OPA364, OPA2364, OPA4364
JAJS006F – SEPTEMBER 2002 – REVISED JUNE 2018

# OPAx363、OPAx364 1.8V、7MHz、90dB CMRR、単一電源、レール·ツー·レール入出力オペアンプ

## 1 特長

- 1.8V動作
- *Micro*Sizeパッケージ
- 帯域幅: 7MHz
- CMRR: 90dB (標準値)
- スルーレート: 5V/µs
- 低オフセット: 500µV (最大値)
- 静止電流: 750µA/チャネル (最大値)
- シャットダウン・モード: チャネルごとに1µA未満

## 2 アプリケーション

- 信号コンディショニング
- データ収集
- プロセス制御
- アクティブ・フィルタ
- 試験用機器

## 3 概要

OPA363およびOPA364ファミリは高性能のCMOSオペアンプで、非常に低い電圧の単一電源による動作に最適化されています。これらの小型低コスト・アンプは、1.8V (±0.9V)～5.5V (±2.75V)の単一電源で動作するよう設計されています。

アプリケーションとして、バッテリ駆動システムでのセンサ・アンプや信号コンディショニングが挙げられます。

OPA363およびOPA364ファミリは、従来の相補入力段で見られるようなクロスオーバーなしに、優れたCMRRを実現しています。この特長により、アナログ/デジタル(A/D)コンバータの駆動において、微分直線性やTHDの劣化なしに優れた性能を発揮できます。入力同相範囲には、負と正の電源の両方が含まれています。出力電圧のスイングは、レールから10mVの範囲内です。

OPA363ファミリにはシャットダウン・モードが搭載されています。ロジック制御により、アンプを通常の動作からスタンバイに切り替えることができ、この状態での消費電流は1µA未満です。

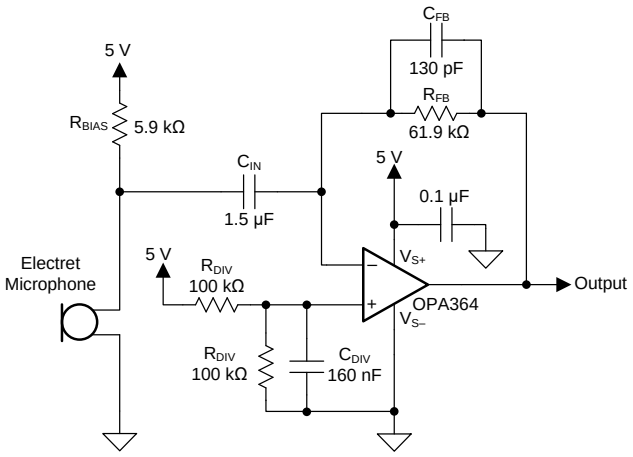
1チャネルのバージョンは、*Micro*Size 5ピンSOT-23 (シャットダウン用には6ピンSOT-23)および8ピンSOICで供給されます。2チャネルのバージョンは、8ピンVSSOP、10ピンVSSOP、16ピンUQFN、8ピンSOICパッケージで供給されます。4チャネルのバージョンは、14ピンTSSOPおよび14ピンSOICパッケージで供給されます。どのバージョンも、–40℃～+125℃での動作が規定されています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| OPA363 | SOT-23 (6) | 2.60mm×1.60mm |
| | SOIC (8) | 4.90mm×3.91mm |
| OPA364 | SOT-23 (5) | 2.60mm×1.60mm |
| | SOIC (8) | 4.90mm×3.91mm |
| OPA2363 | VSSOP (10) | 3.00mm×3.00mm |
| | UQFN (16) | 2.60mm×1.80mm |
| OPA2364 | SOIC (8) | 4.90mm×3.91mm |
| | VSSOP (8) | 3.00mm×3.00mm |
| OPA4364 | SOIC (14) | 8.65mm×3.91mm |
| | TSSOP (14) | 5.00mm×4.40mm |

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

**単一電源のマイク用プリアンプ**



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Revision E (January 2018)** から **Revision F** に変更 **Page**

- 「*製品情報*」表でOPA363 SOT-23 (5)をSOT-23 (6)に 変更 ... 1
- 「*製品情報*」表にOPA363 SOIC (8)パッケージを 追加 ... 1
- 「*製品情報*」表でOPA364 SOT-23 (6)をSOT-23 (5)に 変更 ... 1
- 「*製品情報*」表からOPA2364 VSSOP (10)およびUQFN (16)パッケージを 削除 ... 1
- 「*製品情報*」表からOPA2363 SOIC (8)およびVSSOP (8)パッケージを 削除 ... 1

**Revision D (September 2016)** から **Revision E** に変更 **Page**

- 「*製品情報*」表で、OPA36xおよびOPA236xの型番をOPA364およびOPA2363に 変更 ... 1
- OPA2364デバイスを「*製品情報*」表に 追加 ... 1
- Corrected formatting of pinout drawings in *Pin Configuration and Functions* section ... 4
- Corrected formatting of pinout tables in *Pin Configuration and Functions* section ... 4
- Added a minimum value of 0 V to supply voltage parameter in *Absolute Maximum Ratings* table ... 8
- Added "([V+] – [V–])" to supply voltage parameter in *Absolute Maximum Ratings* table ... 8
- Deleted operating temperature range from *Absolute Maximum Ratings* table ... 8
- Added the word "temperature" to junction and storage temperature ranges in *Absolute Maximum Ratings* table ... 8
- Added "([V+] – [V–])" to supply voltage parameter in *Recommended Operating Conditions* table ... 8
- Changed output voltage swing parameter units from V to mV ... 11
- Deleted temperature range section of *Electrical Characteristics* table ... 11
- Changed PSRR test condition from $V_{CM}$ = 0 to $V_{CM}$ = (V–) in *Electrical Characteristics* table ... 11
- Deleted *Buffered Reference Voltage* subsection in *Application Information* section ... 20
- Changed Figure 33 ... 26
- Added Figure 34 ... 27

- 変更 データシート全体で"IC"を"デバイス"に ..... 28

**Revision C (May 2013) から Revision D に変更** **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ..... 1
- データシートの末尾にあるPOAを参照し、「*パッケージおよび注文情報*」セクションを 削除..... 1

**Revision B (February 2003) から Revision C に変更** **Page**

- データシートを現行フォーマットに変換 ..... 1
- RSVパッケージ(UQFN-16)をデータシートに 追加..... 1
- Added text to last bullet of *Layout Guidelines* section..... 26

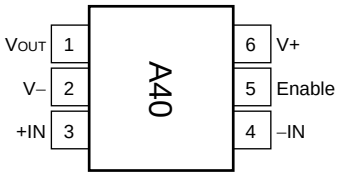
# 5 Device Comparison Table

## 5.1 Device Comparison Table

| | OPA363 | OPA364 | OPA2363 | OPA2364 | OPA4364 |
|---|---|---|---|---|---|
| SOT-23-5 | | X | | | |
| SOT-23-6 (shutdown) | X | | | | |
| MSOP-8 | | | | X | |
| MSOP-10 | | | X | | |
| SO-8 | X | X | | X | |
| TSSOP-14 | | | | | X |
| SO-14 | | | | | X |
| UQFN-16 | | | X | | |

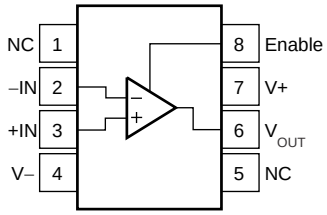
# 6 Pin Configuration and Functions

**OPA363: DBV Package**
**6-Pin SOT-23**
**Top View**




(1) Orient according to marking.

**OPA363: D Package**
**8-Pin SOIC**
**Top View**

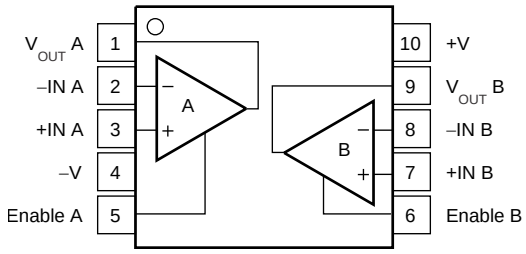



NC- no internal connection

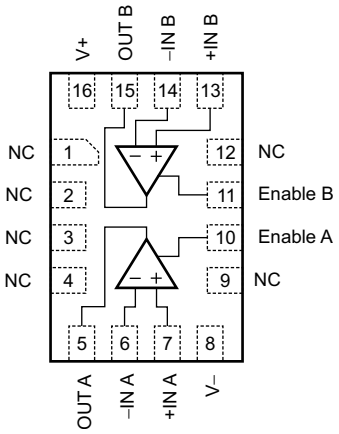
**Pin Functions: OPA363**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC | SOT-23 | | |
| Enable | 8 | 5 | I | Enable |
| –IN | 2 | 4 | I | Negative (inverting) input |
| +IN | 3 | 3 | I | Positive (noninverting) input |
| NC | 1, 5 | — | — | No internal connection (can be left floating) |
| $V_{OUT}$ | 6 | 1 | O | Output |
| V– | 4 | 2 | — | Negative (lowest) power supply |
| V+ | 7 | 6 | — | Positive (highest) power supply |

**OPA2363: DGS Package**
**10-Pin MSOP**
**Top View**




**OPA2363: RSV Package**
**16-Pin UQFN**
**Top View**

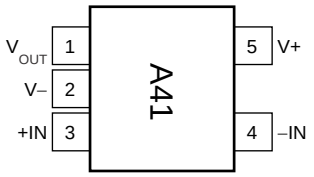



NC- no internal connection

## Pin Functions: OPA2363

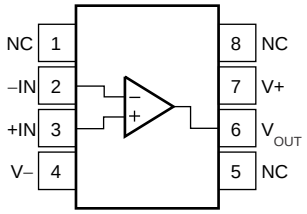
| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | MSOP | UQFN | | |
| Enable A | 5 | 10 | I | Enable A amplifier |
| Enable B | 6 | 11 | I | Enable B amplifier |
| –IN A | 2 | 6 | I | Inverting input, channel A |
| +IN A | 3 | 7 | I | Noninverting input, channel A |
| –IN B | 8 | 14 | I | Inverting input, channel B |
| +IN B | 7 | 13 | I | Noninverting input, channel B |
| NC | — | 1, 2, 3, 4, 9, 12 | — | No internal connection (can be left floating) |
| OUT A | — | 5 | O | Output, channel A |
| OUT B | — | 15 | O | Output, channel B |
| $V_{OUT}$ A | 1 | — | O | Output, channel A |
| $V_{OUT}$ B | 9 | — | O | Output, channel B |
| –V, V– | 4 | 8 | — | Negative (lowest) power supply |
| +V, V+ | 10 | 16 | — | Positive (highest) power supply |

**OPA364: DBV Package**
**5-Pin SOT-23**
**Top View**




(1) Orient according to marking.

**OPA364: D Package**
**8-Pin SOIC**
**Top View**

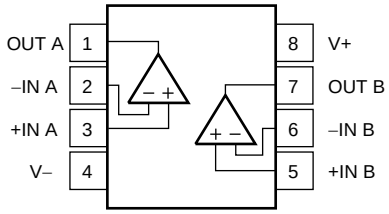



NC - no internal connection

## Pin Functions: OPA364

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC | SOT-23 | | |
| –IN | 2 | 4 | I | Negative (inverting) input |
| +IN | 3 | 3 | I | Positive (noninverting) input |
| NC | 1, 5, 8 | — | — | No internal connection (can be left floating) |
| $V_{OUT}$ | 6 | 1 | O | Output |
| V– | 4 | 2 | — | Negative (lowest) power supply |
| V+ | 7 | 5 | — | Positive (highest) power supply |

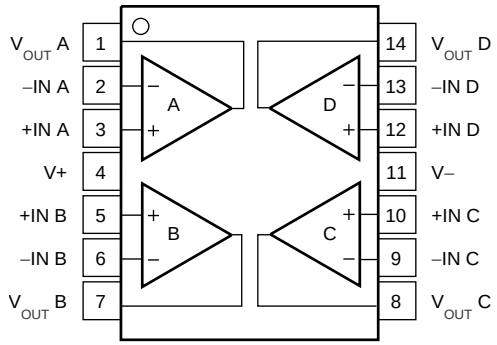
**OPA2364: DGK and D Packages**
**8-Pin MSOP and SOIC**
**Top View**




## Pin Functions: OPA2364

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN B | 5 | I | Noninverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V– | 4 | — | Negative (lowest) power supply |
| V+ | 8 | — | Positive (highest) power supply |

**OPA4364: D and PW Packages**
**14-Pin SOIC and TSSOP**
**Top View**




NC- no internal connection.

## Pin Functions: OPA4364

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN B | 5 | I | Noninverting input, channel B |
| –IN C | 9 | I | Inverting input, channel C |
| +IN C | 10 | I | Noninverting input, channel C |
| –IN D | 13 | I | Inverting input, channel D |
| +IN D | 12 | I | Noninverting input, channel D |
| $V_{OUT}$ A | 1 | O | Output, channel A |
| $V_{OUT}$ B | 7 | O | Output, channel B |
| $V_{OUT}$ C | 8 | O | Output, channel C |
| $V_{OUT}$ D | 14 | O | Output, channel D |
| V– | 11 | — | Negative (lowest) power supply |
| V+ | 4 | — | Positive (highest) power supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply ([V+] – [V–]) | 0 | 5.5 | V |
| | Signal input pin(2) | −0.5 | (V+) + 0.5 | |
| Current | Signal input pin(2) | –10 | 10 | mA |
| | Output short-circuit(3) | Continuous | | mA |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| | Supply voltage ([V+] – [V–]) | 1.8 | | 5.5 | V |
| $T_A$ | Operating temperature | –40 | | 125 | °C |

## 7.4 Thermal Information: OPA363

| THERMAL METRIC(1) | | OPA363 DBV (SOT-23) 5 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 211.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 137 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 39.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 20.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 38.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Thermal Information: OPA364

| THERMAL METRIC(1) | | OPA364 DBV (SOT-23) 6 PINS | OPA364 D (SOIC) 8 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 182.7 | 125.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 130.7 | 73.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 34.1 | 65.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 24.8 | 25.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 33.5 | 65.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.6 Thermal Information: OPA2363

| THERMAL METRIC(1) | | OPA2363 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | DGS (VSSOP) | UQFN (RSV) | |
| | | 8 PINS | 8 PINS | 10 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 125.3 | 171.8 | 166.4 | 112.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 73.7 | 63.2 | 55.9 | 44 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 65.7 | 92.4 | 86.6 | 41.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 25.4 | 9.5 | 6.8 | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.2 | 91 | 85.2 | 41.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.7 Thermal Information: OPA2364

| THERMAL METRIC(1) | | OPA2364 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | DGS (VSSOP) | UQFN (RSV) | |
| | | 8 PINS | 8 PINS | 10 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 125.3 | 171.8 | 166.4 | 112.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 73.7 | 63.2 | 55.9 | 44 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 65.7 | 92.4 | 86.6 | 41.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 25.4 | 9.5 | 6.8 | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.2 | 91 | 85.2 | 41.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.8 Thermal Information: OPA4364

| THERMAL METRIC(1) | | OPA4364 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 82.6 | 107.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 41.1 | 31.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 37.1 | 50.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.4 | 1.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 36.8 | 49.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.9 Electrical Characteristics

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{OUT}$ = $V_S$ / 2, and $V_{CM}$ = $V_S$ / 2, $V_S$ = 1.8 V to 5.5 V, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 5 V (OPA363I, OPA364I) | | | | 500 | µV |
| | | OPA2363I, OPA2364I | | | | 900 | µV |
| | | OPA363AI, OPA364AI, OPA2363AI, OPA2364AI, OPA4364AI | | | 1 | 2.5 | mV |
| $dV_{OS}/dT$ | Drift | $T_A$ = –40°C to +125°C | | | 3 | | µV/°C |
| PSRR | Input offset voltage vs power supply | $V_S$ = 1.8 V to 5.5 V<br>$V_{CM}$ = (V–)<br>$T_A$ = –40°C to +125°C | | | 80 | 330 | µV/V |
| | Channel separation, DC | | | | 1 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | $T_A$ = 25°C | | | ±1 | ±10 | pA |
| | | $T_A$ = –40°C to +125°C | | See *Typical Characteristics* | | | |
| $I_{OS}$ | Input offset current | | | | ±1 | ±10 | pA |
| **NOISE** | | | | | | | |
| $e_n$ | Input voltage noise, | f = 0.1 Hz to 10 Hz | | | 10 | | $µV_{PP}$ |
| $e_n$ | Input voltage noise density | f = 10 kHz | | | 17 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input current noise density | f = 10 kHz | | | 0.6 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | (V–) – 0.1 V < $V_{CM}$ < (V+) + 0.1 V<br>$T_A$ = –40°C to +125°C | | 74 | 90 | | dB |
| **INPUT CAPACITANCE** | | | | | | | |
| | Differential | | | | 2 | | pF |
| | Common-mode | | | | 3 | | pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $R_L$ = 10 kΩ<br>100 mV < $V_O$ < (V+) – 100 mV | $T_A$ = 25°C | 94 | 100 | | dB |
| | | | $T_A$ = 25°C (OPA4364) | 90 | | | dB |
| | | $R_L$ = 10 kΩ<br>100 mV < $V_O$ < (V+) – 100 mV | $V_S$ = 1.8 V to 5.5 V<br>$T_A$ = –40°C to +125°C | 86 | | | dB |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | $C_L$ = 100 pF | | | 7 | | MHz |
| SR | Slew rate | $C_L$ = 100 pF, G = 1 | | | 5 | | V/µs |
| $t_S$ | Settling time | 0.1%, $C_L$ = 100 pF, $V_S$ = 5 V, 4-V step, G = 1 | | | 1 | | µs |
| | | 0.01%, $C_L$ = 100 pF, $V_S$ = 5 V, 4-V step, G = 1 | | | 1.5 | | µs |
| | Overload recovery time | $C_L$ = 100 pF<br>$V_{IN}$ × Gain > $V_S$ | | | 0.8 | | µs |
| THD+N | Total harmonic distortion + noise | $C_L$ = 100 pF, $V_S$ = 5 V, G = 1, f = 20 Hz to 20 kHz | | | 0.002% | | |
| **OUTPUT** | | | | | | | |
| | Voltage output swing | $R_L$ = 10 kΩ, $T_A$ = 25°C | | | 10 | 20 | mV |
| | | $R_L$ = 10 kΩ<br>$T_A$ = –40°C to +125°C | | | | 20 | mV |
| $I_{SC}$ | Short-circuit current | | | See *Typical Characteristics* | | | |
| $C_{LOAD}$ | Capacitive load drive | | | See *Typical Characteristics* | | | |
| **SHUTDOWN (OPA363)** | | | | | | | |
| $t_{OFF}$ | Turnoff time | | | | 1 | | µs |
| $t_{ON}$ | Turnon time (1) | | | | 20 | | µs |
| $V_L$ | Logic low threshold | Shutdown | | | | (V–) + 0.8 | V |
| $V_H$ | Logic high threshold | Amplifier is active | | 0.75 (V+) | | 5.5 | V |
| $I_{Q(sd)}$ | Quiescent current at shutdown (per amplifier) | | | | | 0.9 | µA |

(1) Part is considered enabled when input offset voltage returns to specified range.

## Electrical Characteristics (continued)

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{OUT}$ = $V_S$ / 2, and $V_{CM}$ = $V_S$ / 2, $V_S$ = 1.8 V to 5.5 V, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage range | | 1.8 | | 5.5 | V |
| $I_Q$ | Quiescent current (per amplifier) | $V_S$ = 1.8 V<br>$T_A$ = –40°C to +125°C | | 650 | 750 | µA |
| | | $V_S$ = 3.6 V<br>$T_A$ = –40°C to +125°C | | 850 | 1000 | µA |
| | | $V_S$ = 5.5 V<br>$T_A$ = –40°C to +125°C | | 1.1 | 1.4 | mA |

## 7.10 Typical Characteristics

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{OUT}$ = $V_S$ / 2, and $V_{CM}$ = $V_S$ / 2, (unless otherwise noted)

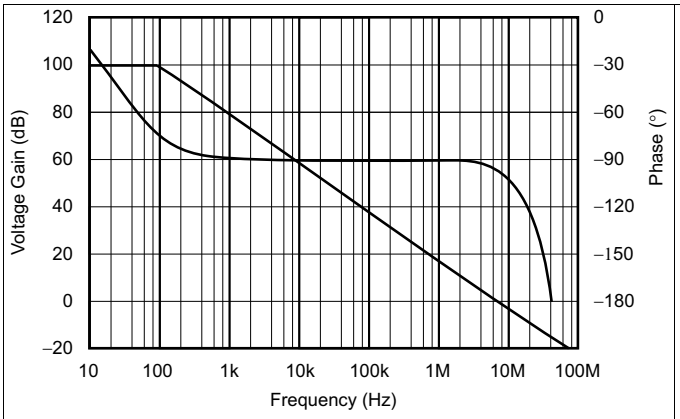



**Figure 1. Open-Loop Gain and Phase vs Frequency**

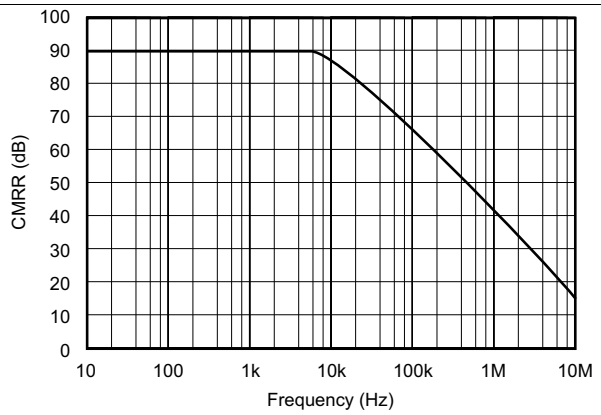



**Figure 2. Common-Mode Rejection Ratio vs Frequency**

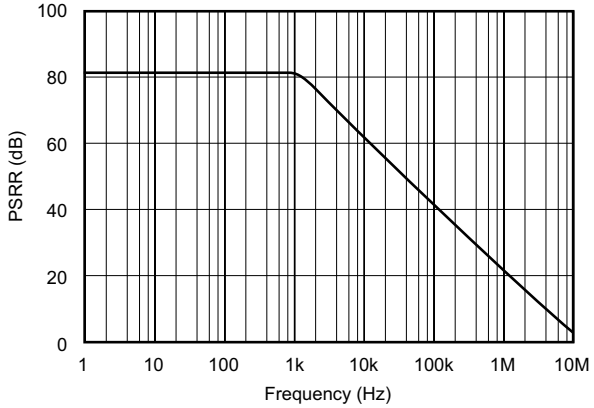



**Figure 3. Power-Supply Rejection Ratio vs Frequency**

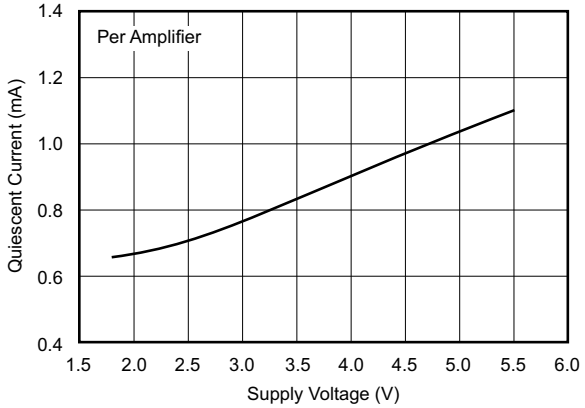



**Figure 4. Quiescent Current vs Supply Voltage**

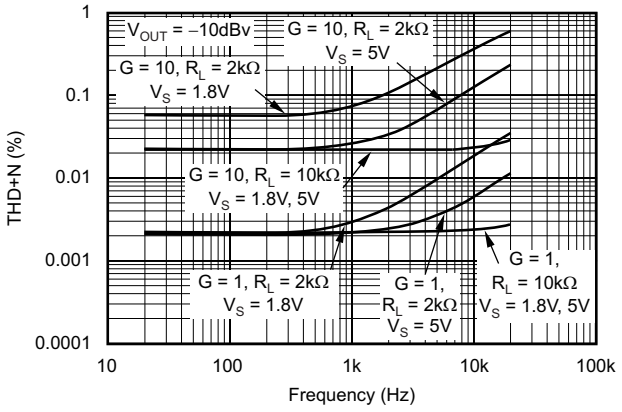



**Figure 5. Total Harmonic Distortion + Noise Ratio vs Frequency**

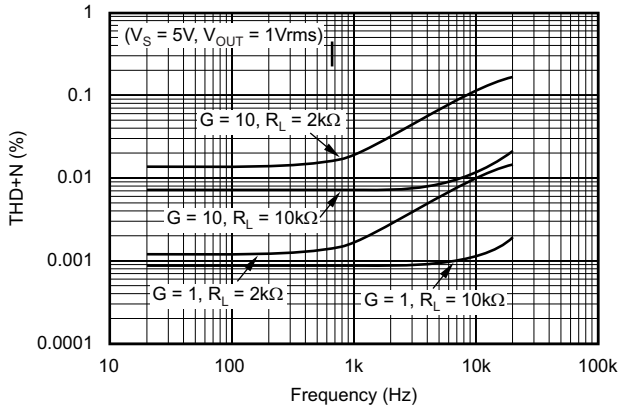



**Figure 6. Total Harmonic Distortion + Noise Ratio vs Frequency**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{OUT}$ = $V_S$ / 2, and $V_{CM}$ = $V_S$ / 2, (unless otherwise noted)

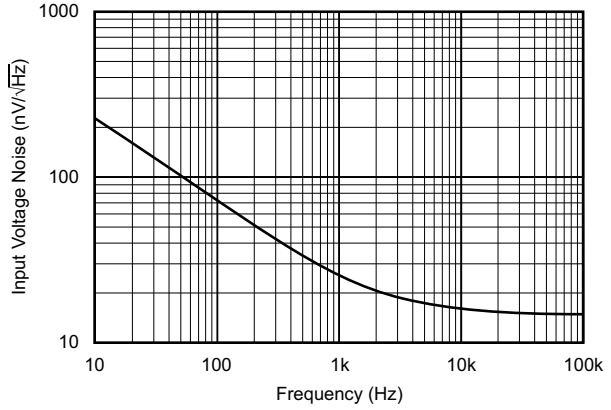



**Figure 7. Input Voltage Noise Spectral Density vs Frequency**

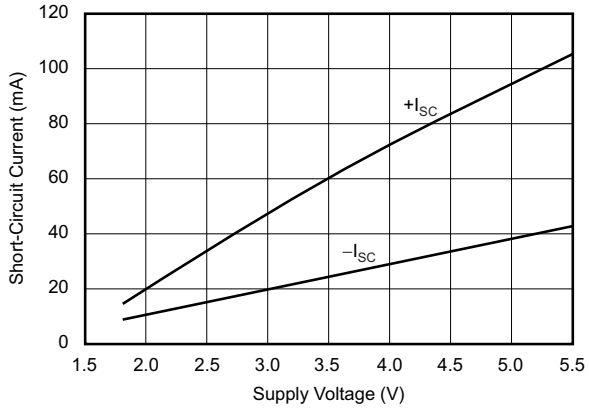



**Figure 8. Short-Circuit Current vs Supply Voltage**

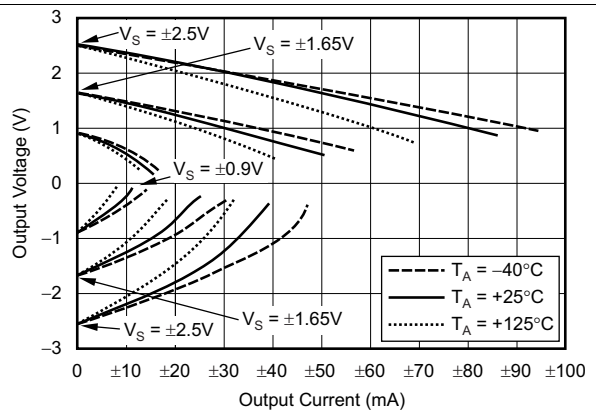



**Figure 9. Output Voltage Swing vs Output Current**

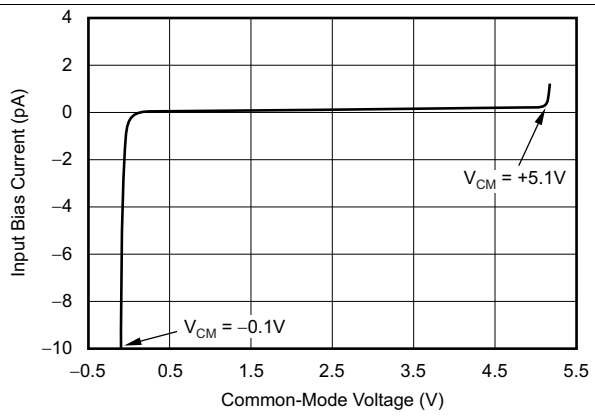



**Figure 10. Input Bias Current vs Input Common-Mode Voltage**

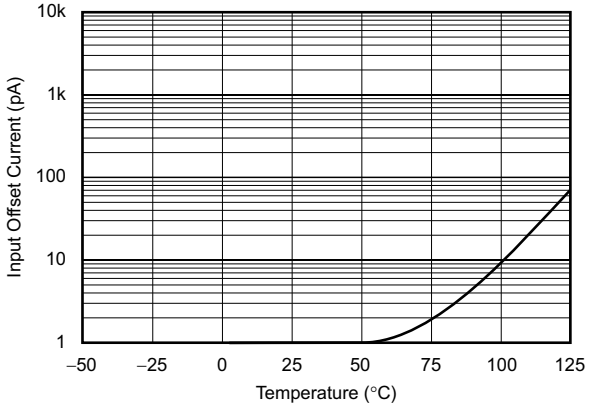



**Figure 11. Input Offset Current vs Temperature**

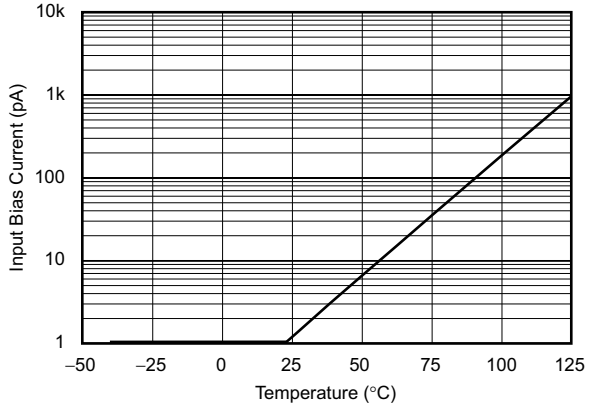



**Figure 12. Input Bias Current vs Temperature**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{OUT}$ = $V_S$ / 2, and $V_{CM}$ = $V_S$ / 2, (unless otherwise noted)

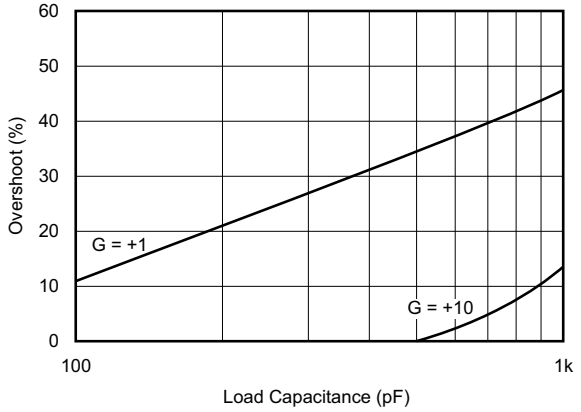



**Figure 13. Small-Signal Overshoot vs Load Capacitance**

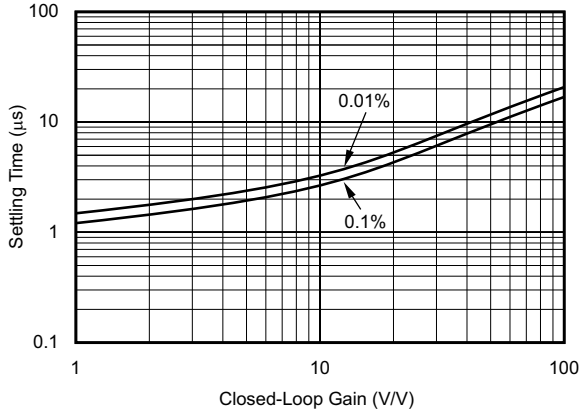



**Figure 14. Settling Time vs Closed-Loop Gain**

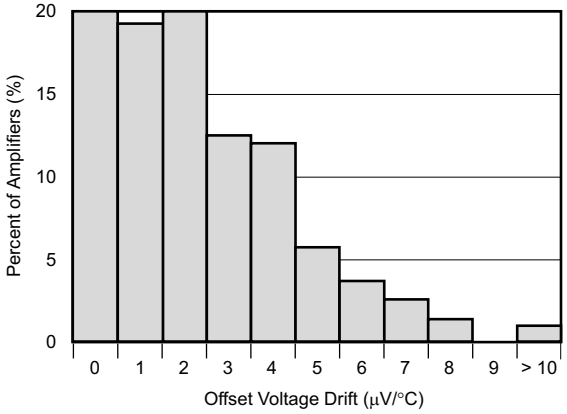



**Figure 15. Offset Drift Distribution**

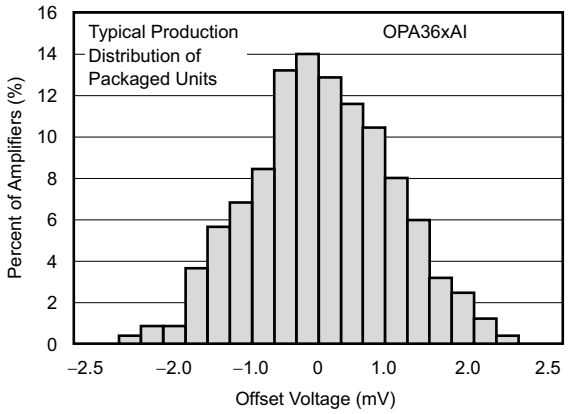



**Figure 16. Offset Voltage Production Distribution**

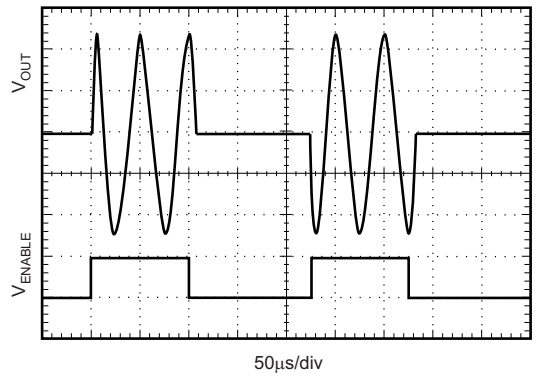



**Figure 17. Output Enable Characteristic ($V_S$ = 5 V, $V_{OUT}$ = 20-kHz Sinusoid)**

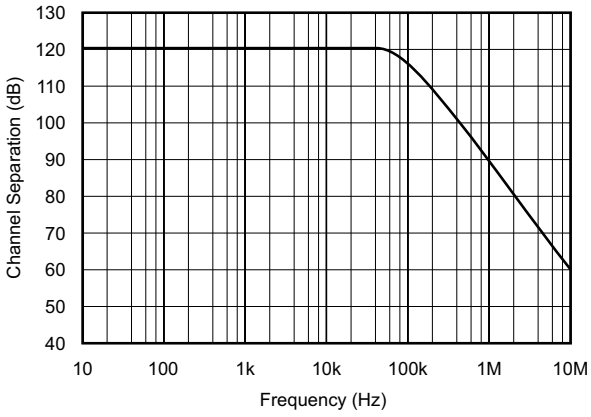



**Figure 18. Channel Separation vs Frequency**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{OUT}$ = $V_S$ / 2, and $V_{CM}$ = $V_S$ / 2, (unless otherwise noted)

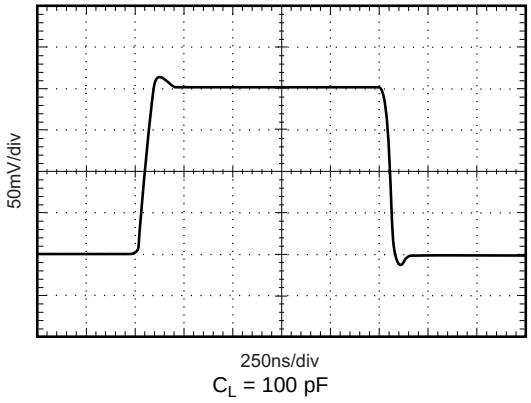



**Figure 19. Small-Signal Step Response**

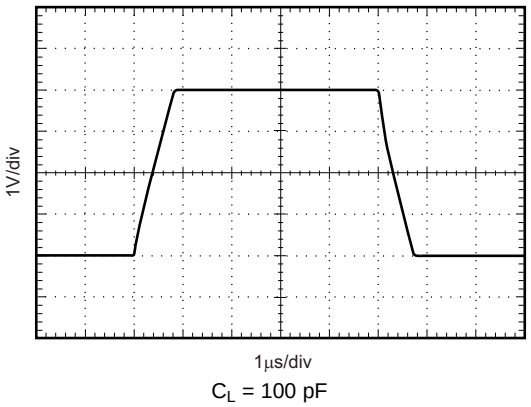


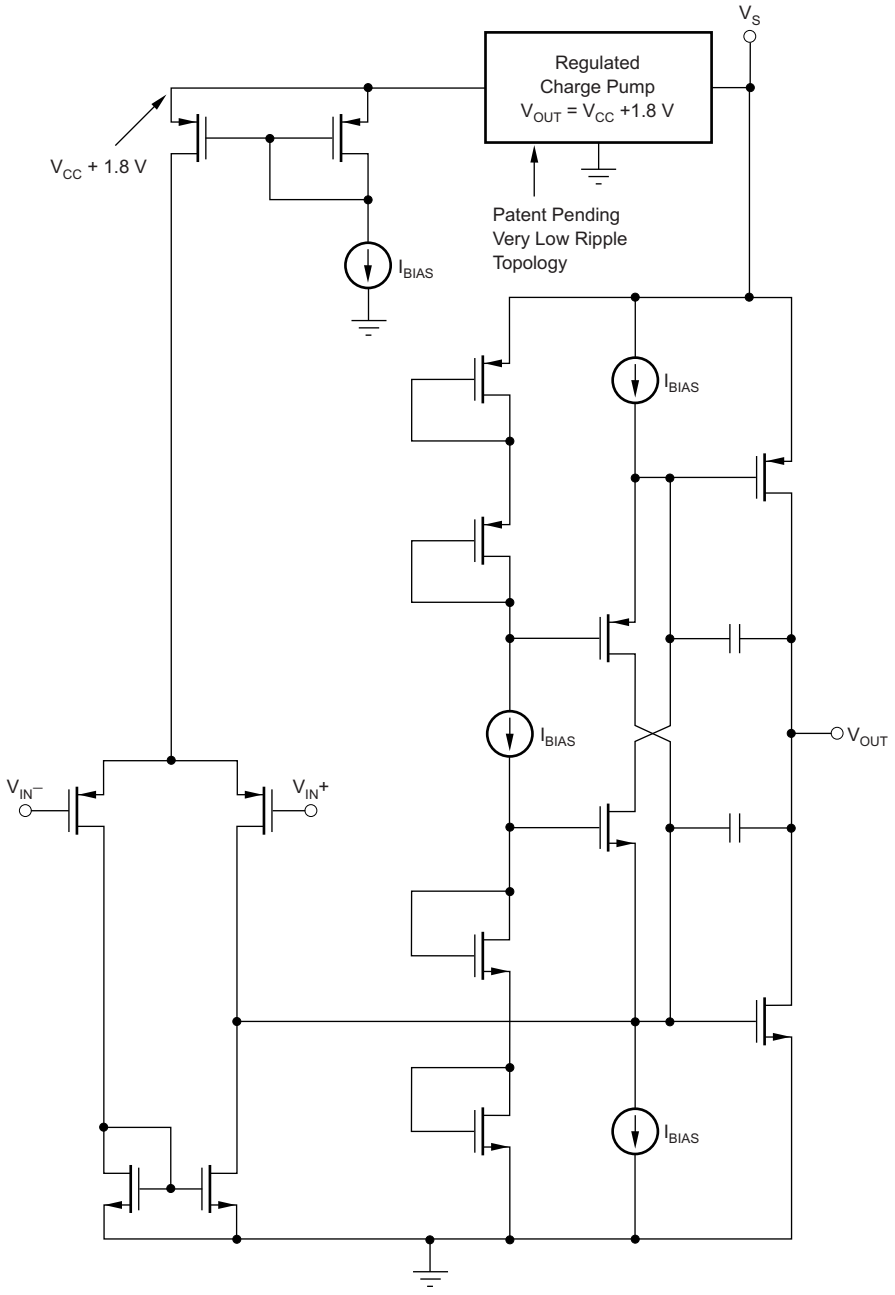

**Figure 20. Large-Signal Step Response**

# 8 Detailed Description

## 8.1 Overview

The OPA363 and OPA364 series op amps are rail-to-rail operational amplifiers with excellent CMRR, low noise, low offset, and wide bandwidth on supply voltages as low as ±0.9 V. The OPA363 features an additional pin for a shutdown and enable function. These families do not exhibit phase reversal and are unity-gain stable. Specified over the industrial temperature range of –40°C to +125°C, the OPA363 and OPA364 families offer precision performance for a wide range of applications.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Rail-to-Rail Input

The OPA363 and OPA364 feature excellent rail-to-rail operation, with supply voltages as low as ±0.9 V. The input common-mode voltage range of the OPA363 and OPA364 family extends 100 mV beyond supply rails. The unique input topology of the OPA363 and OPA364 eliminates the input offset transition region typical of most rail-to-rail, complementary stage operational amplifiers, allowing the OPA363 and OPA364 to provide superior common-mode performance over the entire common-mode input range, as seen in Figure 21. This feature prevents degradation of the differential linearity error and THD when driving A/D converters. A simplified schematic of the OPA363 and OPA364 is shown in the *Functional Block Diagram*.

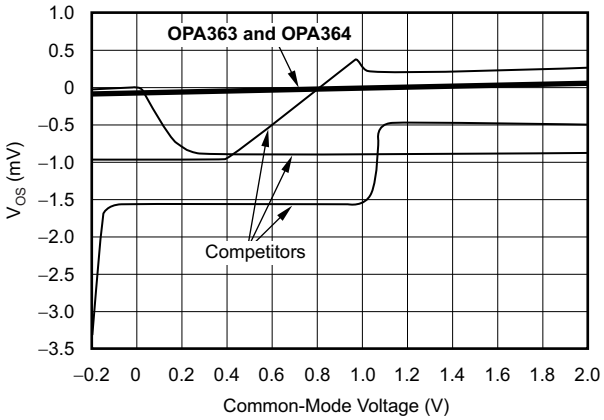



**Figure 21. OPA363 and OPA364 Have Linear Offset Over Entire Common-Mode Range**

### 8.3.2 Operating Voltage

The OPA363 and OPA364 series op amp parameters are fully specified from 1.8 V to 5.5 V. Single 0.1-µF bypass capacitors must be placed across supply pins and as close to the part as possible. Supply voltages higher than 5.5 V (absolute maximum) may cause permanent damage to the amplifier. Many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics*.

### 8.3.3 Capacitive Load

The OPAx363 and OPAx364 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are a few of the factors to consider when determining stability. An op amp in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the output resistance of the op amp to create a pole in the small-signal response, which degrades the phase margin.

In unity gain, the OPAx363 and OPAx364 series op amps perform well with a pure capacitive load up to approximately 1000 pF. The equivalent series resistance (ESR) of the loading capacitor may be sufficient to allow the OPA363 and OPA364 to directly drive very large capacitive loads ( greater than 1 µF). Increasing gain enhances the ability of the amplifier to drive more capacitance; see Figure 13.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in Figure 22. This resistor significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, the load creates a voltage divider, introduces a DC error at the output, and slightly reduces output swing. This error may be insignificant. For example, with $R_L$ = 10 kΩ and $R_S$ = 20 Ω, there is an approximate 0.2% error at the output.

## Feature Description (continued)

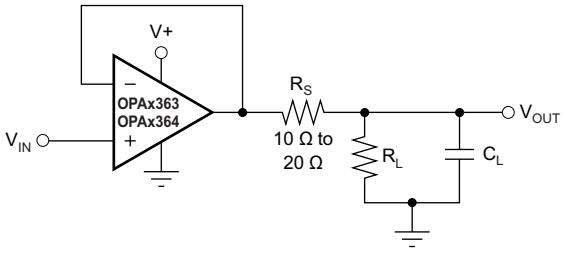





**Figure 22. Improving Capacitive Load Drive**

### 8.3.4 Input and ESD Protection

All OPAx363 and OPAx364 pins are static-protected with internal ESD protection diodes tied to the supplies. These diodes provide overdrive protection if the current is externally limited to 10 mA, as shown in the *Absolute Maximum Ratings* and shown in Figure 23.

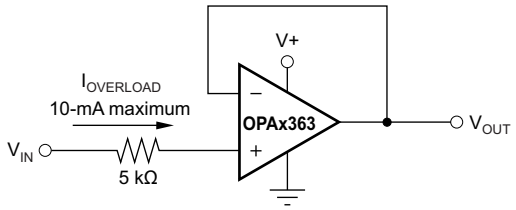





**Figure 23. Input Current Protection**

## 8.4 Device Functional Modes

### 8.4.1 Enable Function

The shutdown (enable) function of the OPAx363 is referenced to the negative supply voltage of the operational amplifier. A logic level HIGH enables the op amp. A valid logic HIGH is defined as voltage greater than 75% of the positive supply applied to the enable pin. The valid logic HIGH signal can be as much as 5.5 V above the negative supply, independent of the positive supply voltage. A valid logic LOW is defined as less than 0.8 V above the negative supply pin. If dual or split power supplies are used, take care to ensure that logic input signals are properly referred to the negative supply voltage. This pin must be connected to a valid high or low voltage or driven, not left open-circuit.

The logic input is a high-impedance CMOS input. Dual op amps are provided separate logic inputs. For battery-operated applications, this feature reduces the average current and extend battery life. The enable time is 20 μs; disable time is 1 μs. When disabled, the output assumes a high-impedance state. This configuration allows the OPAx363 to operate as a *gated* amplifier, or to have the output multiplexed onto a common analog output bus.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Achieving Output Swing to the Op Amp Negative Rail

Some applications require an accurate output voltage swing from 0 V to a positive full-scale voltage. A good single-supply op amp may be able to swing within a few millivolts of single-supply ground, but as the output is driven toward 0 V, the output stage of the amplifier prevents the output from reaching the negative supply rail of the amplifier.

The output of the OPAx363 or OPAx364 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires use of another resistor and an additional, more negative power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 24.

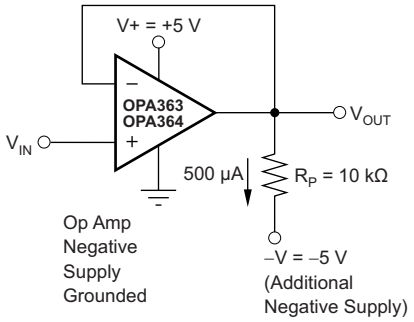





**Figure 24. OPA363 and OPA364 Swing to Ground**

This technique does not work with all op amps. The output stage of the OPAx363 and OPA3x64 allows the output voltage to be pulled below that of most op amps, if approximately 500 µA is maintained through the output stage. To calculate the appropriate value load resistor and negative supply, $R_L$ = –V / 500 µA. The OPAx363 and OPAx364 are characterized to perform well under the described conditions, maintaining excellent accuracy down to 0 V and as low as –10 mV. Limiting and nonlinearity occur below –10 mV, with linearity returning as the output is again driven above –10 mV.

### 9.1.2 Directly Driving the ADS8324 and the MSP430

The OPAx363 and OPAx364 series op amps are optimized for driving medium speed (up to 100-kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The no-crossover input stage of the OPAx363 and OPAx364 directly drive A/D converters without degradation of differential linearity and THD. They provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. Figure 25 and Figure 26 show the OPAx363 and OPAx364 configured to drive the ADS8324 and the 12-bit A/D converter on the MSP430.

## Application Information (continued)

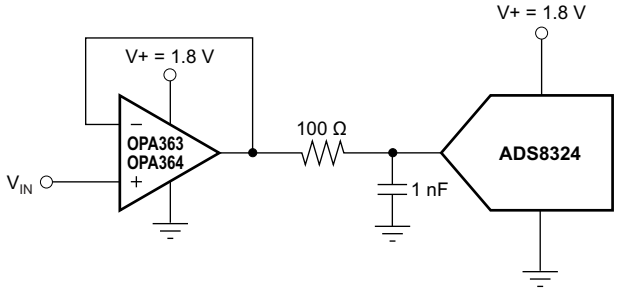





**Figure 25. OPAx363 and OPAx364 Directly Drive the ADS8324**

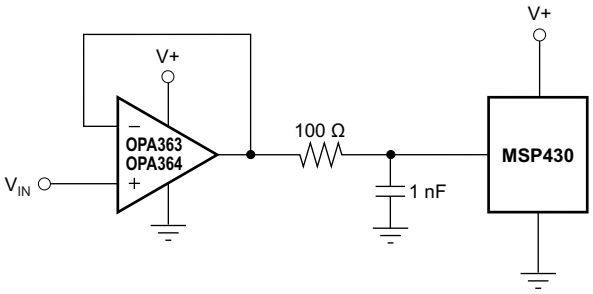





**Figure 26. Driving the 12-Bit A/D Converter on the MSP430**

### 9.1.3 Audio Applications

The OPAx363 and OPAx364 op amp family has linear offset voltage over the entire input common-mode range. Combined with low noise, this feature makes the OPAx363 and OPAx364 suitable for audio applications. Single-supply, 1.8-V operation allows the OPA2363 and OPA2364 to be optimal candidates for dual stereo-headphone drivers and microphone preamplifiers in portable stereo equipment; see Figure 27 and Figure 28.

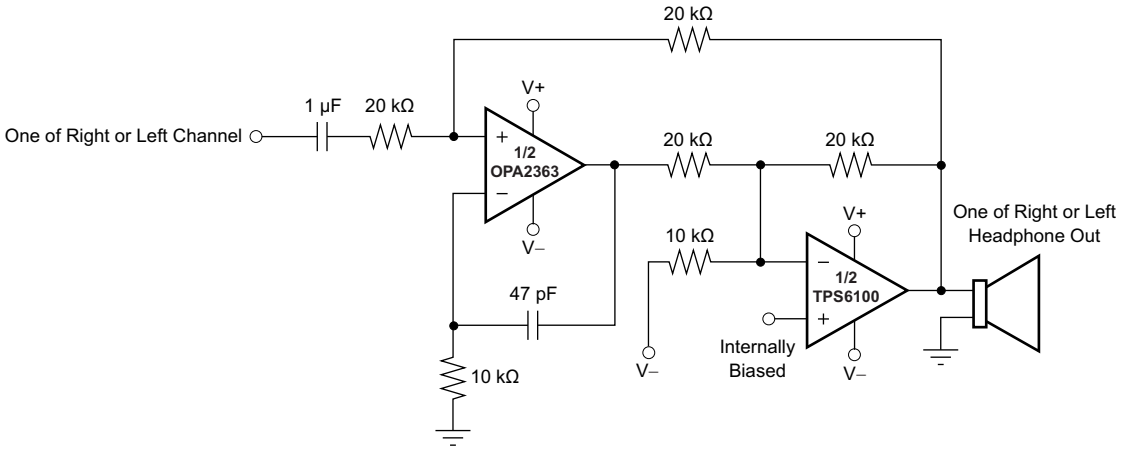





**Figure 27. OPA2363 Configured as Half of a Dual Stereo-Headphone Driver**

## Application Information (continued)

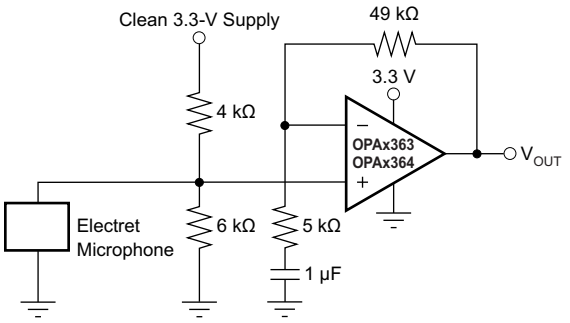





**Figure 28. Microphone Preamplifier**

### 9.1.4 Active Filtering

Low harmonic distortion and noise specifications plus high gain and slew rate make the OPAx363 and OPAx364 optimal candidates for active filtering. Figure 29 shows the OPA2363 configured as a low-distortion, third-order general immittance converter (GIC) filter. Figure 30 shows the implementation of a Sallen-Key, 3-pole, low-pass Bessel filter.

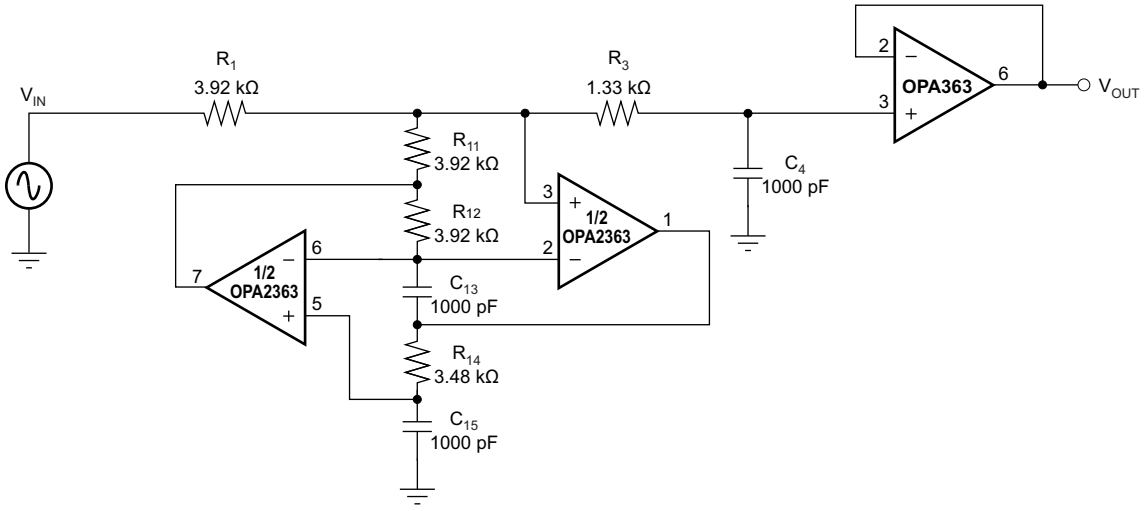





**Figure 29. OPA2363 as a Third-Order, 40-kHz, Low-Pass GIC Filter**

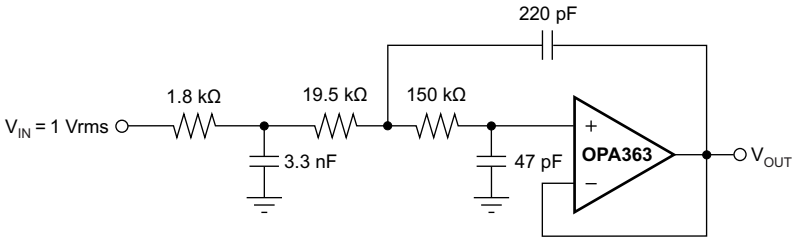





**Figure 30. OPAx363 or OPAx364 Configured as a 3-Pole, 20-kHz, Sallen-Key Filter**

## 9.2 Typical Application

### 9.2.1 Single-Supply Electret Microphone Preamplifier

Electret microphones are commonly used in portable electronics because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The small package size and excellent AC performance of the OPA364 make it an excellent choice for preamplifier circuits for electret microphones. The circuit shown in Figure 31 is a single-supply preamplifier circuit for electret microphones.

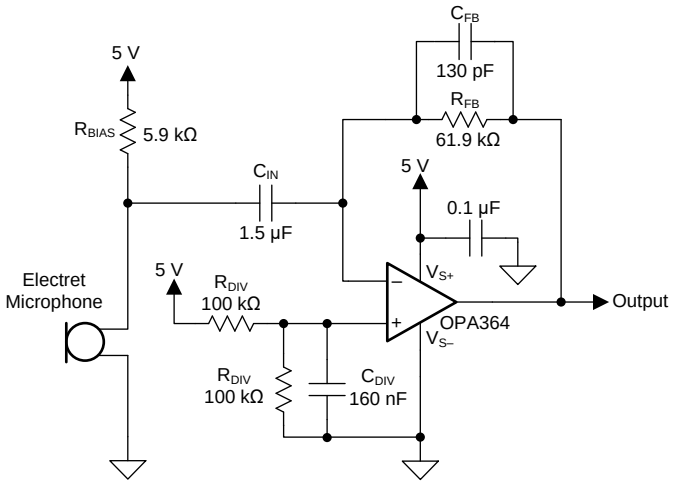





**Figure 31. Preamplifier Circuit for Electret Microphones Using a Single-Supply Voltage**

#### *9.2.1.1 Design Requirements*

- 5-V single supply
- 1-$V_{RMS}$ output for 100-$dB_{SPL}$ input
- 20-Hz to 20-kHz, –3-dB bandwidth
- Microphone sensitivity: 8 µA/Pa
- Microphone operating voltage: 2 V to 10 V
- Microphone bias current: 500 µA

#### *9.2.1.2 Detailed Design Procedure*

In this circuit, the op amp is configured as a transimpedance amplifier which converts the signal current of the microphone into an output voltage. The gain of the circuit is determined by the feedback resistor $R_{FB}$, which must be calculated according to the microphone sensitivity. For this design, a microphone output current of 8 µA per Pascal (Pa) of air pressure was chosen. Using this value, the output current for a sound pressure level of 100 $dB_{SPL}$, or 2 Pa air pressure, is calculated in Equation 1.

$$i_{mic} = \frac{8\ \mu A}{1\ Pa} \times 2\ Pa = 16\ \mu A \tag{1}$$

$R_{FB}$ is then calculated from this current to produce 1-$V_{RMS}$ output for a 100-$dB_{SPL}$ input signal in Equation 2.

$$R_{FB} = \frac{V_O}{i_{mic}} = \frac{1\ V_{RMS}}{16\ \mu A} = 62500 \rightarrow 61.9\ k\Omega \tag{2}$$

The feedback capacitor ($C_{FB}$) is calculated to limit the bandwidth of the amplifier to 20 kHz in Equation 3.

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot R_{FB} \cdot f_H} = \frac{1}{2 \cdot \pi \cdot (61.9\ k\Omega) \cdot (20\ kHz)} = 128.5 \times 10^{-12} \rightarrow 130\ pF \tag{3}$$

## Typical Application (continued)

$R_{BIAS}$ is required to divert the microphone signal current through capacitor $C_{IN}$ rather than flowing from the power supply, $V_{CC}$. Larger values of $R_{BIAS}$ allow for a smaller capacitor to be used for $C_{IN}$ and reduce the overall noise of the circuit. However, the maximum value for $R_{BIAS}$ is limited by the microphone bias current and minimum operating voltage.

The value of $R_{BIAS}$ is calculated in Equation 4.

$$R_{BIAS} = \frac{V_{CC} - V_{MIC}}{I_{BIAS}} = \frac{5\ V - 2\ V}{500\ \mu A} = 6000 \rightarrow 5.9\ k\Omega \tag{4}$$

Input capacitor $C_{IN}$ forms a high-pass filter in combination with resistor $R_{BIAS}$. The filter corner frequency calculation is shown in Equation 5 to place the high-pass corner frequency at 20 Hz.

$$C_{IN} = \frac{1}{2 \cdot \pi \cdot R_{BIAS} \cdot f_L} = \frac{1}{2 \cdot \pi \cdot (5.9\ k\Omega) \cdot (20\ Hz)} = 1.349 \times 10^{-6} \rightarrow 1.5\ \mu F \tag{5}$$

The voltage divider network at the op amp noninverting input is used to bias the op amp output to the mid-supply point ($V_{CC}$ / 2) to maximize the output voltage range of the circuit. This result is easily achieved by selecting the same value for both resistors in the divider. The absolute value of those resistors is limited by the acceptable power-supply current drawn by the voltage divider. Selecting 25 µA as an acceptable limit of supply current gives a value of 100 kΩ for the resistors in the divider, as Equation 6 shows.

$$R_{DIV} = \frac{V_{CC}}{2 \cdot I_{DIV}} = \frac{5\ V}{2 \cdot 25\ \mu A} = 100\ k\Omega \tag{6}$$

Finally, to minimize the additional noise contribution from the voltage divider, a capacitor is placed at the op amp noninverting input. This capacitor forms a low-pass filter with the parallel combination of the voltage divider resistors. Selecting a filter corner frequency of 20 Hz minimizes the noise contribution of the voltage divider inside the amplifier passband; see Equation 7.

$$C_{DIV} = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{DIV}}{2}\right) \cdot f_L} = \frac{1}{2 \cdot \pi \cdot \left(\frac{100\ k\Omega}{2}\right) \cdot (20\ Hz)} = 1.592 \times 10^{-7} \rightarrow 160\ nF \tag{7}$$

#### 9.2.1.3 Application Curve

The transfer function of the microphone preamplifier circuit is shown in Figure 32. The nominal gain of the circuit is 95.82 dB, or 61,800 V per amp of input current. The –3-dB bandwidth limits of the circuit are 17.99 Hz and 19.23 kHz.

## Typical Application (continued)

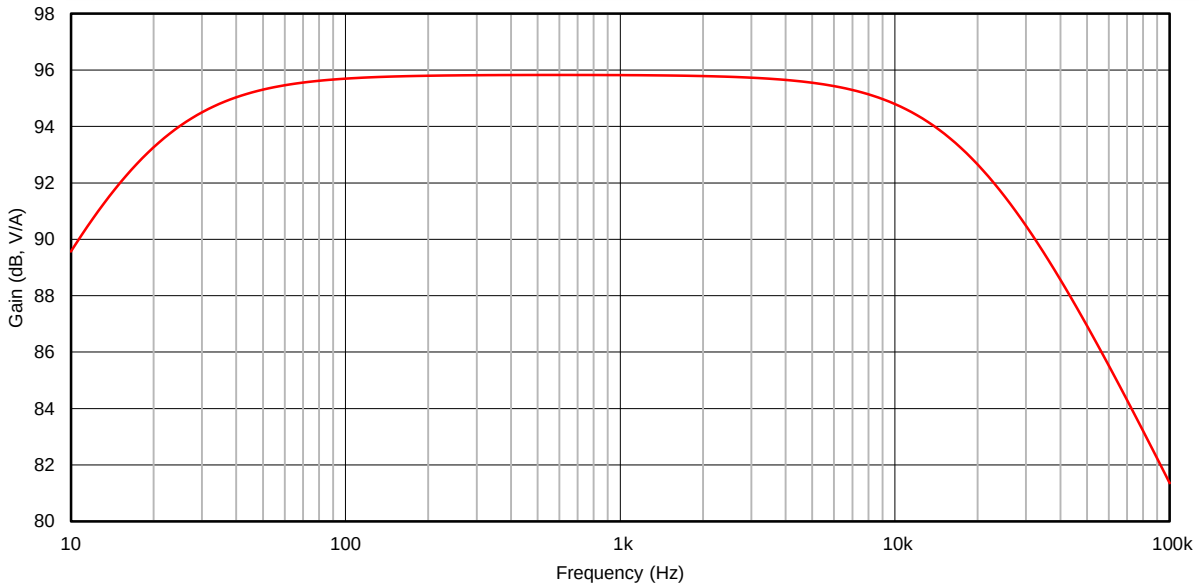



**Figure 32. Microphone Preamplifier Transfer Function**

# 10 Power Supply Recommendations

The OPAx363 and OPAx364 are specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in the *Electrical Characteristics*.

# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 33, keeping $R_F$ and $R_G$ close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

## 11.2 Layout Example

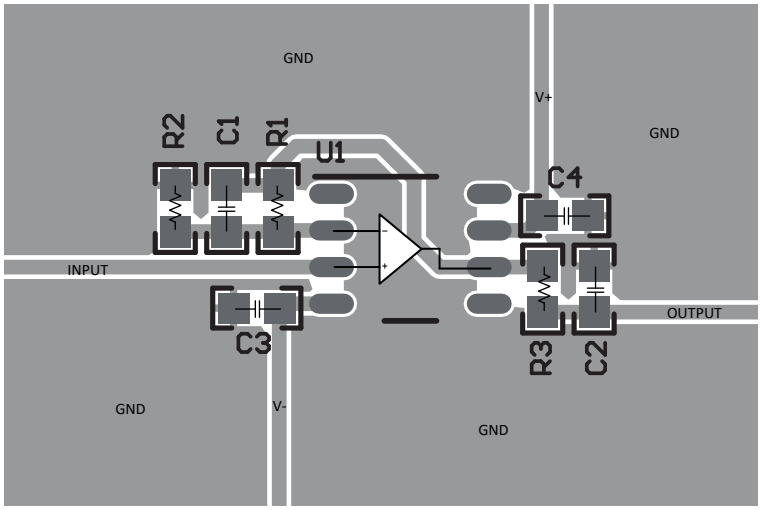



**Figure 33. Operational Amplifier Board Layout for Noninverting Configuration**

## Layout Example (continued)

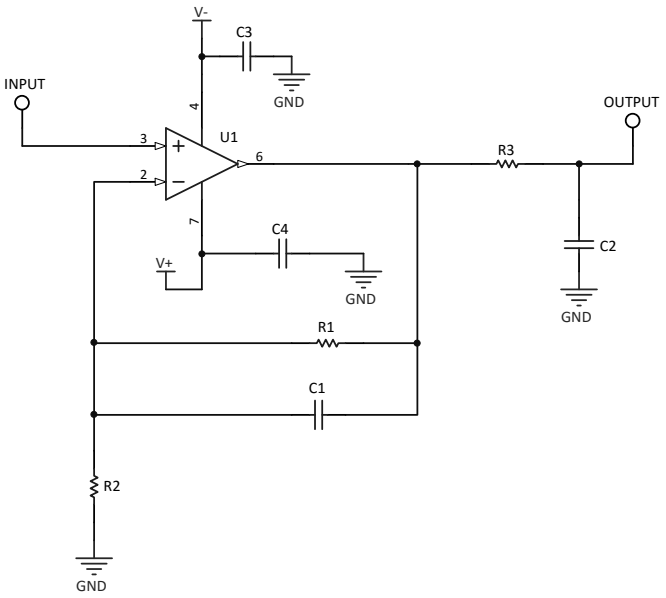



**Figure 34. Layout Example Schematic**

# 12 デバイスおよびドキュメントのサポート

## 12.1 デバイス・サポート

### 12.1.1 開発サポート

#### *12.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)*

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

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注

これらのファイルを使用するには、TINA ソフトウェア ( DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

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#### *12.1.1.2 DIPアダプタ評価モジュール*

DIPアダプタ評価モジュール・ツールを使用すると、小さな表面実装ICのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU (8ピンSOIC)、PW (8ピンTSSOP)、DGK (8ピンMSOP)、DBV (6ピンSOT-23、5ピンSOT-23、3ピンSOT-23)、DCK (6ピンSC-70および5ピンSC-70)、DRL (6ピンSOT-563) のTIパッケージに対応しています。DIPアダプタ評価モジュールは、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

#### *12.1.1.3 ユニバーサル・オペアンプ評価モジュール*

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のデバイス・パッケージ・タイプ向け回路のプロトタイプ作成を容易にします。この評価モジュール基板は、多くの異なる回路を簡単かつ迅速に構築できるように設計されています。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、SOT-23のすべてのパッケージがサポートされています。

---

注

これらの基板には部品が搭載されていないため、ユーザーが独自のデバイスを実装する必要があります。ユニバーサル・オペアンプ評価モジュールを注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

---

#### *12.1.1.4 TI Precision Designs*

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

#### *12.1.1.5 WEBENCH® Filter Designer*

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

## 12.2 ドキュメントのサポート

### 12.2.1 関連資料

以下に示すドキュメントはOPAx363およびOPAx364の使用に関連しており、参照用にお勧めします。すべてのドキュメントは、特に記述のない限りwww.ti.comからダウンロードできます。

- *『AB-045 オペアンプの性能分析』*
- *『AB-067 オペアンプの単一電源動作』*
- *『AB-105 アンプのチューニング』*
- *『QFN/SONのPCB実装』*
- *『クワッド・フラットパック・リード端子なしロジック・パッケージ』*

## 12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

**表 1. 関連リンク**

| 製品 | プロダクト・フォルダ | ご注文はこちら | 技術資料 | ツールとソフトウェア | サポートとコミュニティ |
|---|---|---|---|---|---|
| OPA363 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| OPA2363 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| OPA364 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| OPA2364 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| OPA4364 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |

## 12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™オンライン・コミュニティ** ***TIのE2E ( Engineer-to-Engineer ) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

**設計サポート** ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 12.6 商標

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

## 12.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

## 12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2363AIDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | BHK | Samples |
| OPA2363AIDGST | ACTIVE | VSSOP | DGS | 10 | 250 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | BHK | Samples |
| OPA2363AIRSVR | ACTIVE | UQFN | RSV | 16 | 3000 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | SIN | Samples |
| OPA2363IDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | BHK | Samples |
| OPA2363IDGST | ACTIVE | VSSOP | DGS | 10 | 250 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | BHK | Samples |
| OPA2364AID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 2364 A | Samples |
| OPA2364AIDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 2364 A | Samples |
| OPA2364AIDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | BHL | Samples |
| OPA2364AIDGKT | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | BHL | Samples |
| OPA2364AIDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 2364 A | Samples |
| OPA2364AIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 2364 A | Samples |
| OPA2364ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 2364 | Samples |
| OPA2364IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | Call TI \| SN | Level-2-260C-1 YEAR | -40 to 125 | BHL | Samples |
| OPA2364IDGKT | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | Call TI \| SN | Level-2-260C-1 YEAR | -40 to 125 | BHL | Samples |
| OPA2364IDGKTG4 | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | BHL | Samples |
| OPA2364IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 2364 | Samples |
| OPA363AID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 363 A | |
| OPA363AIDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A40 | Samples |
| OPA363AIDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A40 | Samples |
| OPA363AIDBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A40 | Samples |
| OPA363ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 363 | Samples |
| OPA363IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A40 | Samples |
| OPA363IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A40 | Samples |
| OPA364AID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 364 A | Samples |
| OPA364AIDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A41 | Samples |
| OPA364AIDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A41 | Samples |
| OPA364AIDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A41 | Samples |
| OPA364AIDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 364 A | Samples |
| OPA364ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 364 | Samples |
| OPA364IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A41 | Samples |
| OPA364IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A41 | Samples |
| OPA364IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | A41 | Samples |
| OPA364IDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 364 | Samples |
| OPA364IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OPA 364 | Samples |
| OPA4364AID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA4364A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA4364AIDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA4364A | Samples |
| OPA4364AIDRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA4364A | Samples |
| OPA4364AIPWR | ACTIVE | TSSOP | PW | 14 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 4364A | Samples |
| OPA4364AIPWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 4364A | Samples |
| OPA4364AIPWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 4364A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF OPA4364 :**

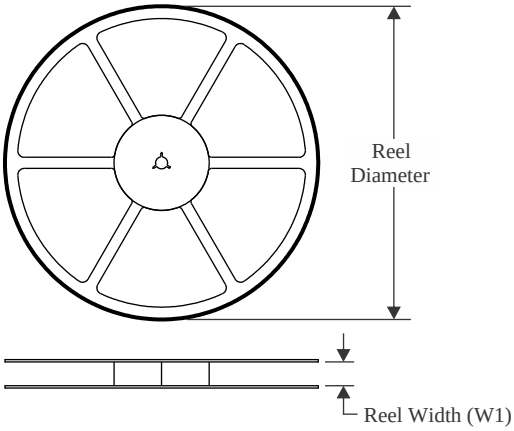
- Automotive : OPA4364-Q1

NOTE: Qualified Version Definitions:

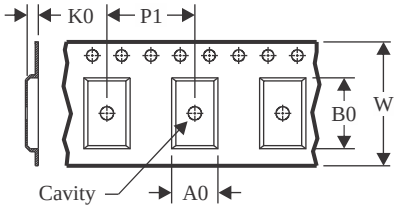
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

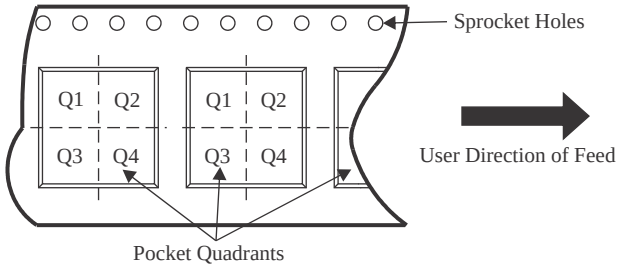



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

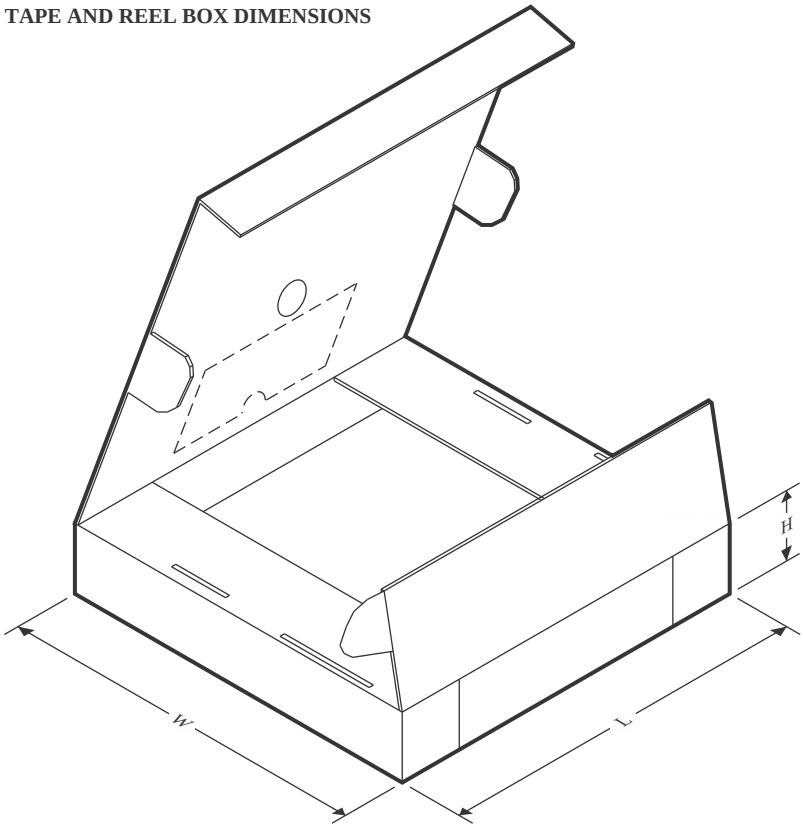
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2363AIRSVR | UQFN | RSV | 16 | 3000 | 177.8 | 12.4 | 2.0 | 2.8 | 0.7 | 4.0 | 12.0 | Q1 |
| OPA2364AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2364IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA363AIDBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA363AIDBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA363IDBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA363IDBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA364AIDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |
| OPA364AIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |
| OPA364AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA364IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |
| OPA364IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |
| OPA364IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA4364AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| OPA4364AIPWR | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA4364AIPWT | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

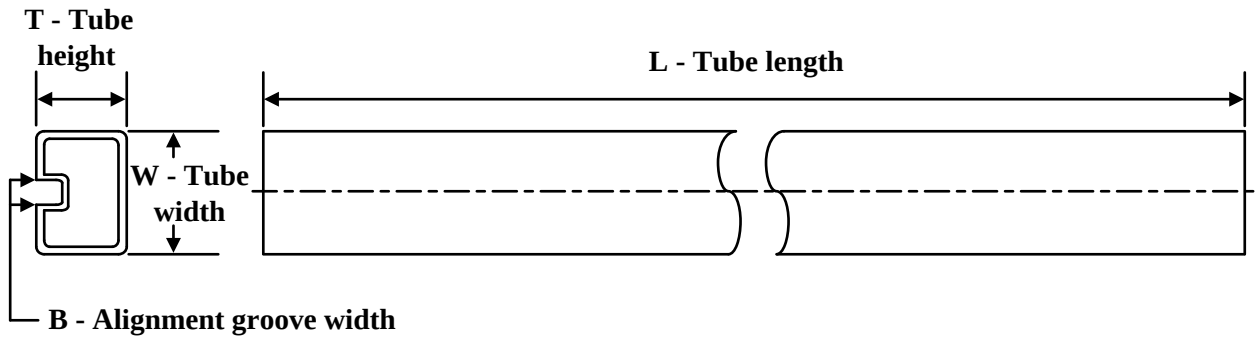
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

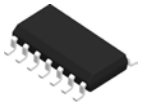
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2363AIRSVR | UQFN | RSV | 16 | 3000 | 223.0 | 270.0 | 35.0 |
| OPA2364AIDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA2364IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA363AIDBVR | SOT-23 | DBV | 6 | 3000 | 565.0 | 140.0 | 75.0 |
| OPA363AIDBVT | SOT-23 | DBV | 6 | 250 | 565.0 | 140.0 | 75.0 |
| OPA363IDBVR | SOT-23 | DBV | 6 | 3000 | 565.0 | 140.0 | 75.0 |
| OPA363IDBVT | SOT-23 | DBV | 6 | 250 | 565.0 | 140.0 | 75.0 |
| OPA364AIDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA364AIDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| OPA364AIDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA364IDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA364IDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| OPA364IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA4364AIDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA4364AIPWR | TSSOP | PW | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA4364AIPWT | TSSOP | PW | 14 | 250 | 210.0 | 185.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| OPA2364AID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA2364AIDG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA2364ID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA363AID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA363ID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA364AID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA364ID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA364IDG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA4364AID | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

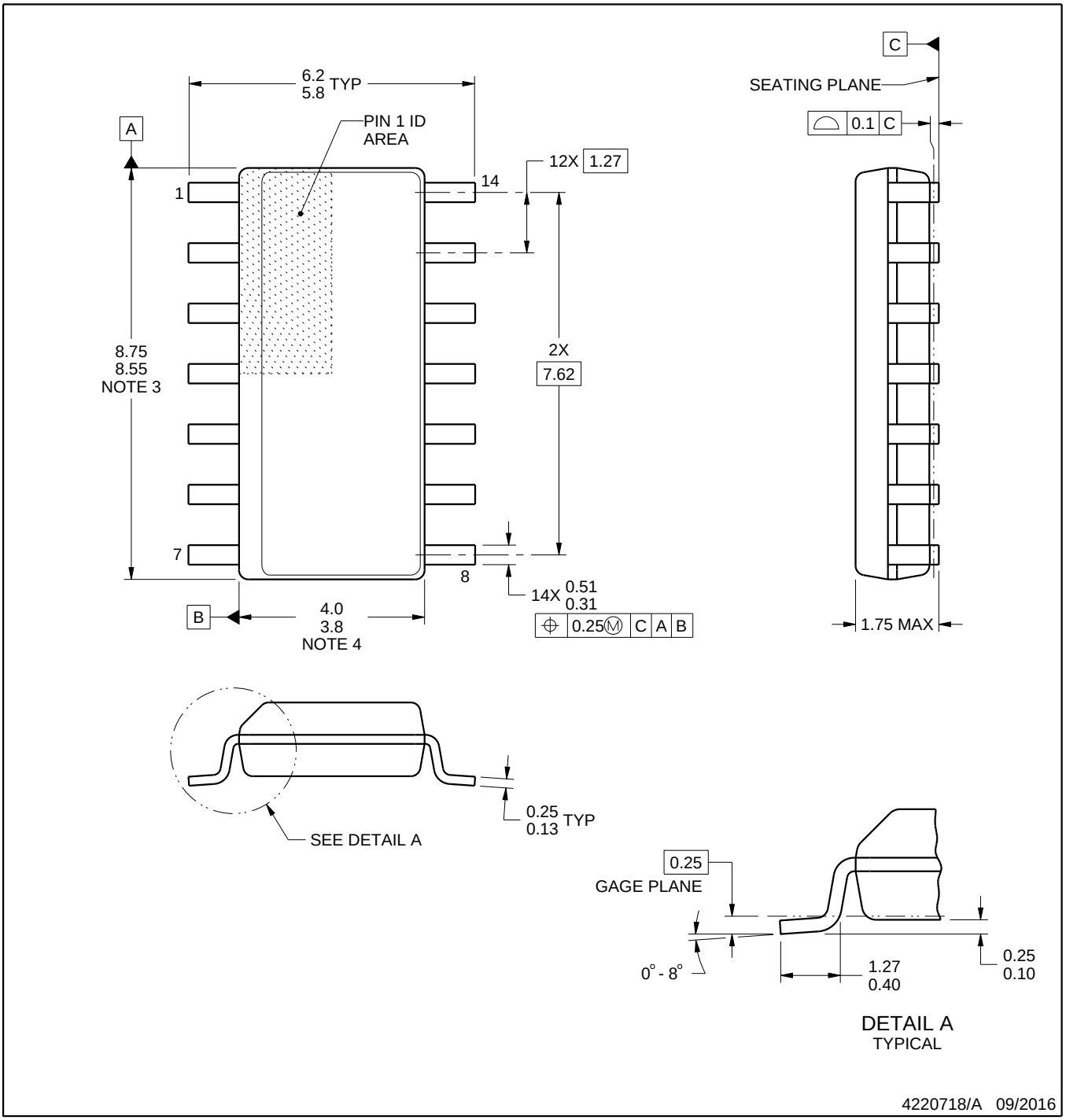


# PACKAGE OUTLINE

## D0014A

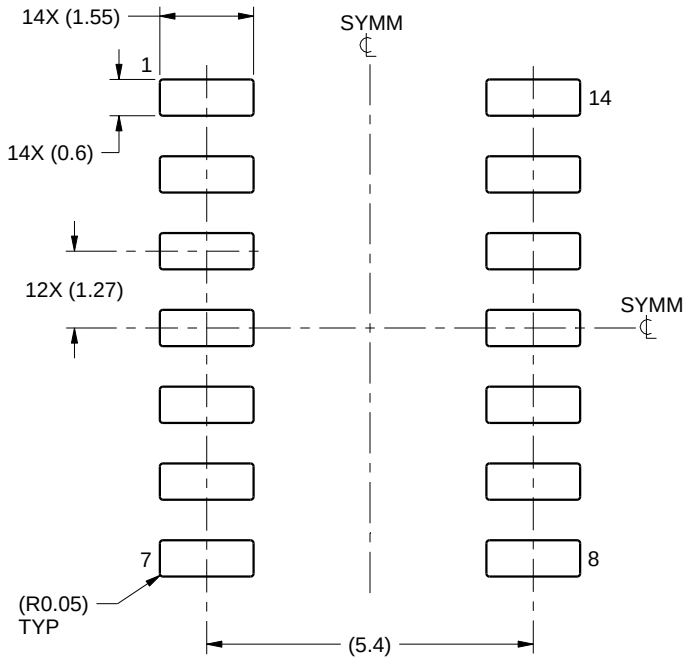
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

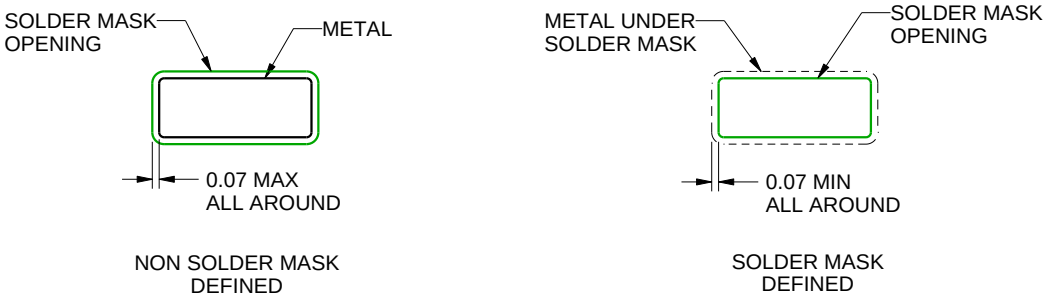



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

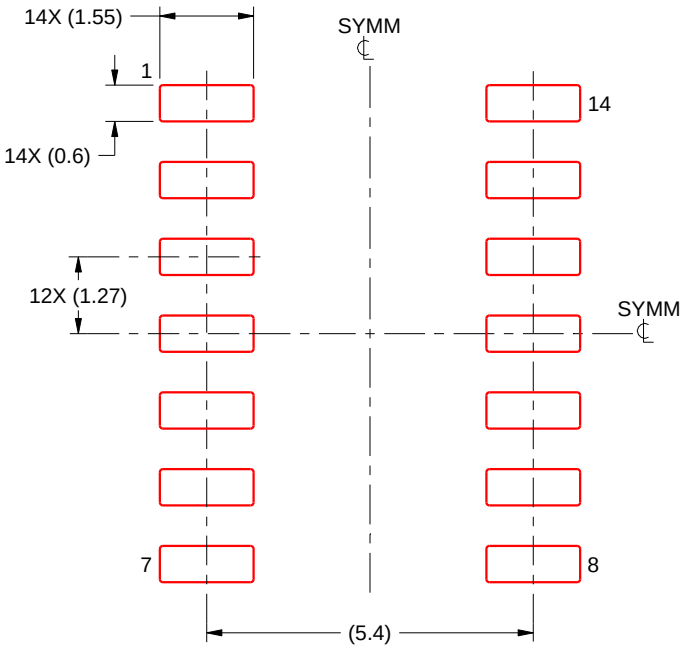
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

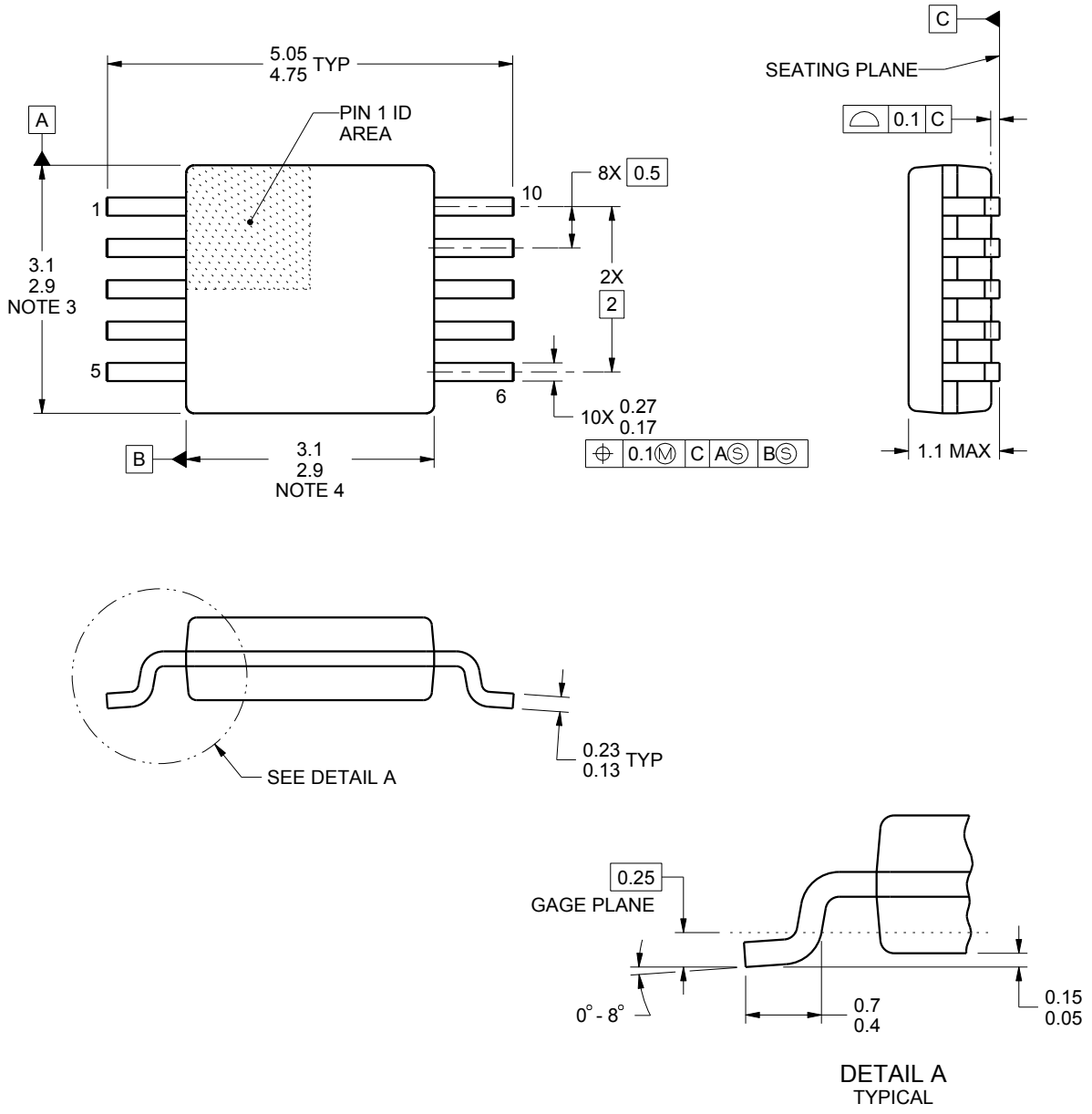
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGS0010A

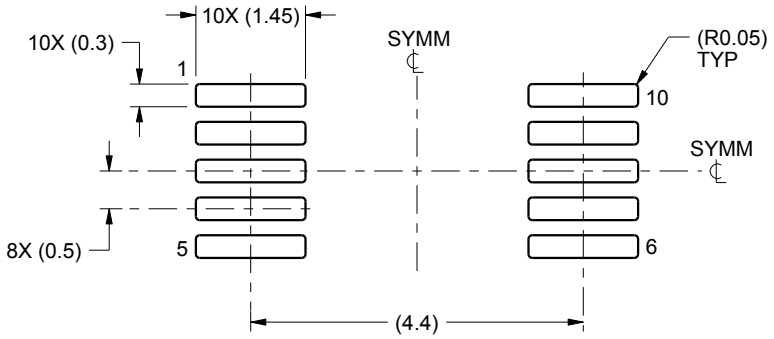
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

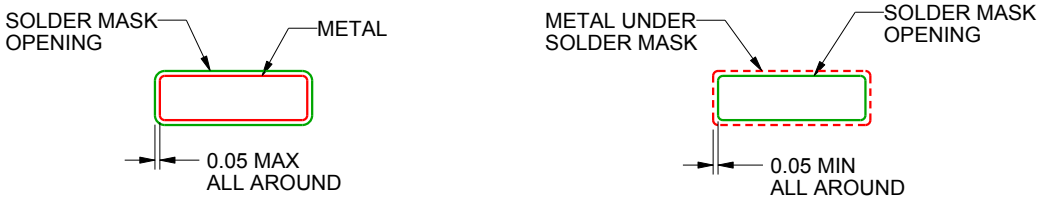



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X

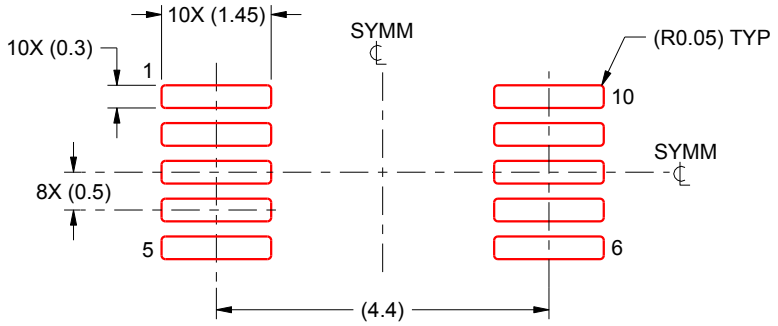



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

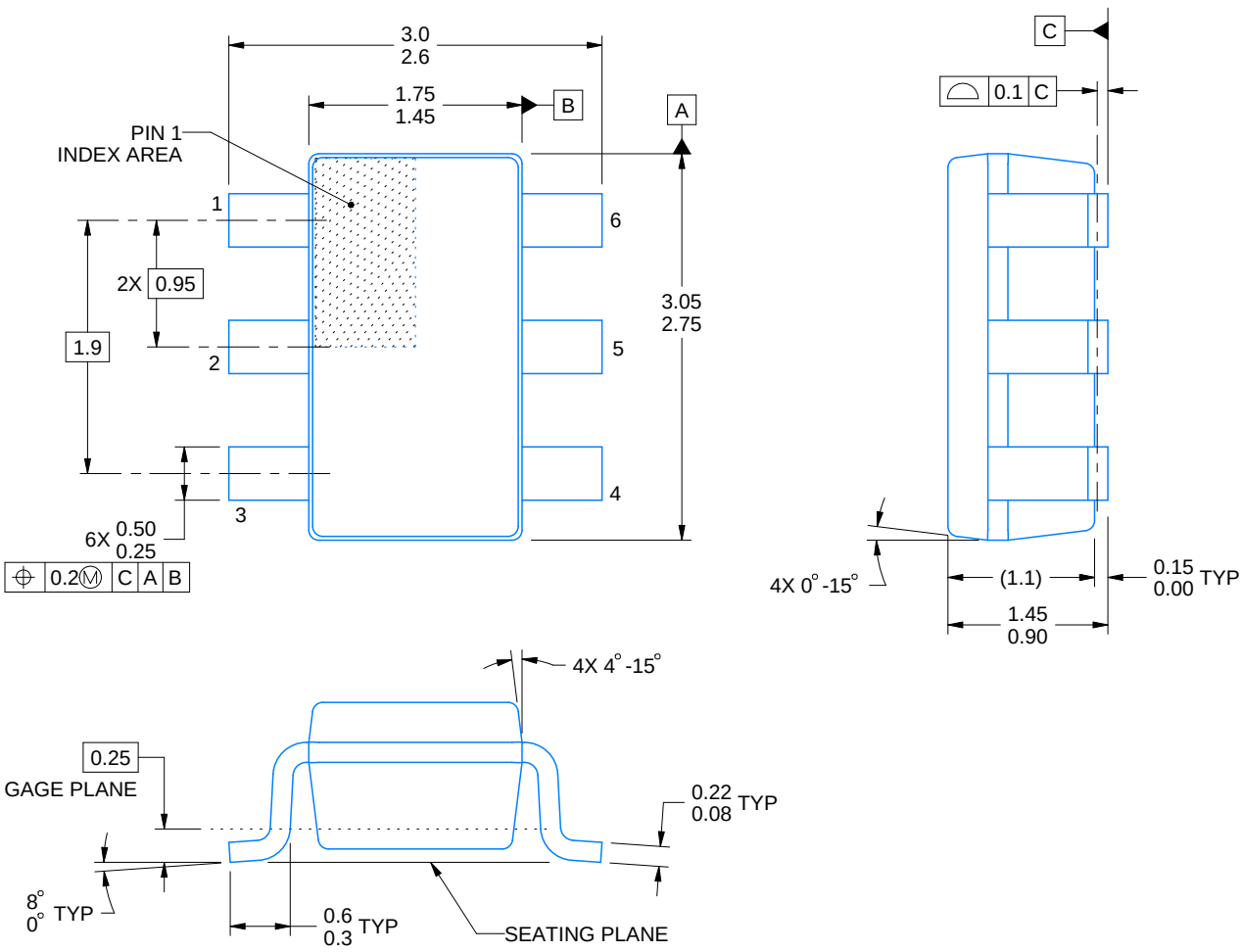
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

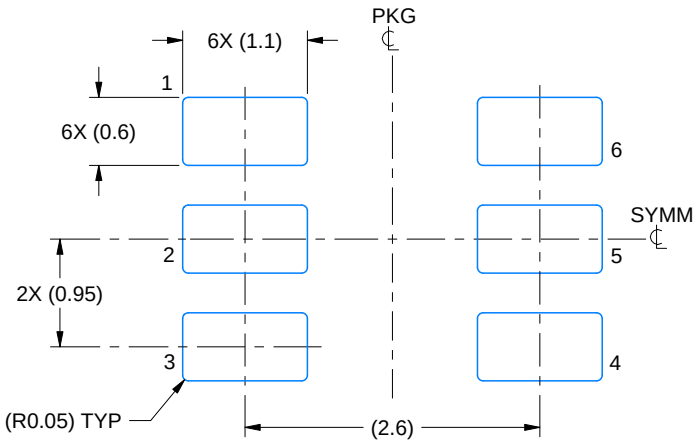
SMALL OUTLINE TRANSISTOR



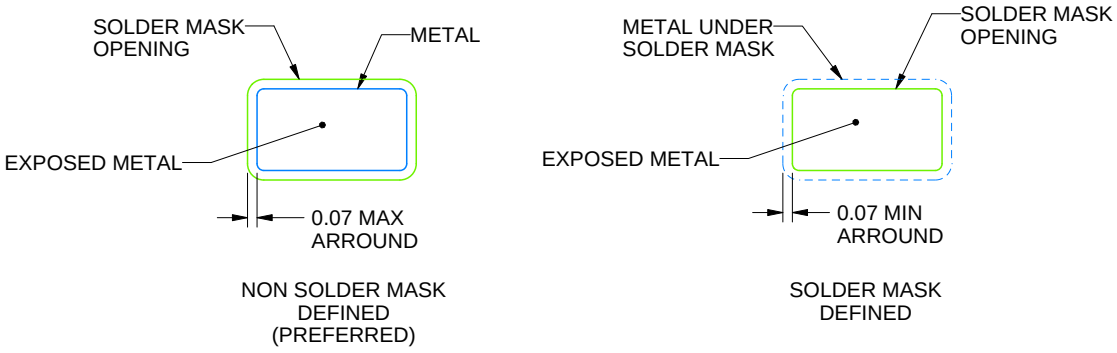

4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

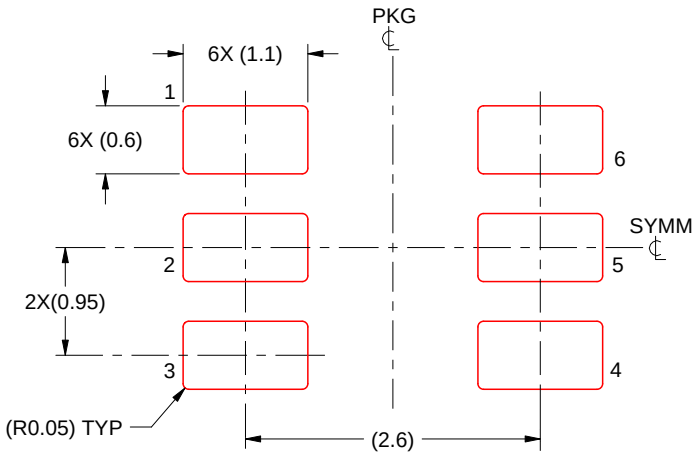



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

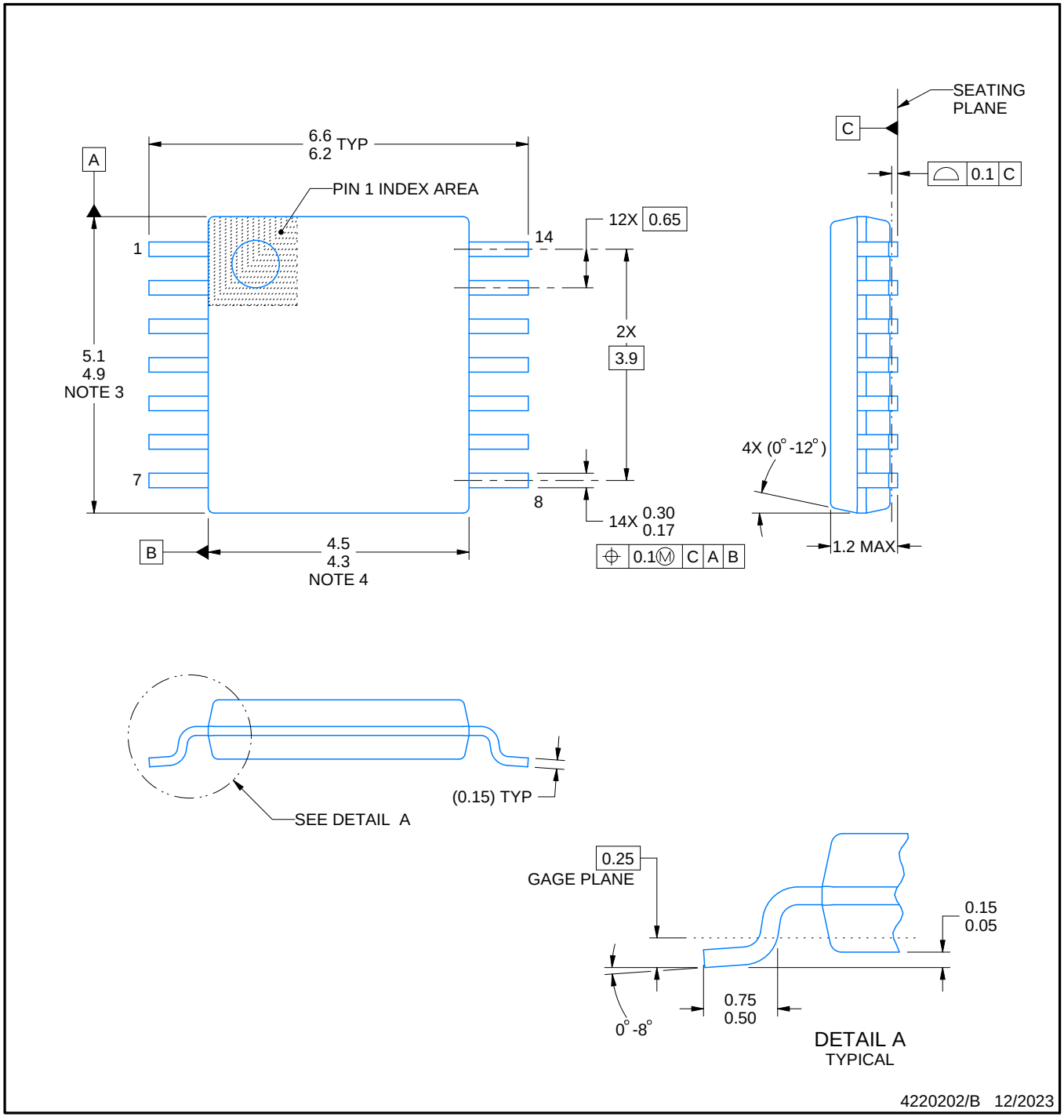
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0014A

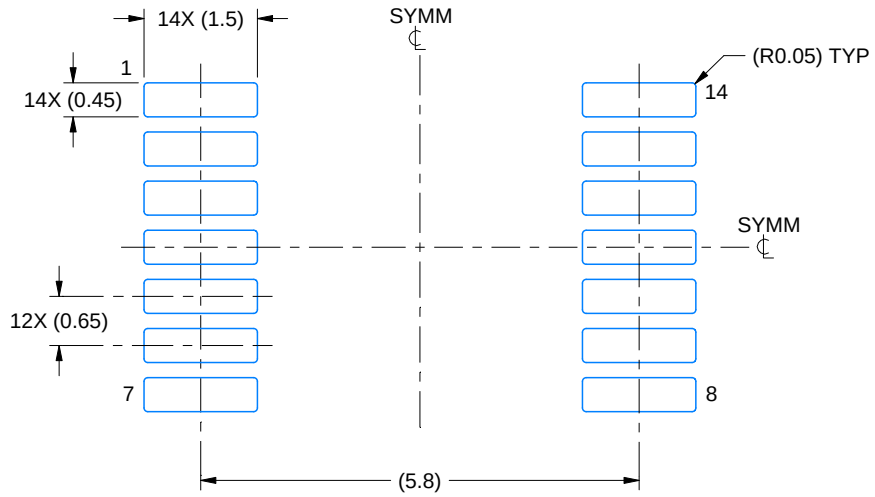
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

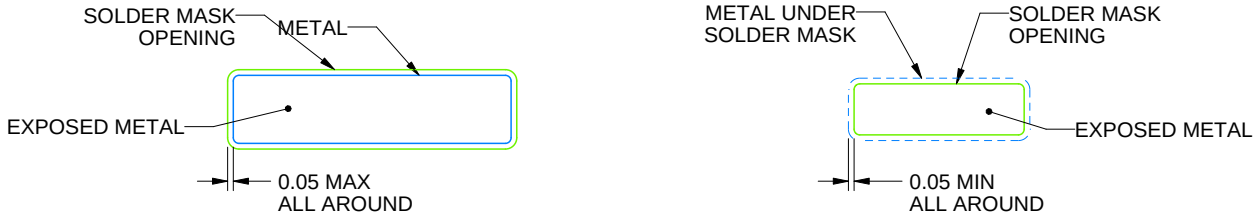



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

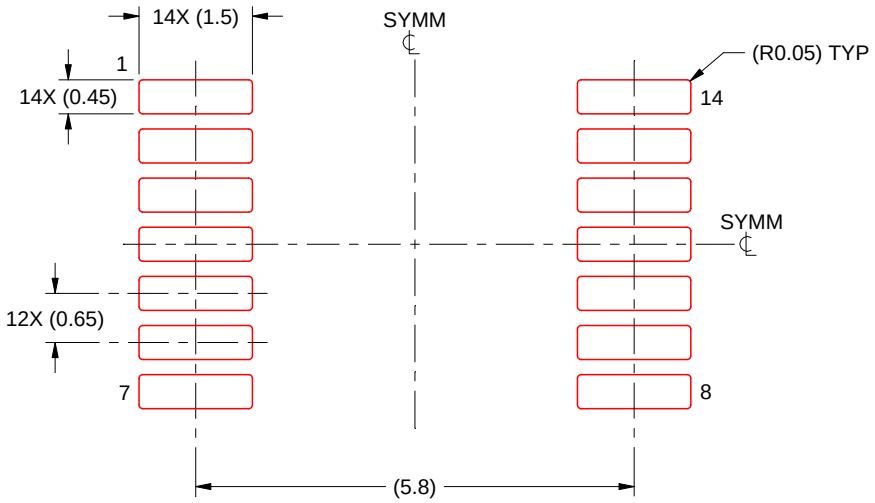



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

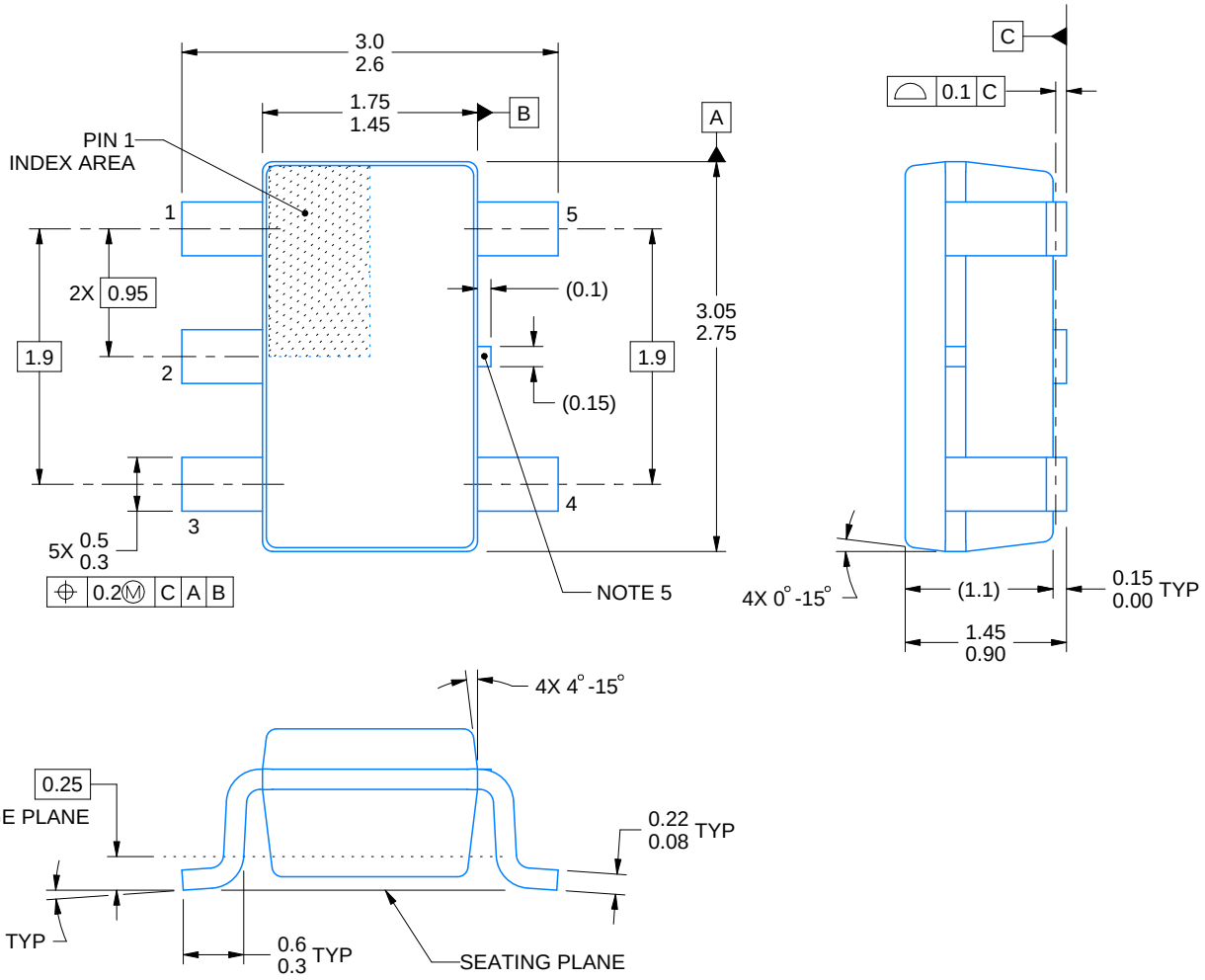
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

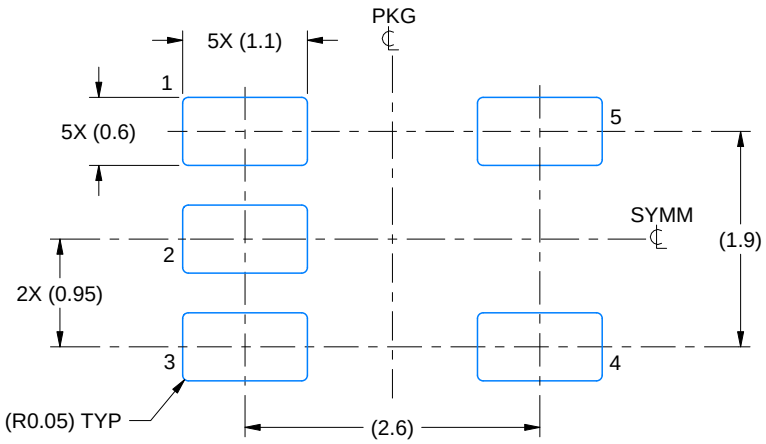
SMALL OUTLINE TRANSISTOR



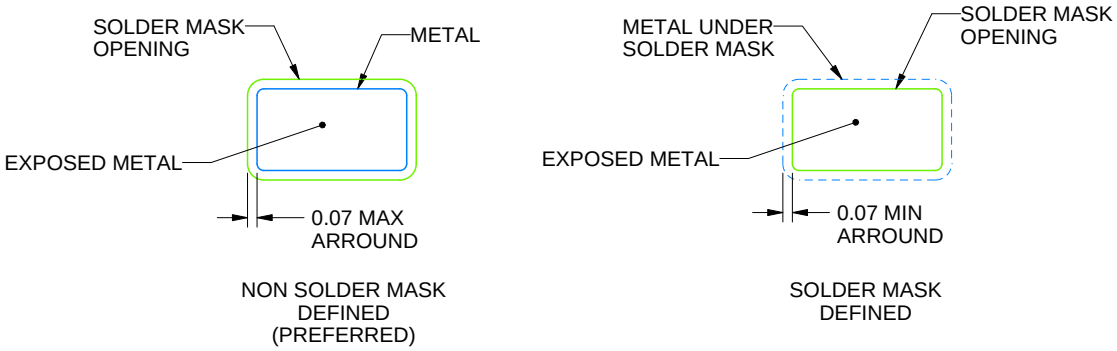

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

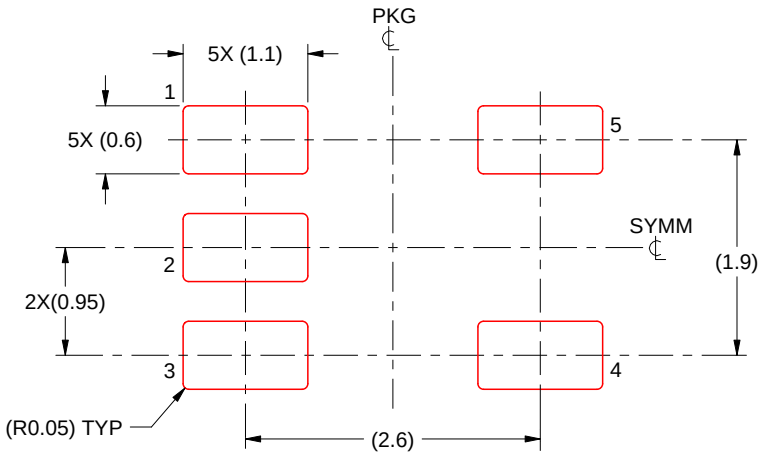



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

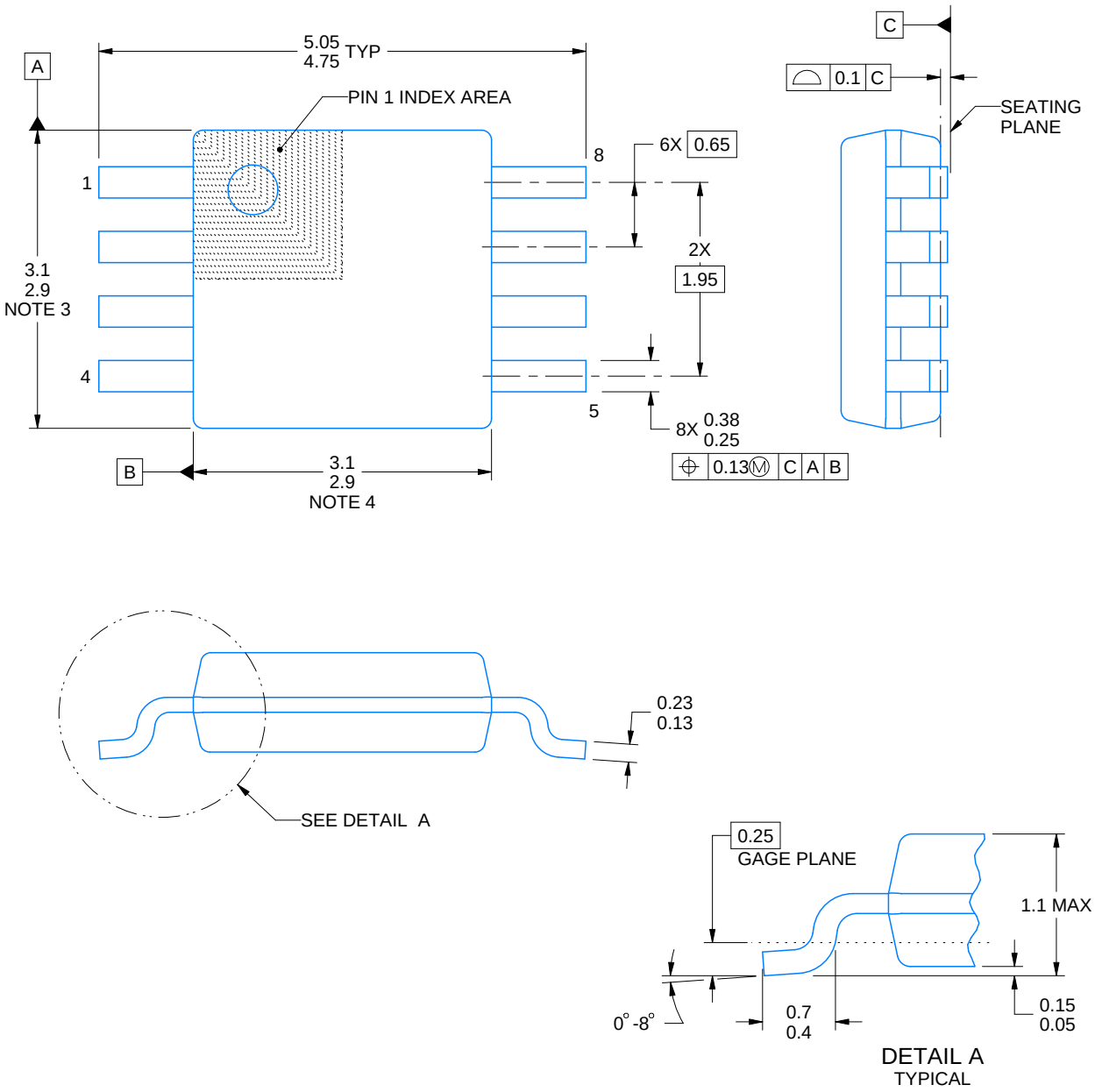
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

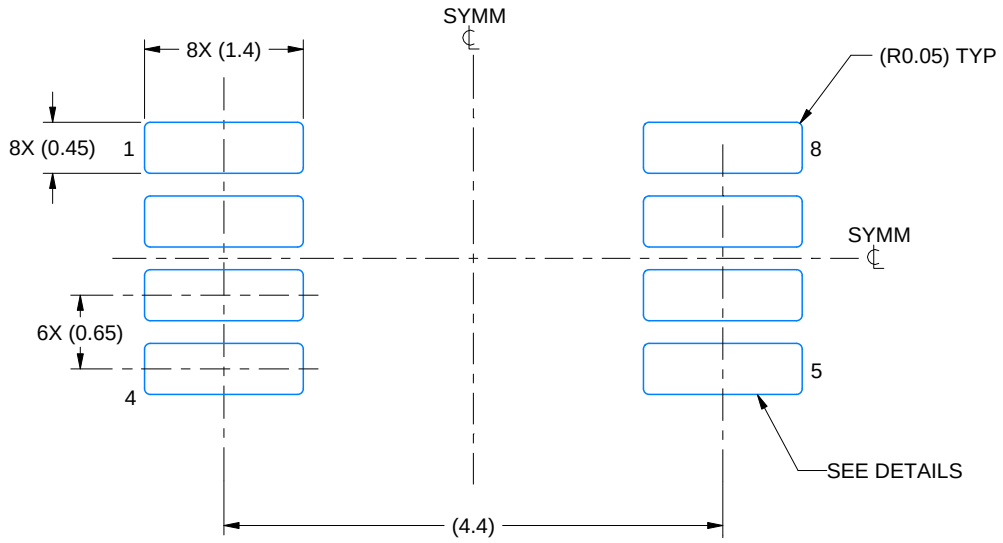
SMALL OUTLINE PACKAGE



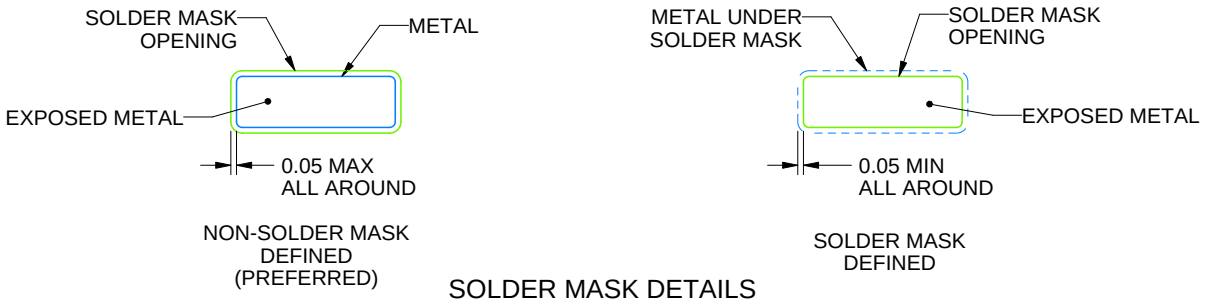

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

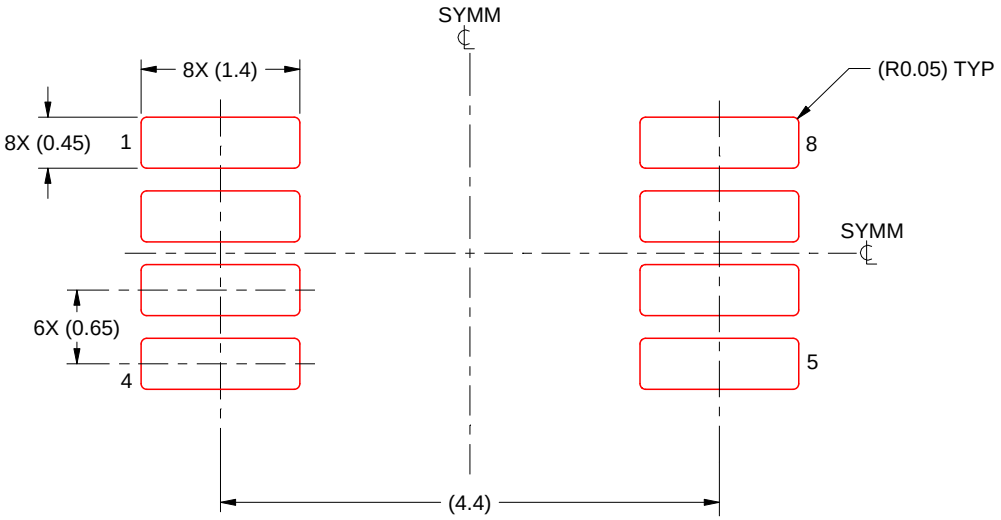



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

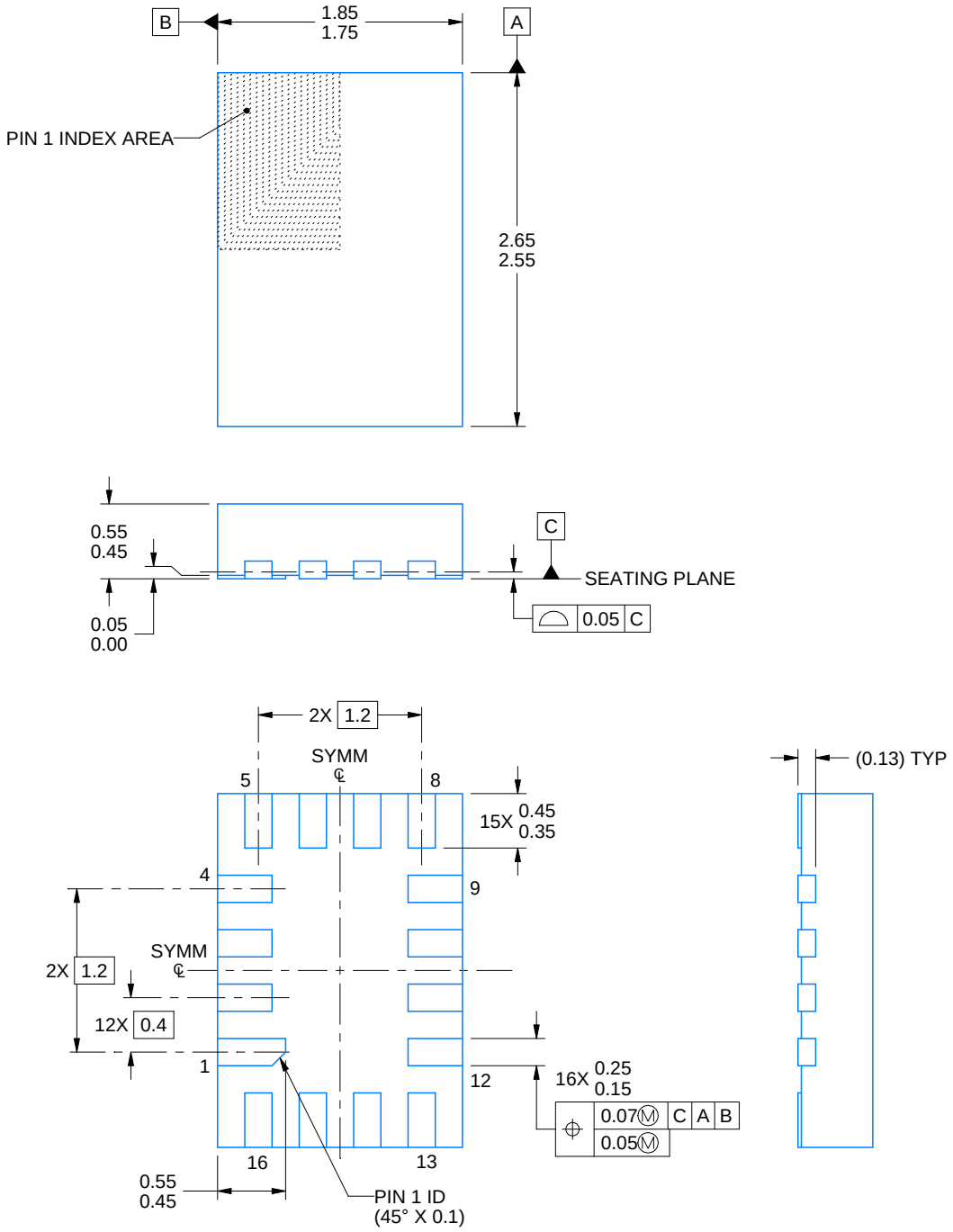
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# RSV0016A

# PACKAGE OUTLINE

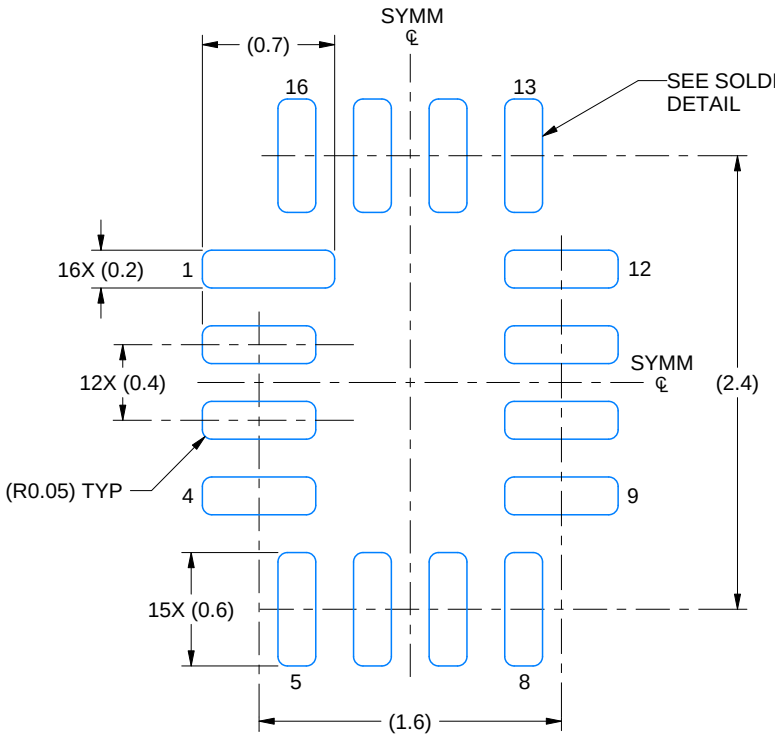
## UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

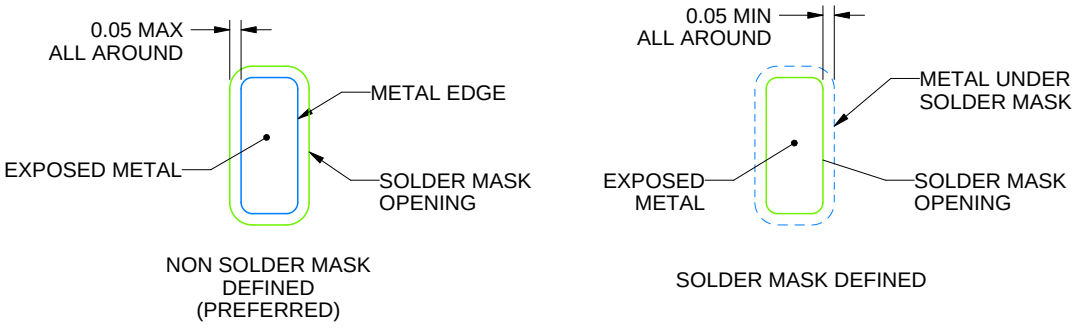



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

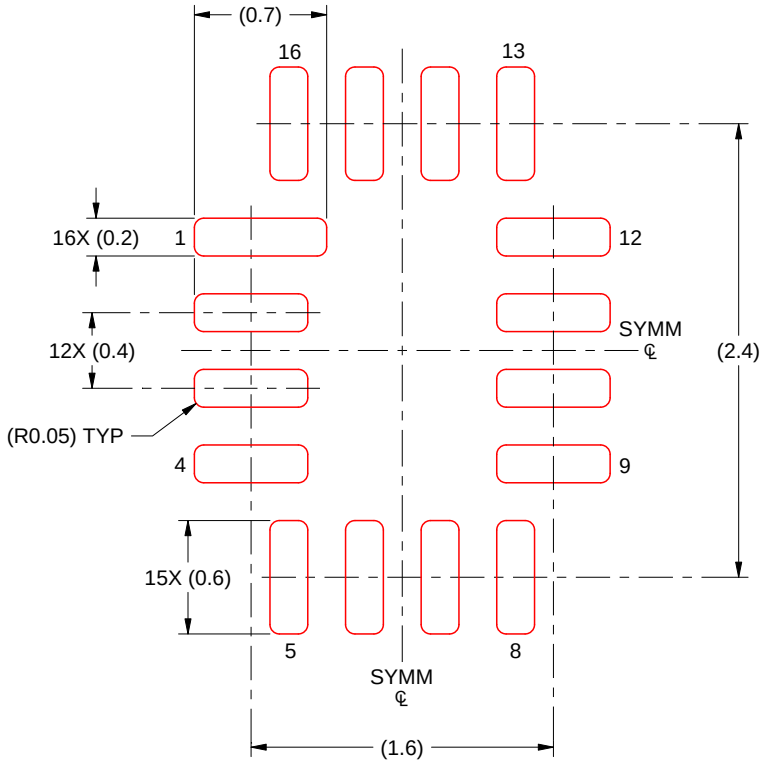



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

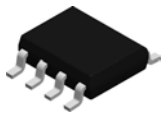



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

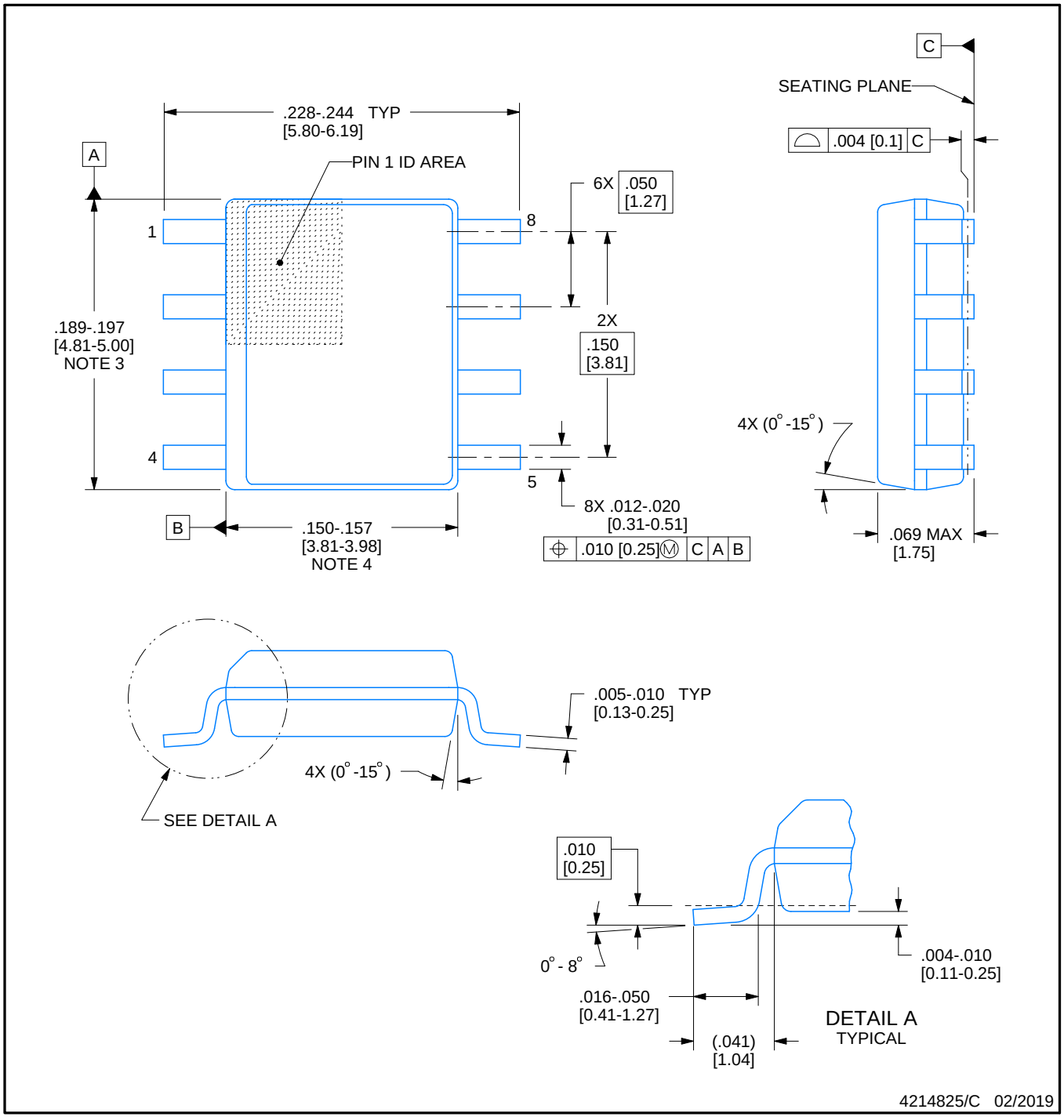


# PACKAGE OUTLINE

## D0008A

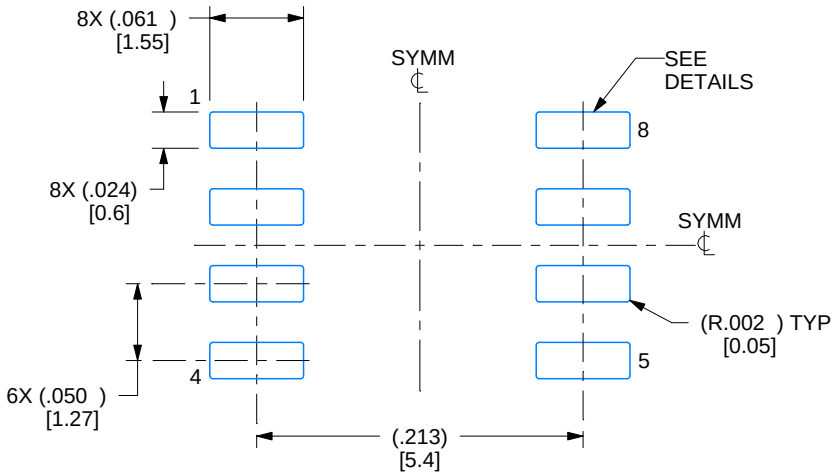
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

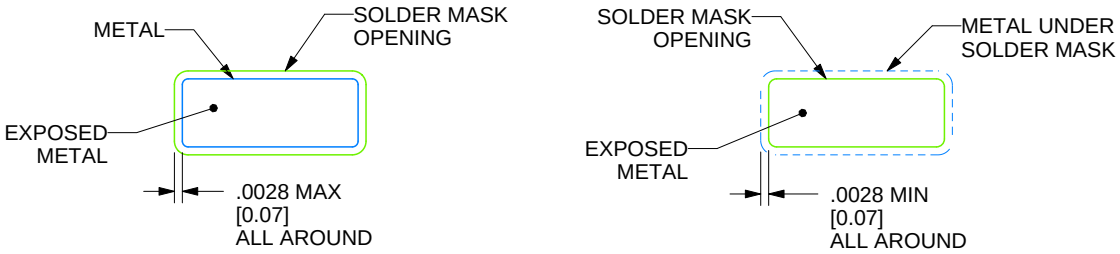



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

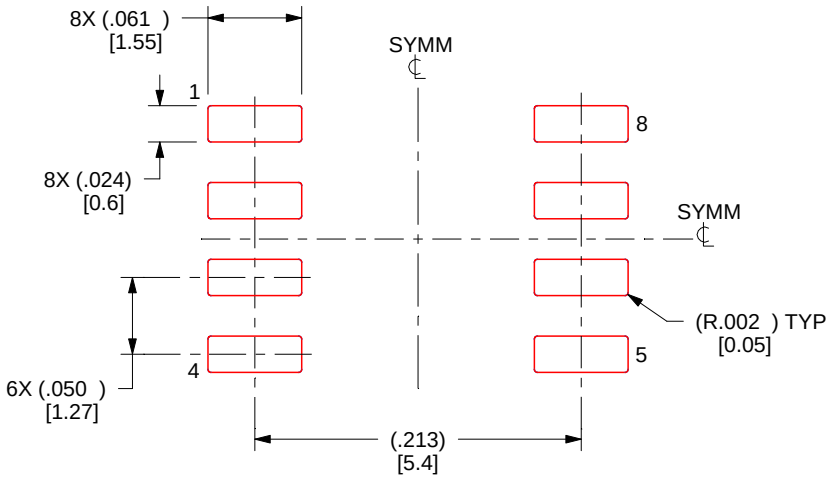
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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