TEXAS INSTRUMENTS
OPA377-Q1, OPA2377-Q1, OPA4377-Q1
JAJSC74A – MAY 2016 – REVISED MAY 2016

OPAx377-Q1 低ノイズ、低静止電流、高精度の車載用グレード・オペアンプ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～+125°C
  - デバイスHBM ESD分類レベル3A
  - デバイスCDM ESD分類レベルC6
- 低ノイズ: 7.5nV/√Hz 、 1kHz時
- 0.1Hz～10Hzのノイズ: 0.8μV_{PP}
- 静止電流: 760µA (標準値)
- 低いオフセット電圧: 250µV (標準値)
- ゲイン帯域幅積: 5.5MHz
- レール・ツー・レールの入出力
- 単一電源動作
- 電源電圧: 2.2V～5.5V
- 容積を削減できるパッケージ
  - SOT-23、VSSOP、TSSOP

2 アプリケーション

- アクティブ・クルーズ・コントロール
- パーク・アシスト
- タイヤ圧力の監視
- インフォテインメント
- アクティブ・フィルタリング
- センサ・シグナル・コンディショニング

3 概要

OPAx377-Q1ファミリのオペアンプは広い帯域幅をもつCMOSアンプです。0.76mA (標準値)の低静止電流で動作して、超低ノイズ、低入力バイアス電流、低オフセット電圧を実現します。

OPAx377-Q1オペアンプは低電圧の単一電源アプリケーション用に最適化されています。非常に優れたAC/DC性能のため、小信号のコンディショニング、オーディオ、アクティブ・フィルタなどの広範なアプリケーションにとって理想的なオペアンプとなっています。OPAx377-Q1オペアンプは電源範囲が広く、PSRRが非常に優れているため、バッテリから直接レギュレーションなしで動作するアプリケーションにとっても魅力的です。

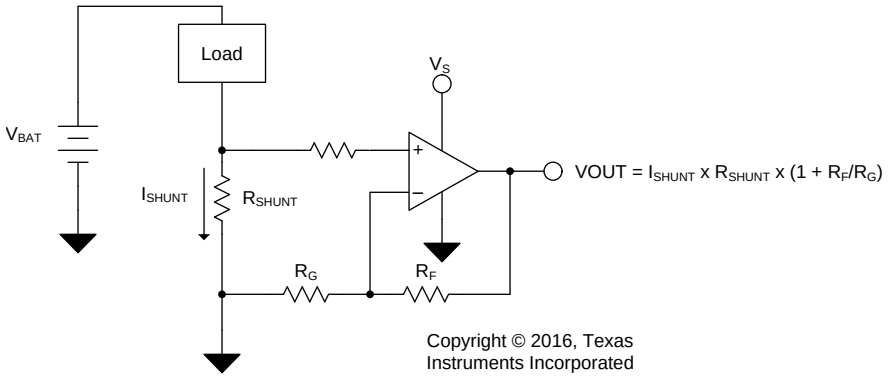
OPA377-Q1はSOT23-5パッケージで提供されます。デュアル・バージョンのOPA2377-Q1はMSOP-8パッケージ、クワッド・バージョンのOPA4377-Q1はTSSOP-14パッケージで提供されます。どのバージョンも、–40°C～+125°Cの動作が保証されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA377-Q1	SOT-23 (5)	2.90mm×1.60mm
OPA2377-Q1	VSSOP (8)	3.00mm×3.00mm
OPA4377-Q1	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ローサイドの電流感知アンプ



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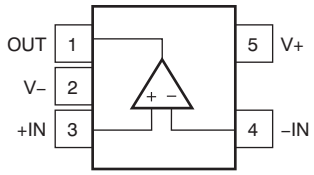
4 改訂履歴

2016年5月 発行のものから更新 **Page**

- 製品のステータスを*製品プレビュー*から*量産データ*へ変更 ... 1

5 Pin Configuration and Functions

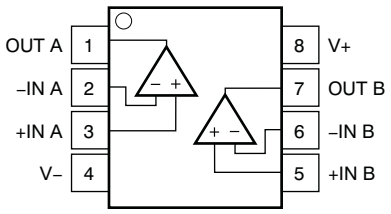
OPA377-Q1: DBV Package
5-Pin SOT23
Top View



Pin Functions: OPA377-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	DBV		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
NC	—	—	No internal connection (can be left floating)
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

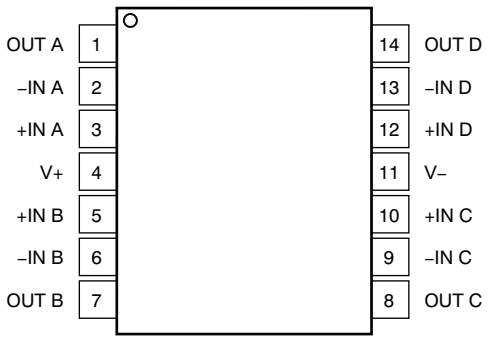
OPA2377-Q1: DGK Package
8-Pin VSSOP and SOIC
Top View



Pin Functions: OPA2377-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	DGK		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4377-Q1: PW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4377-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	PW		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage		7	V
	Signal input terminal voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Signal input terminal current(2)	–10	10	mA
	Output short-circuit current(3)		Continuous	
T_A	Operating temperature	–40	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Supply voltage	2.2	5.5	V
T_A	Operating temperature	–40	150	°C

6.4 Thermal Information: OPA377-Q1

THERMAL METRIC(1)		OPA377-Q1 DBV (SOT23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	273.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2377-Q1

THERMAL METRIC(1)		OPA2377-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information: OPA2377-Q1 (continued)

THERMAL METRIC(1)		OPA2377-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

6.6 Thermal Information: OPA4377-Q1

THERMAL METRIC(1)		OPA4377-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics: V_S = 2.2 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		0.25	1	mV
	Input offset voltage versus temperature	At T_A = –40°C to +125°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V+) – 1.3 V		5		µV/V
dV_{OS}/dT	Input offset voltage versus drift	At T_A = –40°C to +125°C		0.32	2	µV/°C
PSRR	Input offset voltage versus power supply	At T_A = 25°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V+) – 1.3 V		5	28	µV/V
	Channel separation, dc (dual, quad)			0.5		µV/V
INPUT BIAS CURRENT						
I_{IB}	Input bias current			±0.2	±10	pA
	Input bias current versus temperature			See *Typical Characteristics*		pA
I_{OS}	Input offset current			±0.2	±10	pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		0.8		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		7.5		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.3 V	70	90		dB
INPUT CAPACITANCE						
	Differential			6.5		pF
	Common-mode			13		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	50 mV < V_O < (V+) – 50 mV, R_L = 10 kΩ	112	134		dB
		100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ		126		dB
FREQUENCY RESPONSE, V_S = 5.5 V						

Electrical Characteristics: V_S = 2.2 V to 5.5 V (continued)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GBW	Gain-bandwidth product			5.5		MHz
SR	Slew rate	G = +1		2		V/µs
t_S	Settling time	At 0.1%, 2-V step, G = +1		1.6		µs
		At 0.01%, 2-V step, G = +1		2		µs
	Overload recovery time	V_{IN} × Gain > V_S		0.33		µs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 10 kΩ		0.00027%		
OUTPUT						
	Voltage output swing from rail	At T_A = 25°C, R_L = 10 kΩ		10	20	mV
		At T_A = –40°C to +125°C, R_L = 10 kΩ			40	mV
I_{SC}	Short-circuit current			+30/–50		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		
R_O	Open-loop output impedance			150		Ω
POWER SUPPLY						
V_S	Specified voltage		2.2		5.5	V
I_Q	Quiescent current (per amplifier)	At T_A = 25°C, I_O = 0, V_S = 5.5 V		0.76	1.05	mA
		At T_A = –40°C to +125°C			1.2	mA
TEMPERATURE						
	Specified temperature		–40		+125	°C

6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

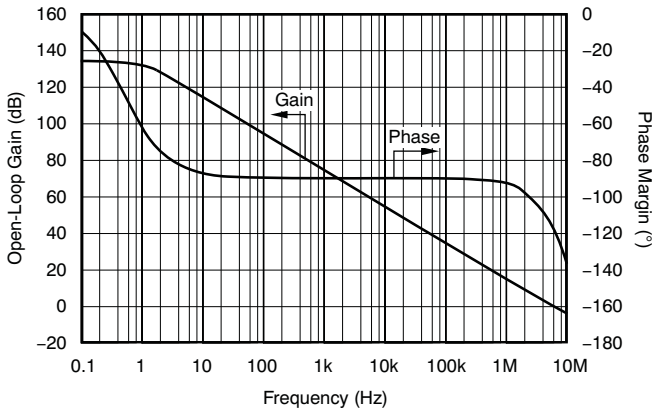


Figure 1. Open-Loop Gain and Phase vs Frequency

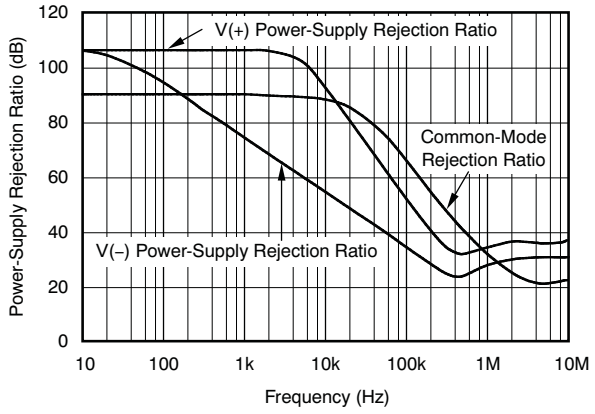


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

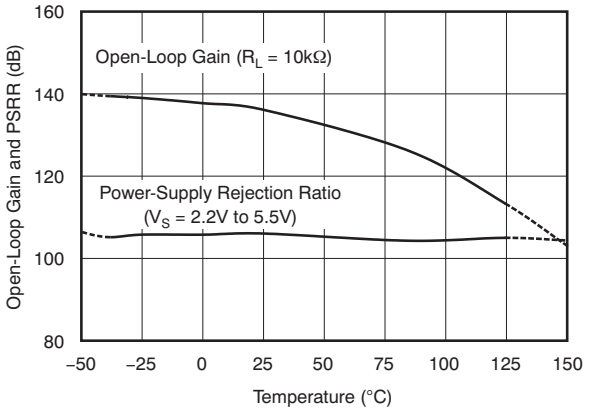


Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

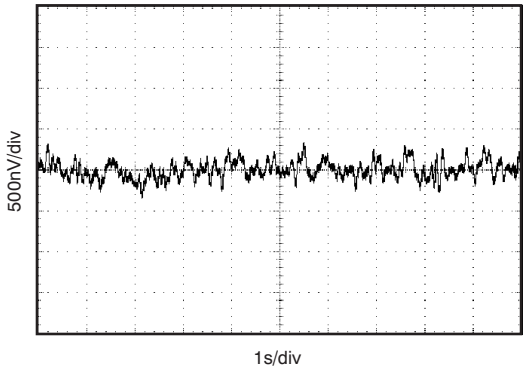


Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise

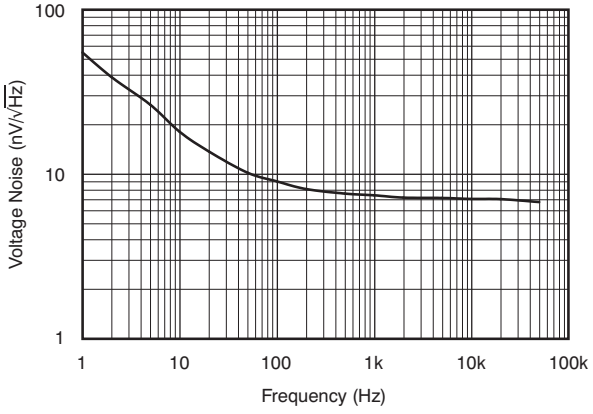


Figure 5. Input Voltage Noise Spectral Density

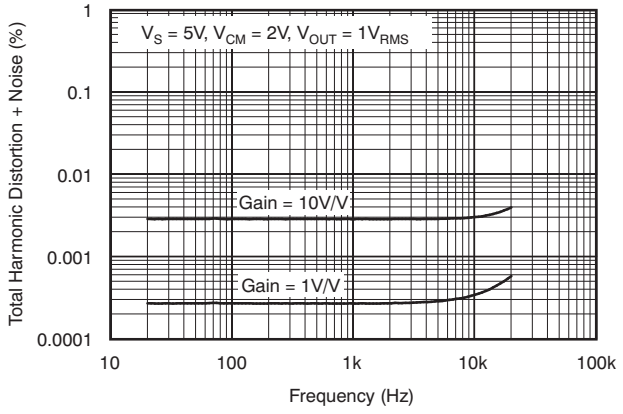


Figure 6. Total Harmonic Distortion and Noise vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

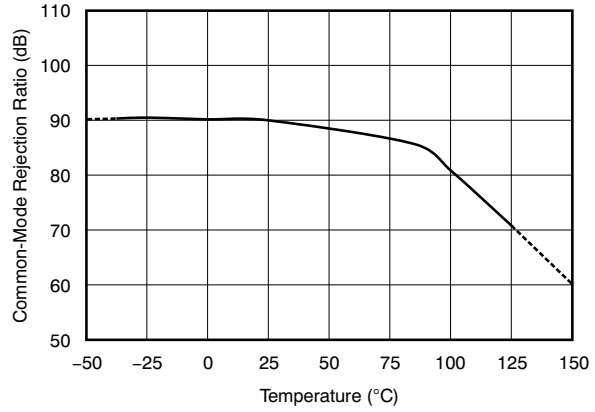


Figure 7. Common-Mode Rejection Ratio vs Temperature

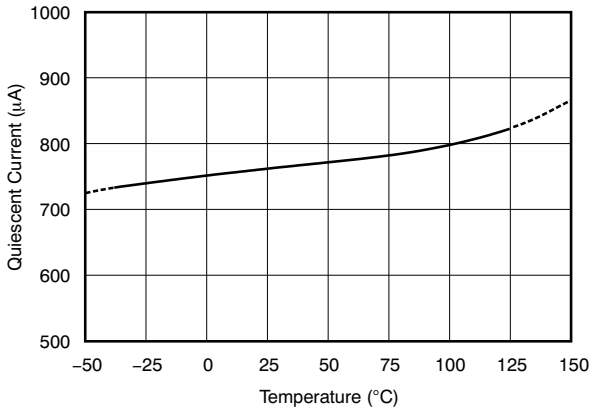


Figure 8. Quiescent Current vs Temperature

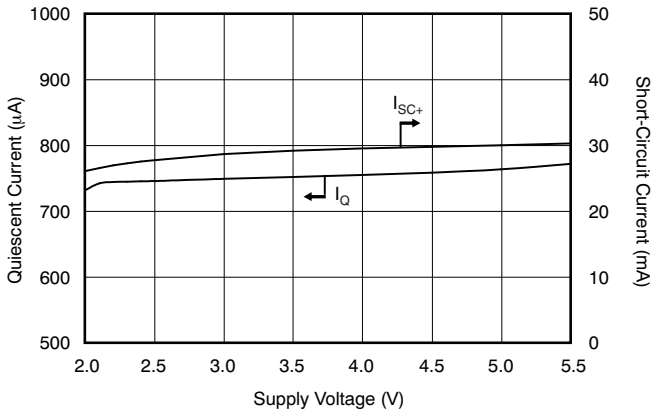


Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage

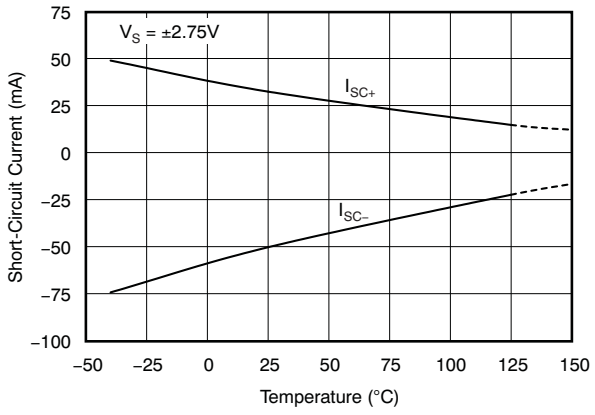


Figure 10. Short-Circuit Current vs Temperature

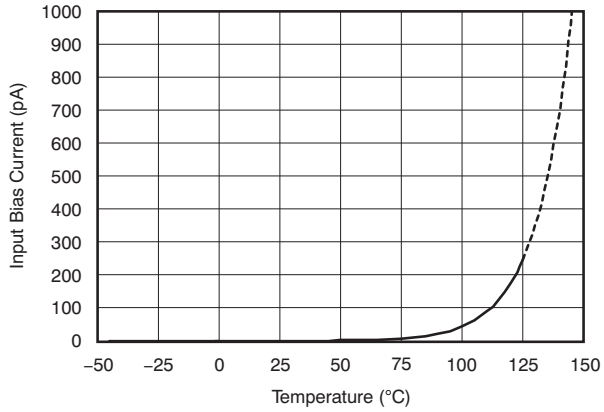


Figure 11. Input Bias Current vs Temperature

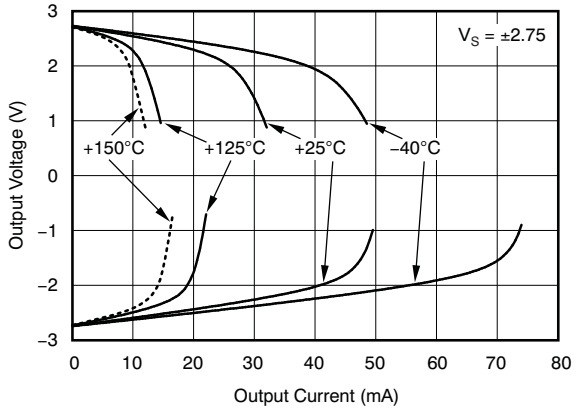


Figure 12. Output Voltage vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

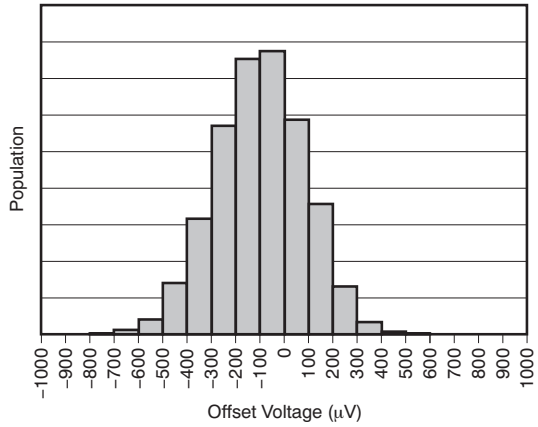


Figure 13. Offset Voltage Production Distribution

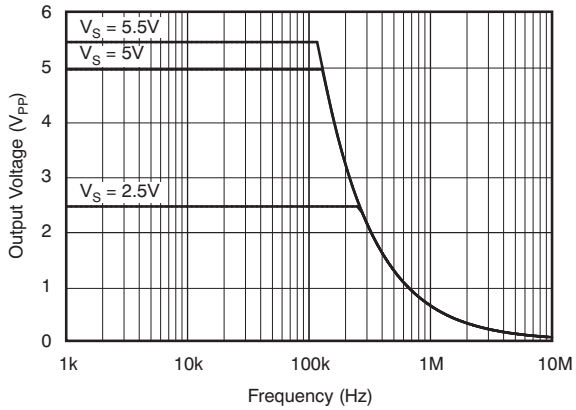


Figure 14. Maximum Output Voltage vs Frequency

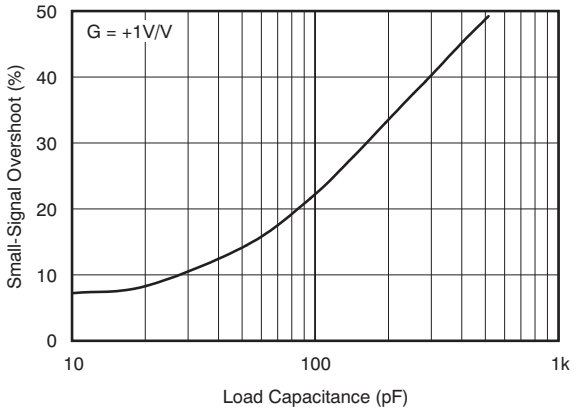


Figure 15. Small-Signal Overshoot vs Load Capacitance

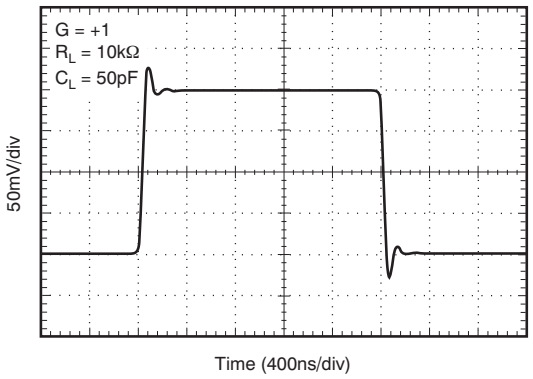


Figure 16. Small-Signal Pulse Response

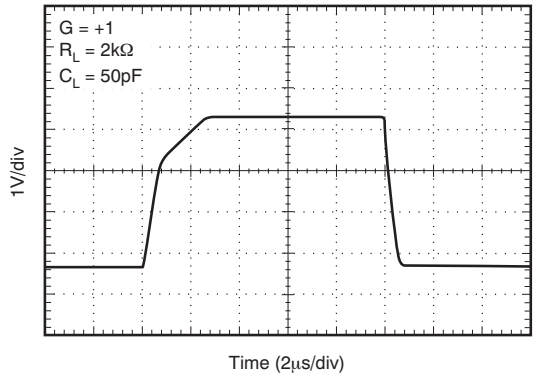


Figure 17. Large-Signal Pulse Response

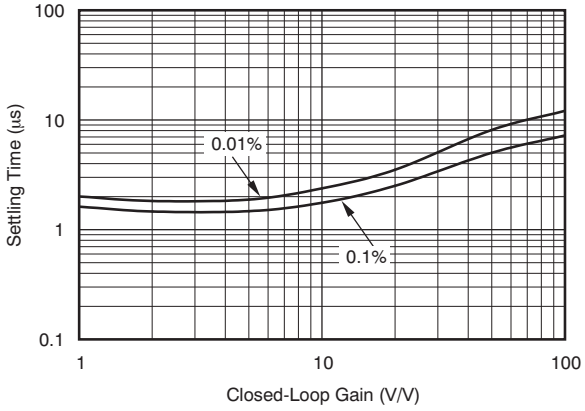


Figure 18. Settling Time vs Closed-Loop Gain

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

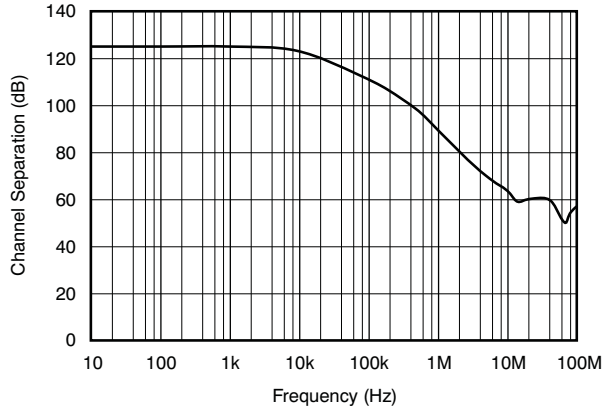


Figure 19. Channel Separation vs Frequency

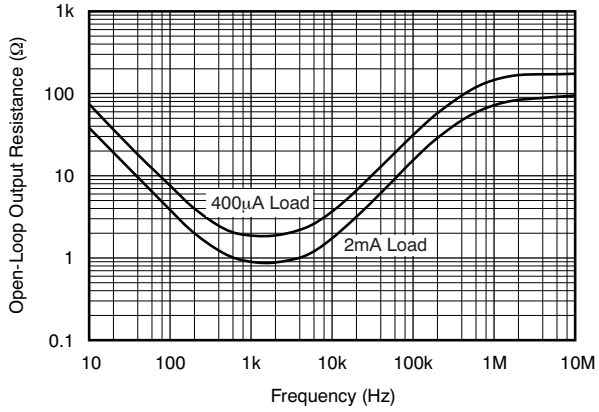


Figure 20. Open-Loop Output Resistance vs Frequency

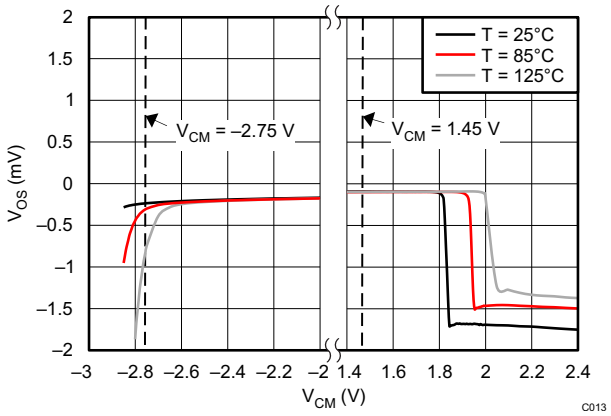


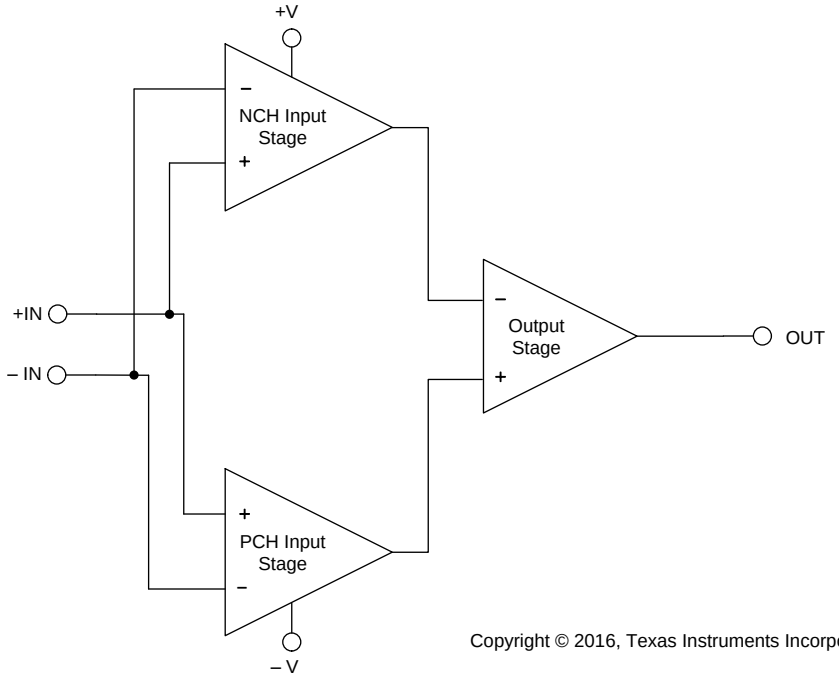
Figure 21. Input Offset Voltage vs Common-Mode Voltage

7 Detailed Description

7.1 Overview

The OPAx377-Q1 family belongs to a new generation of low-noise operational amplifiers, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery-powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx377-Q1 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx377-Q1 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is low, from approximately (V–) to (V+) – 1 V, as shown in Figure 22. The offset voltage increases as common-mode voltage exceeds (V+) – 1 V. Common-mode rejection is specified from (V–) to (V+) – 1.3 V.

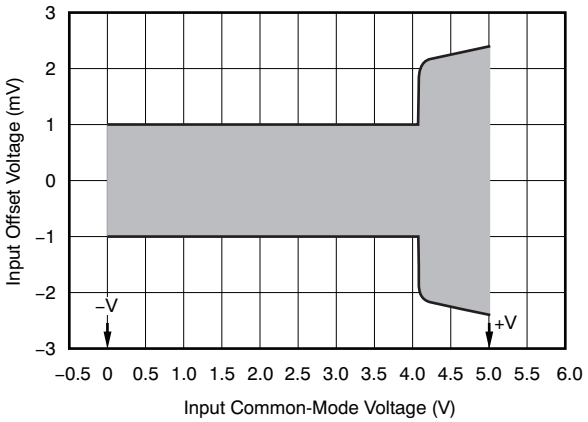


Figure 22. Offset and Common-Mode Voltage

7.3.3 Input and ESD Protection

The OPAx377-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table.

Figure 23 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.

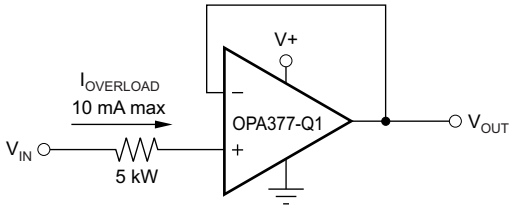


Figure 23. Input Current Protection

Feature Description (continued)

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from the nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx377-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 75 MHz (–3 dB), with a roll-off of 20 dB per decade.

7.3.5 Capacitive Load and Stability

The OPAx377-Q1 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx377-Q1 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

The OPAx377-Q1 in a unity-gain configuration can directly drive up to 250-pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot, Figure 15. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 24. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L, and is generally negligible at low output current levels.

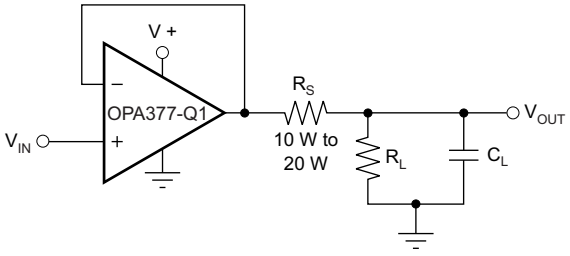


Figure 24. Improving Capacitive Load Drive

7.4 Device Functional Modes

The OPAx377-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPAx376-Q1 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx377-Q1 family of operational amplifiers is built on a precision analog CMOS technology featuring low noise and low offset voltage. The OPAx377-Q1 family delivers excellent offset voltage (250 μV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. These 5.5-MHz CMOS op amps operate on 760 μA (typical) quiescent current.

8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA377-Q1 is ideally suited to construct high-speed, high-precision active filters. Figure 25 shows a second-order, low-pass filter commonly encountered in signal processing applications.

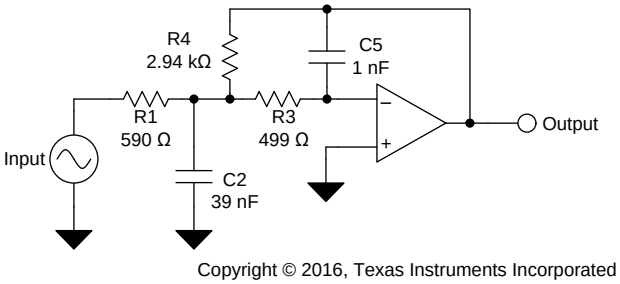


Figure 25. Typical Application Schematic

8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 25. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Typical Application (continued)

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

8.2.3 Application Curve

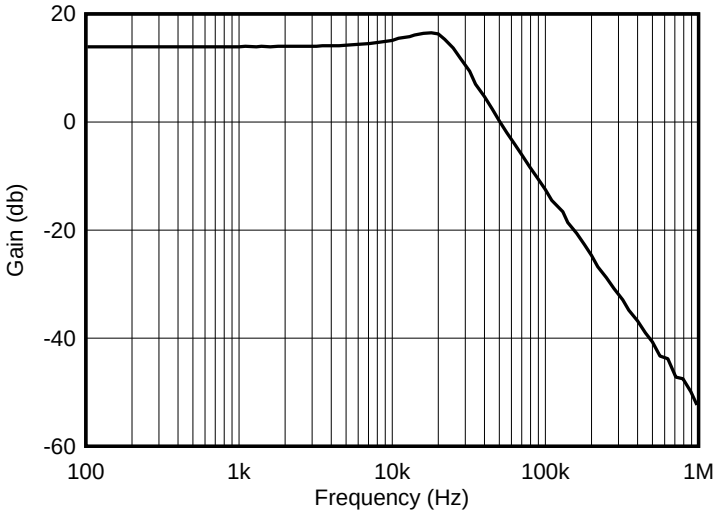


Figure 26. Low-Pass Filter Transfer Function

9 Power Supply Recommendations

The OPAx377-Q1 family of devices is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to the application report, *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 28, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

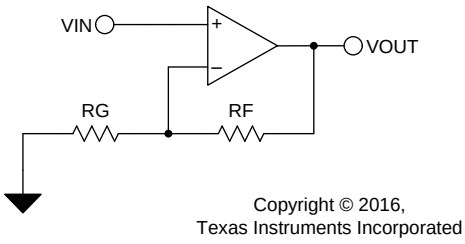


Figure 27. Typical Schematic for PCB Layout Example

Layout Example (continued)

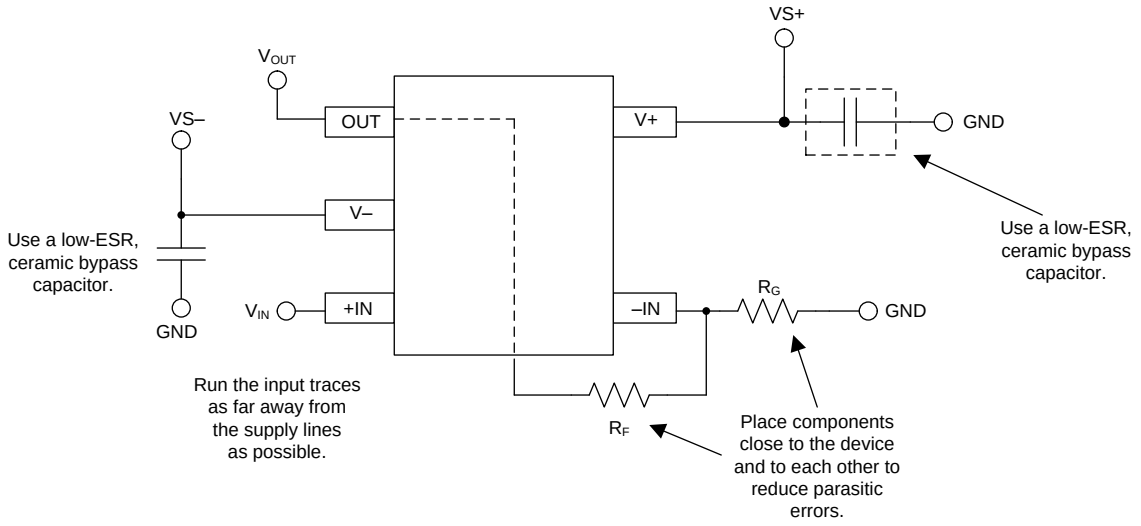


Figure 28. Typical PCB Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。 TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには従来型のDC、トランジェント、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINAソフトウェア(DesignSoft™製)またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

11.1.1.2 DIPアダプタ評価モジュール

DIPアダプタ評価モジュールツールを使用すると、小さな表面実装ICのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU(SOIC-8)、PW(TSSOP-8)、DGK(MSOP-8)、DBV(SOT23-6、SOT23-5、およびSOT23-3)、DCK(SC70-6およびSC70-5)、およびDRL(SOT563-6)のTIパッケージに対応しています。DIPアダプタ評価モジュールは、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

11.1.1.3 ユニバーサル・オペアンプ評価モジュール

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のICパッケージ・タイプ向けの回路のプロトタイプ作成を容易にします。評価モジュール基板の設計により、多くの異なる回路を簡単かつ迅速に構築できます。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、およびSOT23のパッケージがすべてサポートされています。

注

これらの基板には部品が搭載されていないため、ユーザーが独自のICを供給する必要があります。ユニバーサル・オペアンプ評価モジュールを注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

11.1.1.4 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

11.1.1.5 WEBENCH®Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下をを参照してください:

- *『基板のレイアウト技法』*、SLOA089
- *『オペアンプのゲイン安定性、第3部: ACゲイン誤差の解析』*、SLYT383
- *『オペアンプのゲイン安定性、第2部: DCゲイン誤差の解析』*、SLYT374
- *『オペアンプのパフォーマンス解析』*、SBOS054
- *『鉛フリー仕上げ部品の保管寿命評価』*、SZZA046
- *『オペアンプの単一電源動作』*、SBOA059
- *『アンプのチューニング』*、SBOA067
- *『完全差動アクティブ・フィルタにおける無限ゲイン、MFBフィルタ・トポロジの使用』*、SLYT343

11.3 コミュニティ・リソース

以下のリンクから、TIのコミュニティ・リソースにアクセスできます。リンクされているコンテンツは、投稿者のコンテンツがそのまま掲載されたものです。TIがこの内容を保証するものではなく、また必ずしもTIの見解が反映されたものではありません。TIの使用条件を参照してください。

"TI E2E™オンライン・コミュニティ" — ***TIのE2E（Engineer-to-Engineer）*** コミュニティ。エンジニア間の情報共有をサポートする目的で作成されたものです。e2e.ti.comで質問し、知識を共有し、アイディアを検討するなど、技術的な問題を解決するためのコミュニティ・サイトです。

"設計サポート" — ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.6 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2377QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2377	Samples
OPA377QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	377Q	Samples
OPA4377AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4377Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

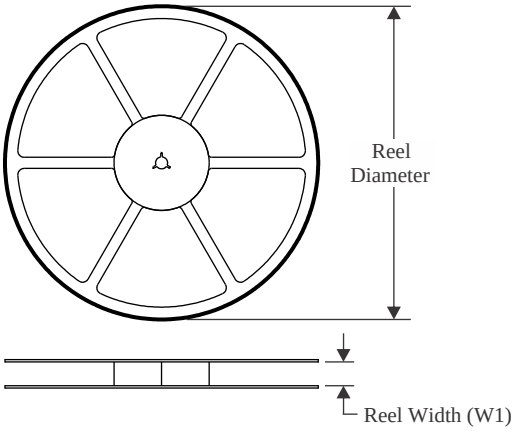
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

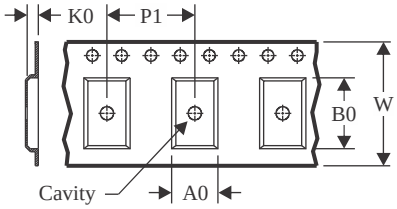
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

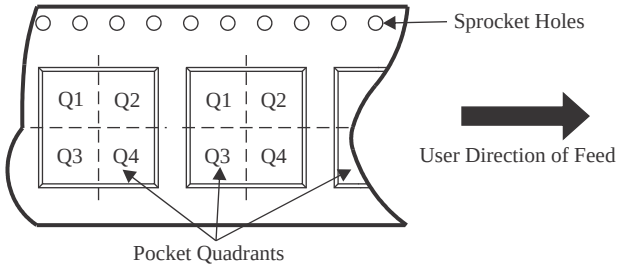


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

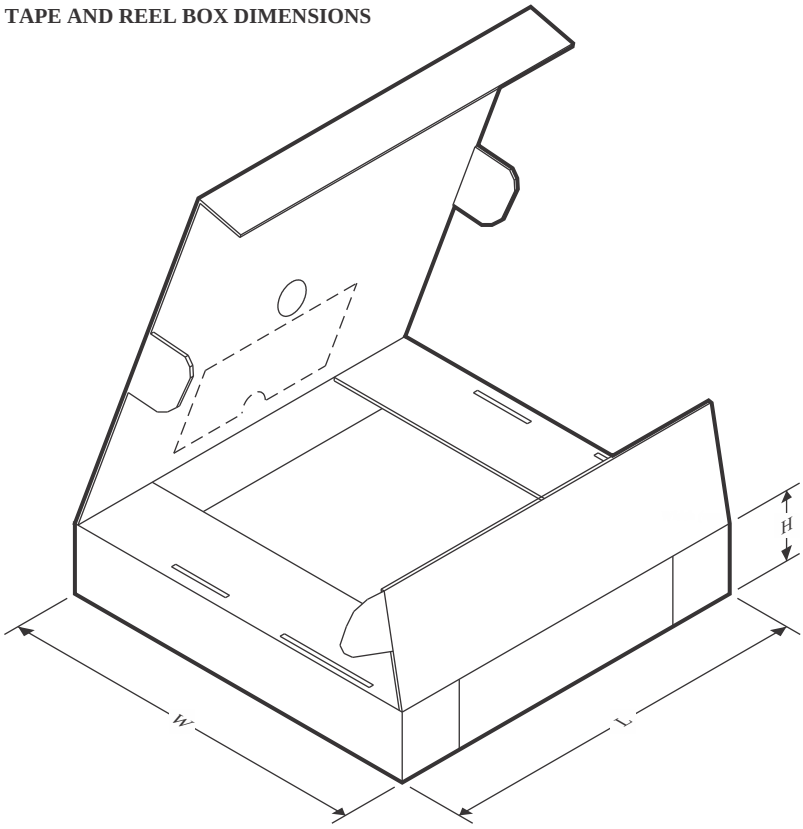
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2377QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA377QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA4377AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

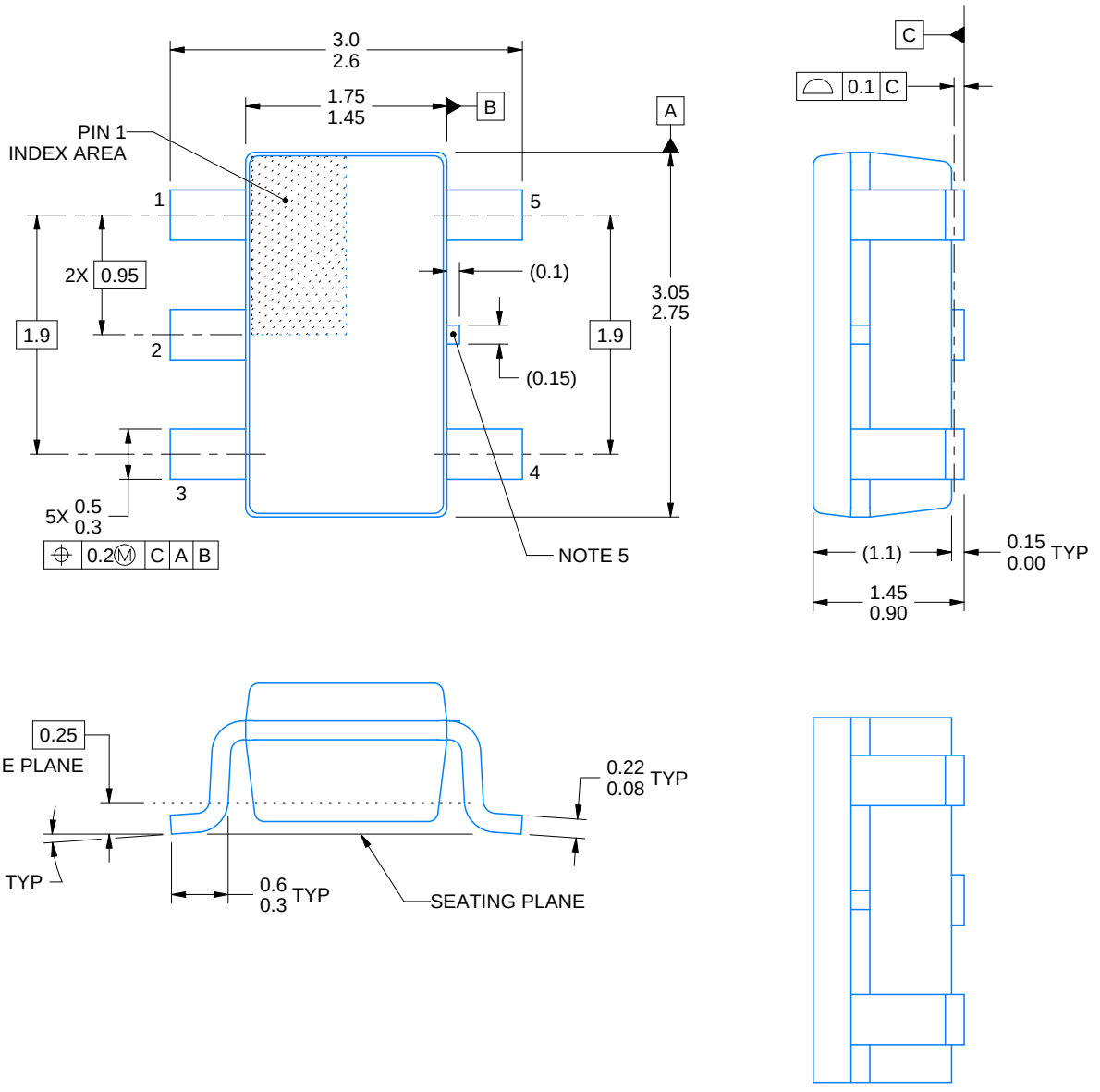
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2377QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA377QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA4377AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

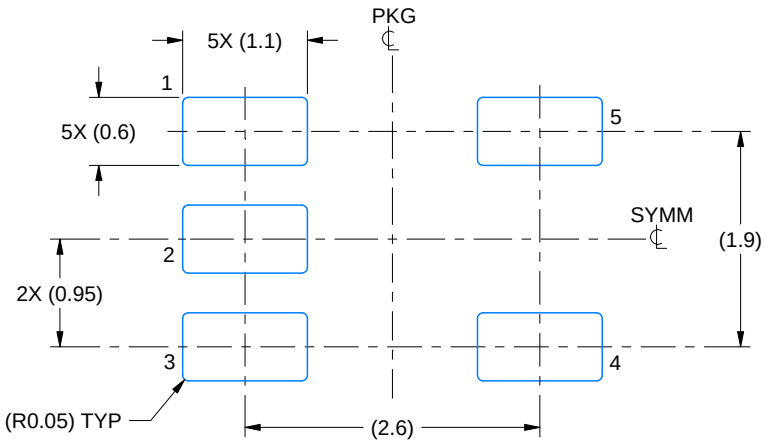


ALTERNATIVE PACKAGE SINGULATION VIEW

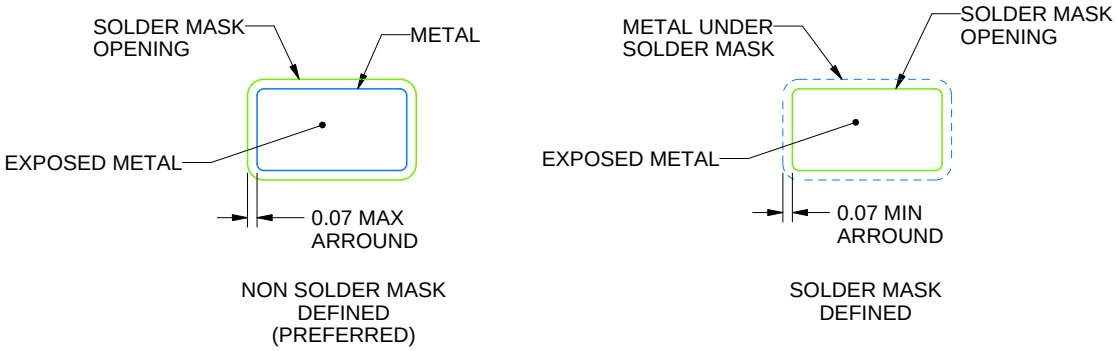
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

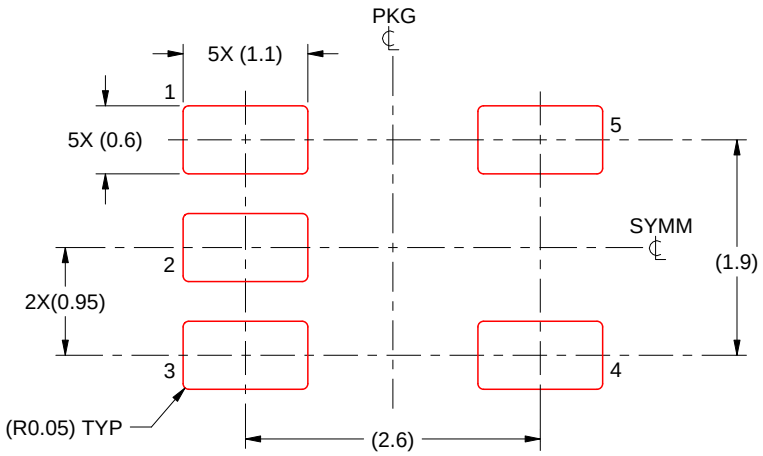


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



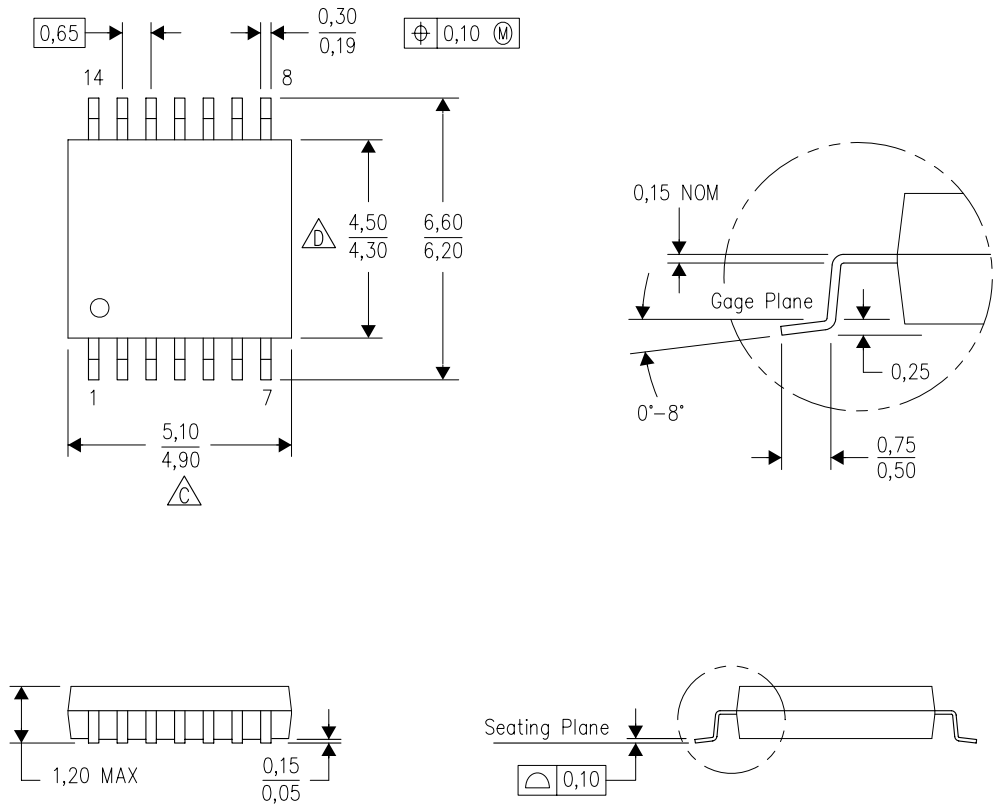
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

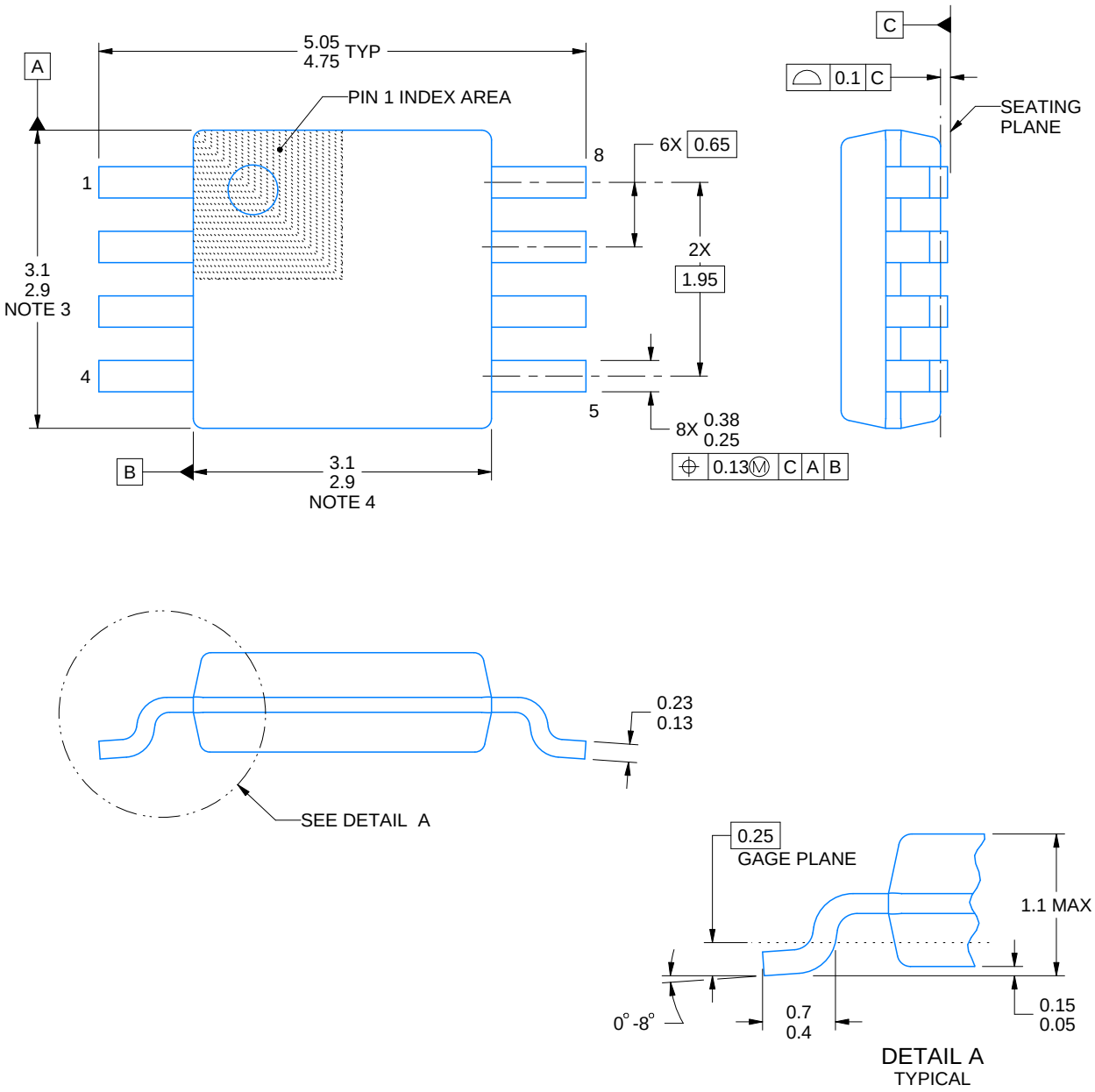
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

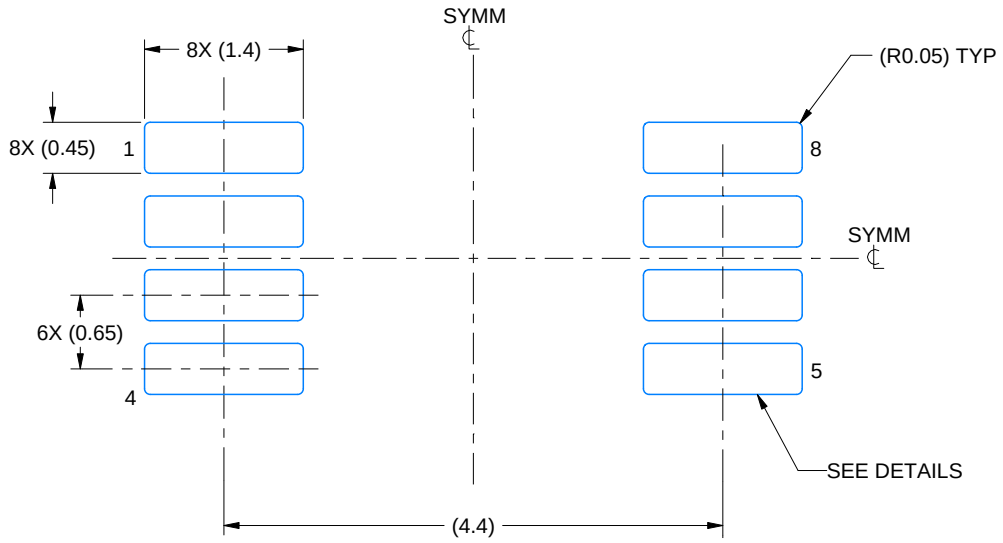
SMALL OUTLINE PACKAGE



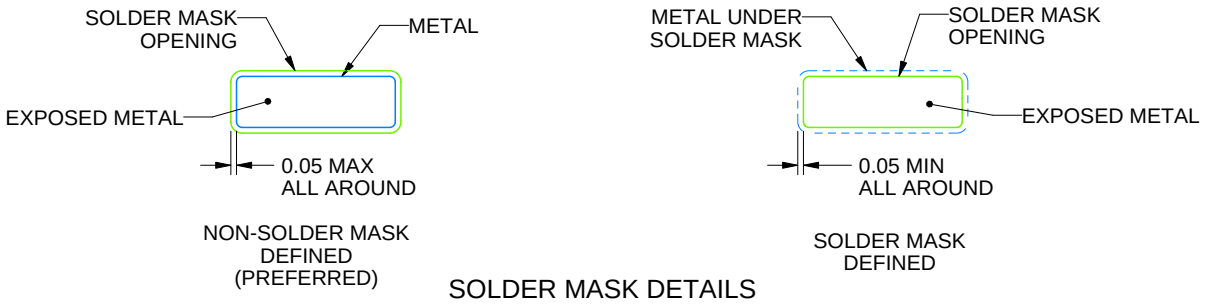
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

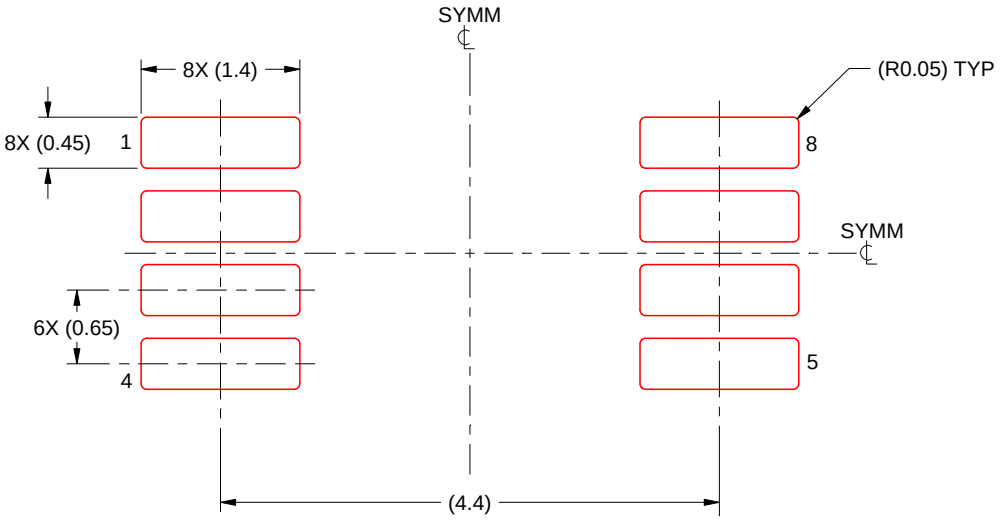


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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