OPAx365 50MHz、ゼロ・クロスオーバー、低歪み、高 CMRR、RRI/O、単一電源オペアンプ

1 特長

- ゲイン帯域幅:50MHz
- ゼロ・クロスオーバー歪みトポロジ:
  - 優れた THD+N:0.0004%
  - CMRR:100dB (最小値)
  - レール・ツー・レール入出力
    - 電源レールを 100mV 超える入力
- 低ノイズ:100kHz 時に 4.5nV/√Hz
- スルーレート:25V/µs
- 高速セトリング:0.3µs で 0.01%
- 精度:
  - 低オフセット:100µV
  - 低い入力バイアス電流:0.2pA
- 2.2V～5.5V で動作

2 アプリケーション

- シグナル・コンディショニング
- データ・アクイジション
- プロセス制御
- アクティブ・フィルタ
- 試験用機器
- オーディオ
- 広帯域アンプ

3 概要

OPA365 および OPA2365 (OPAx365) は、ゼロ・クロスオーバー・シリーズのレール・ツー・レール、高性能、CMOS オペアンプであり、非常に低電圧の単一電源アプリケーション用に最適化されています。レール・ツー・レール入出力、低ノイズ (4.5nV/√Hz)、高速動作 (50MHz のゲイン帯域幅) から、これらのデバイスはサンプリング A/D コンバータ (ADC) を駆動するために理想的です。アプリケーションとしては、オーディオ、信号コンディショニング、センサ・アンプなどが挙げられます。

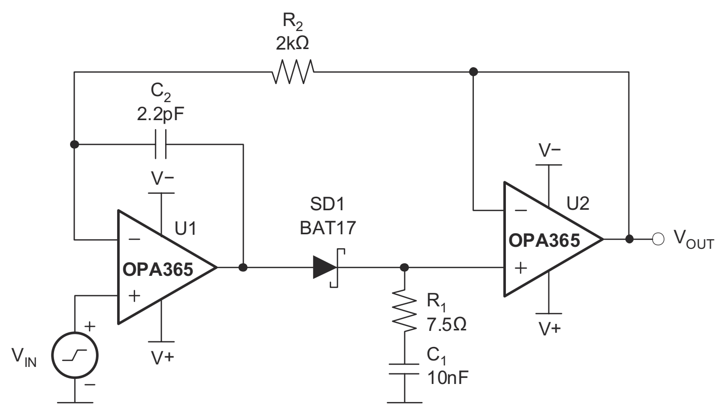
特別な長所として、同相除去率 (CMRR) が非常に優れていること、入力ステージにクロスオーバー歪みがないこと、入力インピーダンスが高いこと、レール・ツー・レール入出力のスイングが挙げられます。入力同相範囲には、負と正の電源の両方が含まれています。出力電圧のスイングは、レールから 10mV の範囲内です。

OPA365 (シングル・バージョン) は超小型 SOT23-5 (SOT-5) および SOIC-8 パッケージで供給されます。OPA2365 (デュアル・バージョン) は、SOIC-8 パッケージで供給されます。すべてのバージョンは、-40℃～+125℃での動作が規定されています。シングル・バージョンとデュアル・バージョンは同じ仕様で、設計の柔軟性を最大限に高めます。

製品情報

部品番号	チャネル数	パッケージ (1)
OPA365	シングル	D (SOIC、8)
		DBV (SOT-23、5)
OPA2365	デュアル	D (SOIC、8)

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



高速セトリング・ピーク検出器

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (April 2020) to Revision G (May 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Added new row for TLVx365 in *Device Comparison Table*	3

Changes from Revision E (August 2016) to Revision F (April 2020)	Page
• Added *Device Comparison Table*	3

Changes from Revision D (June 2009) to Revision E (August 2016)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• 「概要」セクションの最後の段落に現在のパッケージ指定子を追加	1

5 Device Comparison Table

DEVICE	INPUT TYPE	OFFSET DRIFT, TYPICAL (µV/ºC)	MINIMUM GAIN STABLE	I_Q/CHANNEL, TYPICAL (mA)	GAIN BANDWIDTH (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/$\sqrt{Hz}$)
OPAx365	CMOS	1	1 V/V	4.6	50	25	4.5
TLVx365	CMOS	0.4	1 V/V	4.6	50	27	4.5
OPAx607	CMOS	0.3	6 V/V	0.9	50	24	3.8
OPAx837	Bipolar	0.4	1 V/V	0.6	50	105	4.7

6 Pin Configuration and Functions

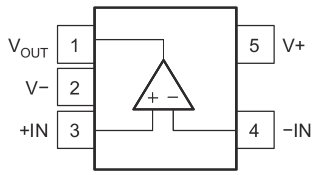
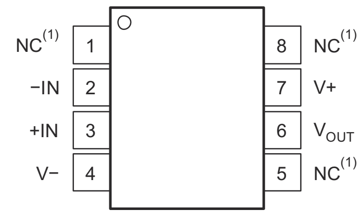


図 6-1. OPA365: DBV Package, 5-Pin SOT-23 (Top View)



(1) NC denotes no internal connection.

図 6-2. OPA365: D Package, 8-Pin SOIC (Top View)

Pin Functions: OPA365

PIN			TYPE	DESCRIPTION
NAME	SOIC	SOT		
–IN	2	4	Input	Negative (inverting) input
+IN	3	3	Input	Positive (noninverting) input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply
V_{OUT}	6	1	Output	Output

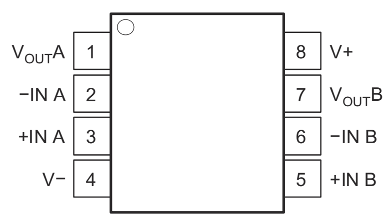


図 6-3. OPA2365: D Package, 8-Pin SOIC (Top View)

Pin Functions: OPA2365

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Negative (inverting) input signal, channel A
+IN A	3	Input	Positive (noninverting) input signal, channel A
–IN B	6	Input	Negative (inverting) input signal, channel B
+IN B	5	Input	Positive (noninverting) input signal, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply
$V_{OUT}A$	1	Output	Output, channel A
$V_{OUT}B$	7	Output	Output, channel B

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).[(1)]

		MIN	MAX	UNIT
Voltage	Supply voltage		5.5	V
	Signal input terminals, voltage[(2)]	–0.5	0.5	V
Current	Signal input terminals, current[(2)]	–10	10	mA
	Output short-circuit[(3)]	Continuous		
Temperature	Operating, T_A	–40	150	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	
		Machine model	±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

	MIN	NOM	MAX	UNIT
Power supply voltage, (V+) – (V–)	2.2		5.5	V
Specified temperature	−40		+125	°C
Operating temperature	−40		+150	°C

7.4 Thermal Information: OPA365

THERMAL METRIC[(1)]		OPA365		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.9	140.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.4	89.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.2	80.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	28.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.9	80.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2365

THERMAL METRIC[1]		OPA2365 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				100	200	µV
dV_{OS}/dT	Input offset voltage versus drift		At T_A = −40°C to +125°C		1		µV/°C
PSRR	Input offset voltage versus power supply		V_S = 2.2 V to 5.5 V, at T_A = −40°C to +125°C		10		µV/V
	Channel separation, DC				0.2		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±10	pA
		Over temperature	At T_A = −40°C to +125°C	See セクション 7.7			
I_{OS}	Input offset current				±0.2	±10	pA
NOISE							
e_n	Input voltage noise		f = 0.1 Hz to 10 Hz		5		$µV_{PP}$
e_n	Input voltage noise density		f = 100 kHz		4.5		nV/√Hz
i_n	Input current noise density		f = 10 kHz		4		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio		(V−) − 0.1 V ≤ V_{CM} ≤ (V+) + 0.1 V, at T_A = −40°C to +125°C	100	120		dB
INPUT CAPACITANCE							
	Differential				6		pF
	Common-mode				2		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		R_L = 10 kΩ, 100 mV < V_O < (V+) – 100 mV, at T_A = −40°C to +125°C	100	120		dB
			R_L = 600 Ω, 200 mV < V_O < (V+) – 200 mV	100	120		dB
			R_L = 600 Ω, 200 mV < V_O < (V+) – 200 mV, at T_A = −40°C to +125°C	94			dB

7.6 Electrical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		V_S = 5 V		50		MHz
SR	Slew rate		V_S = 5 V, G = 1		25		V/µs
t_S	Settling time	0.1%	V_S = 5 V, 4-V step, G = +1		200		ns
		0.01%	V_S = 5 V, 4-V step, G = +1		300		
	Overload recovery time		V_S = 5 V, V_{IN} × Gain > V_S		< 0.1		µs
THD+N	Total harmonic distortion + noise[(1)]		V_S = 5 V, R_L = 600 Ω, V_O = 4 V_{PP}, G = 1, f = 1 kHz		0.0004%		
OUTPUT							
	Voltage output swing from rail		R_L = 10 kΩ, V_S = 5.5 V, at T_A = −40°C to +125°C		10	20	mV
I_{SC}	Short-circuit current				±65		mA
C_L	Capacitive load drive				See セクション 7.7		
	Open-loop output impedance		f = 1 MHz, I_O = 0 mA		30		Ω
POWER SUPPLY							
V_S	Specified voltage range			2.2		5.5	V
I_Q	Quiescent current per amplifier		I_O = 0 mA		4.6	5	mA
		Over temperature	At T_A = −40°C to +125°C			5	

(1) 3rd-order filter; bandwidth 80 kHz at −3 dB.

7.7 Typical Characteristics

at T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

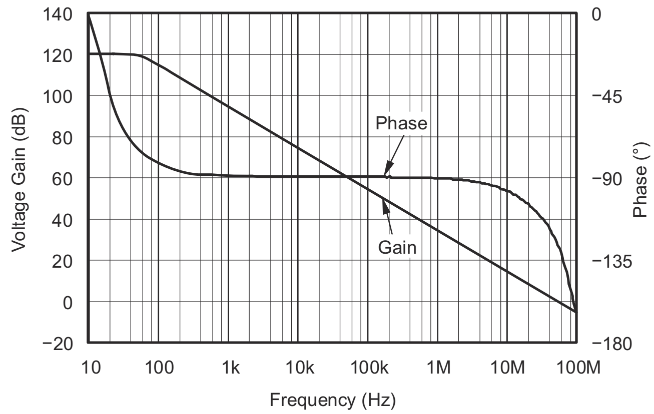


図 7-1. Open-Loop Gain and Phase vs Frequency

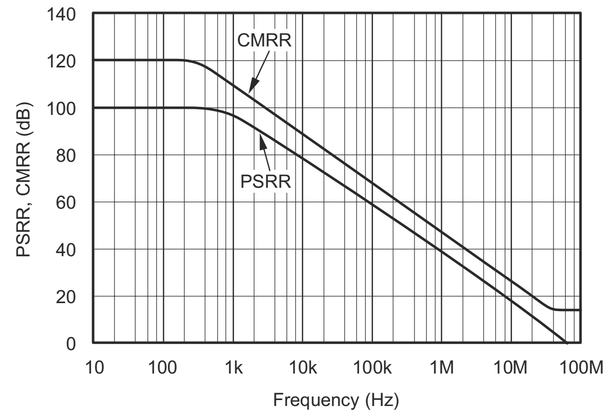


図 7-2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

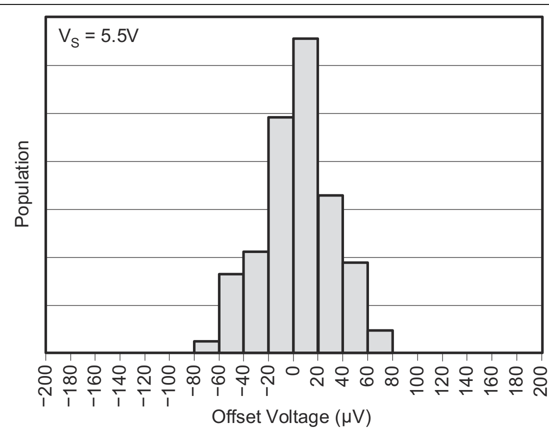


図 7-3. Offset Voltage Production Distribution

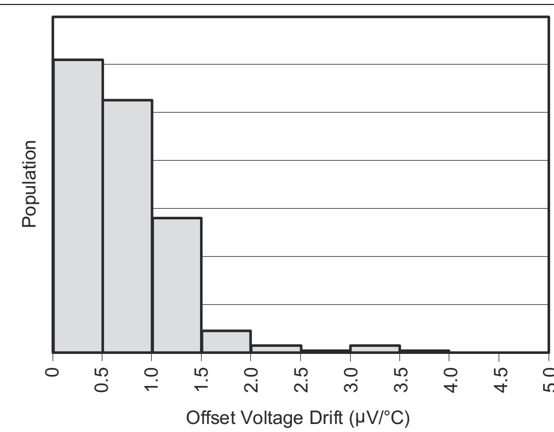


図 7-4. Offset Voltage Drift Production Distribution

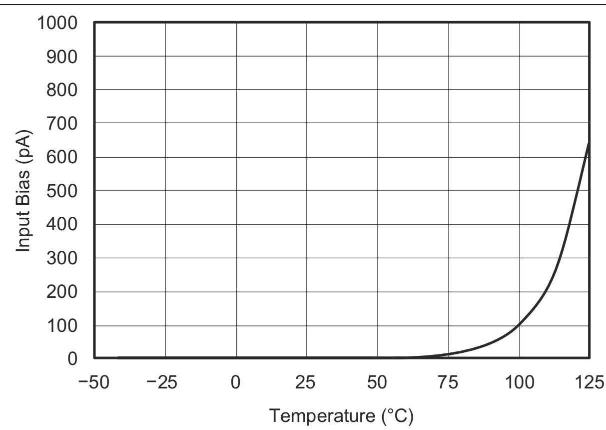


図 7-5. Input Bias Current vs Temperature

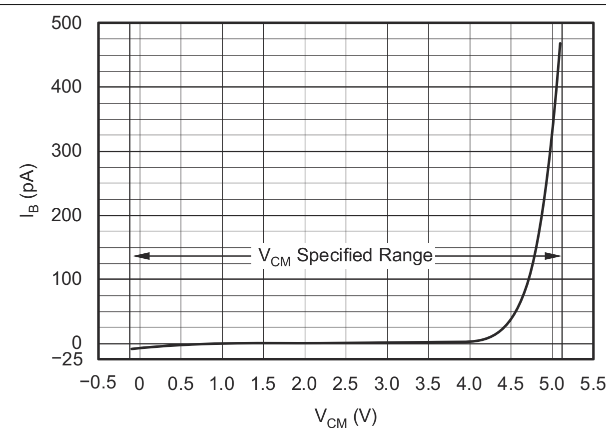


図 7-6. Input Bias Current vs Common-Mode Voltage

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

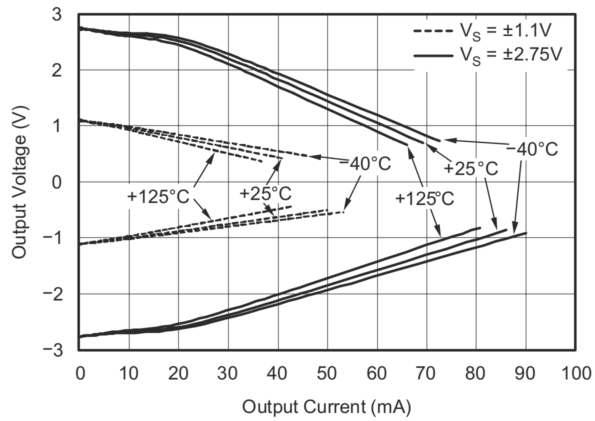


図 7-7. OPA365 Output Voltage vs Output Current

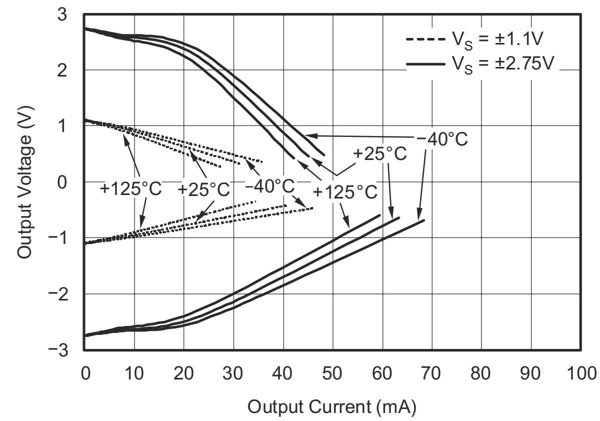


図 7-8. OPA2365 Output Voltage vs Output Current

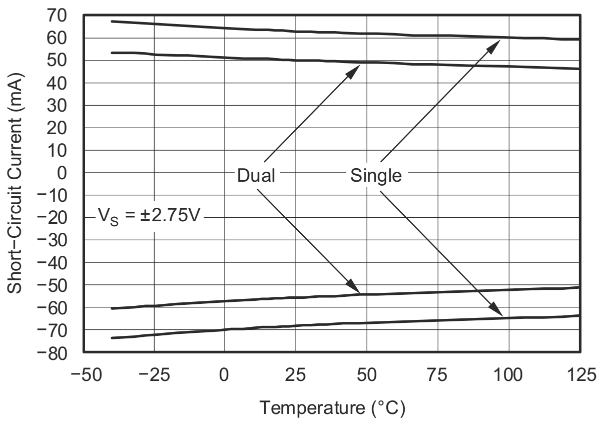


図 7-9. Short-Circuit Current vs Temperature

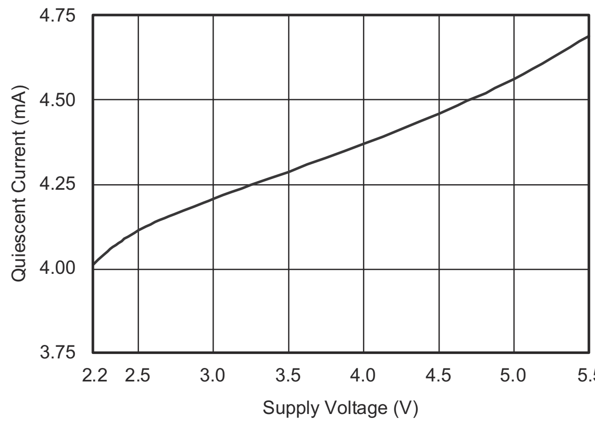


図 7-10. Quiescent Current vs Supply Voltage

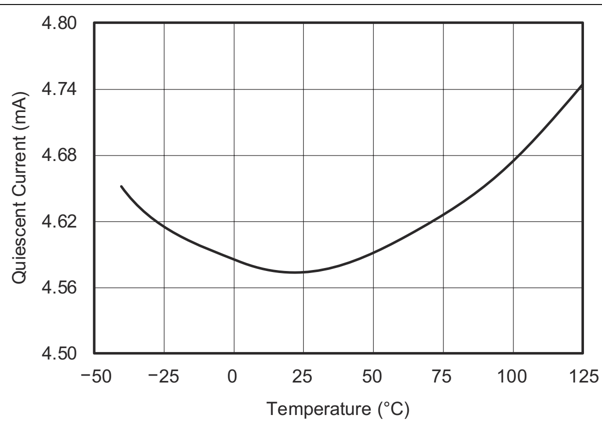


図 7-11. Quiescent Current vs Temperature

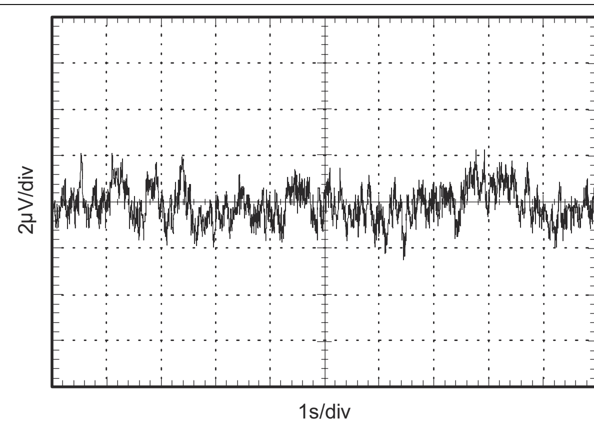


図 7-12. 0.1-Hz to 10-Hz Input Voltage Noise

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

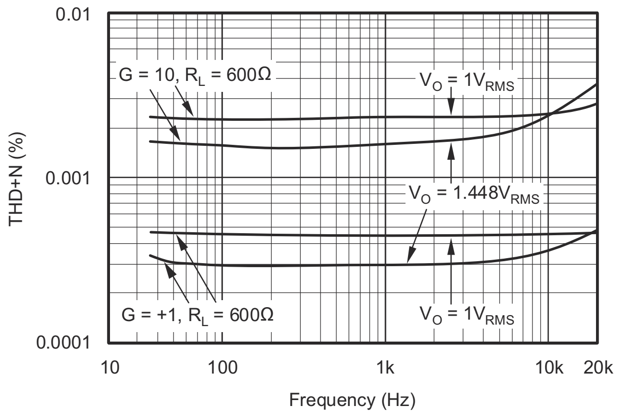


図 7-13. Total Harmonic Distortion + Noise vs Frequency

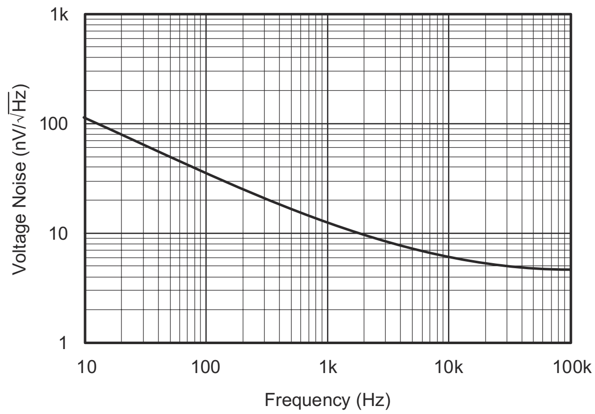


図 7-14. Input Voltage Noise Spectral Density

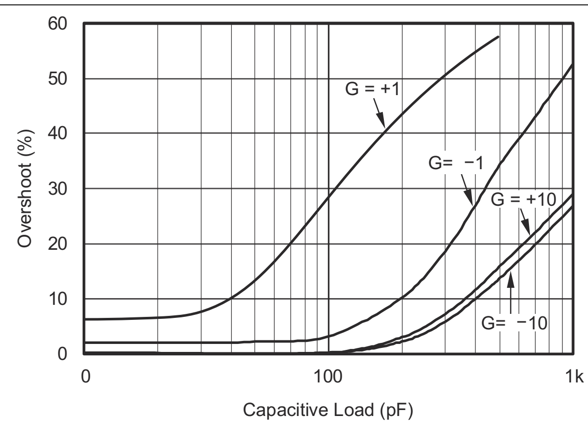


図 7-15. Overshoot vs Capacitive Load

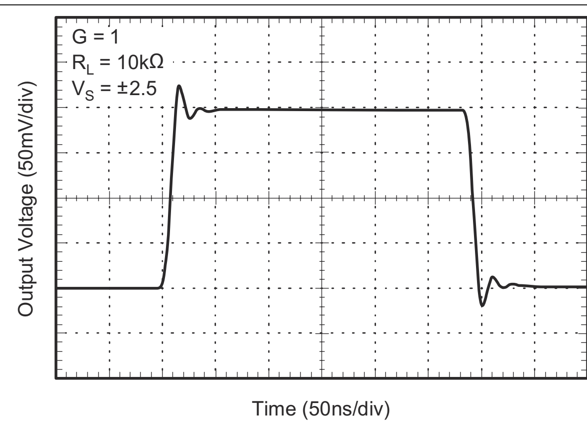


図 7-16. Small-Signal Step Response

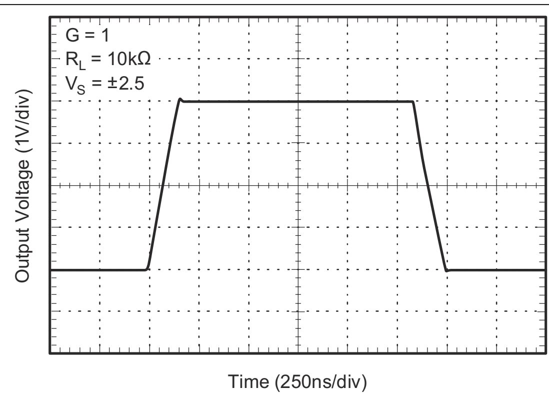


図 7-17. Large-Signal Step Response

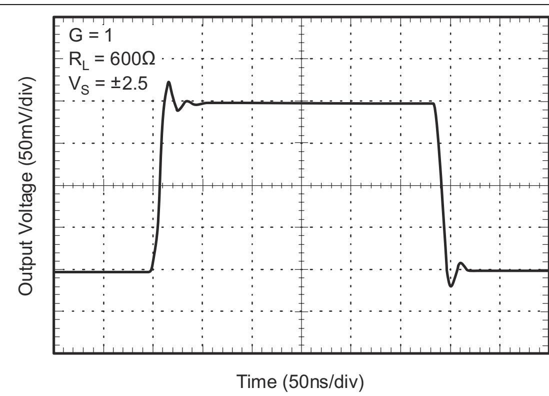


図 7-18. Small-Signal Step Response

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

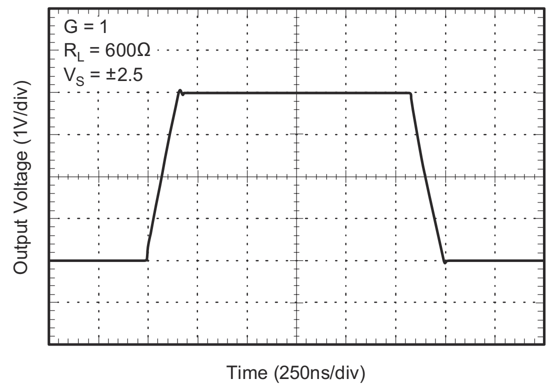


図 7-19. Large-Signal Step Response

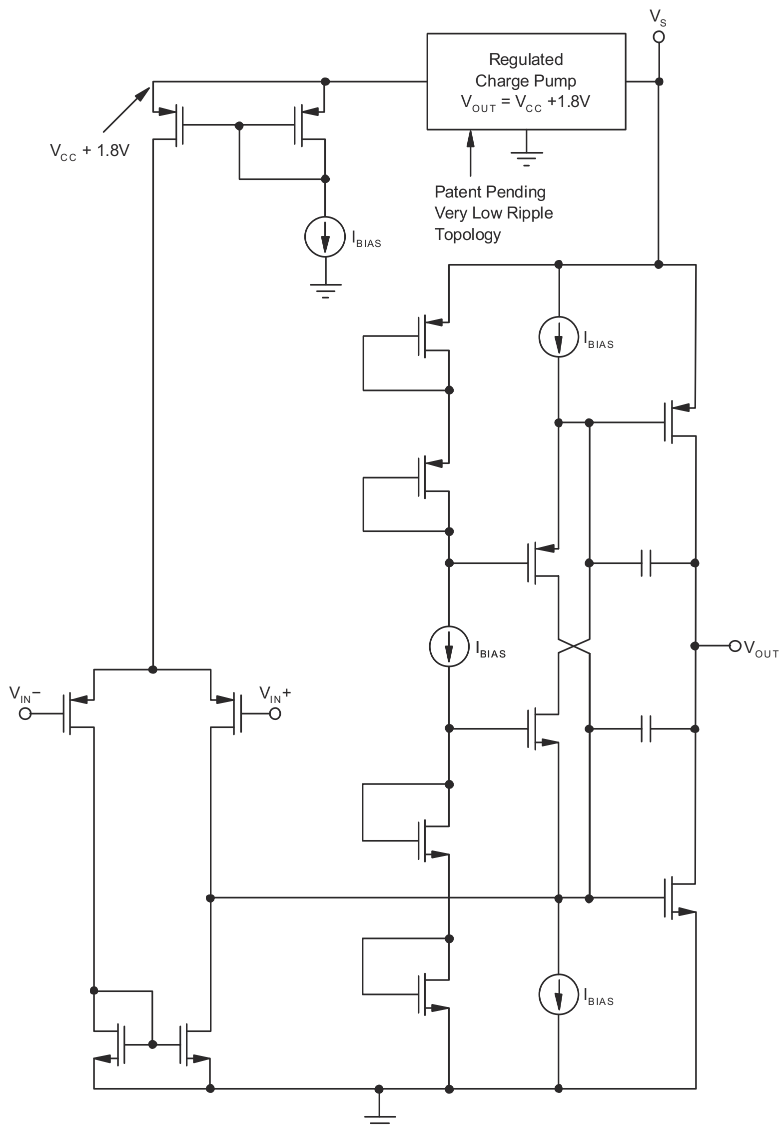
8 Detailed Description

8.1 Overview

The OPAx365 series of operational amplifiers feature rail-to-rail, high performance that make these devices an excellent choice for driving ADCs. Other typical applications include signal conditioning, cell phone power amplifier control loops, audio, and sensor amplification. The OPAx365 is a wideband amplifier that can be operated with either a single supply or dual supplies.

Furthermore, the OPA365 amplifier parameters are fully specified from 2.2 V to 5.5 V. Many of the specifications apply from −40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *セクション 7.7*.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Rail-to-Rail Input

The OPAx365 product family features true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). A unique zerø-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary stage operational amplifiers. This topology also allows the OPAx365 to provide excdellent common-mode performance over the entire input range, which extends 100 mV beyond both power-supply rails, as shown in 図 8-1. When driving ADCs, the highly linear V_{CM} range of the OPAx365 makes sure that the op amp or ADC system linearity performance is not compromised.

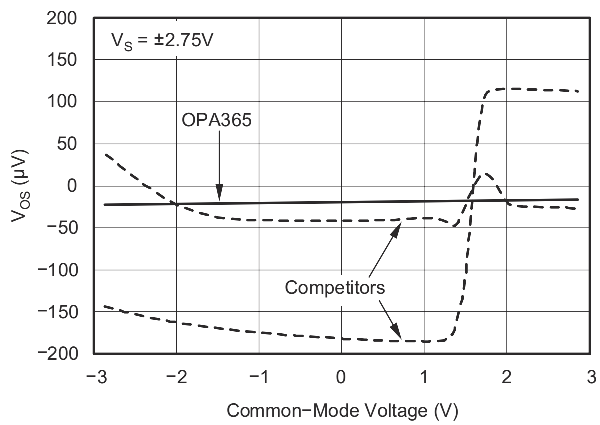


図 8-1. OPA365 Linear Offset Over the Entire Common-Mode Range

For a simplified schematic illustrating the rail-to-rail input circuitry, see *セクション 8.2*.

8.3.2 Input and ESD Protection

The OPAx365 devices incorporate internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, provided that the current is limited to 10 mA, as stated in *セクション 7.1*. 図 8-2 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to the minimum in noise-sensitive applications.

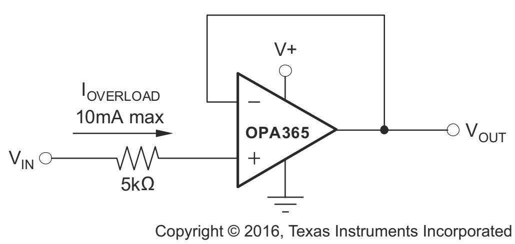


図 8-2. Input Current Protection

8.3.3 Capacitive Loads

The OPAx365 can be used in applications where driving a capacitive load is required. As with all op amps, there can be specific instances where the OPAx365 become unstable, leading to oscillation. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (+1 – V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

When operating in the unity-gain configuration, the OPAx365 remain stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains; see also 図 7-15.

図 8-3 shows one technique to increase the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider is sometimes insignificant. For instance, with a load resistance, R_L = 10 kΩ, and R_S = 20 Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600 Ω, which the OPAx365 are able to drive, the error increases to 7.5%.

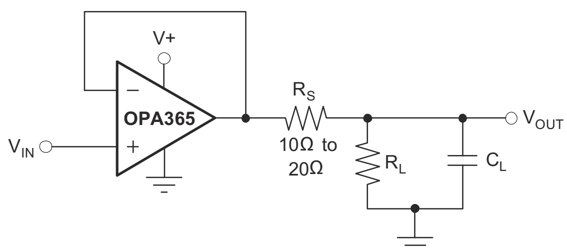


図 8-3. Improving Capacitive Load Drive

8.3.4 Achieving an Output Level of Zero Volts (0 V)

Certain single-supply applications require the op amp output to swing from 0 V to a positive full-scale voltage and have high accuracy. An example is an op amp employed to drive a single-supply ADC having an input range from 0 V to 5 V. Rail-to-rail output amplifiers with very light output loading can achieve an output level within millivolts of 0 V (or $+V_S$ at the high end), but not 0 V. Furthermore, the deviation from 0 V only becomes greater as the load current required increases. This increased deviation is a result of limitations of the CMOS output stage.

When a pulldown resistor is connected from the amplifier output to a negative voltage source, the OPAx365 can achieve an output level of 0 V, and even a few millivolts below 0 V. Below this limit, nonlinearity and limiting conditions become evident. 図 8-4 illustrates a circuit using this technique.

A pulldown current of approximately 500 µA is required when the OPAx365 is connected as a unity-gain buffer. A practical termination voltage (V_{NEG}) is −5 V, but other convenient negative voltages also can be used. Pulldown resistor R_L is calculated from $R_L = [(V_O - V_{NEG}) / (500\ \mu A)]$.

Using a minimum output voltage (V_O) of 0 V, $R_L = [0\ V - (-5\ V)] / (500\ \mu A)] = 10\ k\Omega$. Keep in mind that lower termination voltages result in smaller pulldown resistors that load the output during positive output voltage excursions.

注

This technique does not work with all op amps; apply only to op amps such as the OPAx365 that have been specifically designed to operate in this manner. Also, operating the OPAx365 output at 0 V changes the output-stage operating conditions, resulting in somewhat lower open-loop gain and bandwidth.

Keep these precautions in mind when driving a capacitive load because these conditions can affect circuit transient response and stability.

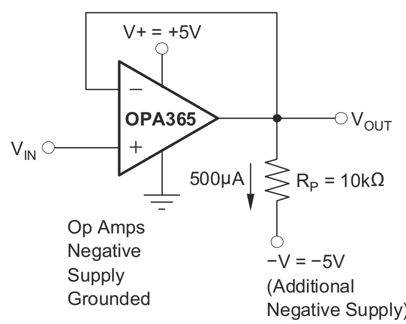


図 8-4. Swing-to-Ground

8.3.5 Active Filtering

The OPAx365 are an excellent choice for active filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. 図 8-5 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, rolloff is −40 dB/dec. The Butterworth response is great for applications requiring predictable gain characteristics such as the antialiasing filter used ahead of an ADC.

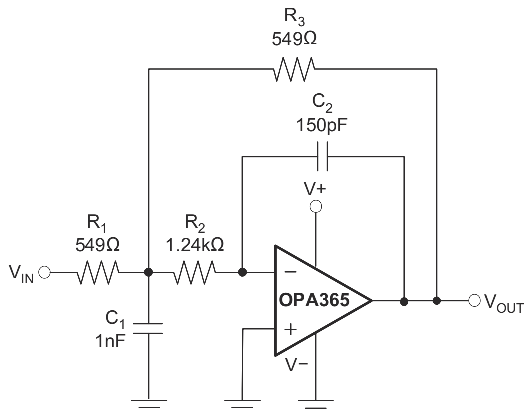


図 8-5. Second-Order Butterworth, 500-kHz Low-Pass Filter

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

- Add an inverting amplifier.
- Add an additional second-order MFB stage.
- Use a noninverting filter topology such as Sallen-Key.

The Sallen-Key topology is shown in 図 8-6.

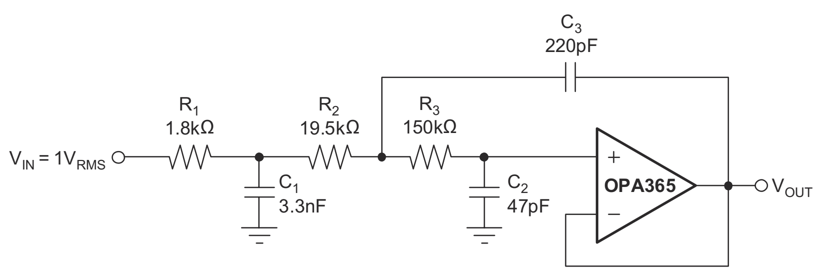


図 8-6. Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

8.4 Device Functional Modes

The OPA365 family has a single functional mode and are operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPA365 family is 5.5 V (±2.75 V).

9 Application and Implementation

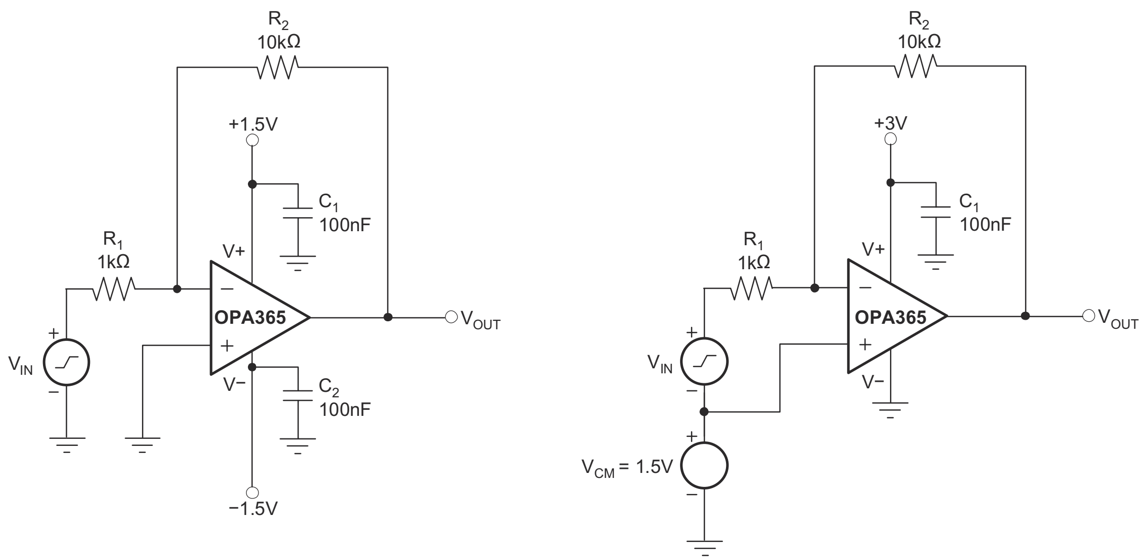
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.1.1 Basic Amplifier Configurations

As with other single-supply op amps, the OPAx365 can be operated with either a single supply or dual supplies. 図 9-1 shows a typical dual-supply connection, which is accompanied by a single-supply connection. The OPAx365 are configured as a basic inverting amplifier with a gain of −10 V/V. The dual-supply connection has an output voltage centered on zero, while the single-supply connection has an output centered on the common-mode voltage V_{CM}. For the circuit shown, this voltage is 1.5 V, but can be any value within the common-mode input voltage range. The OPAx365 V_{CM} range extends 100 mV beyond the power-supply rails.



a) Dual Supply Connection

b) Single−Supply Connection

図 9-1. Basic Circuit Connections

図 9-2 shows a single-supply, electret microphone application where V_{CM} is provided by a resistive divider. The divider also provides the bias voltage for the electret element.

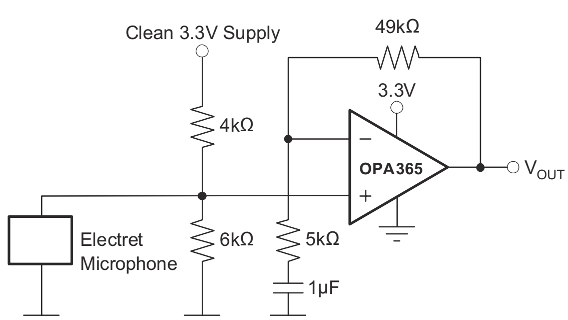


図 9-2. Microphone Preamplifier

9.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx365 are designed to construct high-speed, high-precision active filters. 図 9-3 illustrates a second-order low-pass filter commonly encountered in signal processing applications.

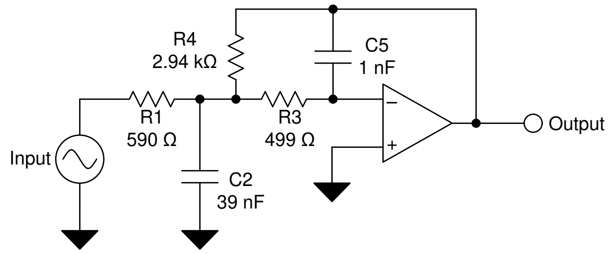


図 9-3. Second-Order Low-Pass Filter

9.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

9.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in 図 9-3. Use 式 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \tag{1}$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated using 式 2.

$$\text{Gain} = \frac{R_4}{R_1}$$
$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \tag{2}$$

Software tools are readily available to simplify filter design. The filter design tool is a simple, powerful, and easy-to-use active filter design program. The filter design tool allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

9.2.3 Application Curve

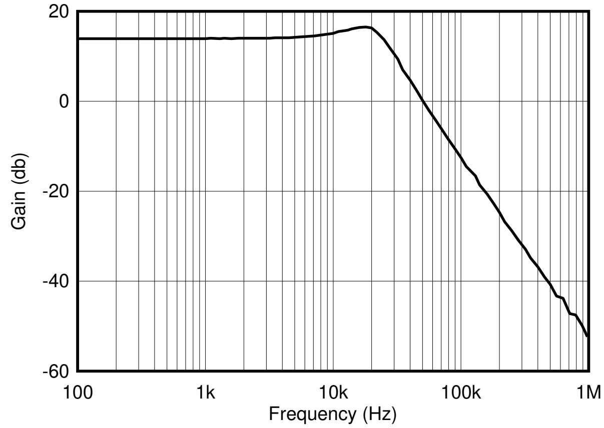


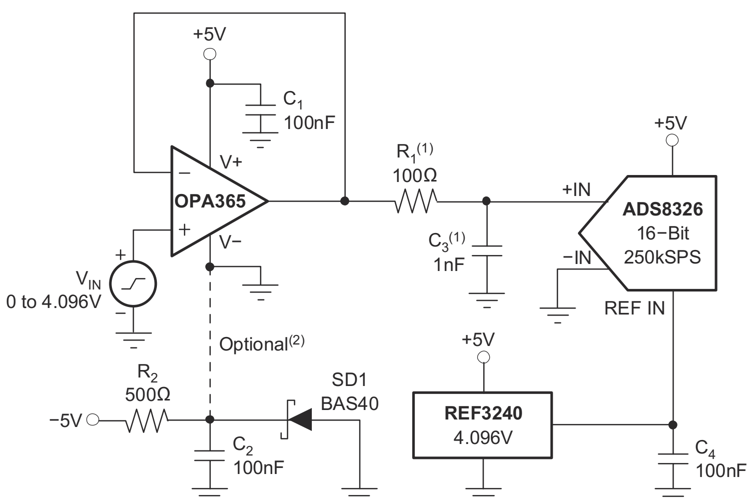
図 9-4. OPA365 Second-Order 25 kHz, Chebyshev, Low-Pass Filter

9.3 System Examples

9.3.1 Driving an Analog-to-Digital Converter

Very wide common-mode input range, rail-to-rail input and output voltage capability, and high speed make the OPAx365 excellent drivers for modern ADCs. Also, because the OPAx365 are free of the input offset transition characteristics inherent to some rail-to-rail CMOS op amps, these devices provide low THD and excellent linearity throughout the input voltage swing range.

図 9-5 shows the OPA365 driving an ADS8326, 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer and has an output swing to 0 V, making these devices directly compatible with the ADC minus full-scale input level. The 0-V level is achieved by powering the OPA365 V− pin with a small negative voltage established by the diode forward voltage drop. A small, signal-switching diode or Schottky diode provides a negative supply voltage of −0.3 V to −0.7 V. The supply rail-to-rail is equal to V+, plus the small negative voltage.



(1) Suggested value; can require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground due to op amp output swing limitations. If a negative power supply is available, this simple circuit creates a −0.3-V supply to allow output swing to true ground potential.

図 9-5. Driving the ADS8326

One method to drive an ADC that negates the need for an output swing down to 0 V uses a slightly compressed ADC full-scale input range (FSR). For example, 図 9-6 shows that the 16-bit ADS8361 has a maximum FSR of 0 V to 5 V when powered by a 5-V supply and V_{REF} of 2.5 V. The idea is to match the ADC input range with the op-amp full-linear output-swing range; for example, an output range of 0.1 V to 4.9 V. The reference output from the ADS8361 ADC is divided down from 2.5 V to 2.4 V using a resistive divider. The ADC FSR then becomes 4.8 V_{PP} centered on a common-mode voltage of 2.5 V. Current from the ADS8361 reference pin is limited to approximately ±10 µA. Here, 5 µA is used to bias the divider. The resistors must be precise to maintain the ADC gain accuracy. An additional benefit of this method is the elimination of the negative supply voltage; these devices require no additional power-supply current.

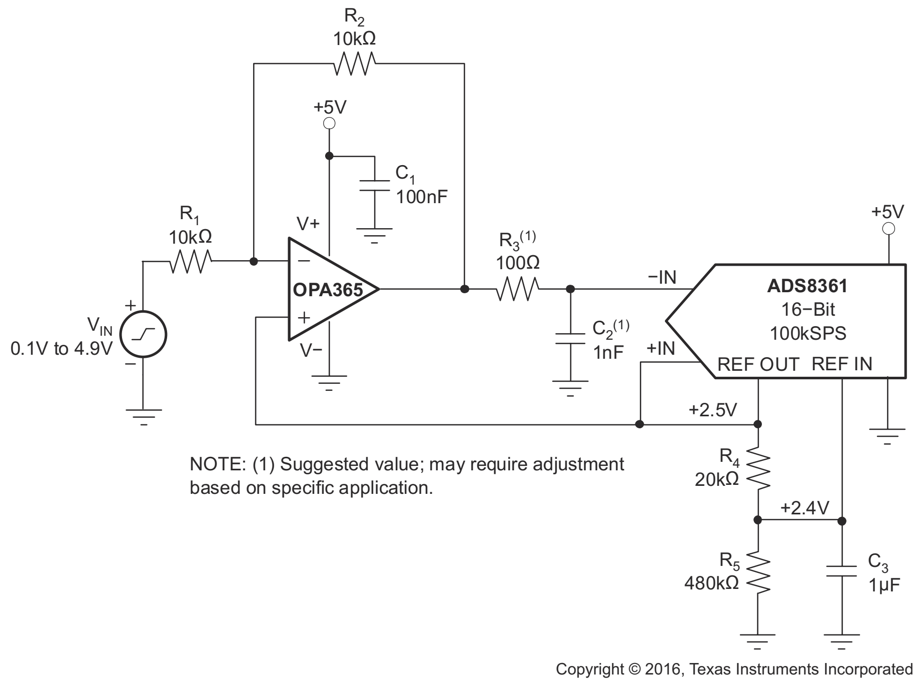


図 9-6. Driving the ADS8361

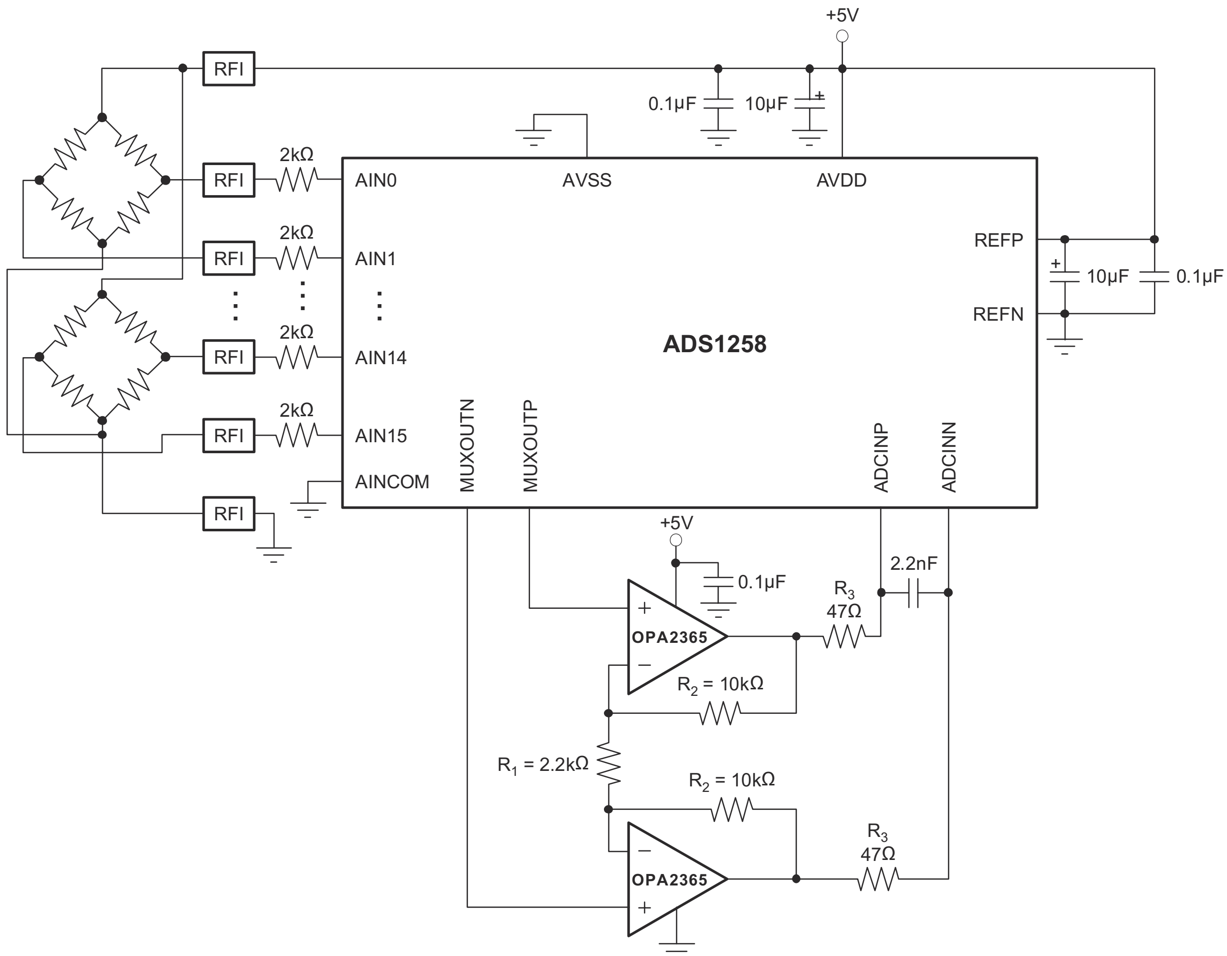
A resistor-capacitor (RC) network, consisting of R_1 and C_1, is included between the op amp and the ADS8361. The RC network not only provides a high-frequency filter function, but more importantly serves as a charge reservoir used for charging the converter internal hold capacitance. This capability maintains the op-amp output linearity as the ADC input characteristics change throughout the conversion cycle. Depending on the particular application and ADC, some optimization of the R_1 and C_1 values can be required for best transient performance.

図 9-7 illustrates the OPA2365 dual op amp providing signal conditioning within an ADS1258 bridge sensor circuit. The OPA2365 is connected as a differential-in and differential-out amplifier after the ADS1258 16:1 multiplexer. The voltage gain for this stage is approximately 10 V/V. Driving the ADS1258 internal ADC in differential mode, rather than in a single-ended mode, exploits the full linearity performance capability of the converter. For best common-mode rejection, the two R_2 resistors must be closely matched.

Note that in 図 9-7, the amplifiers, bridges, ADS1258, and internal reference are powered by the same single 5-V supply. This ratiometric connection helps cancel excitation voltage drift effects and noise. For best performance, the 5-V supply must be as free as possible from noise and transients.

When the ADS1258 data rate is set to maximum and the chop feature is enabled, this circuit yields 12 bits of noise-free resolution with a 50-mV full-scale input.

The chop feature is used to reduce the ADS1258 offset and offset drift to very low levels. A 2.2-nF capacitor is required across the ADC inputs to bypass the sampling currents. The 47-Ω resistors provide isolation for the OPA2365 outputs from the relatively large, 2.2-nF capacitive load.



NOTE: G = 1 + $2R_2/R_1$. Match R_2 resistors for optimum CMRR.

図 9-7. Conditioning Input Signals to the ADS1258 on a Single Supply

9.4 Power Supply Recommendations

The OPAx365 family is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *セクション 7.7*.

9.5 Layout

9.5.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - The OPAx365 are capable of high-output current (in excess of 65 mA). Applications with low-impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1-µF solid tantalum capacitors can improve dynamic performance in these applications.

- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As 図 9-8 shows, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

9.5.2 Layout Example

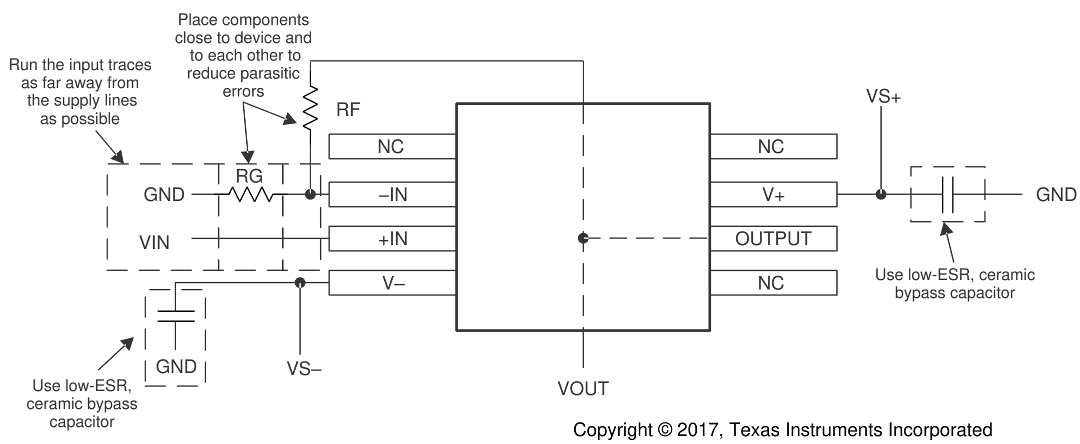


図 9-8. Layout Recommendation

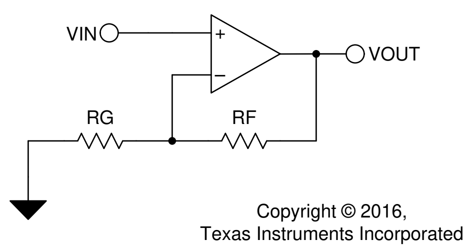


図 9-9. Schematic Representation

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

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TINA-TI™ シミュレーション・ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI シミュレーション・ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション・ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

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10.1.1.3 DIP アダプタ評価基板

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10.1.1.4 DIYAMP-EVM

DIYAMP-EVM は、実際のアンプ回路を提供する独自の評価基板 (EVM) であり、設計コンセプトの迅速な評価とシミュレーションの検証を実現します。この評価基板は、3 つの業界標準パッケージ (SC70、SOT23、SOIC) で供給されており、シングル / デュアル電源向けに、アンプ、フィルタ、安定性補償、コンパレータの各構成など、12 の一般的なアンプ構成が可能です。

10.1.1.5 TI のリファレンス・デザイン

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10.1.1.6 フィルタ設計ツール

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10.2 Documentation Support

10.2.1 Related Documentation

The following documents are relevant to using the OPAx365, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- Texas Instruments, *FilterPro™ MFB and Sallen-Key Low-Pass Filter Design Program User Guide*
- Texas Instruments, *Low Power Input and Reference Driver Circuit for ADS8318 and ADS8319* application report
- Texas Instruments, *Op Amp Performance Analysis* application bulletin
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application bulletin
- Texas Instruments, *The Best of Baker's Best – Amplifiers eBook*

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2365AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2365A	Samples
OPA2365AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2365A	Samples
OPA2365AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2365A	Samples
OPA2365AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2365A	Samples
OPA365AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O365A	Samples
OPA365AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAVQ	Samples
OPA365AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAVQ	Samples
OPA365AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAVQ	Samples
OPA365AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAVQ	Samples
OPA365AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O365A	Samples
OPA365AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O365A	Samples
OPA365AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O365A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2365, OPA365 :

- Automotive : OPA2365-Q1, OPA365-Q1

- Enhanced Product : OPA365-EP

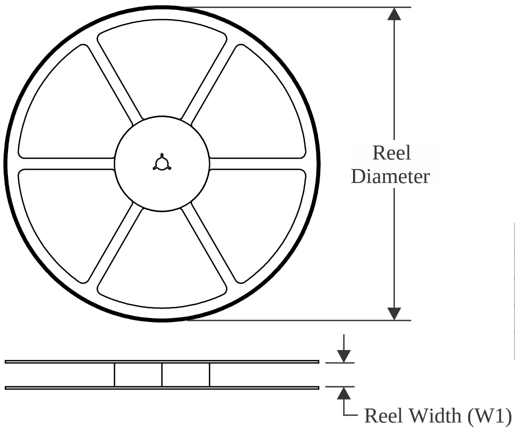
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

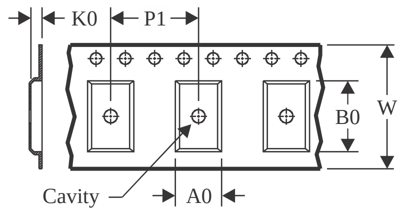
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

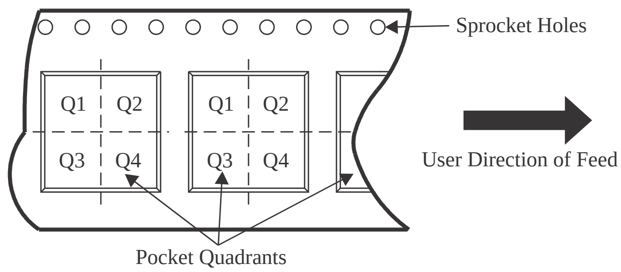


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

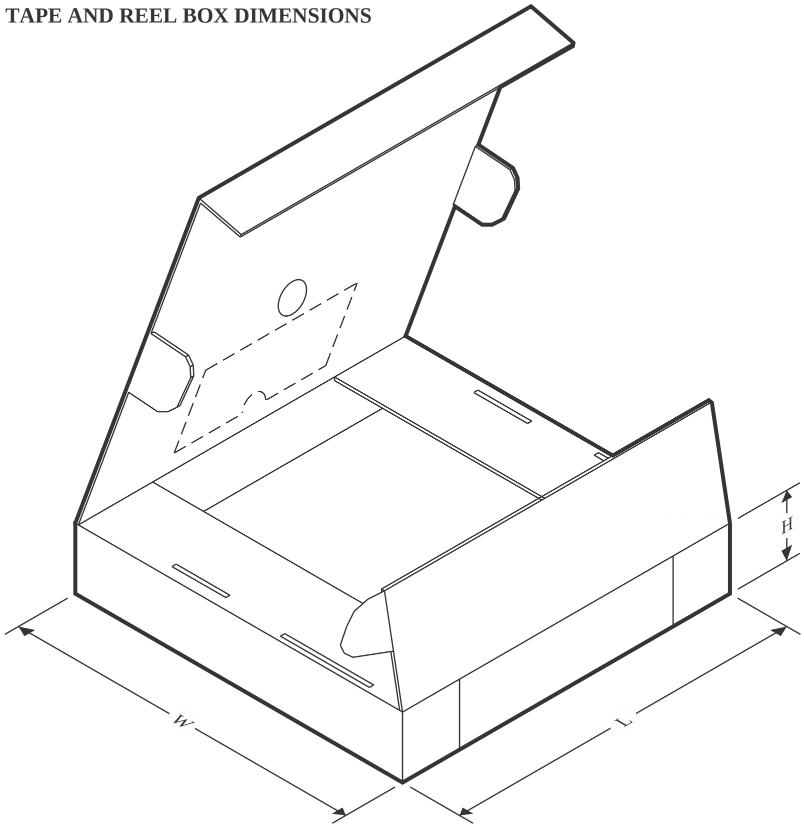
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2365AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA365AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA365AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA365AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

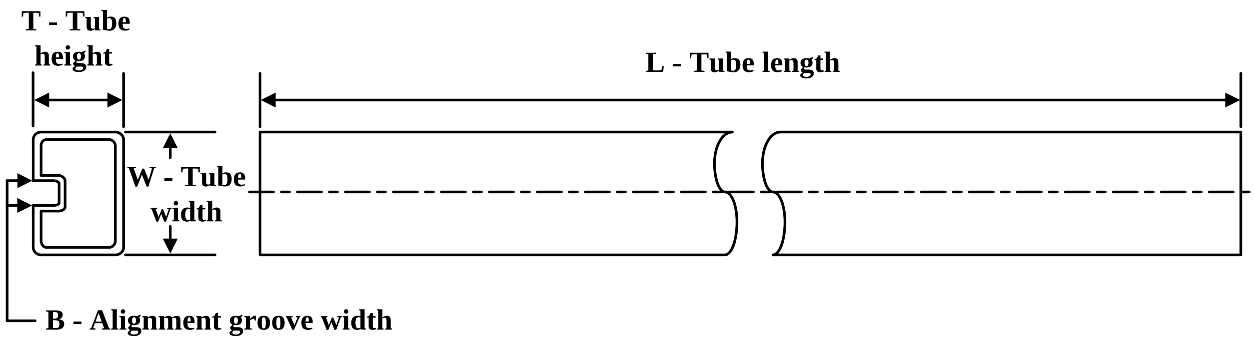
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

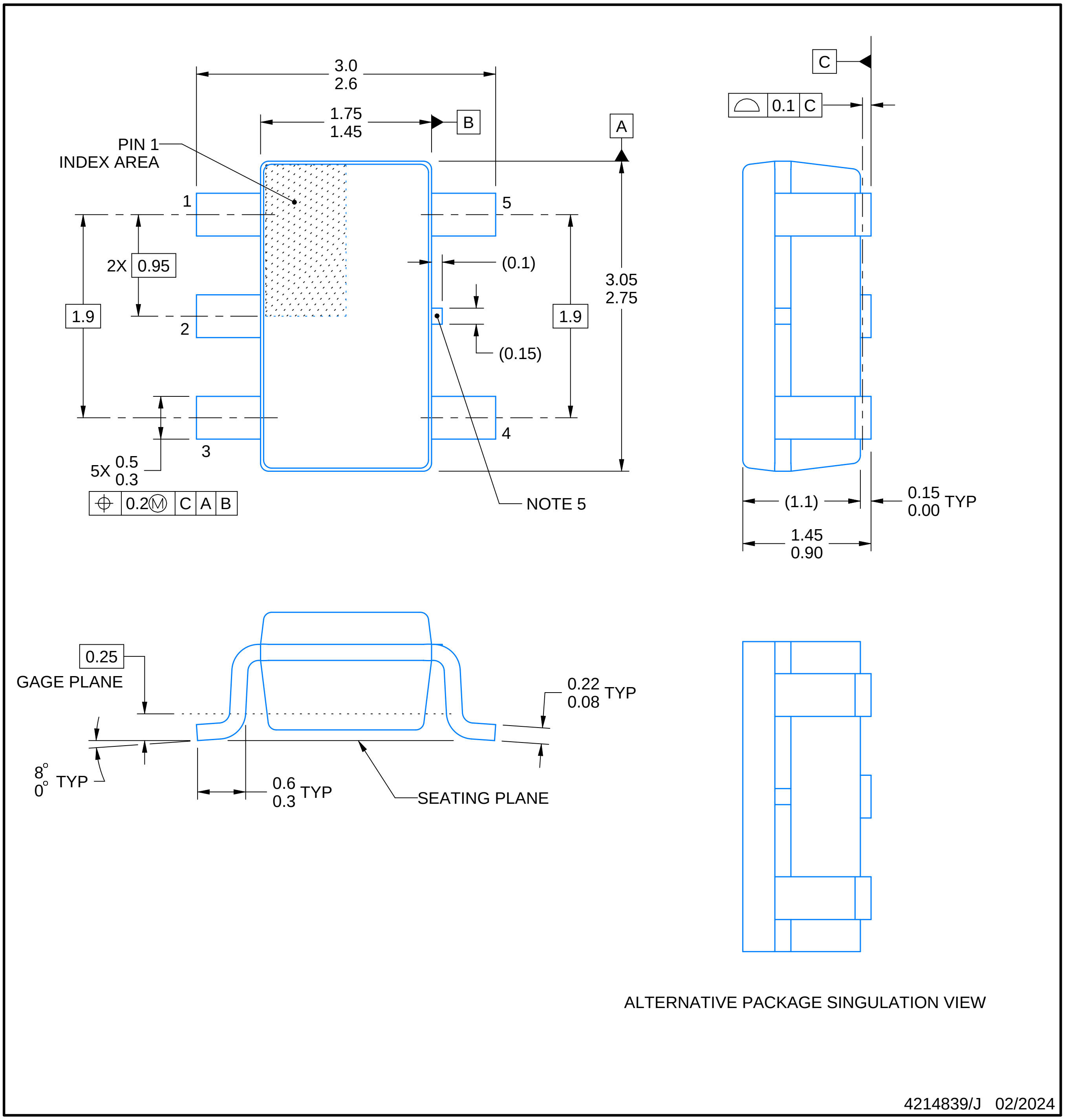
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2365AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA365AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA365AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA365AIDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

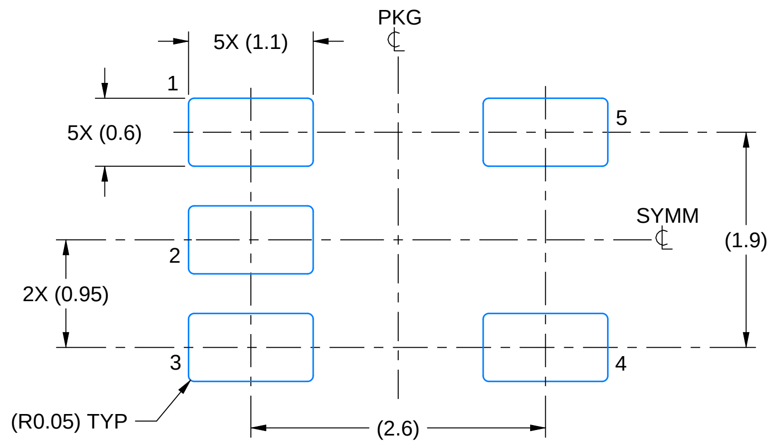
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2365AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2365AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA365AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA365AIDG4	D	SOIC	8	75	506.6	8	3940	4.32



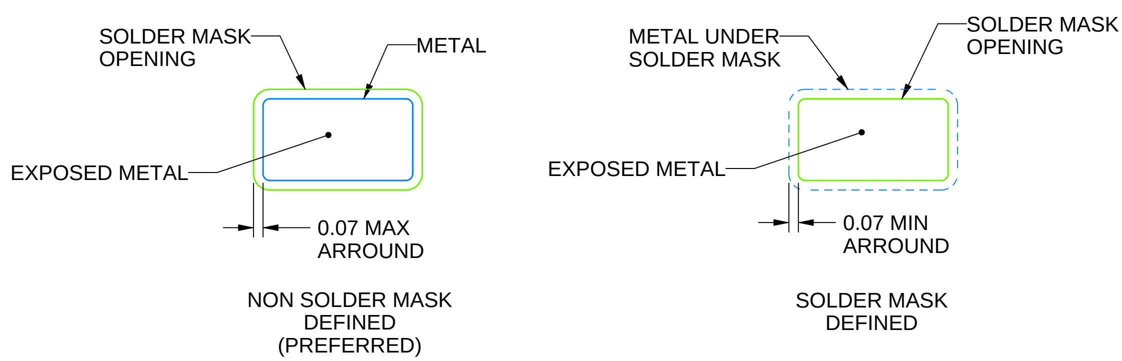
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

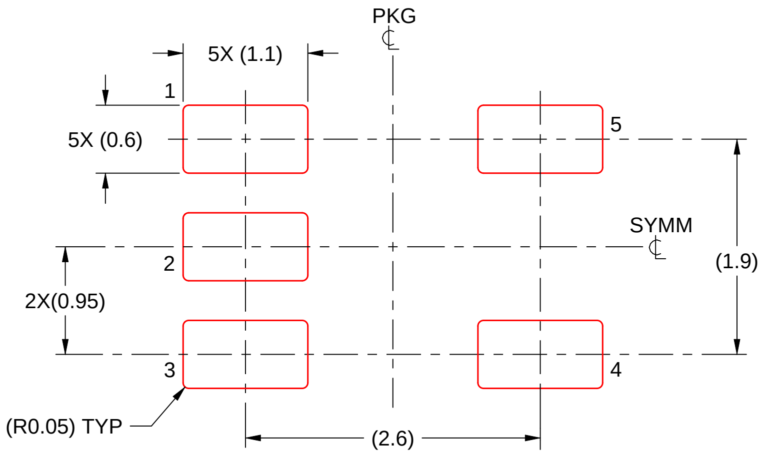


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

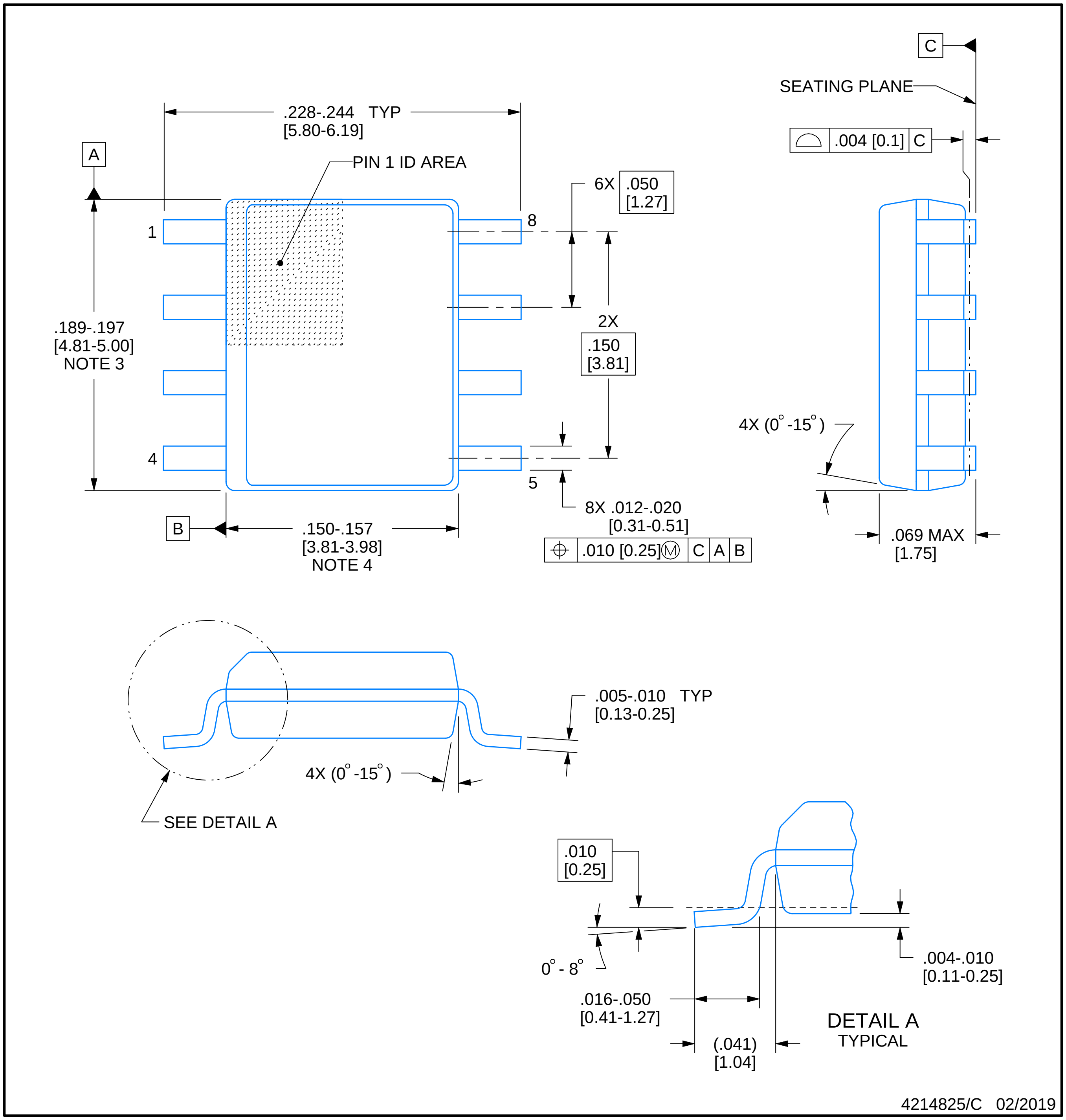


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

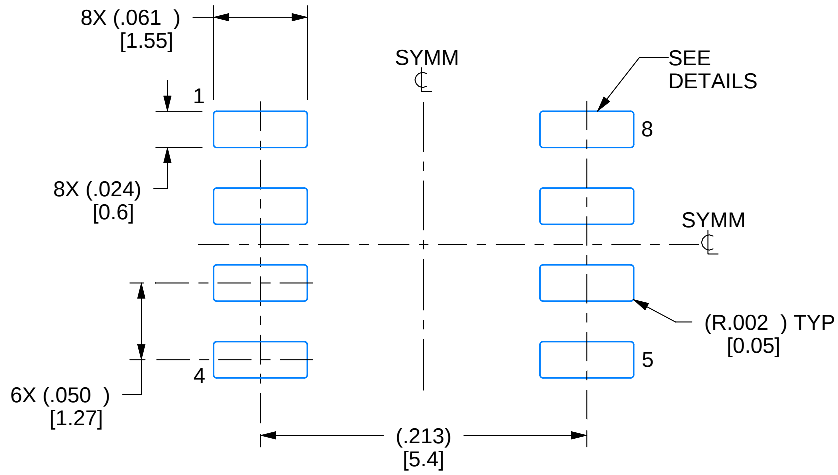
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

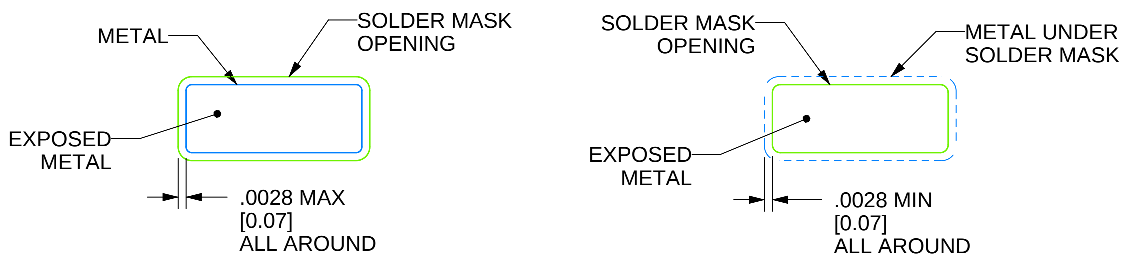


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

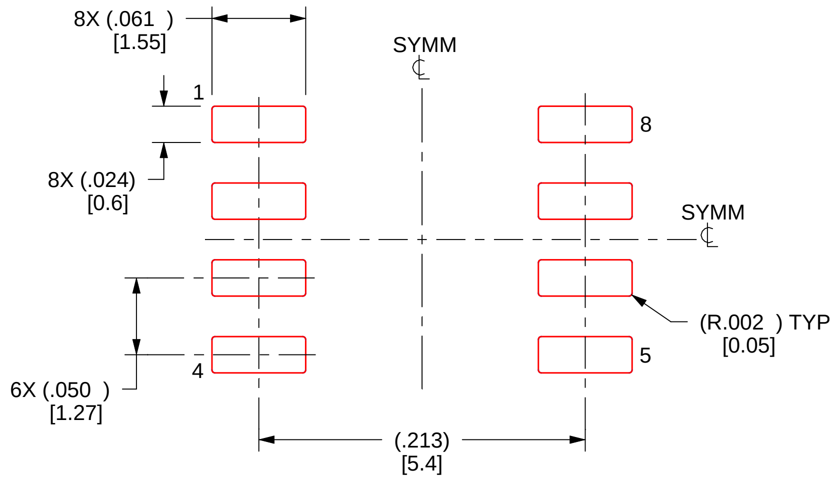
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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