TEXAS INSTRUMENTS
OPA197, OPA2197, OPA4197
JAJSEY7C – JANUARY 2016 – REVISED MARCH 2018

OPAx197 36V、高精度、レール・ツー・レール入力/出力、低オフセット電圧オペアンプ

1 特長

- 低いオフセット電圧: ±100µV (最大値)
- 低いオフセット電圧ドリフト係数: ±2.5µV/℃ (最大値)
- 低ノイズ: 1kHz時に5.5nV/√Hz
- 高い同相除去: 120dB (最小値)
- 低いバイアス電流: ±5pA (標準値)
- レール・ツー・レール入出力
- 広い帯域幅: 10MHz GBW
- 高いスルー・レート: 20V/µs
- 低い静止電流: アンプごとに1mA (標準値)
- 広い電源電圧範囲: ±2.25V～±18V、+4.5V～+36V
- EMIおよびRFIフィルタ入力
- 差動入力電圧範囲は電源レールまで
- 高い容量性負荷駆動能力: 1nF
- 業界標準パッケージ
  - シングル: SOIC-8、SOT-5、VSSOP-8
  - デュアル: SOIC-8、VSSOP-8
  - クワッド: SOIC-14およびTSSOP-14

2 アプリケーション

- 多重化データ収集システム
- テストおよび計測機器
- 高分解能のADCドライバ・アンプ
- SAR ADCリファレンス・バッファ
- プログラマブル・ロジック・コントローラ
- ハイサイドおよびローサイドの電流センシング
- 高精度のコンパレータ

3 概要

OPAx197ファミリ(OPA197、OPA2197、OPA4197)は新世代の36Vオペアンプです。

これらのデバイスは、レール・ツー・レールの入力/出力、低いオフセット(標準値±25µV)、低いオフセット・ドリフト係数(標準値±0.25µV/℃)、10MHz帯域幅など、DC精度とAC特性が非常に優れています。

電源レールまでの差動入力電圧範囲、大きな出力電流(±65mA)、1nFまでの大きな容量性負荷の駆動能力、高いスルー・レート(20V/µs)など独自の特長から、OPA197は高電圧の産業アプリケーション向けの、堅牢で高性能なオペアンプです。

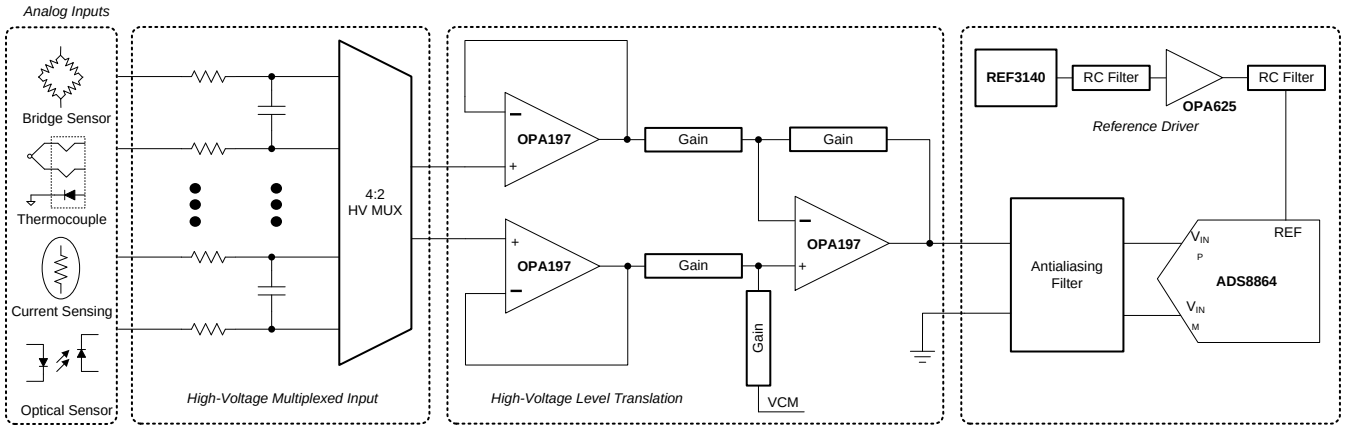
OPA197ファミリのオペアンプは標準のパッケージで供給され、-40℃～+125℃で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA197	SOIC (8)	4.90mm×3.90mm
	SOT (5)	2.90mm×1.60mm
	VSSOP (8)	3.00mm×3.00mm
OPA2197	SOIC (8)	4.90mm×3.90mm
	VSSOP (8)	3.00mm×3.00mm
OPA4197	SOIC (14)	8.65mm×3.90mm
	TSSOP (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

高電圧の多重化データ収集システムにおけるOPA197



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4 改訂履歴

Revision B (October 2016) から **Revision C** に変更 **Page**

- 「低いオフセット電圧: ±250µV (最大値)」を「低いオフセット電圧: ±100µV (最大値)」に 変更 ... 1
- Changed *Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)* Input offset voltage V_S = ±18 V under OFFSET VOLTAGE from "±250" to "±100"; remove "T_A = 0°C to 85°C" and "T_A = –40°C to +125°C" rows from same ... 7
- Changed *Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)* Input offset voltage V_{CM} = (V+) – 1.5 V under OFFSET VOLTAGE from "±250" to "±100"; remove "T_A = 0°C to 85°C" and "T_A = –40°C to +125°C" rows from same ... 7
- Changed *Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)* Input offset voltage V_S = ±2.25 V, V_{CM} = (V+) – 3 V under OFFSET VOLTAGE from "±250" to "±100"; remove "T_A = 0°C to 85°C" and "T_A = –40°C to +125°C" rows from same ... 9
- Changed *Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)* Input offset voltage V_S = ±3 V, V_{CM} = (V+) – 1.5 V under OFFSET VOLTAGE from "±250" to "±100"; remove "T_A = 0°C to 85°C" and "T_A = –40°C to +125°C" rows from same ... 9
- Changed "0" on Frequency (Hz) axis to "0.1" ... 11
- Changed "....to achieve a very low offset voltage of 250 µV (max)..." to "...to achieve a very low offset voltage of 100 µV (maximum)..." ... 19

Revision A (July 2016) から **Revision B** に変更 **Page**

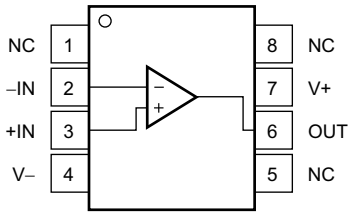
- Added new row for PW package to *Input bias current* parameter ... 7
- Added new row for PW package to *Input offset current* parameter ... 7
- Added new footnote (1) to *Open-loop gain* parameter ... 7
- Changed *Slew rate* parameter from 20 V/µs : to 14 V/µs ... 10

2016年1月 発行のものから更新 **Page**

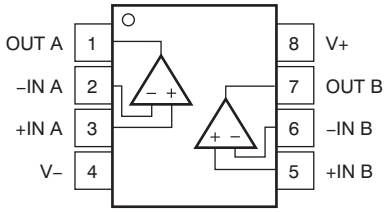
- Added OPA2197 and OPA4197 CDM values to ESD Ratings table ... 5

5 Pin Configuration and Functions

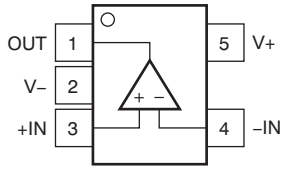
D and DGK Packages: OPA197
8-Pin SOIC and VSSOP
Top View



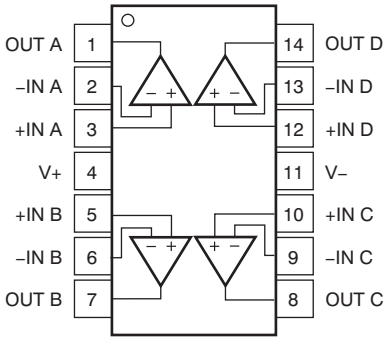
D and DGK Packages: OPA2197
8-Pin SOIC and VSSOP
Top View



DBV Package: OPA197
5-Pin SOT
Top View



D and PW Packages: OPA4197
14-Pin SOIC and TSSOP
Top View



Pin Functions: OPA197

PIN			I/O	DESCRIPTION
NAME	OPA197			
	D (SOIC), DGK (VSSOP)	DBV (SOT)		
+IN	3	3	I	Noninverting input
–IN	2	4	I	Inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V+	7	5	—	Positive (highest) power supply
V–	4	2	—	Negative (lowest) power supply

Pin Functions: OPA2197 and OPA4197

PIN			I/O	DESCRIPTION
NAME	OPA2197	OPA4197		
	D (SOIC), DGK (VSSOP)	D (SOIC), PW (TSSOP)		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input,,channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	—	Positive (highest) power supply
V–	4	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		Dual supply		±20	V
		Single supply		40	
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit(2)			Continuous		
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
ALL DEVICES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
OPA197				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V
OPA2197				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	V
OPA4197				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Dual supply	±2.25		±18	V
	Single supply	4.5		36	
Operating temperature, T_A		–40		125	°C

6.4 Thermal Information: OPA197

THERMAL METRIC(1)		OPA197			UNIT
		D (SOIC)	DBV (SOT)	DGK (VSSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	158.8	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	60.1	60.7	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	44.8	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	1.6	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	4.2	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2197

THERMAL METRIC(1)		OPA2197		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53.9	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.3	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4197

THERMAL METRIC(1)		OPA4197		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.3	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±18 V			±25	±100	µV
		V_{CM} = (V+) – 1.5 V			±10	±100	
dV_{OS}/dT	Input offset voltage drift	V_S = ±18 V, V_{CM} = (V+) – 3 V	T_A = –40°C to +125°C		±0.5	±2.5	µV/°C
		V_S = ±18 V, V_{CM} = (V+) – 1.5 V			±0.8	±4.5	
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±1	±3	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
			PW package only			±15	
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
			PW package only			±10	
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.30		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		$nV/\sqrt{Hz}$
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
i_n	Input current noise density	f = 1 kHz			1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
			T_A = –40°C to +125°C	110	126		
		V_S = ±18 V, (V+) – 1.5 V < V_{CM} < (V+)		100	120		
			T_A = –40°C to +125°C	80	100		
		V_S = ±18 V, (V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain(1)	V_S = ±18 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		120	134		dB
			T_A = –40°C to +125°C	110	126		
		V_S = ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		120	143		
			T_A = –40°C to +125°C	110	134		

(1) For OPA2197, OPA4197: When driving high current loads on multiple channels, make sure the junction temperature does not exceed 125°C.

Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	V_S = ± 18 V, G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±18 V, G = 1, 10-V step		1.4		µs
			V_S = ±18 V, G = 1, 5-V step		0.9		
		To 0.001%	V_S = ±18 V, G = 1, 10-V step		2.1		
			V_S = ±18 V, G = 1, 5-V step		1.8		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			200		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00008%		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	25	mV
			R_{LOAD} = 10 kΩ		95	125	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	25	
			R_{LOAD} = 10 kΩ		95	125	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, See Figure 26			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.3	mA
		T_A = –40°C to +125°C, I_O = 0 A				1.5	
TEMPERATURE							
	Thermal protection(2)				140		°C

(2) For a detailed description of thermal protection, see the *Thermal Protection* section.

6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±2.25 V, V_{CM} = (V+) – 3 V			±5	±100	µV
		(V+) – 3.5 V < V_{CM} < (V+) – 1.5 V		See *Common-Mode Voltage Range* section			
		V_S = ±3 V, V_{CM} = (V+) – 1.5 V			±10	±100	µV
dV_{OS}/dT	Input offset voltage drift	V_S = ±2.25 V, V_{CM} = (V+) – 3 V	T_A = –40°C to +125°C		±0.5	±2.5	µV/°C
		V_S = ±2.25 V, V_{CM} = (V+) – 1.5 V			±0.8	±4.5	
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C, V_{CM} = V_S / 2 – 0.75 V			±2		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V, f = 0.1 Hz to 10 Hz			1.30		μV_{PP}
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V, f = 0.1 Hz to 10 Hz			4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		nV/√Hz
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
i_n	Input current noise density		f = 1 kHz		1.5		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 3 V		90	110		dB
			T_A = –40°C to +125°C	88	104		
		V_S = ±2.25 V, (V+) – 1.5 V < V_{CM} < (V+)		94	120		
			T_A = –40°C to +125°C	77	100		
		V_S = ±2.25 V, (V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±2.25 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		104	126		dB
			T_A = –40°C to +125°C	100	114		
		V_S = ±2.25 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		104	134		
			T_A = –40°C to +125°C	100	120		

Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 1-V step			14		V/µs
t_s	Settling time	To 0.01%	V_S = ±3 V, G = 1, 5-V step		1		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			200		ns
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	25	mV
			R_{LOAD} = 10 kΩ		95	125	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	25	
			R_{LOAD} = 10 kΩ		95	125	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current	V_S = ±2.25 V			±65		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Figure 26			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.3	mA
			T_A = –40°C to +125°C			1.5	
TEMPERATURE							
	Thermal protection(1)				140		°C

(1) For a detailed description of thermal protection, see the *Thermal Protection* section.

6.9 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1, Figure 2, Figure 3
Offset Voltage Drift Distribution	Figure 4
Offset Voltage vs Temperature	Figure 5
Offset Voltage vs Common-Mode Voltage	Figure 6, Figure 7, Figure 8
Offset Voltage vs Power Supply	Figure 9
Open-Loop Gain and Phase vs Frequency	Figure 10
Closed-Loop Gain and Phase vs Frequency	Figure 11
Input Bias Current vs Common-Mode Voltage	Figure 12
Input Bias Current vs Temperature	Figure 13
Output Voltage Swing vs Output Current (maximum supply)	Figure 14, Figure 15
CMRR and PSRR vs Frequency	Figure 16
CMRR vs Temperature	Figure 17
PSRR vs Temperature	Figure 18
0.1-Hz to 10-Hz Noise	Figure 19
Input Voltage Noise Spectral Density vs Frequency	Figure 20
THD+N Ratio vs Frequency	Figure 21
THD+N vs Output Amplitude	Figure 22
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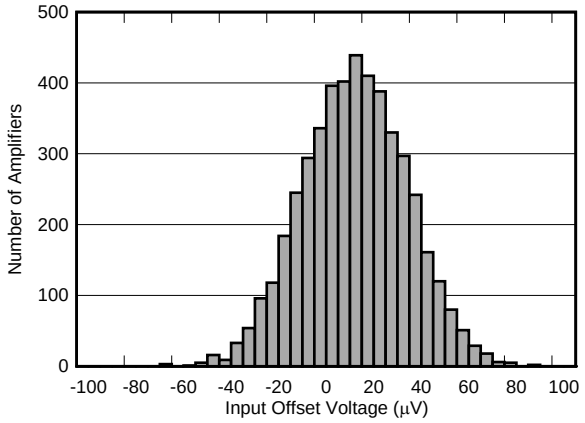
Small Signal Overshoot vs Capacitive Load (100-mV output step)	Figure 27, Figure 28
No Phase Reversal	Figure 29
Positive Overload Recovery	Figure 30
Negative Overload Recovery	Figure 31
Small-Signal Step Response (100 mV)	Figure 32, Figure 33
Large-Signal Step Response	Figure 34
Settling Time	Figure 35, Figure 36, ,
Short-Circuit Current vs Temperature	Figure 37
Maximum Output Voltage vs Frequency	Figure 38
Propagation Delay Rising Edge	Figure 39
Propagation Delay Falling Edge	Figure 40

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



4770 production units

Figure 1. Offset Voltage Production Distribution at 25°C

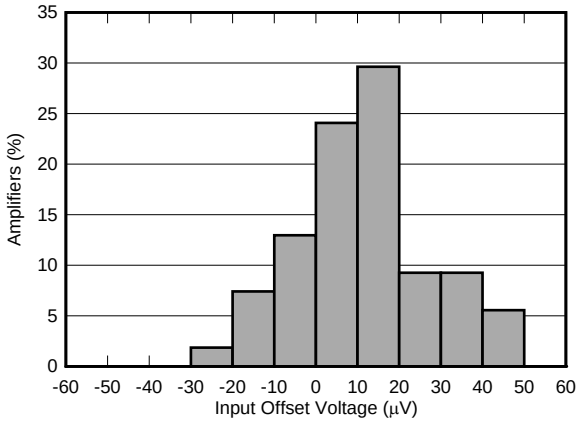


Figure 2. Offset Voltage Production Distribution at 125°C

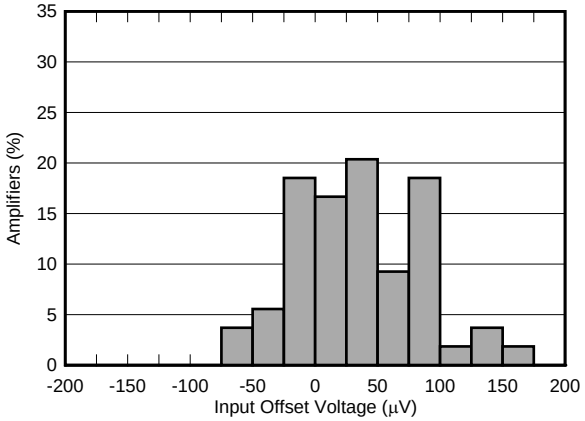


Figure 3. Offset Voltage Production Distribution at –40°C

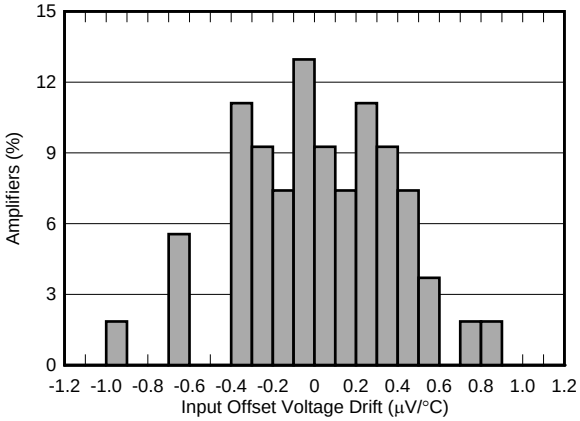
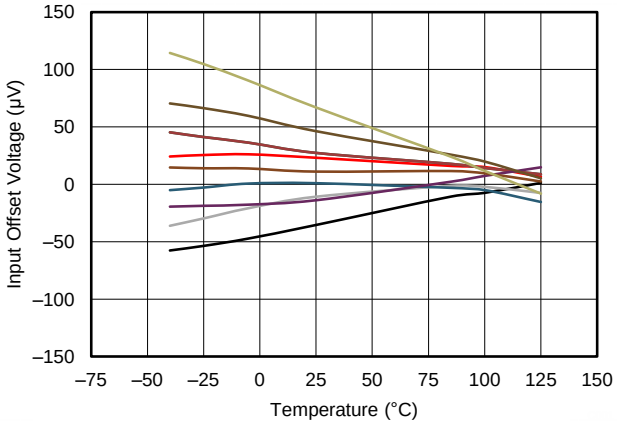
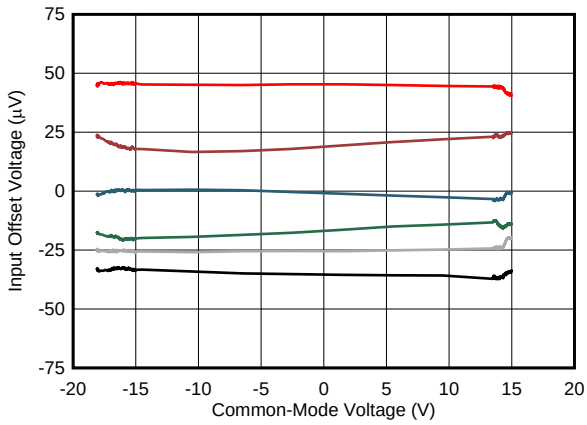


Figure 4. Offset Voltage Drift Distribution from –40°C to +125°C



9 typical units

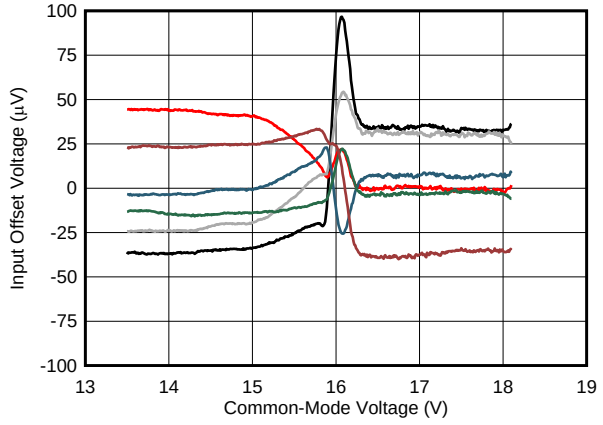
Figure 5. Offset Voltage vs Temperature



6 typical units

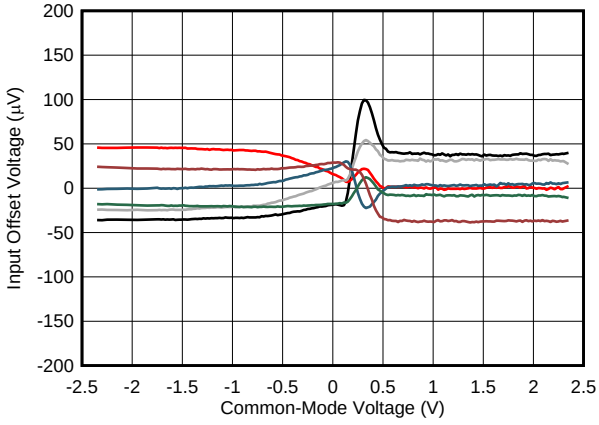
Figure 6. Offset Voltage vs Common-Mode Voltage

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



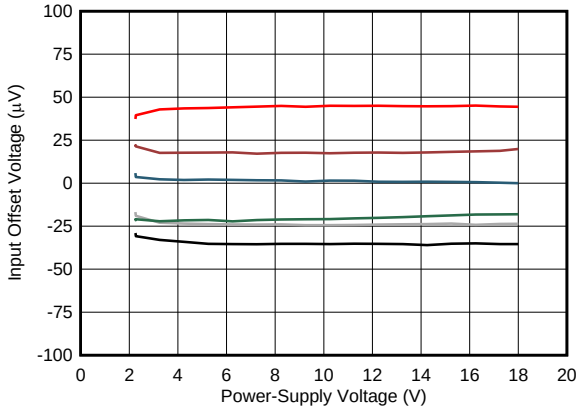
6 typical units

Figure 7. Offset Voltage vs Common-Mode Voltage



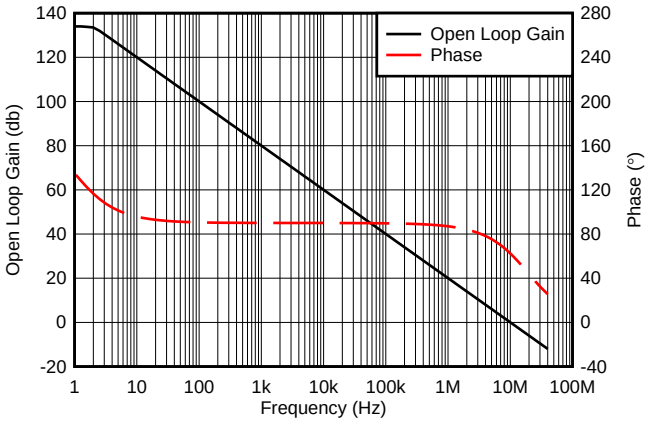
6 typical units

Figure 8. Offset Voltage vs Common-Mode Voltage



6 typical units

Figure 9. Offset Voltage vs Power Supply



C_{LOAD} = 15 pF

Figure 10. Open-Loop Gain and Phase vs Frequency

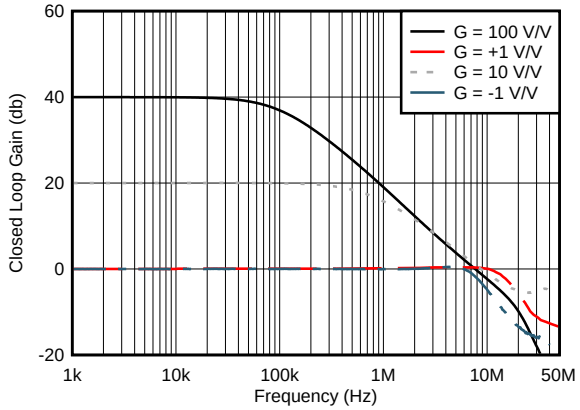


Figure 11. Closed-Loop Gain and Phase vs Frequency

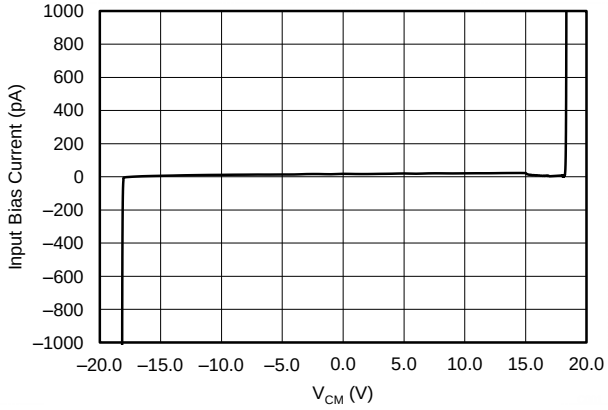


Figure 12. Input Bias Current vs Common-Mode Voltage

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

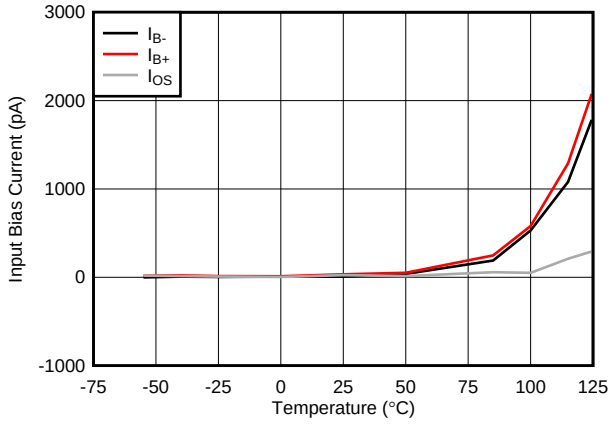


Figure 13. Input Bias Current vs Temperature

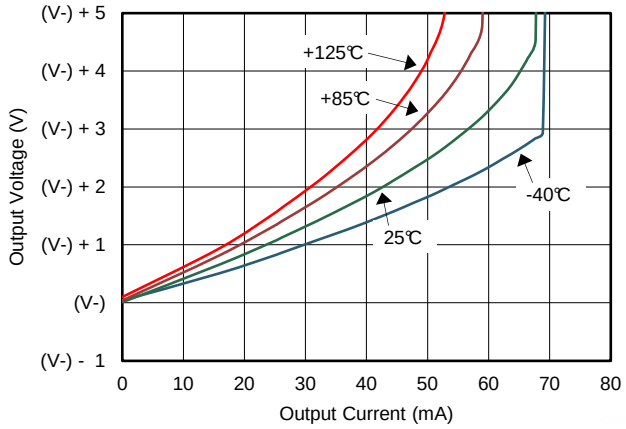


Figure 14. Output Voltage Swing from Negative Power Supply vs Output Current (Maximum Supply)

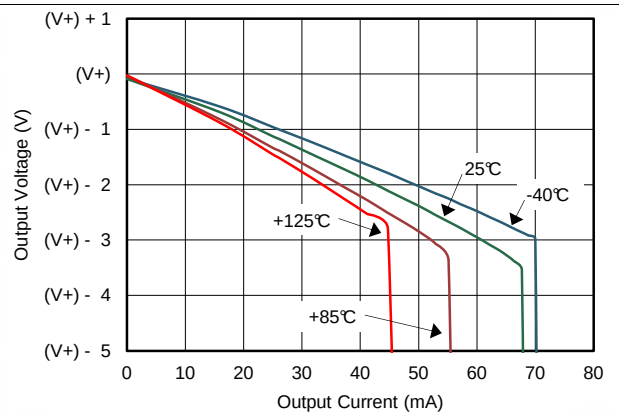


Figure 15. Output Voltage Swing from Positive Power Supply vs Output Current (Maximum Supply)

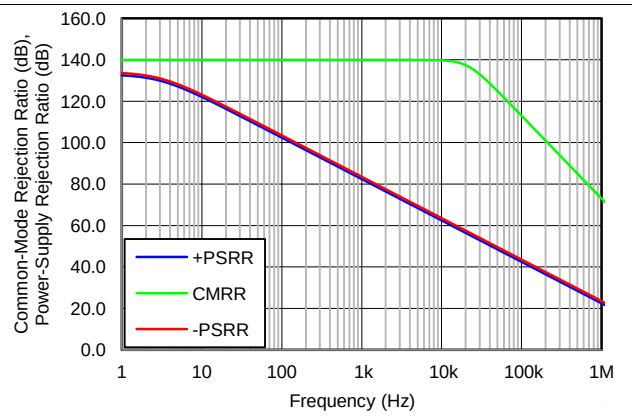


Figure 16. CMRR and PSRR vs Frequency

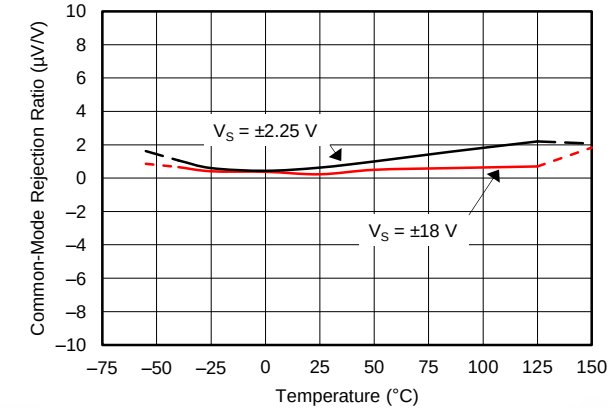


Figure 17. CMRR vs Temperature

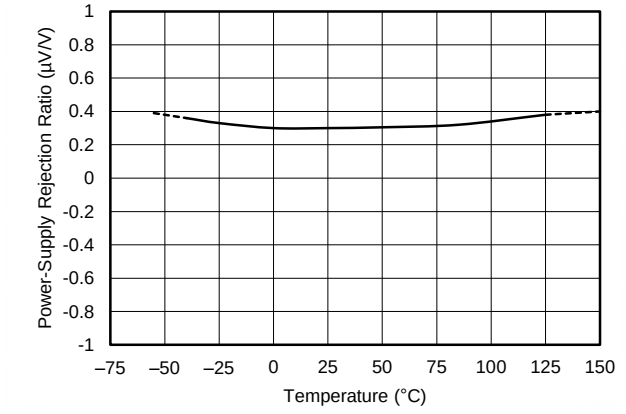
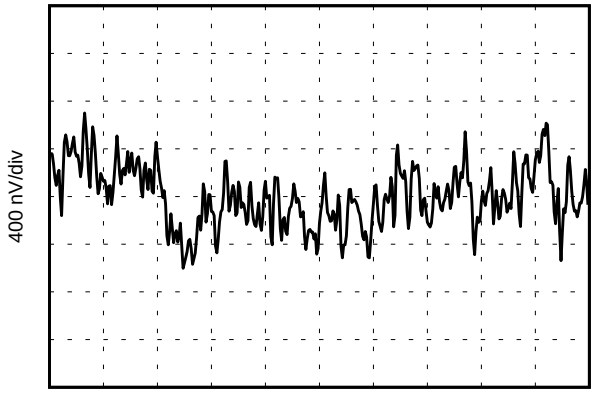


Figure 18. PSRR vs Temperature

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



Peak-to-peak noise = V_{RMS} × 6.6 = 1.30 V_{PP}

Figure 19. 0.1-Hz to 10-Hz Noise

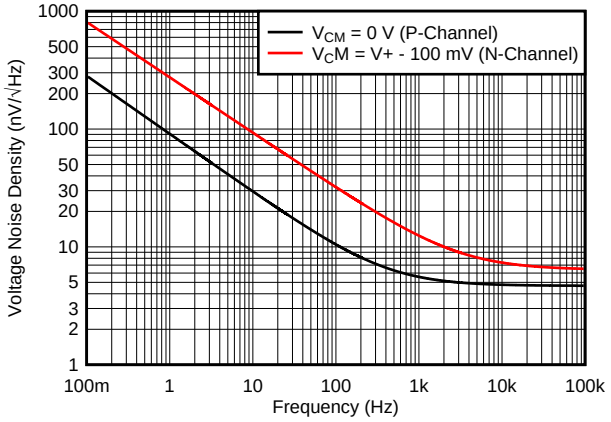
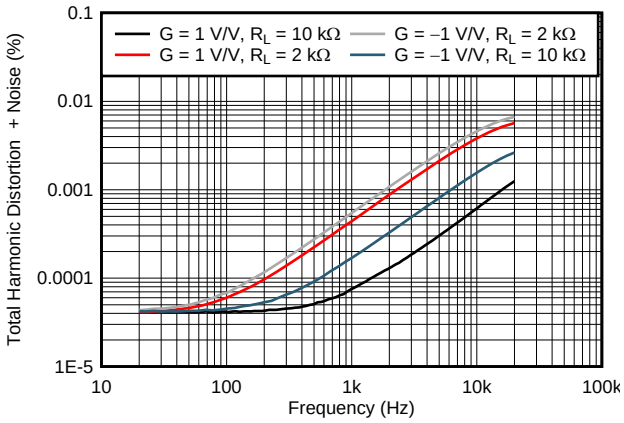
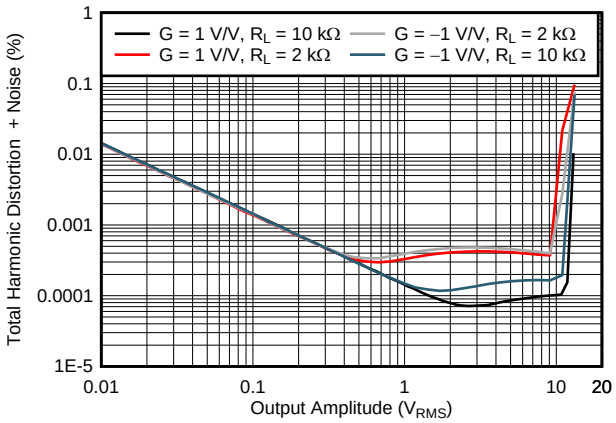


Figure 20. Input Voltage Noise Spectral Density vs Frequency



V_{OUT} = 3.5 V_{RMS}, BW = 80 kHz

Figure 21. THD+N Ratio vs Frequency



f = 1 kHz, BW = 80 kHz

Figure 22. THD+N vs Output Amplitude

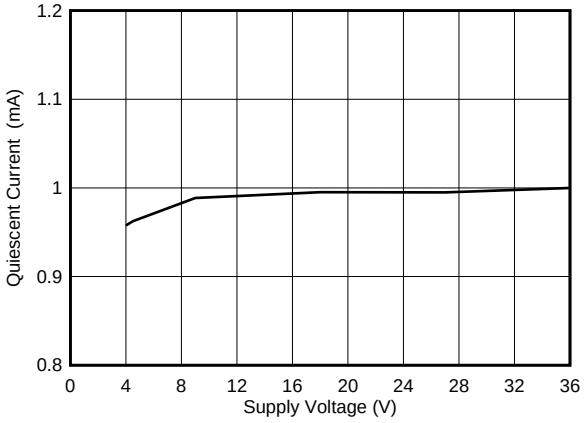


Figure 23. Quiescent Current vs Supply Voltage

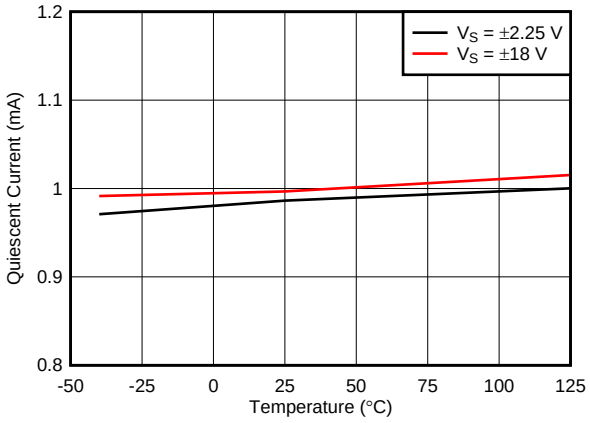


Figure 24. Quiescent Current vs Temperature

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

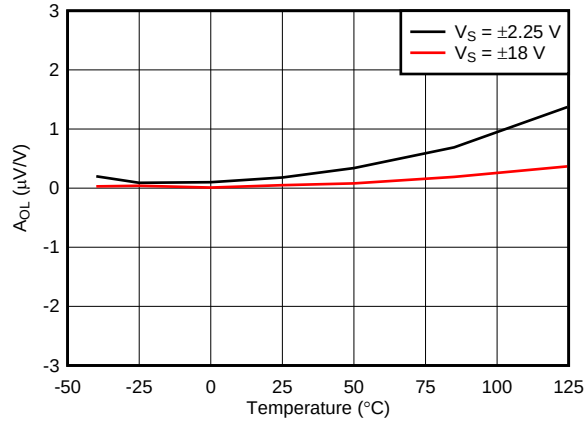


Figure 25. Open-Loop Gain vs Temperature

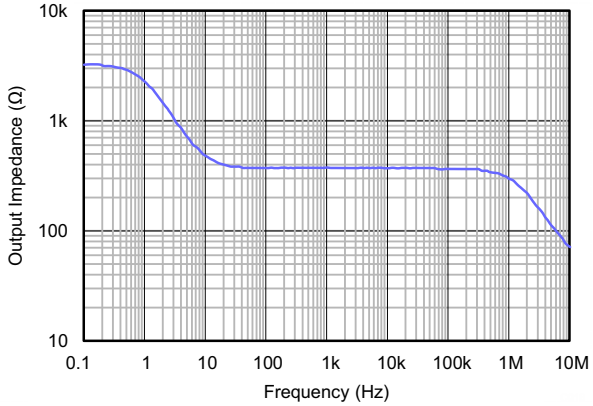
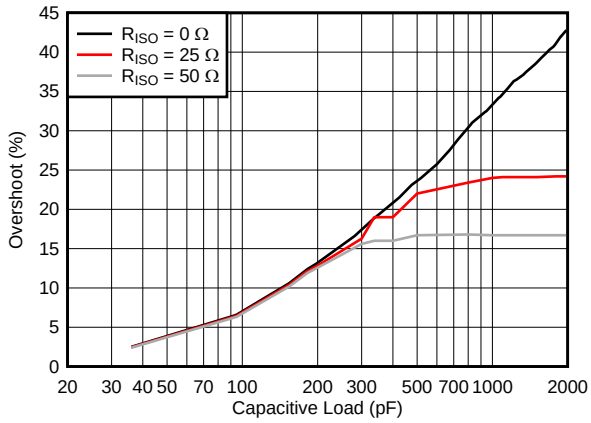
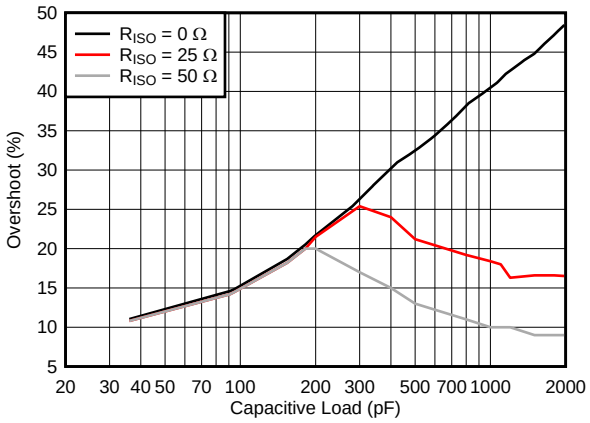


Figure 26. Open-Loop Output Impedance vs Frequency



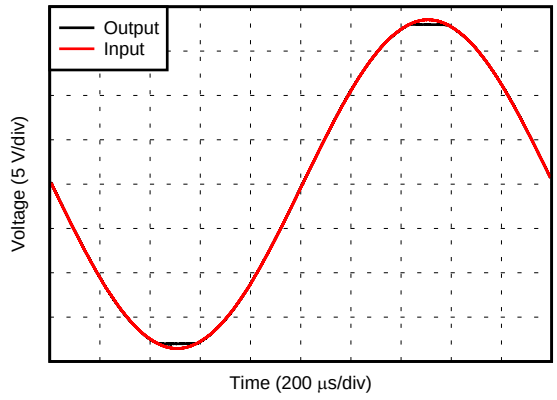
G = –1 V/V

Figure 27. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



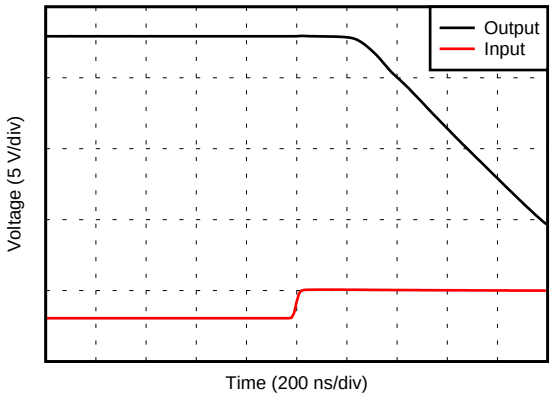
G = 1 V/V

Figure 28. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



V_S = ±18 V, input = ±18.5 V_{PP}

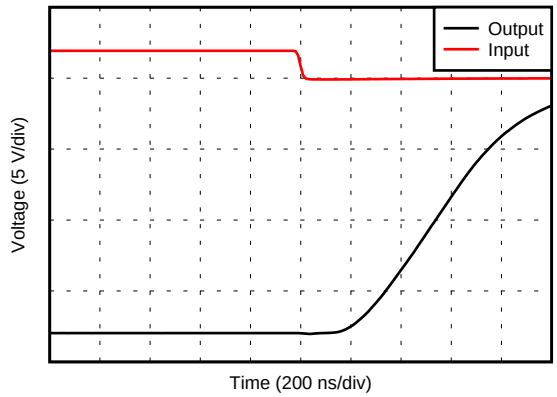
Figure 29. No Phase Reversal



G = –10 V/V

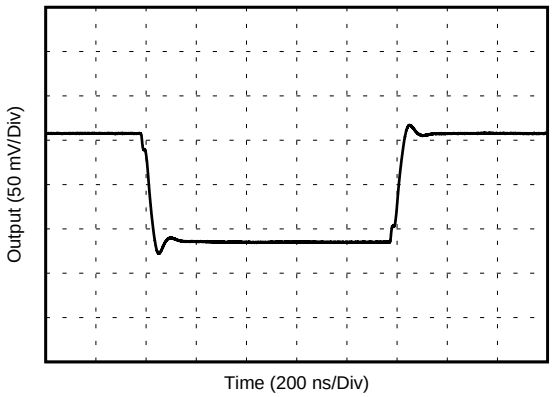
Figure 30. Positive Overload Recovery

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



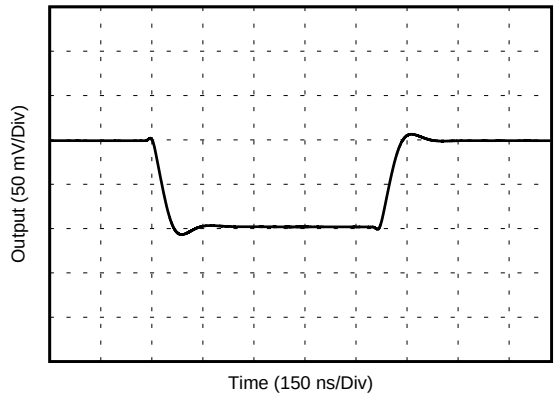
G = –10 V/V

Figure 31. Negative Overload Recovery



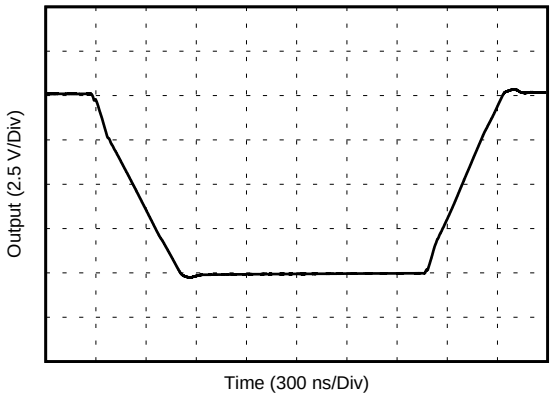
G = 1 V/V

Figure 32. Small-Signal Step Response



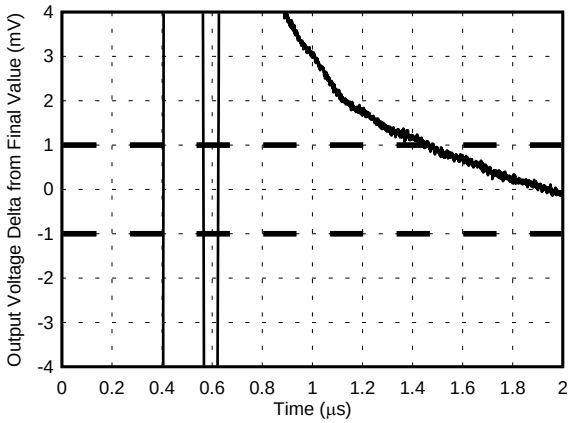
G = –1 V/V

Figure 33. Small-Signal Step Response



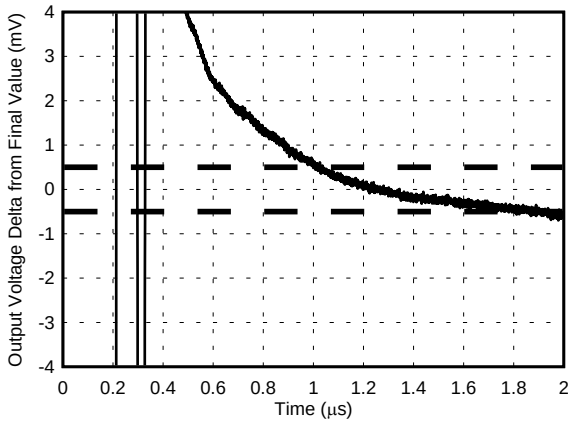
G = 1 V/V

Figure 34. Large-Signal Step Response



G = 1, 0.01% settling = ±1 mV, step applied at t = 0

Figure 35. Settling Time (10-V Positive Step)



G = 1, 0.01% settling = ±500 µV, step applied at t = 0

Figure 36. Settling Time (5-V Positive Step)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

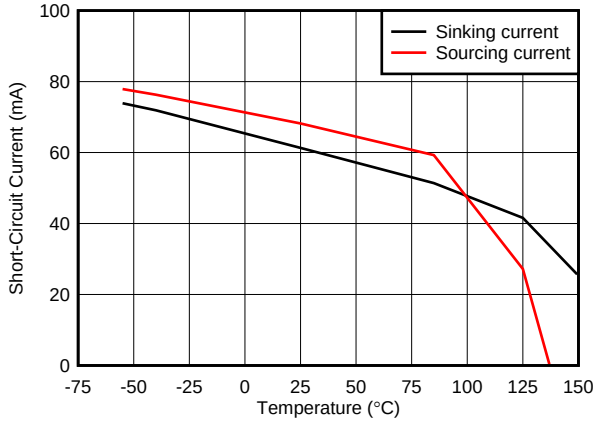


Figure 37. Short-Circuit Current vs Temperature

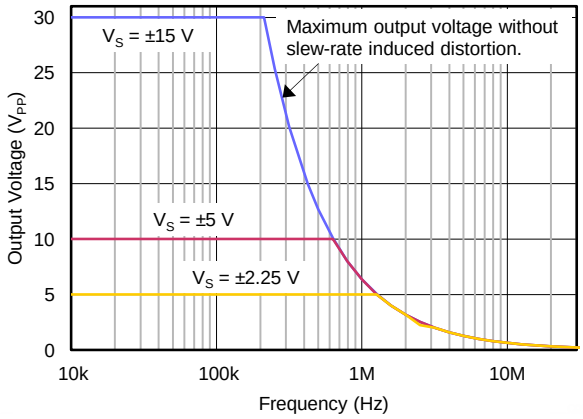


Figure 38. Maximum Output Voltage vs Frequency

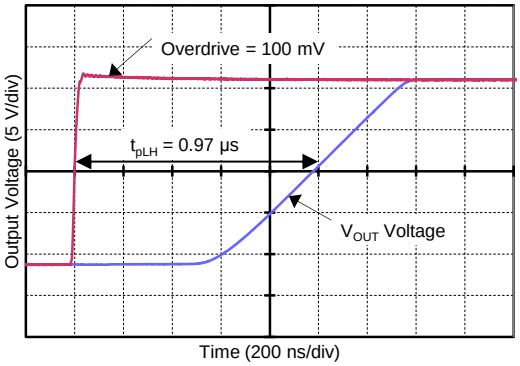


Figure 39. Propagation Delay Rising Edge

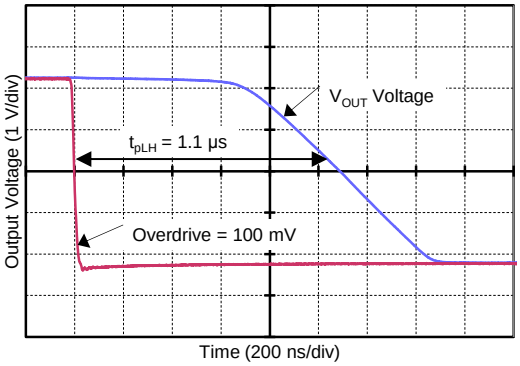


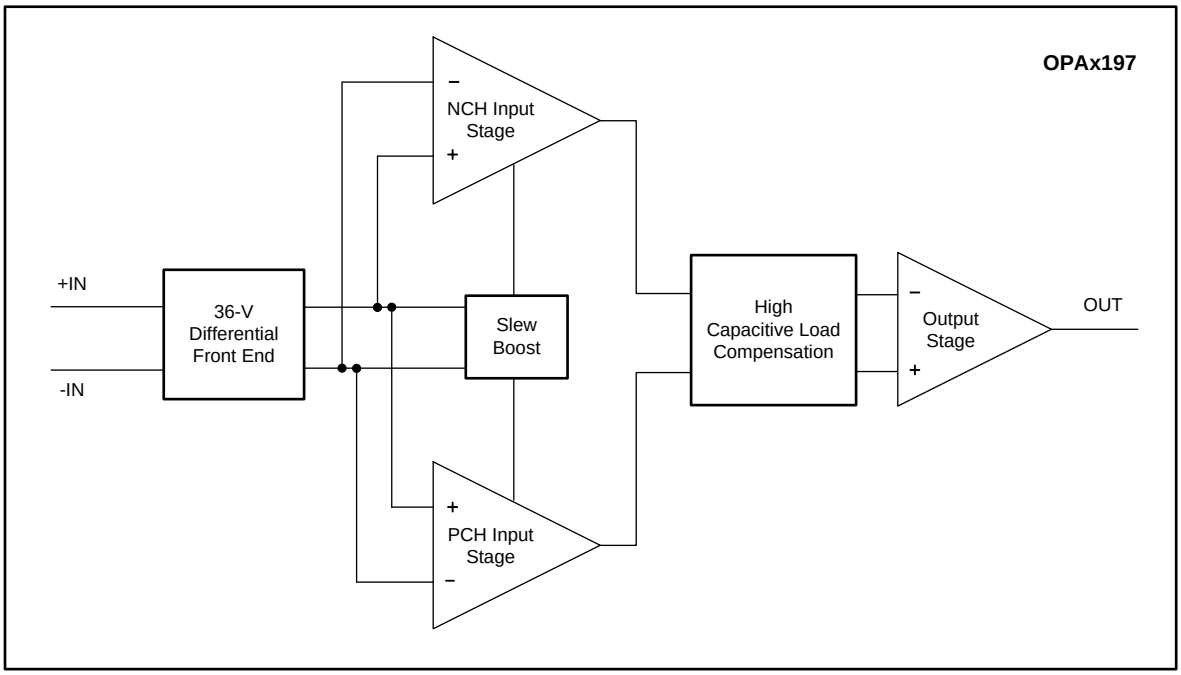
Figure 40. Propagation Delay Falling Edge

7 Detailed Description

7.1 Overview

The OPAx197 uses a patented two-temperature trim architecture to achieve a very low offset voltage of 250 µV (max) and low voltage offset drift of 0.75 µV/°C (maximum) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The OPAx197 uses a unique input architecture to eliminate the need for input protection diodes, but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 41 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 42. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current, and resulting in extended settling time, as shown in Figure 43.

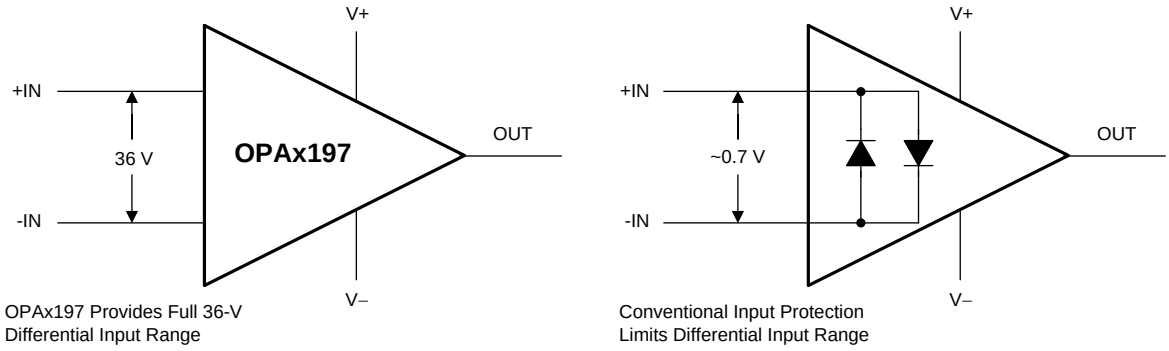


Figure 41. OPA197 Input Protection Does Not Limit Differential Input Capability

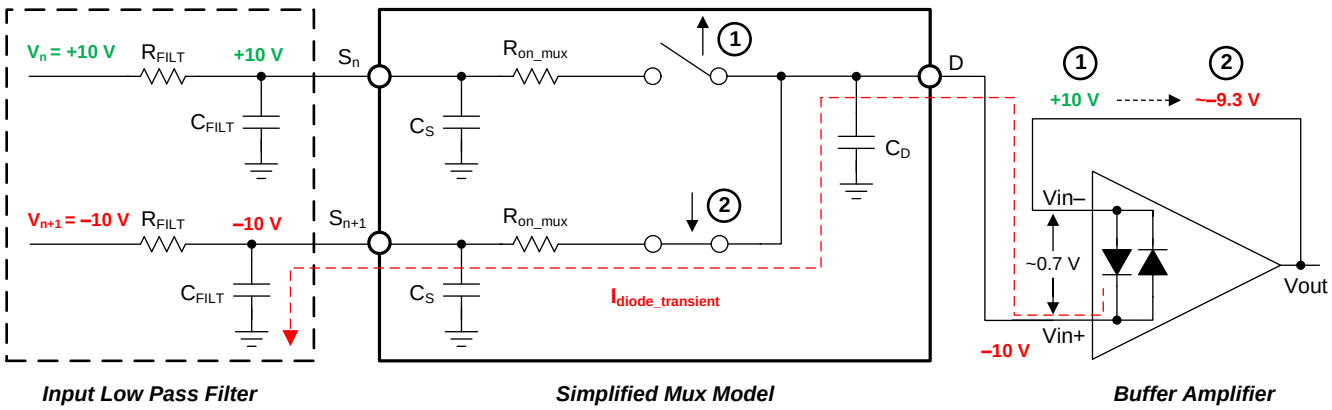


Figure 42. Back-to-Back Diodes Create Settling Issues

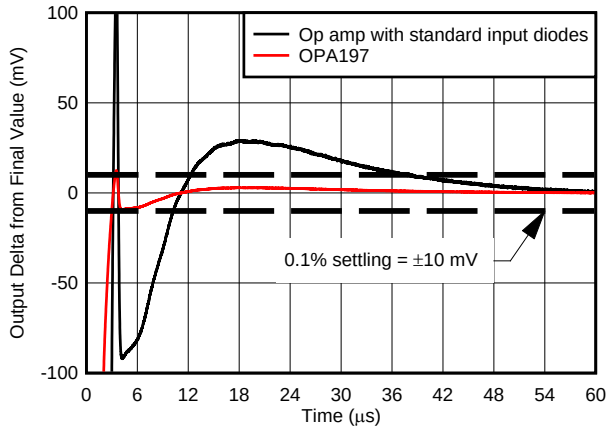


Figure 43. OPA197 Protection Circuit Maintains Fast-Settling Transient Response

Feature Description (continued)

The OPAx197 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA197 can tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems, as shown in Figure 53.

7.3.2 EMI Rejection

The OPAx197 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx197 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 44 shows the results of this testing on the OPA197. Table 2 shows the EMIRR IN+ values for the OPA197 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the application report *EMI Rejection Ratio of Operational Amplifiers*, SBOA128, available for download from www.ti.com.

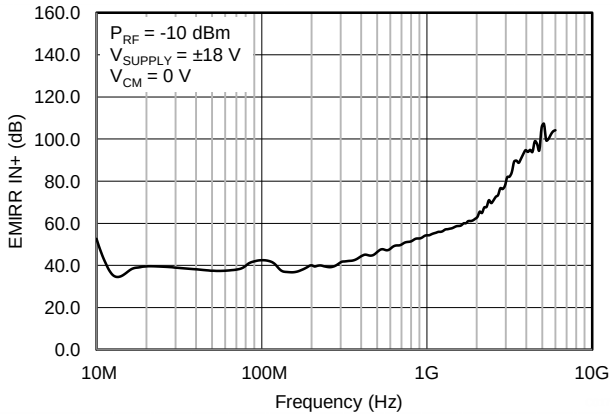


Figure 44. EMIRR Testing

Table 2. OPA197 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.0 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.5 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.7 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105.5 dB

7.3.3 Phase Reversal Protection

The OPAx197 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx197 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 45.

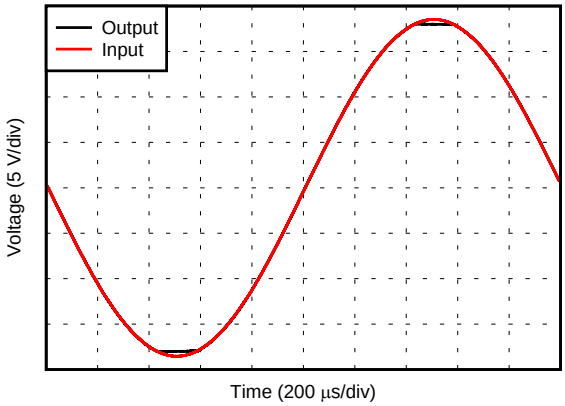


Figure 45. No Phase Reversal

7.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx197 is 150°C. Exceeding this temperature causes damage to the device. The OPAx197 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 46 shows an application example for the OPA197 that has significant self heating (159°C) because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 46 depicts how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

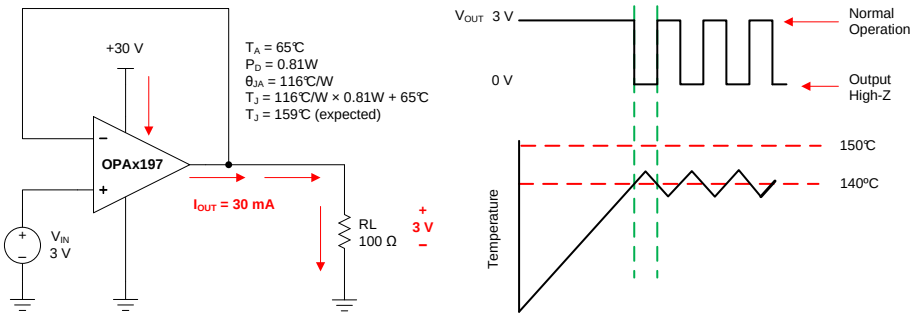


Figure 46. Thermal Protection

7.3.5 Capacitive Load and Stability

The OPAx197 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 47 and Figure 48. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

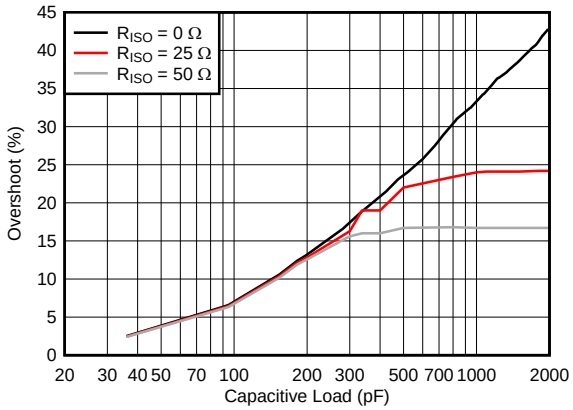


Figure 47. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = –1 V/V)

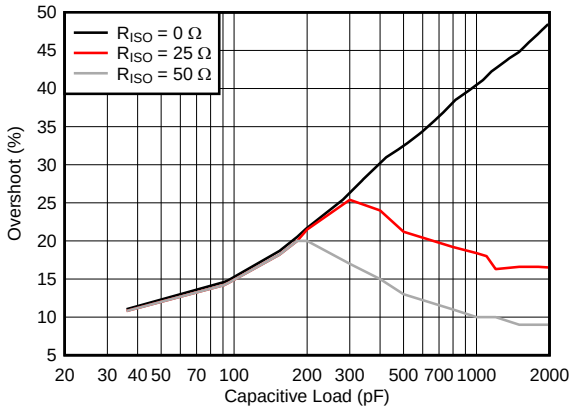


Figure 48. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = 1 V/V)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10-Ω to 20-Ω) resistor, R_{ISO}, in series with the output, as shown in Figure 49. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPA197 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 49 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin, and results using the OPA197 are summarized in Table 3. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

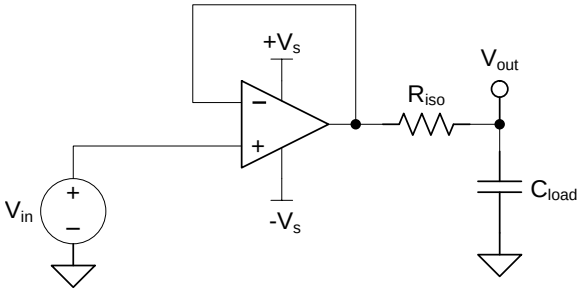


Figure 49. Extending Capacitive Load Drive with the OPA197

Table 3. OPA197 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE									
Capacitive Load	100 pF		1000 pF		0.01 µF		0.1 µF		1 µF	
Phase Margin	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°
R_{ISO} (Ω)	47.0	360.0	24.0	100.0	20.0	51.0	6.2	15.8	2.0	4.7
Measured Overshoot (%)	23.2 8.6	10.4	22.5	9.0	22.1	8.7	23.1	8.6	21.0	8.6
Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDU032, *Capacitive Load Drive Solution using an Isolation Resistor* .

7.3.6 Common-Mode Voltage Range

The OPAx197 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 50. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation outside this region.

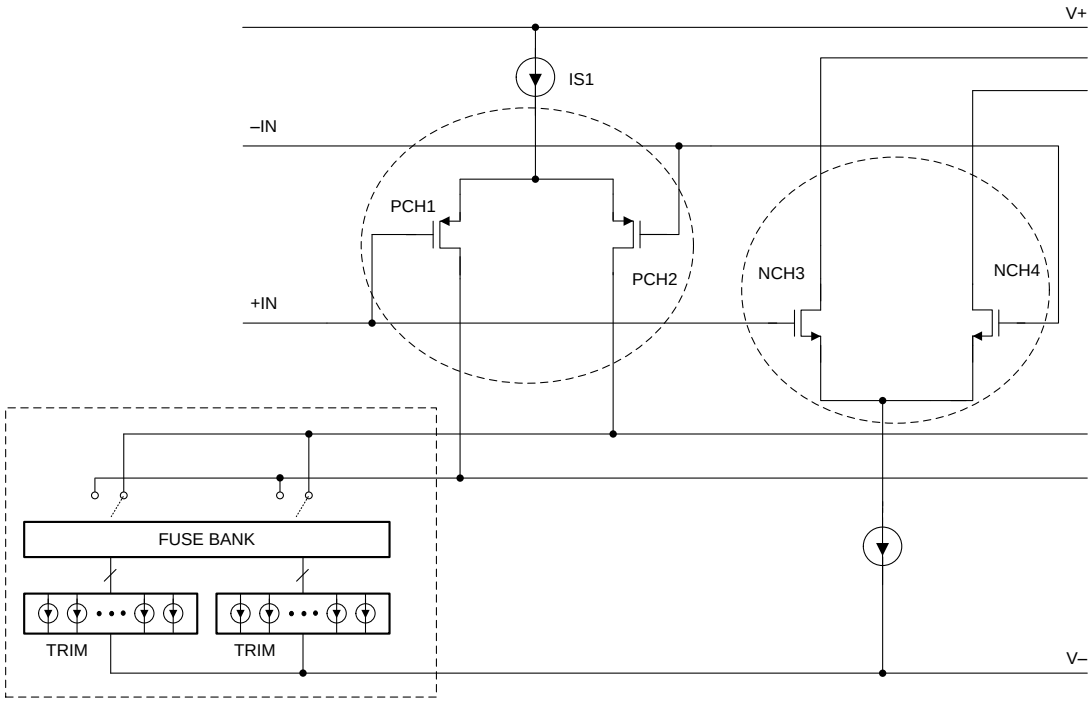


Figure 50. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx197 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode voltage range, as shown in Figure 51.

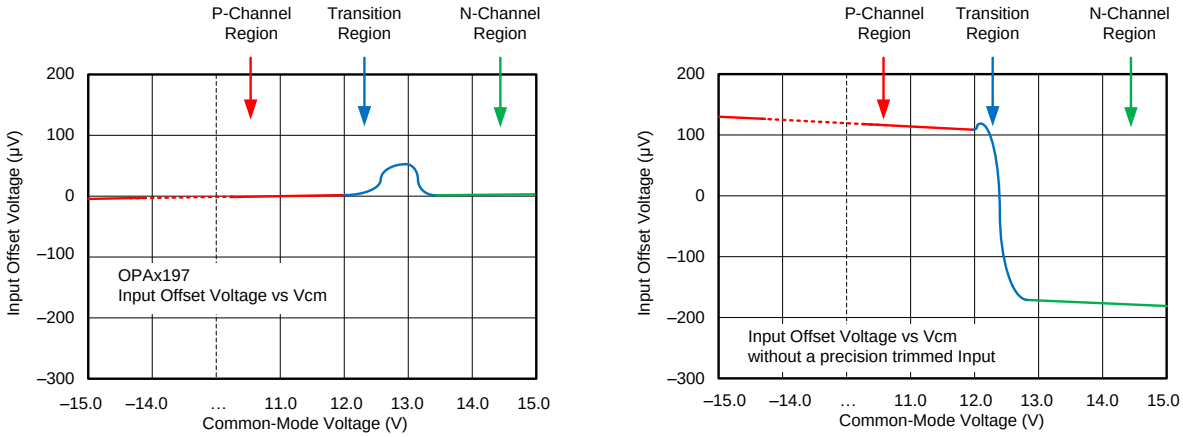


Figure 51. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 52 for an illustration of the ESD circuits contained in the OPAx197 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

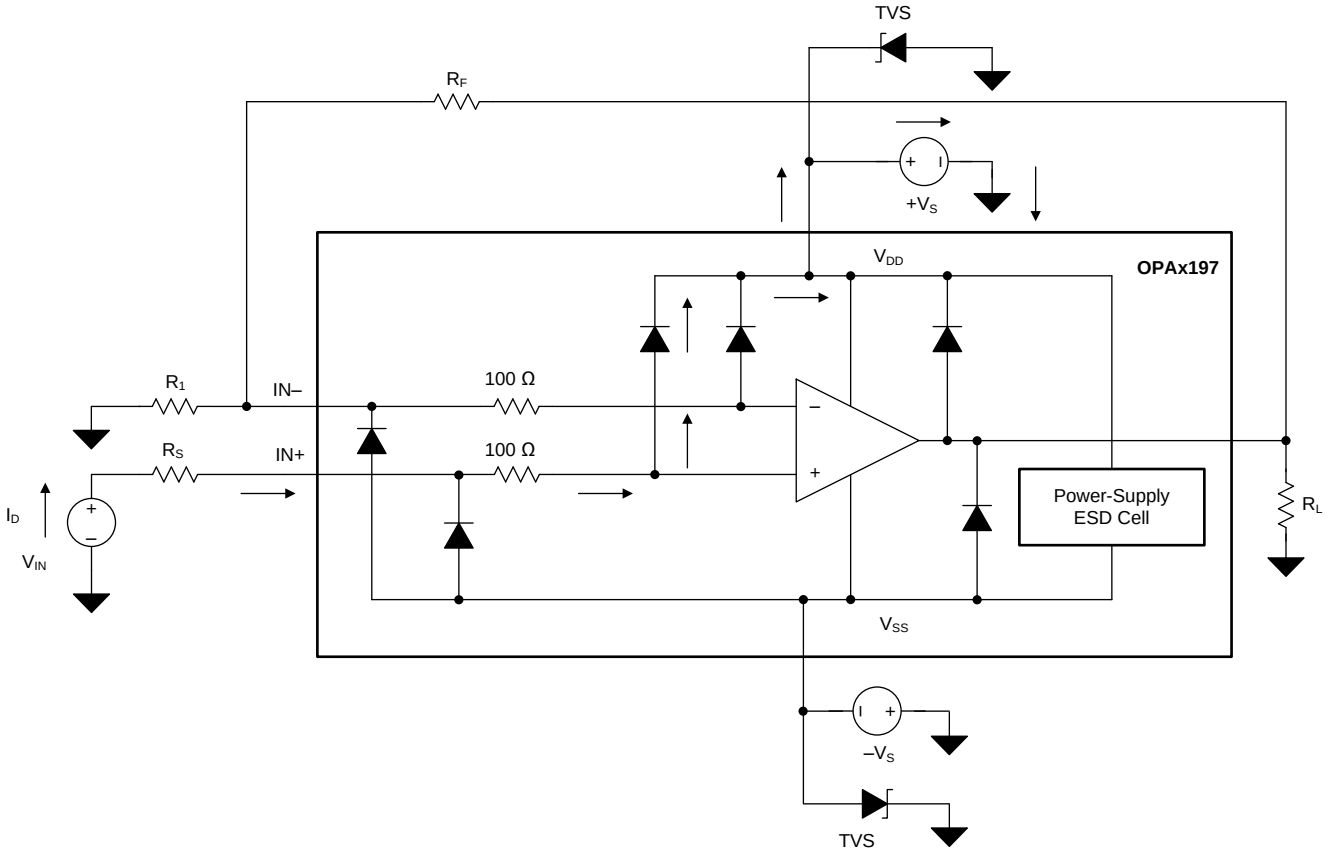


Figure 52. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx197 is approximately 200 ns.

7.4 Device Functional Modes

The OPAx197 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx197 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx197 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input/output, ultralow offset voltage and offset voltage drift, as well as 10-MHz bandwidth and high capacitive load drive. These features make the OPAx197 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 16-Bit Precision Multiplexed Data-Acquisition System

Figure 53 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This application example explains the process for optimizing the precision, high-voltage, front-end drive circuit using the OPA197 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

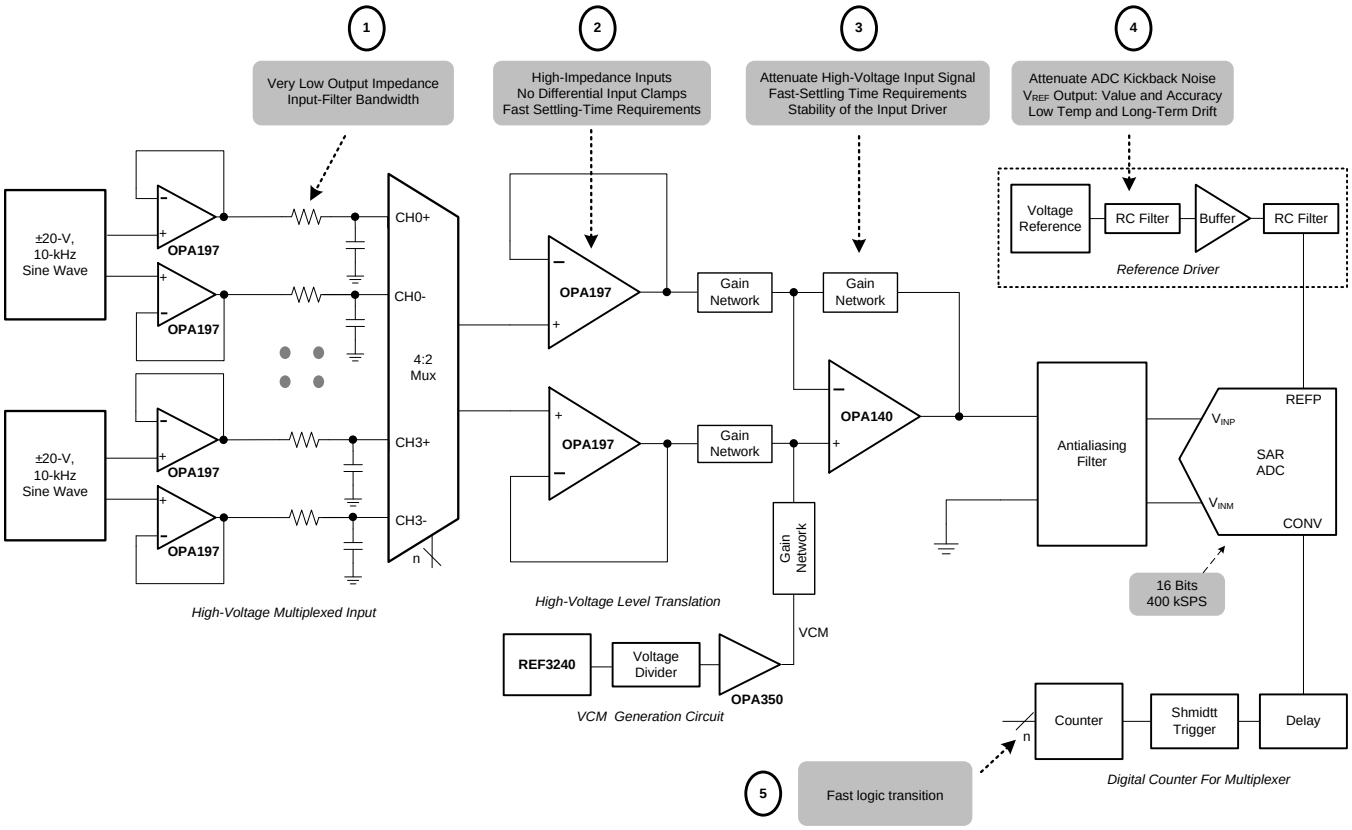


Figure 53. OPA197 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

Typical Applications (continued)

8.2.1.1 Design Requirements

The primary objective is to design a ±20 V, differential 4-channel multiplexed data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10 kHz full-scale pure sine-wave input. The design requirements for this block design are:

- System Supply Voltage: ±15 V
- ADC Supply Voltage: 3.3 V
- ADC Sampling Rate: 400 kSPS
- ADC Reference Voltage (REFP): 4.096 V
- System Input Signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

8.2.1.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal high voltage multiplexed data acquisition system for highest system linearity and fast settling. The overall system block diagram is shown in Figure 53. The circuit is a multichannel data acquisition signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for mux and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision multiplexed data acquisition system are the mux input analog front-end and the high-voltage level translation SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. The diagram includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely low impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input while maintaining the amplifier stability. The next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

8.2.1.3 Application Curve

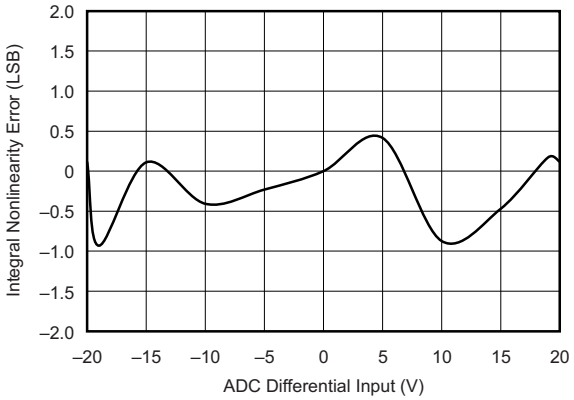


Figure 54. ADC 16-Bit Linearity Error for the Multiplexed Data Acquisition Block

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU181, *16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion*.

8.2.2 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx197 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems.Figure 55 shows the OPA197 in a slew-rate limit design.

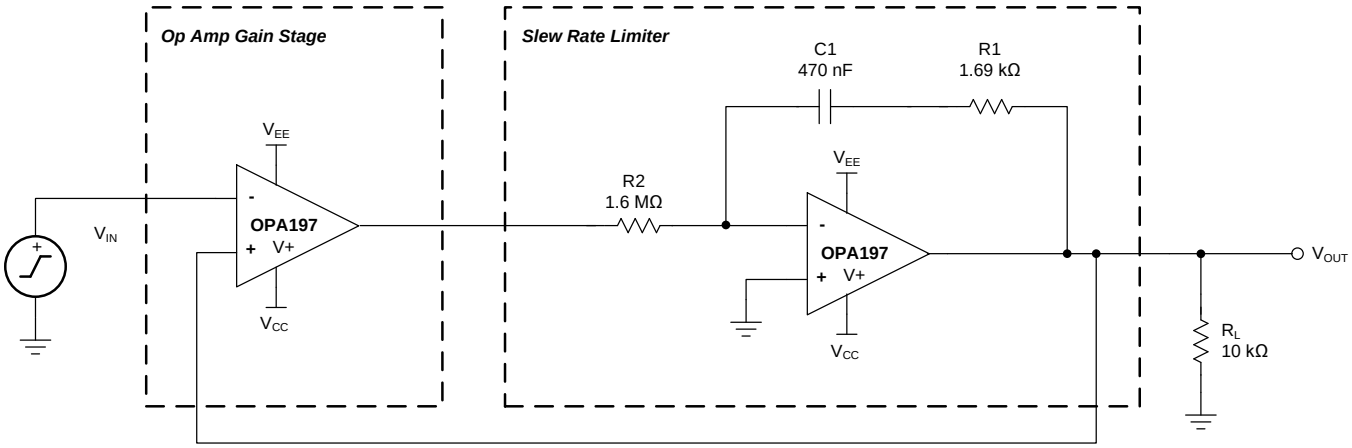


Figure 55. Slew Rate Limiter Uses One Op Amp

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU026, *Slew Rate Limiter Uses One Op Amp*.

8.2.3 Precision Reference Buffer

The OPAx197 features high output current drive capability and low input offset voltage, making the device an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10-µF ceramic capacitor shown in Figure 56, R_{ISO}, a 37.4-Ω isolation resistor, provides separation of two feedback paths for optimal stability. Feedback path number one is through R_F and is directly at the output, V_{OUT}. Feedback path number two is through R_{Fx} and C_F and is connected at the output of the op amp. The optimized stability components shown for the 10-µF load give a closed-loop signal bandwidth at V_{OUT} of 4 kHz, while still providing a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: R_F, R_{Fx}, C_F, and R_{ISO}.

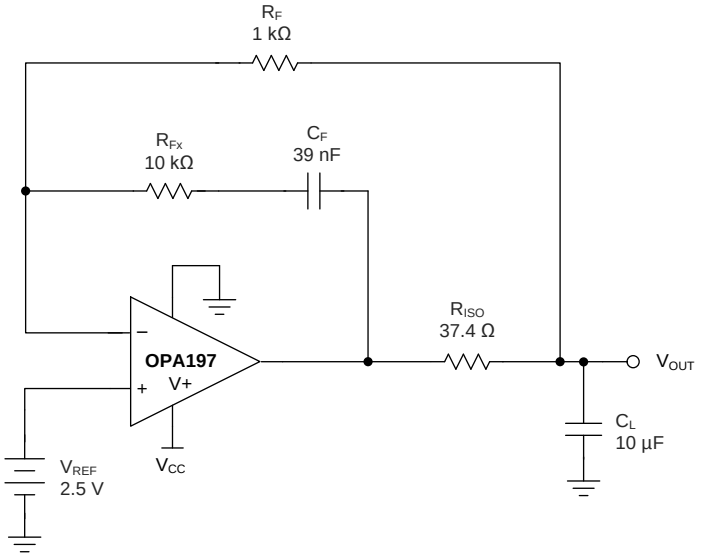


Figure 56. Precision Reference Buffer

9 Power Supply Recommendations

The OPAx197 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

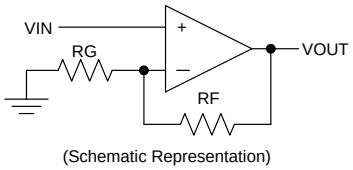
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 57, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



(Schematic Representation)

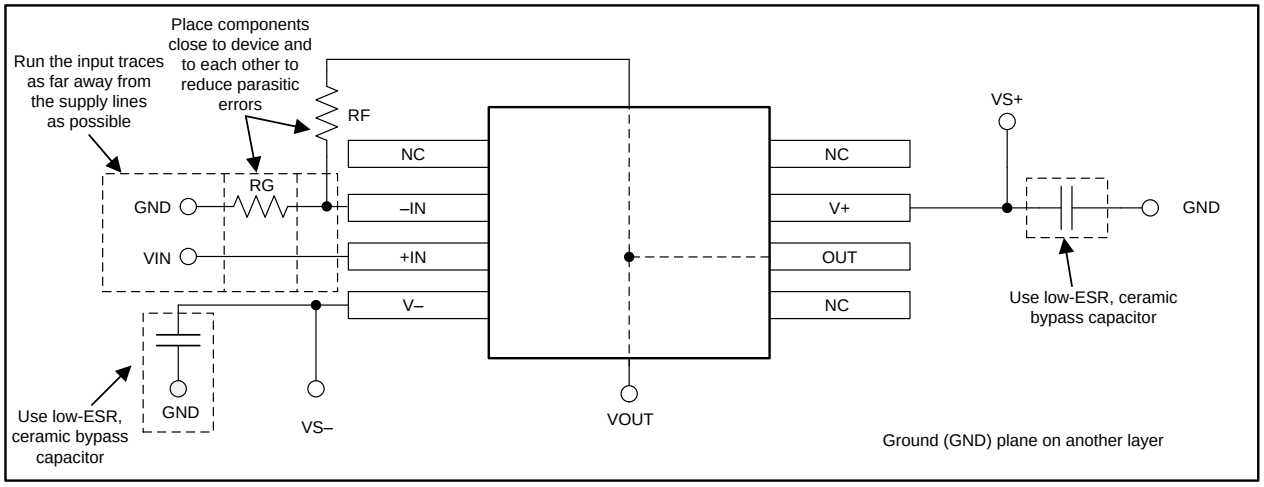


Figure 57. Operational Amplifier Board Layout for Noninverting Configuration

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

11.1.1.2 TI Precision Designs

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11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『基板のレイアウト技法』*(SLOA089)
- *『誰でも使えるオペアンプ』*(SLOD006)

11.3 関連リンク

表 4 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA197	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2197	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4197	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

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11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.6 商標

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA197ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA197	Samples
OPA197IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12MV	Samples
OPA197IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12MV	Samples
OPA197IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12ST	Samples
OPA197IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12ST	Samples
OPA197IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA197	Samples
OPA2197ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2197	Samples
OPA2197IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4HV	Samples
OPA2197IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4HV	Samples
OPA2197IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2197	Samples
OPA4197ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4197	Samples
OPA4197IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4197	Samples
OPA4197IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	OPA4197	Samples
OPA4197IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	OPA4197	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

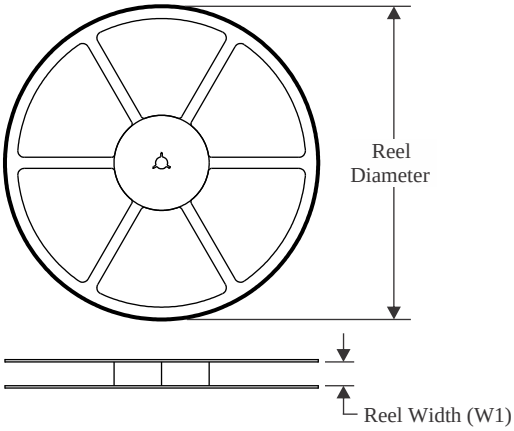
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

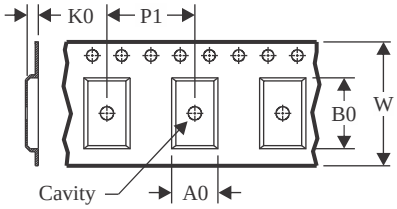
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

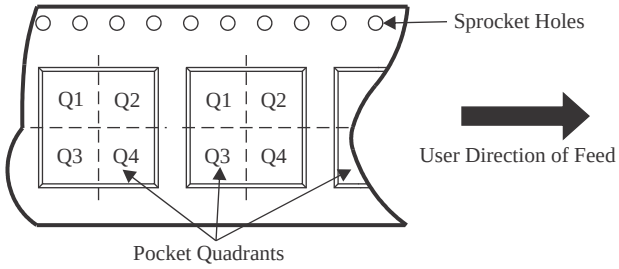


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

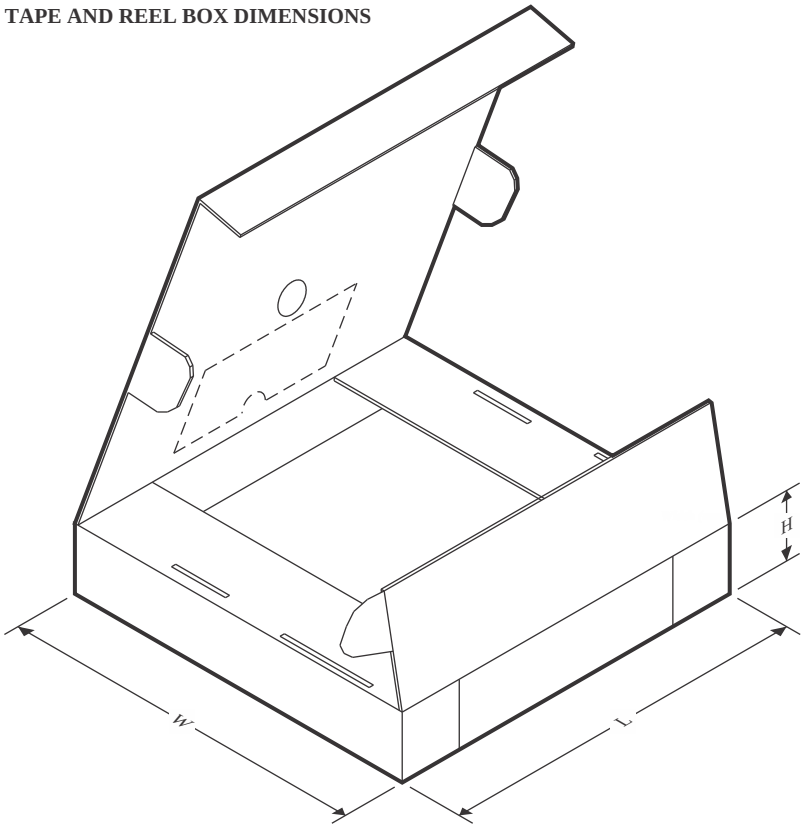
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA197IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA197IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA197IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA197IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA197IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2197IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2197IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2197IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4197IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4197IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

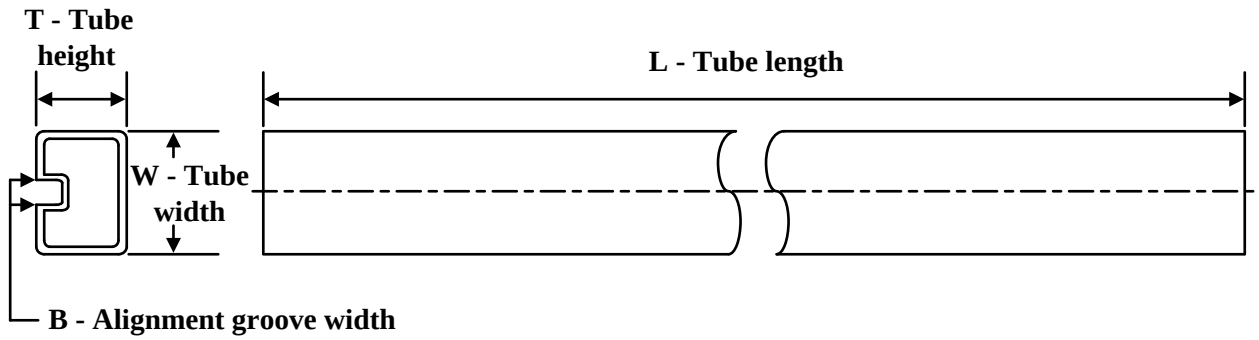
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

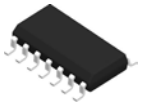
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA197IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA197IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA197IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA197IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
OPA197IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2197IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA2197IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
OPA2197IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4197IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4197IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA197ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2197ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4197ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4197IPW	PW	TSSOP	14	90	508	8.5	3250	2.8

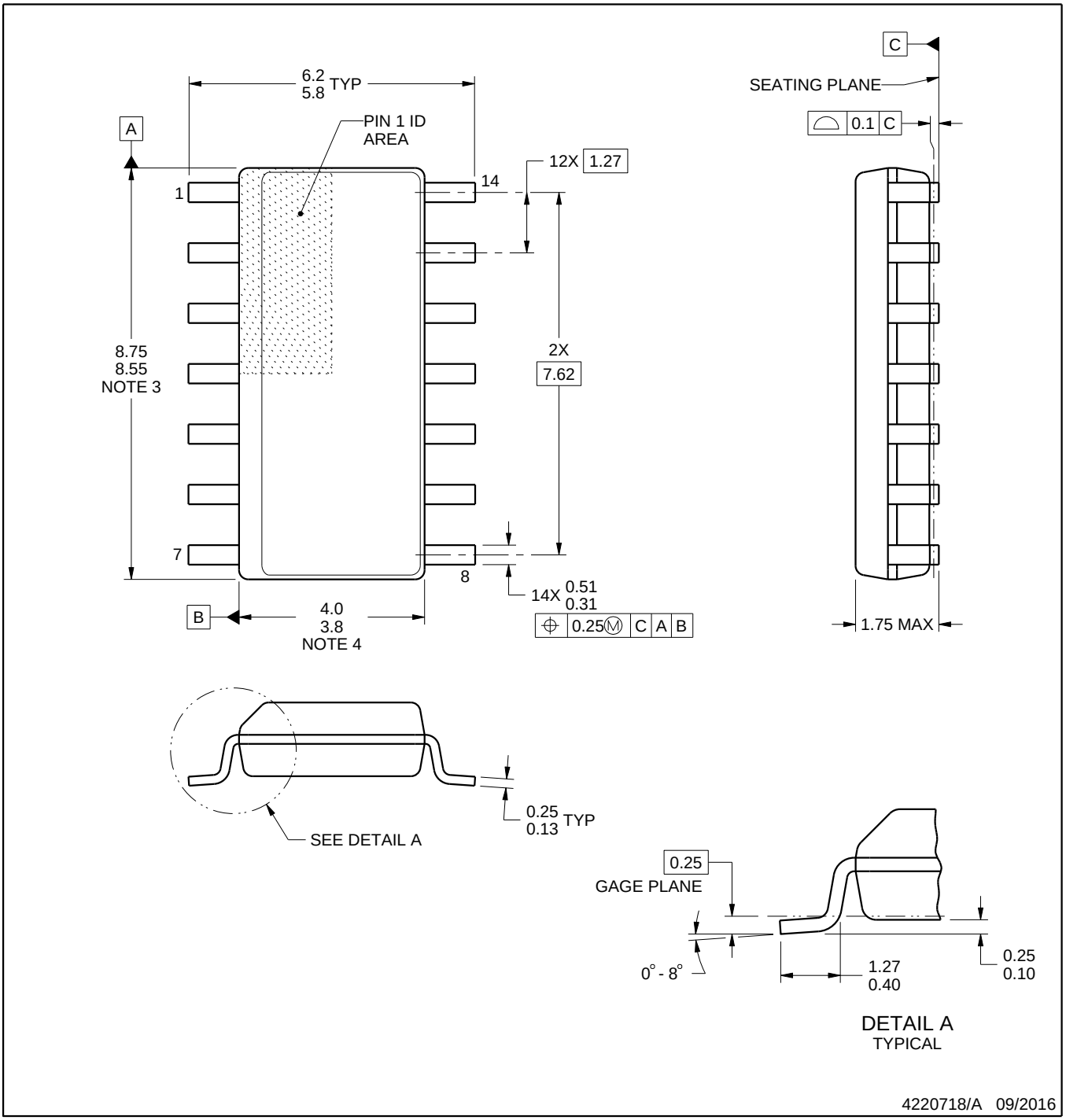


PACKAGE OUTLINE

D0014A

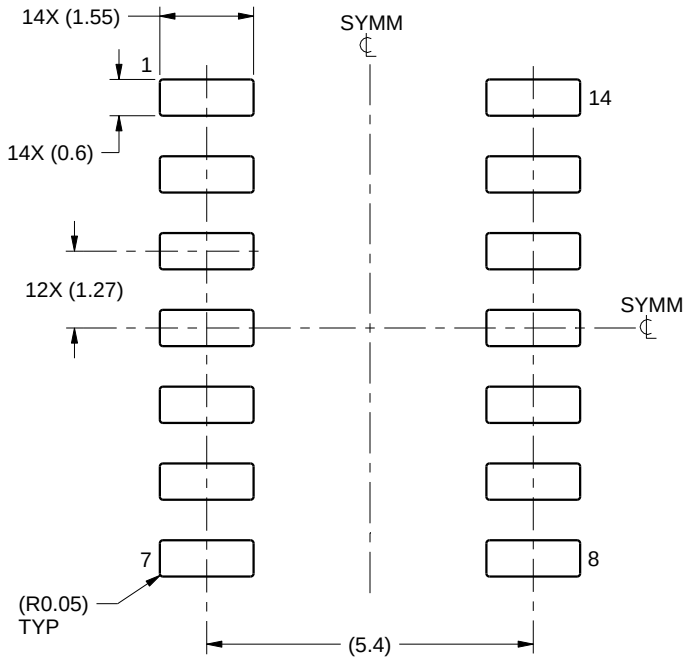
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

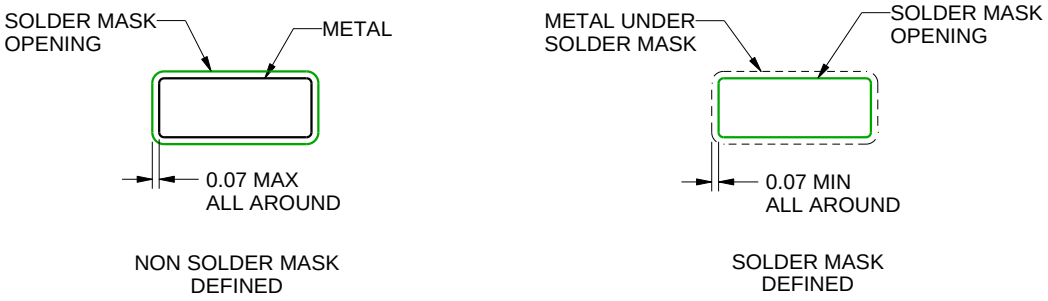


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

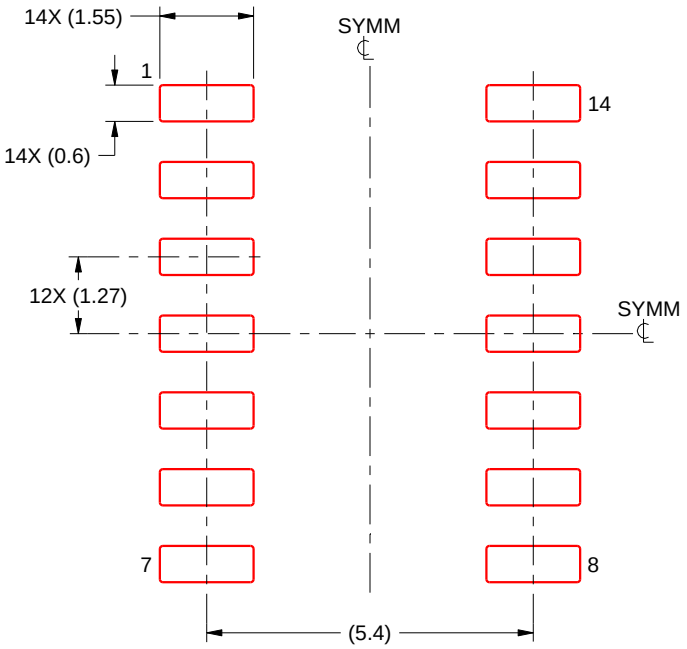
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

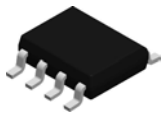


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

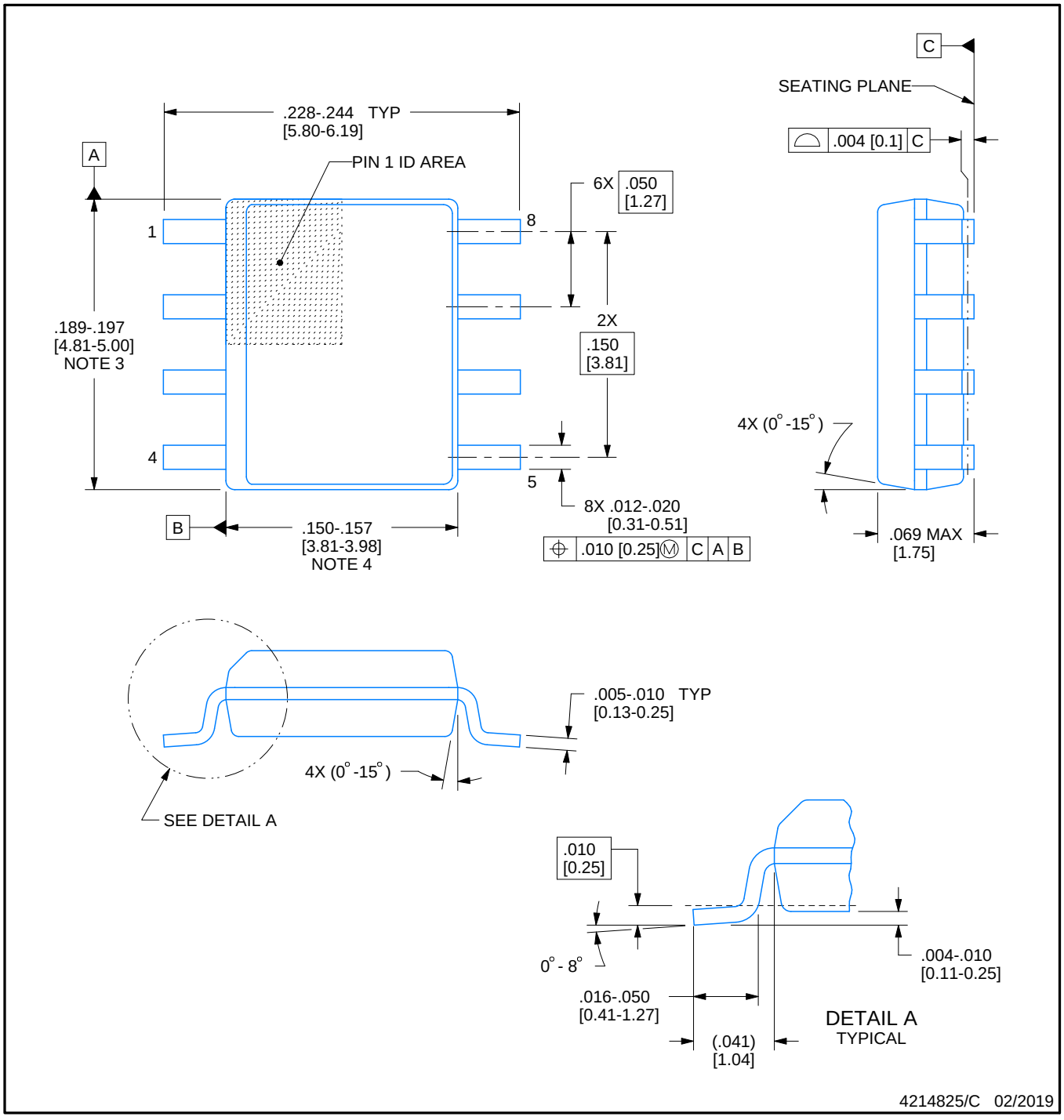


PACKAGE OUTLINE

D0008A

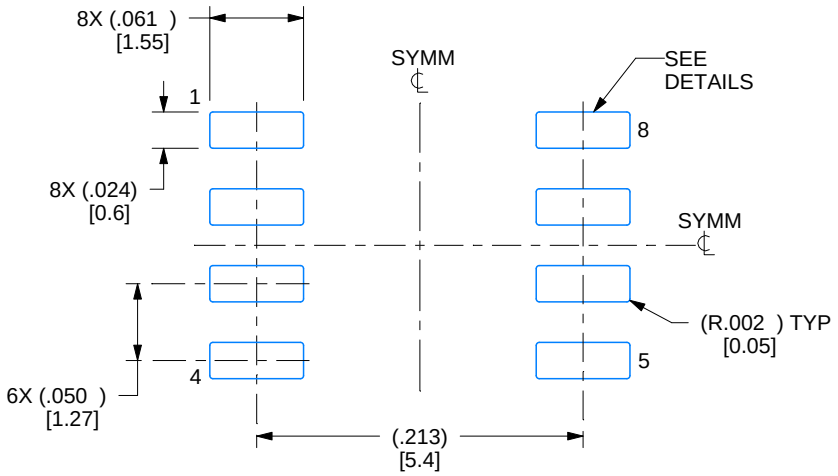
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

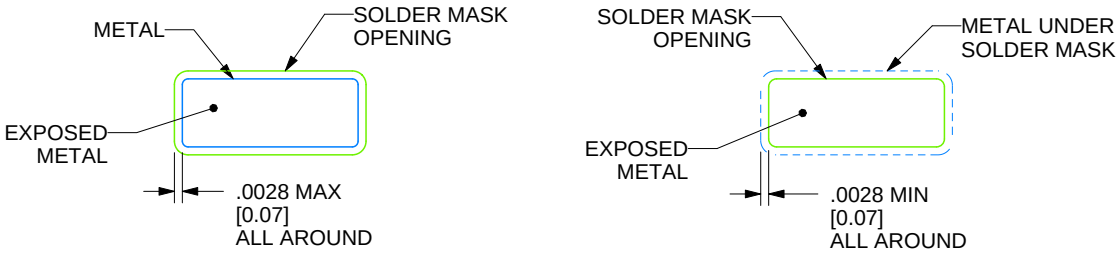


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

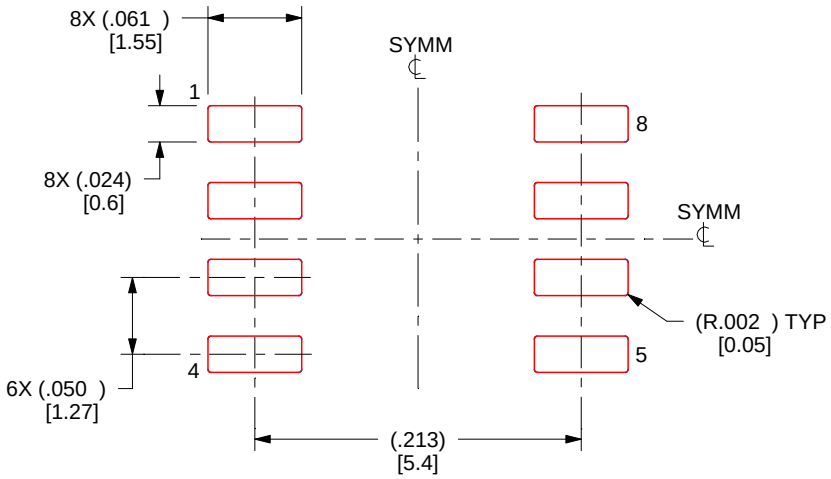
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

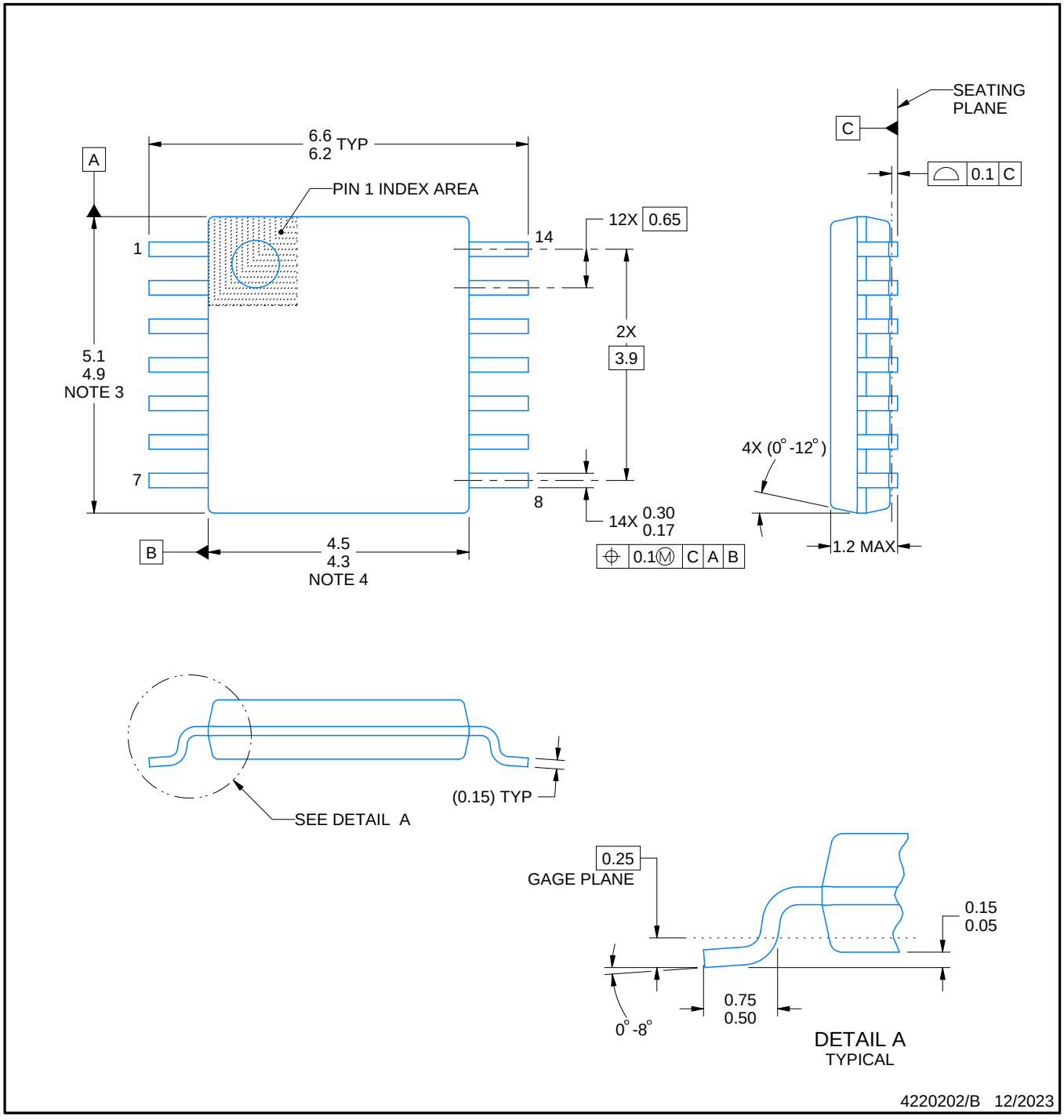
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

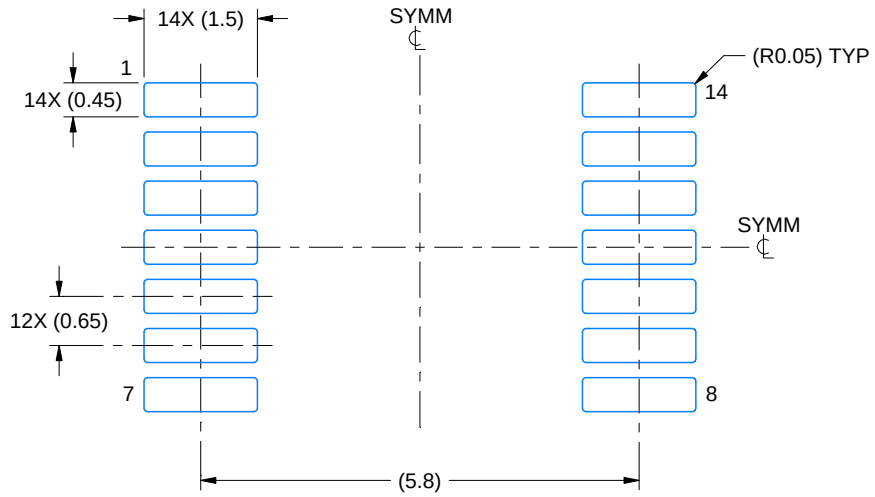
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

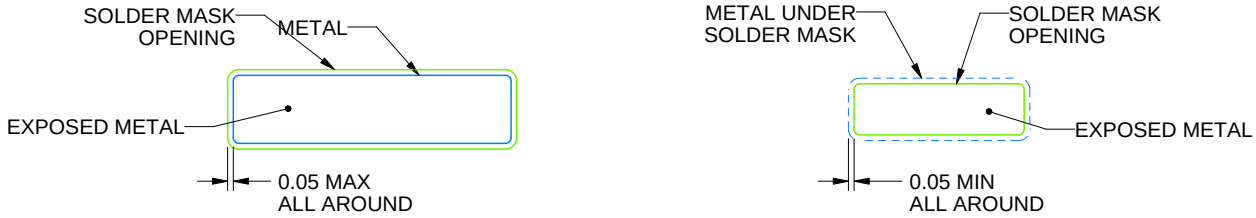


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

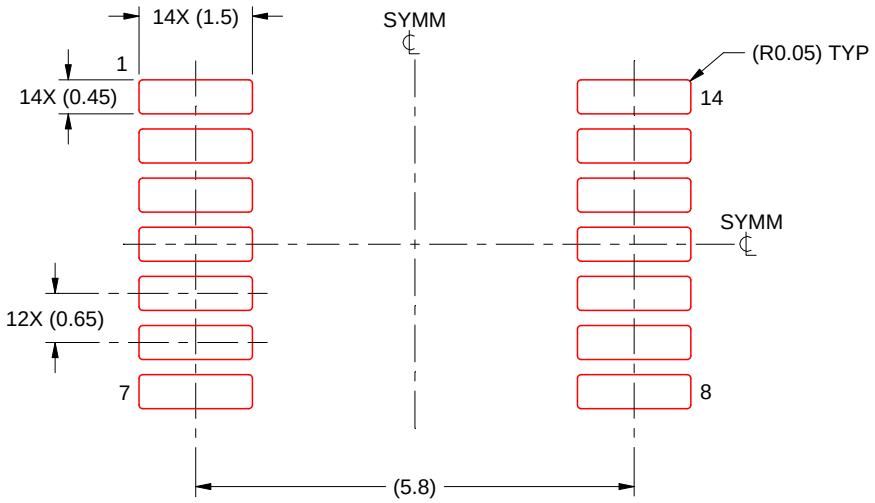


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

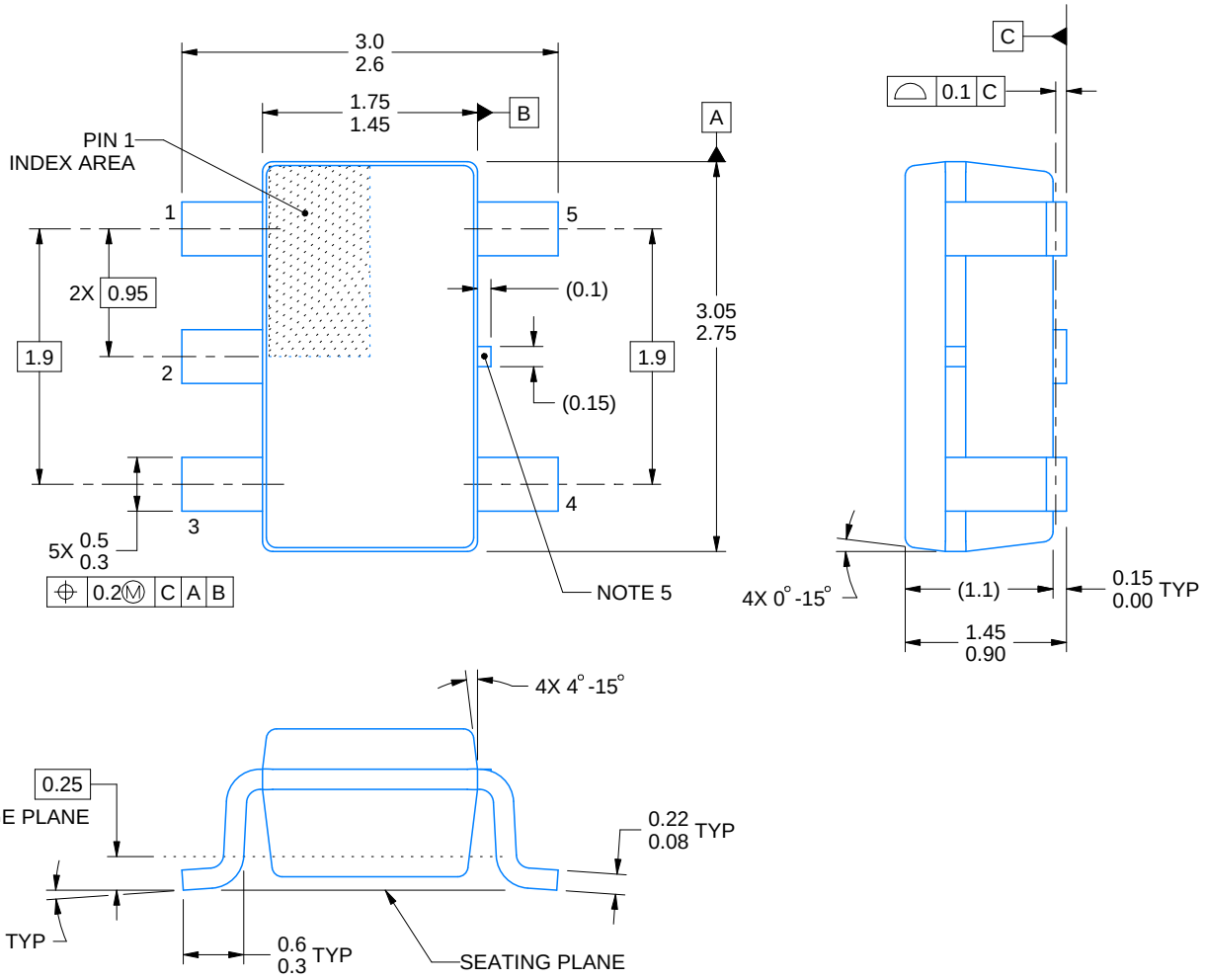
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

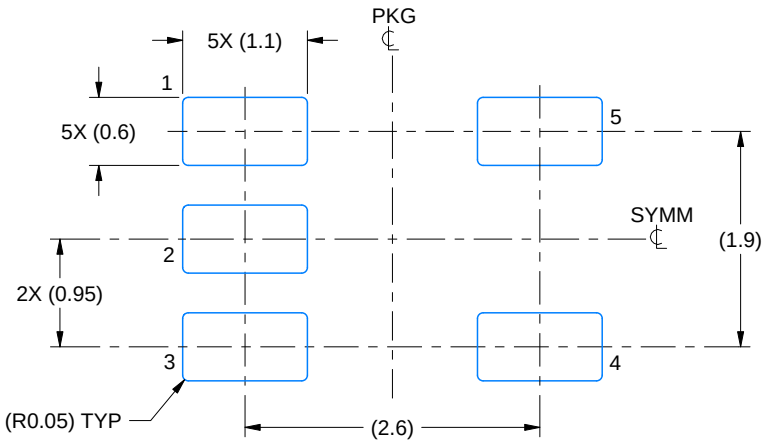
SMALL OUTLINE TRANSISTOR



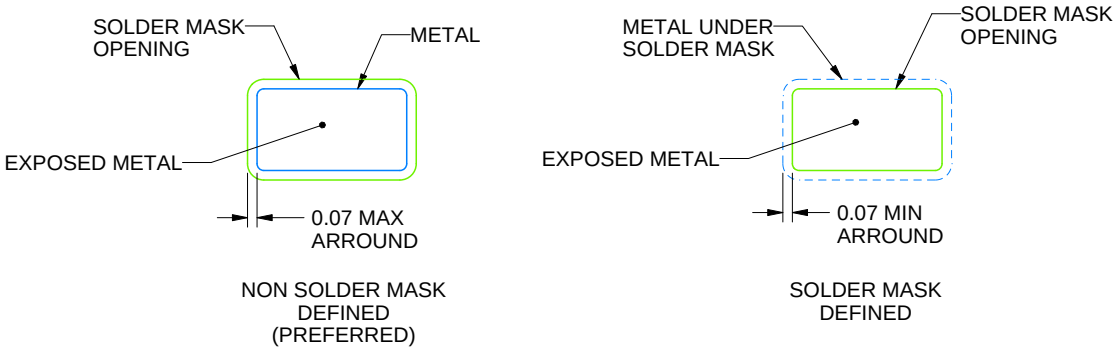
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

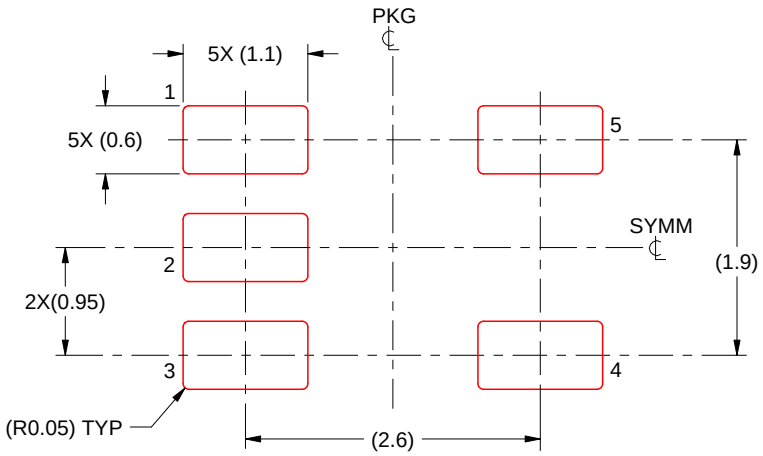


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

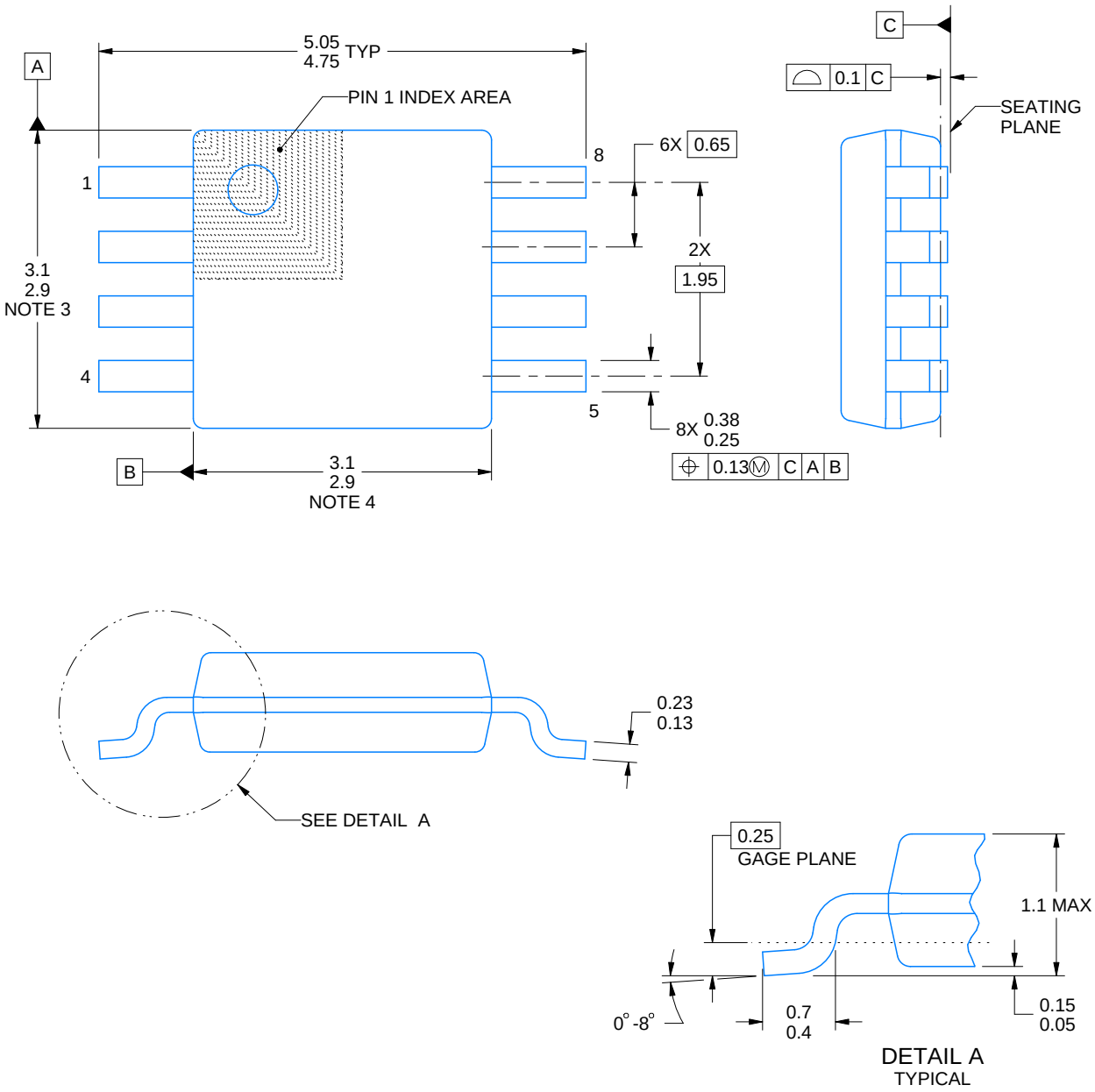
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

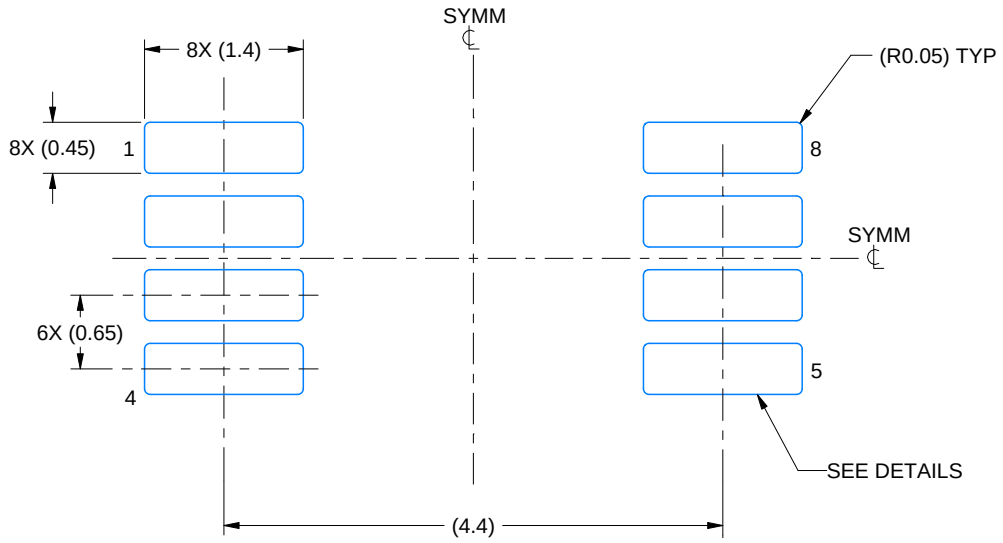
SMALL OUTLINE PACKAGE



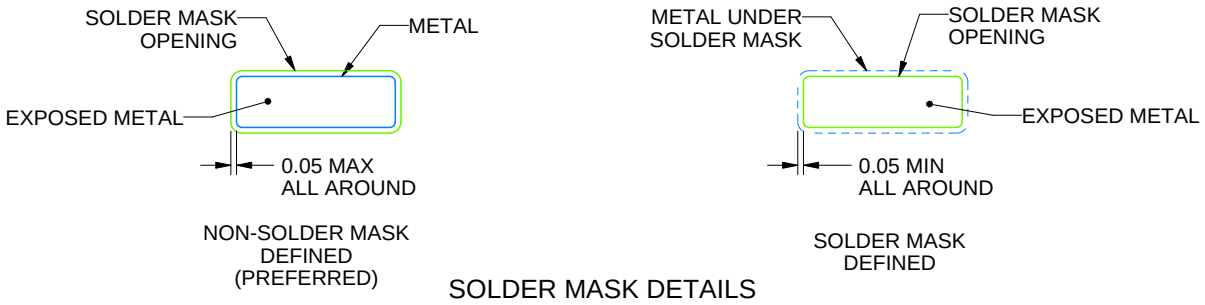
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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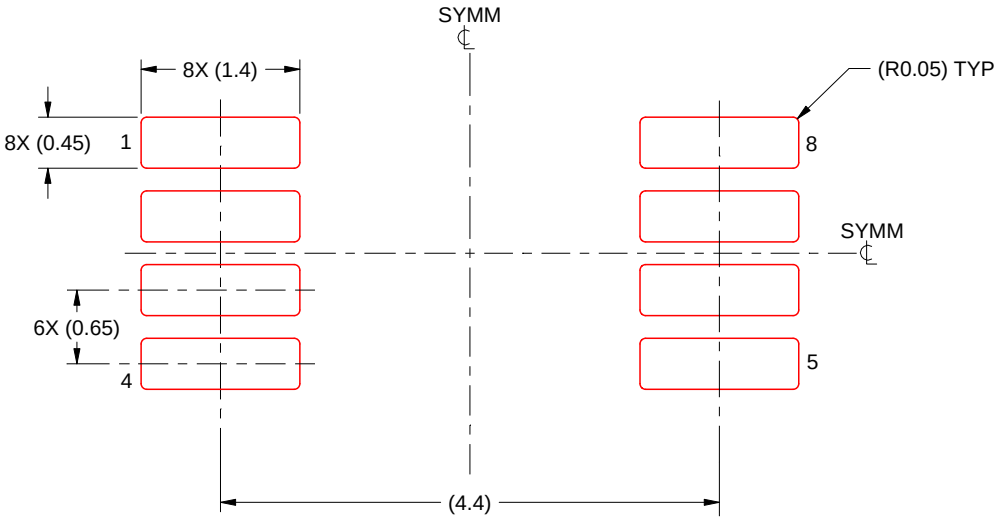
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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