TEXAS INSTRUMENTS
OPA4990-Q1
JAJSRQ2A – OCTOBER 2023 – REVISED FEBRUARY 2024

OPAx990-Q1 車載 40V レール ツー レール入出力、低オフセット電圧、低消費電力オペアンプ

1 特長

- 低いオフセット電圧:±300µV
- 低いオフセット電圧ドリフト:±0.6µV/℃
- 低ノイズ: 30 nV/√Hz1kHz 時
- 大きい同相除去:115dB
- 低いバイアス電流:±10pA
- レール ツー レール入出力
- 多重化に適したコンパレータ入力:
  - 電源レールまでの差動入力でアンプが動作
  - アンプを開ループで、またはコンパレータとして使用可能
- 広い帯域幅:1.1MHz GBW
- 高いスルーレート:4.5V/µs
- 低い静止電流:アンプ 1 個あたり 120µA
- 広い電源範囲:±1.35V～±20V、2.7V～40V
- 堅牢な EMIRR 性能:1.8GHz 時に 78dB
- 差動および同相入力電圧範囲は電源レールまで

2 アプリケーション

- AEC-Q100 グレード 1 アプリケーションに最適化
- HEV/EV のインバータおよびモータ制御
- オンボード充電器 (OBC) およびワイヤレス充電器
- HEV/EV のバッテリ管理システム (BMS)
- ボディ・エレクトロニクスおよび照明
- インフォテインメントおよびクラスタ
- パッシブ型安全運転支援システム
- パワートレイン電流センサ
- ハイサイド電流センス

3 概要

OPAx990-Q1 ファミリ (OPA990-Q1、OPA2990-Q1、OPA4990-Q1) は、高電圧 (40V) の汎用オペアンプ ファミリです。これらのデバイスは、レール ツー レールの入出力、低いオフセット (±300µV、標準値)、低いオフセットドリフト (±0.6µV/℃、標準値) などの優れた DC 精度と AC 性能を備えています。

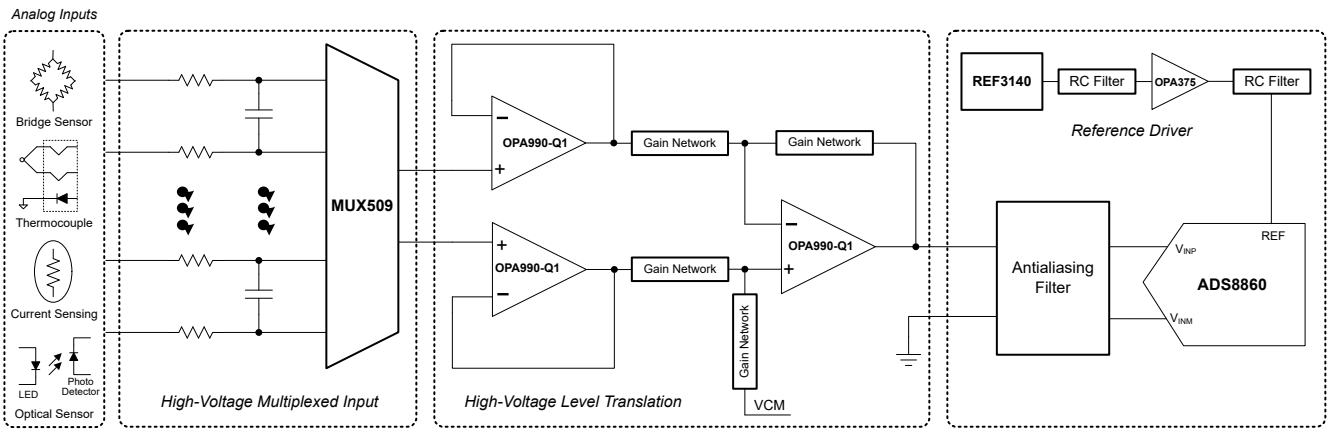
OPAx990-Q1 は、電源レールまでの差動および同相入力電圧範囲、大きい短絡電流 (±80mA)、高いスルーレート (4.5V/µs) などの独自機能を備えており、高電圧車載用アプリケーション向けの非常に柔軟で堅牢な高性能オペアンプです。

OPAx990-Q1 ファミリのオペアンプは、いくつかの標準パッケージ (SOT-23、SOIC、TSSOP など) で供給され、-40℃～125℃で動作が規定されています。

製品情報

部品番号	チャネル数	パッケージ (1)	本体サイズ (公称)(3)
OPA990-Q1	シングル	DBV (SOT-23、5)(2)	2.9mm × 1.6mm
		DCK (SC70、5)(2)	2mm × 1.25mm
OPA2990-Q1	デュアル	D (SOIC、8)(2)	4.9mm × 3.9mm
		DGK (VSSOP、8)(2)	3mm × 3mm
OPA4990-Q1	クワッド	D (SOIC、14)(2)	8.65mm × 3.9mm
		PW (TSSOP、14)	5mm × 4.4mm

(1) 詳細については、セクション 10 を参照してください。
(2) このパッケージはプレビューのみです。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



OPAx990-Q1 高電圧の多重化データ収集システムにおいて

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4 Pin Configuration and Function

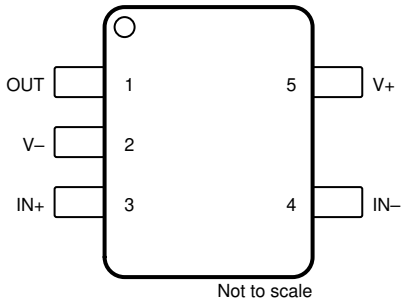

図 4-1. OPA990-Q1 DBV Package, 5-Pin SOT-23 (Top View)

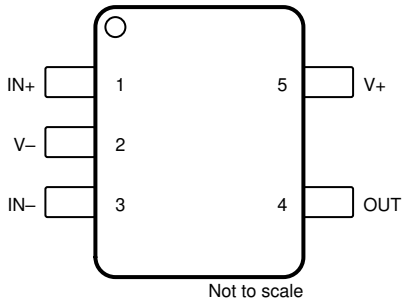

図 4-2. OPA990-Q1 DCK Package, 5-Pin SC70 (Top View)

表 4-1. Pin Functions: OPA990-Q1

PIN			TYPE(1)	DESCRIPTION
NAME	DBV	DCK		
IN+	3	1	I	Noninverting input
IN–	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

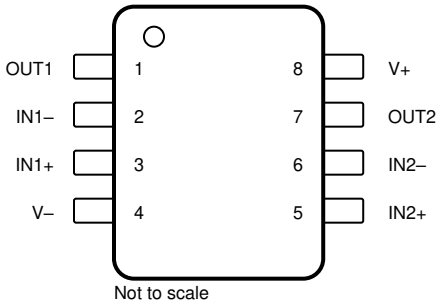

図 4-3. OPA2990-Q1 D and DGK Package, 8-Pin SOIC and VSSOP (Top View)

表 4-2. Pin Functions: OPA2990-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) I = input, O = output

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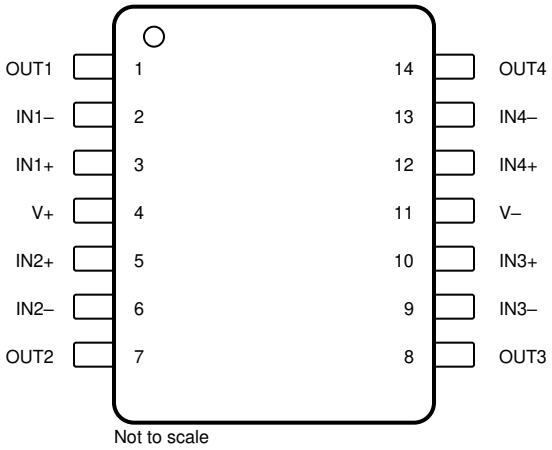

図 4-4. OPA4990-Q1 D and PW Package, 14-Pin SOIC and TSSOP (Top View)

表 4-3. Pin Functions: OPA4990-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
NC	—	—	Do not connect
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(3)	–10	10	mA
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction. For more information, see the *Thermal Protection* section.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	40	V
V_I	Input voltage range	(V–) – 0.2	(V+) + 0.2	V
T_A	Specified temperature	–40	125	°C

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5.4 Thermal Information for Single Channel

THERMAL METRIC(1)		OPA990-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.1	204.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.6	116.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.5	51.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.2	24.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.3	51.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		OPA2990-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.7	189.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.7	75.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.2	111.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.8	15.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.4	109.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		OPA4990-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.2	134.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.2	55.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.1	79.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.4	9.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.7	78.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.3	±2.1	mV
			T_A = –40°C to 125°C			±2.26	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.6		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 4V to 40V	T_A = –40°C to 125°C		±0.1	±1.3	µV/V
		V_{CM} = V–, V_S = 2.7V to 40V(1)			±0.75	±10	
	Channel separation	f = 0Hz			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±5		pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			6		μV_{PP}
					1		μV_{RMS}
e_N	Input voltage noise density	f = 1kHz			30		nV/√Hz
		f = 10kHz			28		
i_N	Input current noise	f = 1kHz			2		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 40V, (V–) – 0.1V < V_{CM} < (V+) – 2V (PMOS pair)	T_A = –40°C to 125°C	97	115		dB
		V_S = 4V, (V–) – 0.1V < V_{CM} < (V+) – 2V (PMOS pair)		72	90		
		V_S = 2.7V, (V–) – 0.1V < V_{CM} < (V+) – 2V (PMOS pair)(1)		70	90		
		V_S = 2.7 – 40V, (V+) – 1V < V_{CM} < (V+) + 0.1V (NMOS pair)			80		
		(V+) – 2V < V_{CM} < (V+) – 1V		See Offset Voltage (Transition Region) in the *Typical Characteristics* section			
INPUT CAPACITANCE							
Z_{ID}	Differential				540 || 3		GΩ ||pF
Z_{ICM}	Common-mode				6 || 1		TΩ ||pF

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5.7 Electrical Characteristics (続き)

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V		120	145		dB
			T_A = –40°C to 125°C		142		
		V_S = 4V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V		104	130		
			T_A = –40°C to 125°C		125		
		V_S = 2.7V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V(1)		99	118		dB
			T_A = –40°C to 125°C		117		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				1.1		MHz
SR	Slew rate	V_S = 40V, G = +1, C_L = 20pF			4.5		V/µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{STEP} = 10V , G = +1, CL = 20pF			4		µs
		To 0.1%, V_S = 40V, V_{STEP} = 2V , G = +1, CL = 20pF			2		
		To 0.01%, V_S = 40V, V_{STEP} = 10V , G = +1, CL = 20pF			5		
		To 0.01%, V_S = 40V, V_{STEP} = 2V , G = +1, CL = 20pF			3		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			60		°
	Overload recovery time	V_{IN} × gain > V_S			600		ns
THD+N	Total harmonic distortion + noise	V_S = 40V, V_O = 1V_{RMS}, G = 1, f = 1kHz			0.00162%		
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40V, R_L = no load		2		mV
			V_S = 40V, R_L = 10kΩ		45	60	
			V_S = 40V, R_L = 2kΩ		200	300	
			V_S = 2.7V, R_L = no load		1		
			V_S = 2.7V, R_L = 10kΩ		5	20	
			V_S = 2.7V, R_L = 2kΩ		25	50	
I_{SC}	Short-circuit current				±80		mA
C_{LOAD}	Capacitive load drive			See Small-Signal Overshoot vs Capacitive Load in the *Typical Characteristics* section			
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0 A			575		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	OPA2990-Q1, OPA4990-Q1, I_O = 0 A			120	150	µA
			T_A = –40°C to 125°C			160	
		OPA990-Q1, I_O = 0 A			130	170	
			T_A = –40°C to 125°C			175	
	Turn-on time	At T_A = 25°C, V_S = 40V, V_S ramp rate > 0.3V/µs			40		µs

(1) Specified by characterization only.

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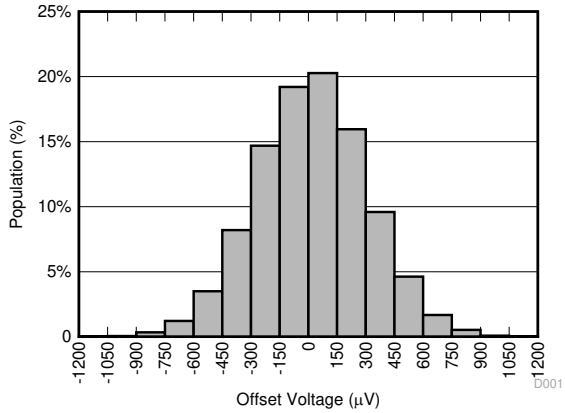
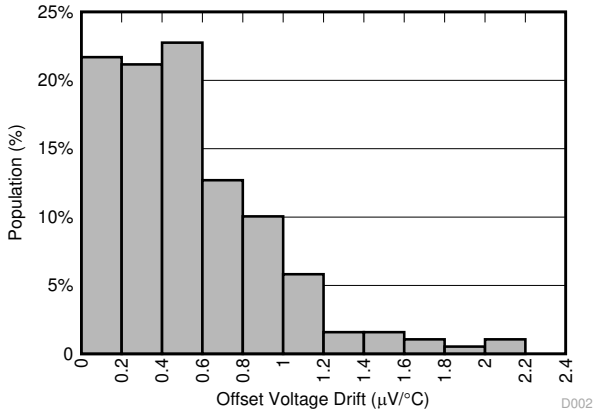
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



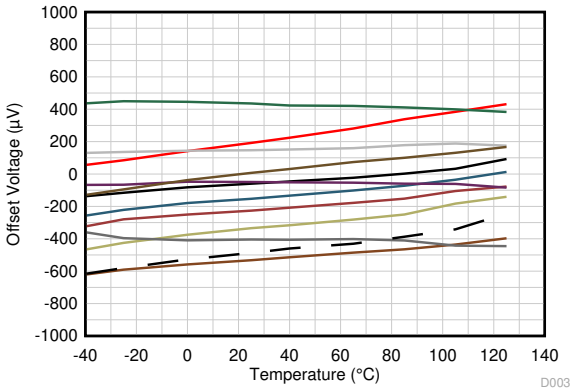
Distribution from 15526 amplifiers, T_A = 25°C

図 5-1. Offset Voltage Production Distribution



Distribution from 190 amplifiers

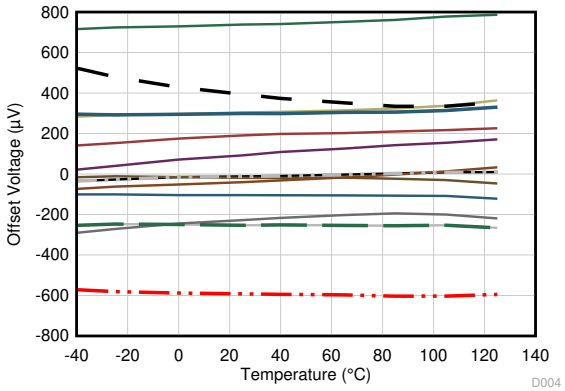
図 5-2. Offset Voltage Drift Distribution



V_{CM} = V+

Each color represents one sample device.

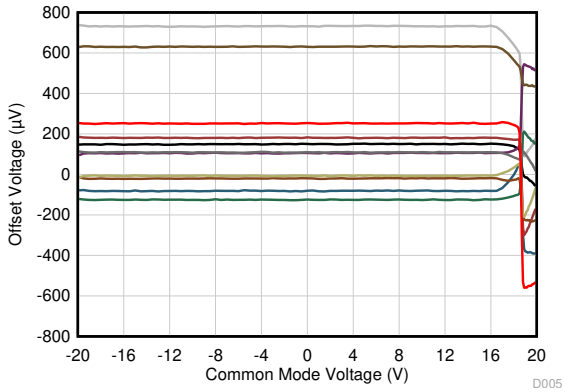
図 5-3. Offset Voltage vs Temperature



V_{CM} = V–

Each color represents one sample device.

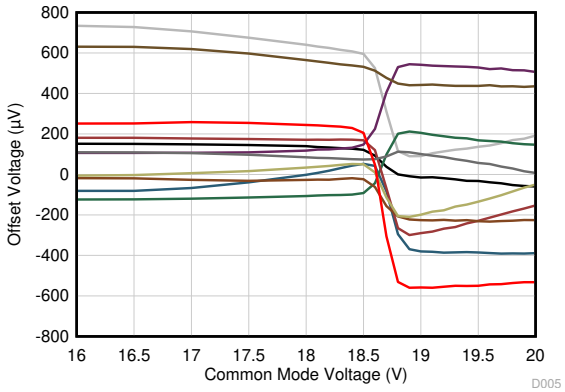
図 5-4. Offset Voltage vs Temperature



T_A = 25°C

Each color represents one sample device.

図 5-5. Offset Voltage vs Common-Mode Voltage



T_A = 25°C

Each color represents one sample device.

図 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

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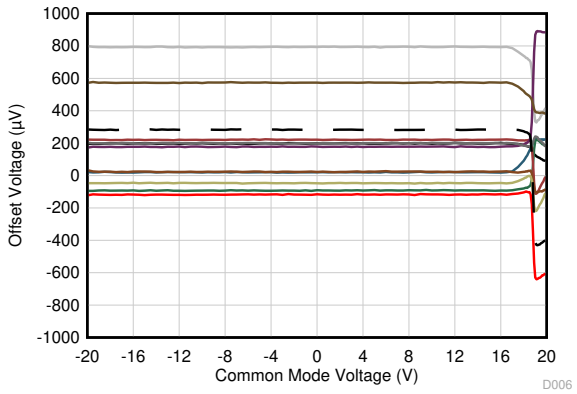
5.8 Typical Characteristics (continued)

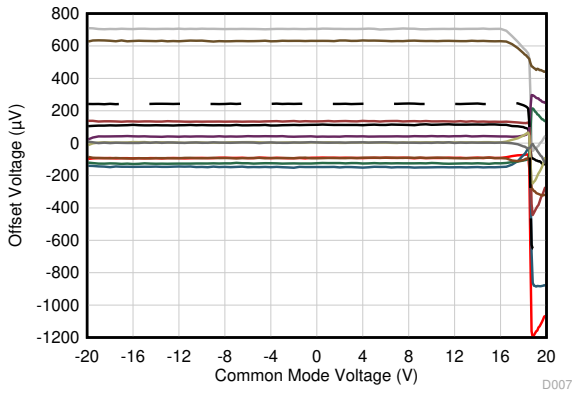
at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



T_A = 125°C

Each color represents one sample device.

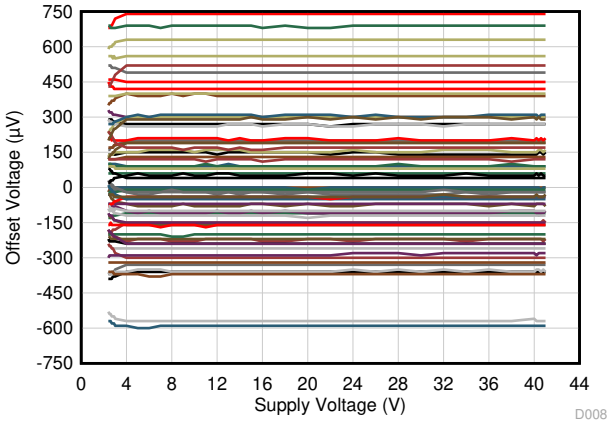
図 5-7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Each color represents one sample device.

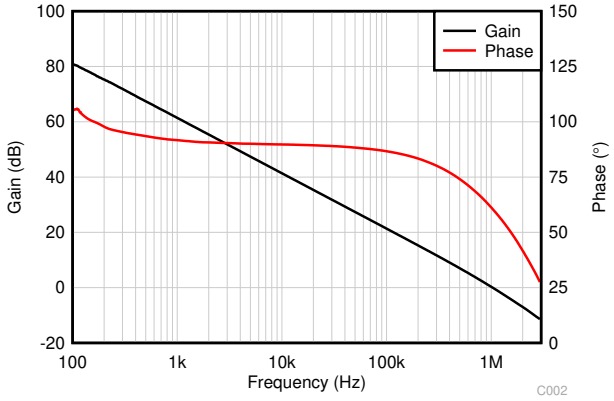
図 5-8. Offset Voltage vs Common-Mode Voltage



V_{CM} = V–

Each color represents one sample device.

図 5-9. Offset Voltage vs Power Supply



C_L = 20pF

図 5-10. Open-Loop Gain and Phase vs Frequency

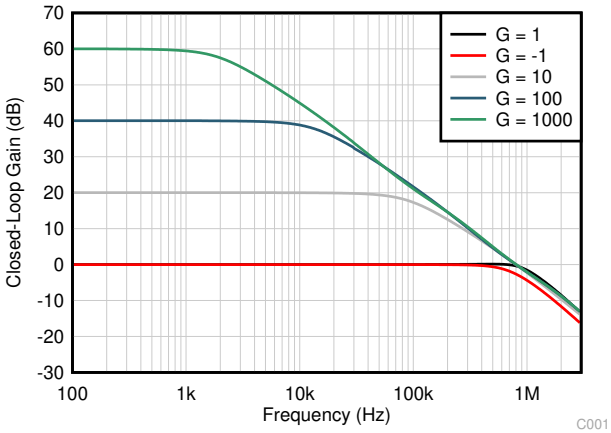


図 5-11. Closed-Loop Gain vs Frequency

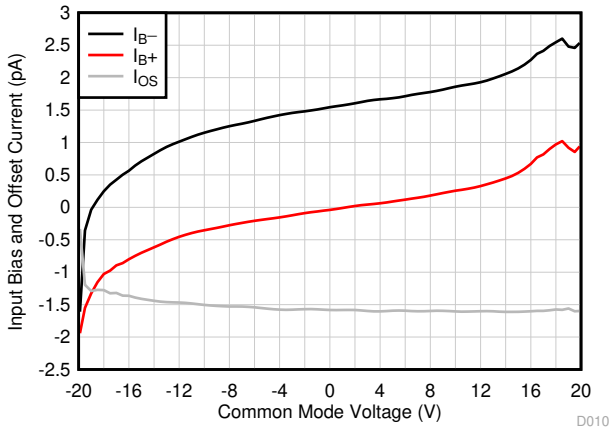


図 5-12. Input Bias Current vs Common-Mode Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)

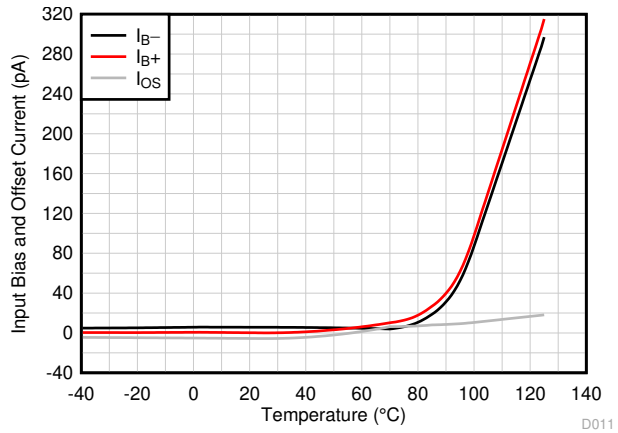


図 5-13. Input Bias Current vs Temperature

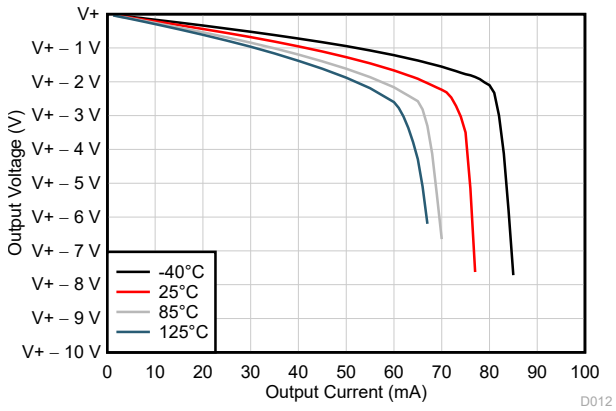


図 5-14. Output Voltage Swing vs Output Current (Sourcing)

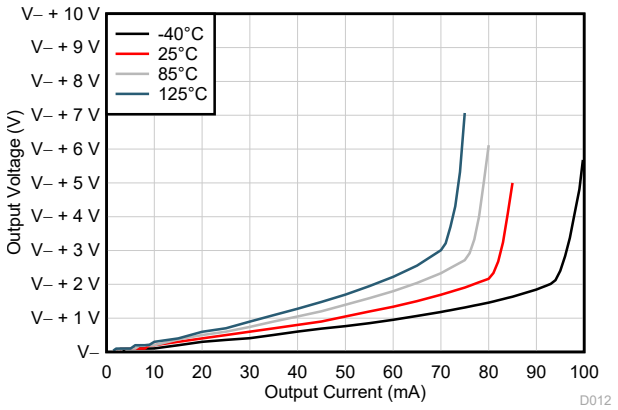
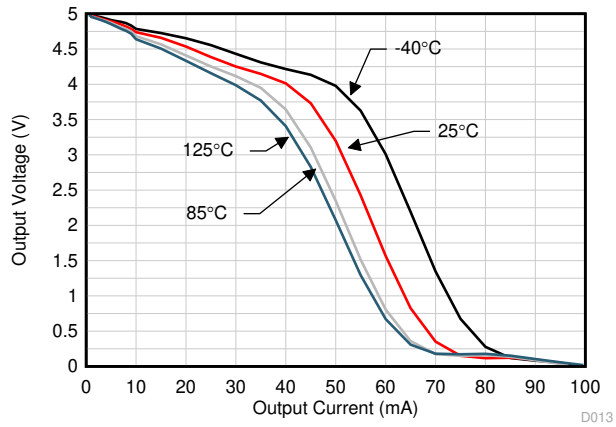
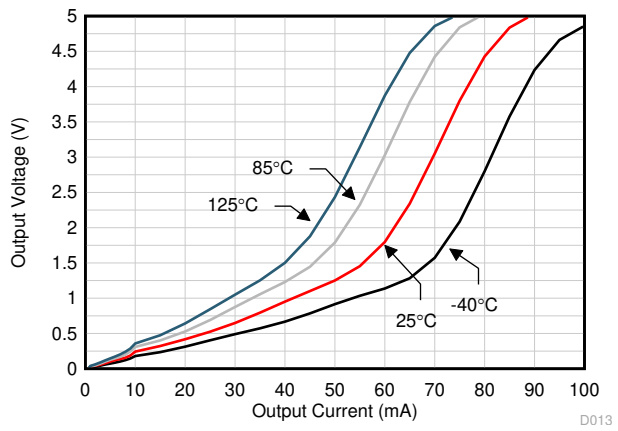


図 5-15. Output Voltage Swing vs Output Current (Sinking)



V_S = 5V

図 5-16. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5V

図 5-17. Output Voltage Swing vs Output Current (Sinking)

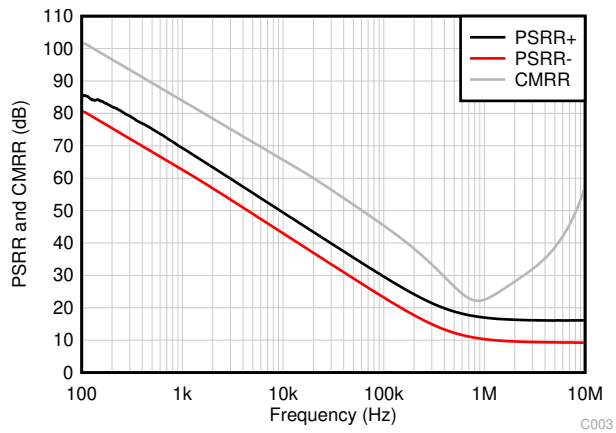


図 5-18. CMRR and PSRR vs Frequency

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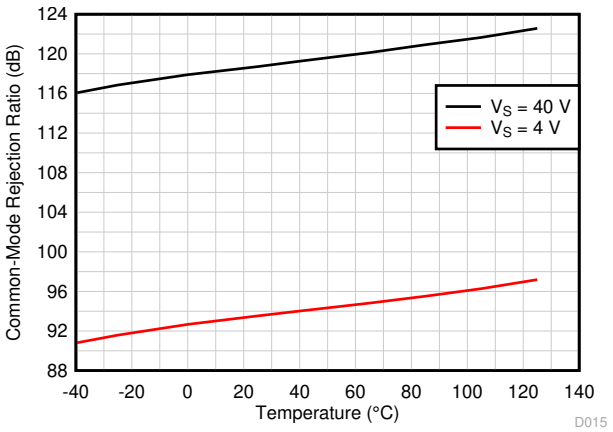
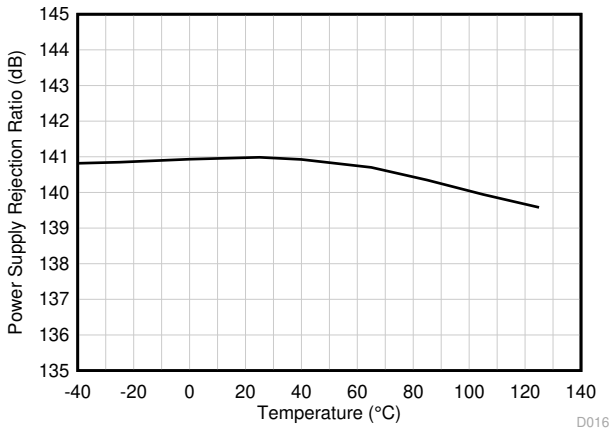
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



f = 0Hz

図 5-19. CMRR vs Temperature (dB)



f = 0Hz

図 5-20. PSRR vs Temperature (dB)

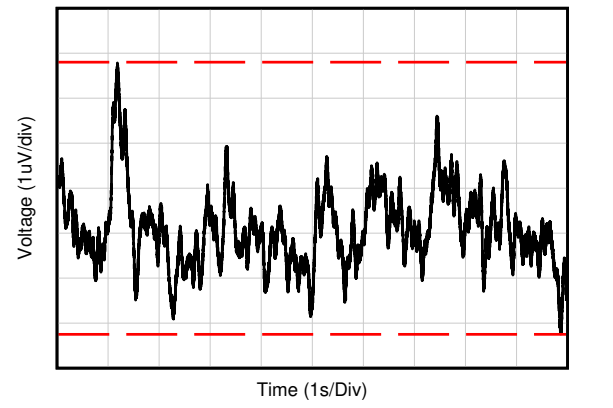


図 5-21. 0.1Hz to 10Hz Noise

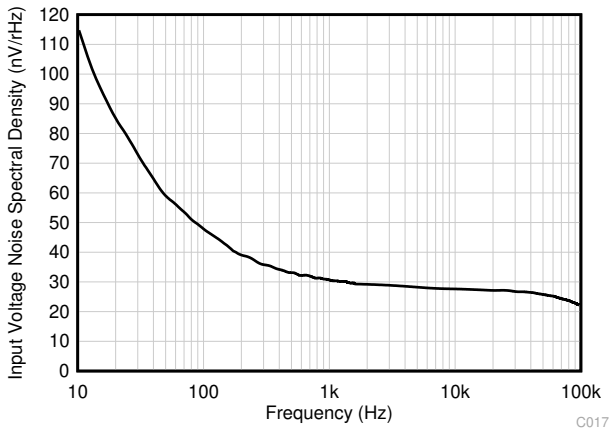
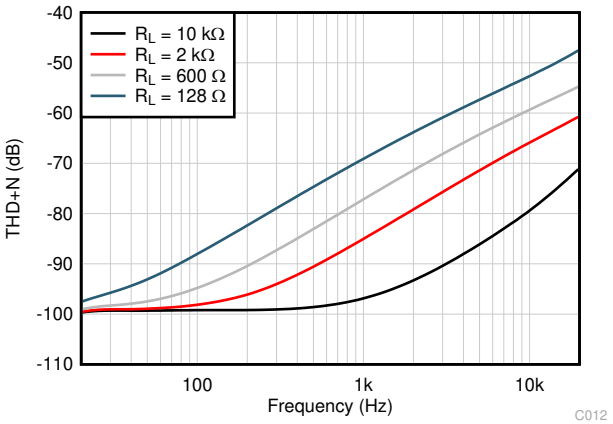
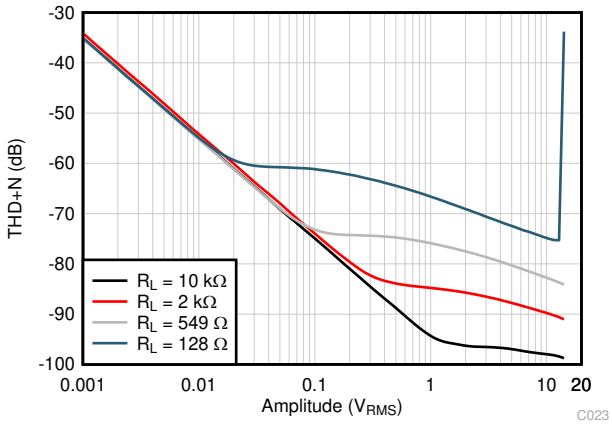


図 5-22. Input Voltage Noise Spectral Density vs Frequency



BW = 80kHz, V_{OUT} = 1V_{RMS}

図 5-23. THD+N Ratio vs Frequency

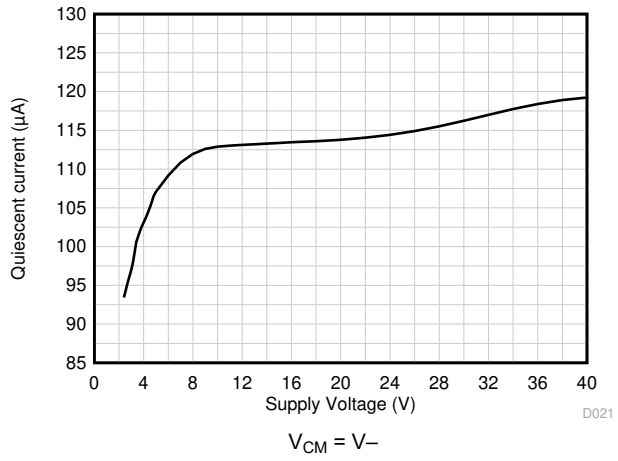


BW = 80kHz, f = 1kHz

図 5-24. THD+N vs Output Amplitude

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



V_{CM} = V–

図 5-25. Quiescent Current vs Supply Voltage

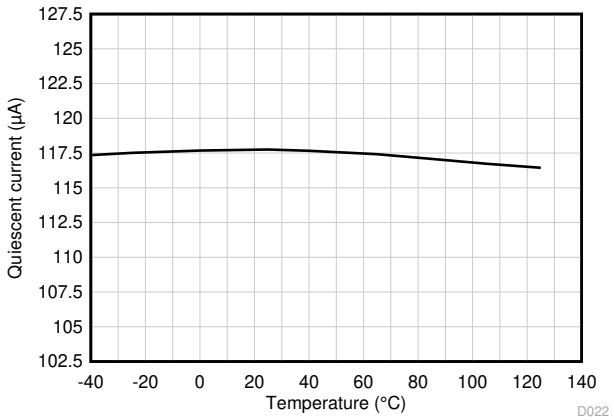


図 5-26. Quiescent Current vs Temperature

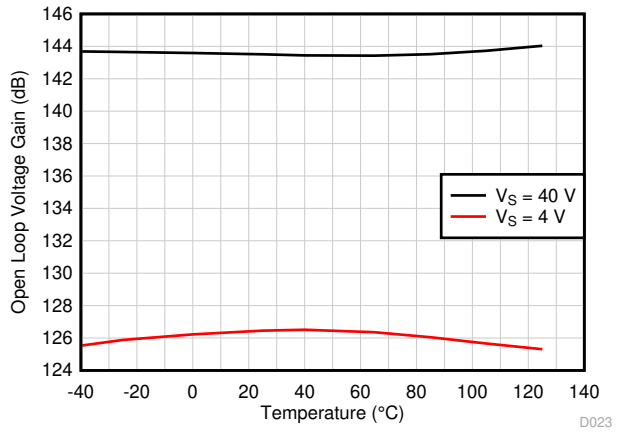


図 5-27. Open-Loop Voltage Gain vs Temperature (dB)

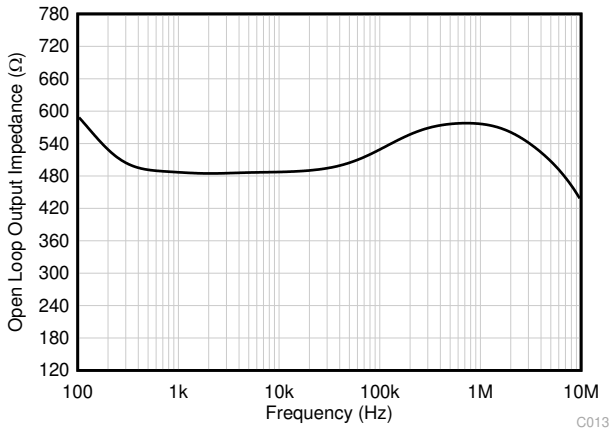
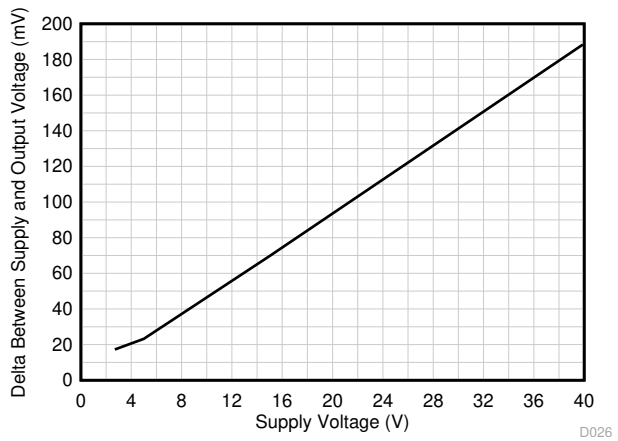
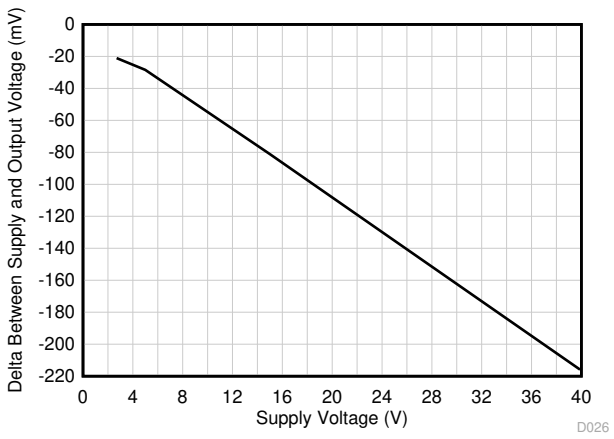


図 5-28. Open-Loop Output Impedance vs Frequency



R_L = 2 kΩ

図 5-29. Output Swing vs Supply Voltage, Positive Swing



R_L = 2 kΩ

図 5-30. Output Swing vs Supply Voltage, Negative Swing

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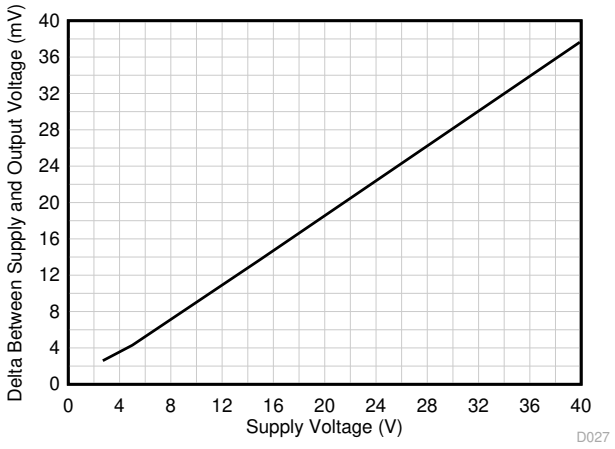
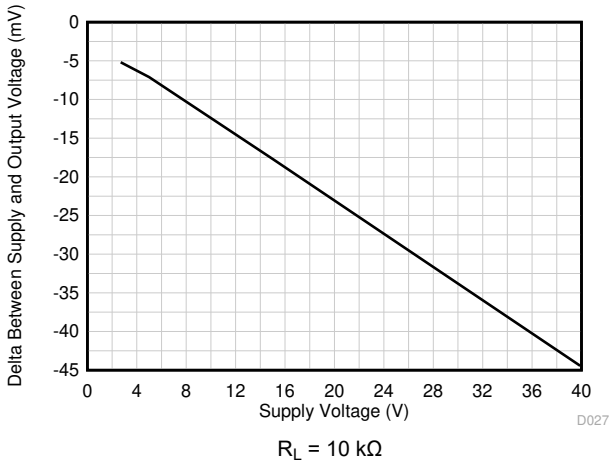
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



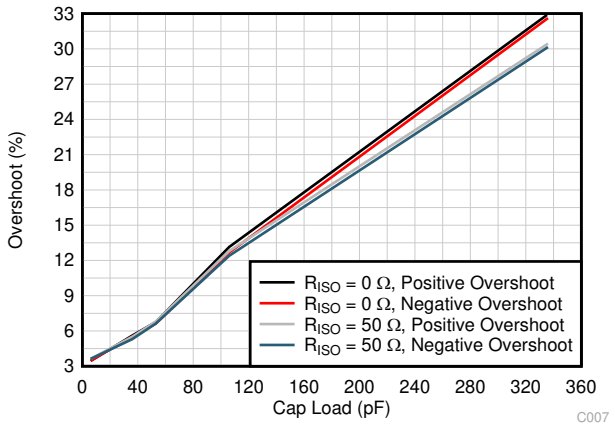
R_L = 10 kΩ

図 5-31. Output Swing vs Supply Voltage, Positive Swing



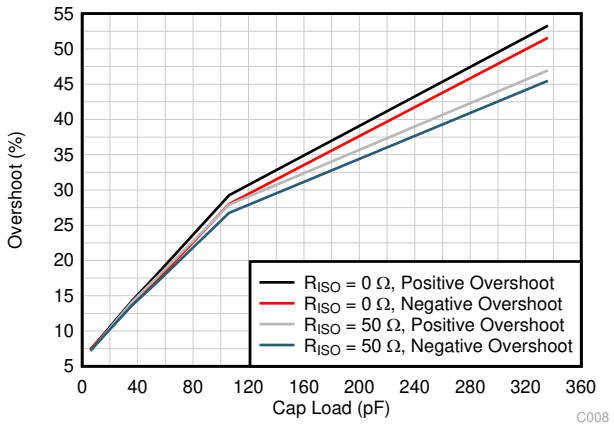
R_L = 10 kΩ

図 5-32. Output Swing vs Supply Voltage, Negative Swing



G = –1, 10mV output step

図 5-33. Small-Signal Overshoot vs Capacitive Load



G = 1, 10mV output step

図 5-34. Small-Signal Overshoot vs Capacitive Load

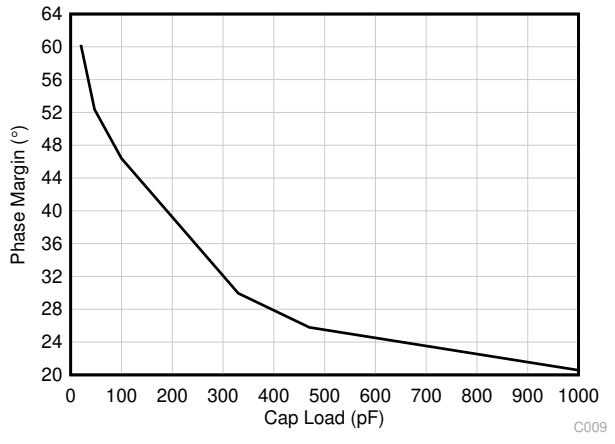
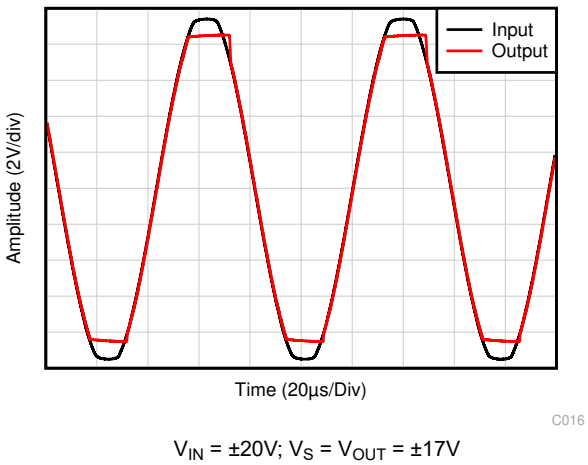


図 5-35. Phase Margin vs Capacitive Load

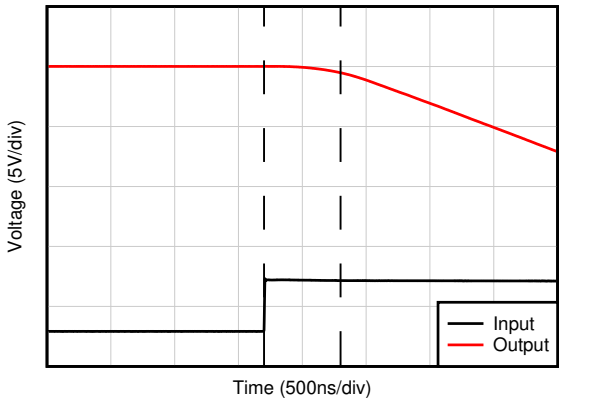


V_{IN} = ±20V; V_S = V_{OUT} = ±17V

図 5-36. No Phase Reversal

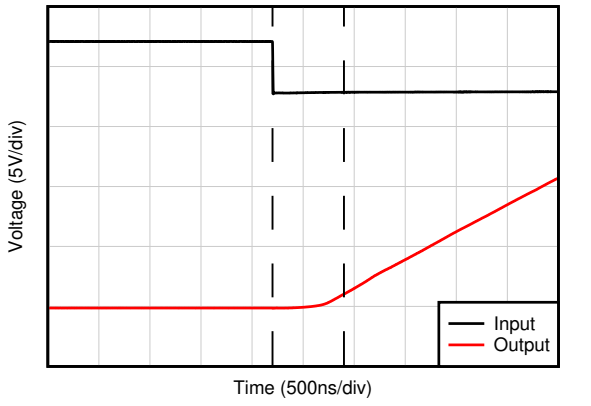
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



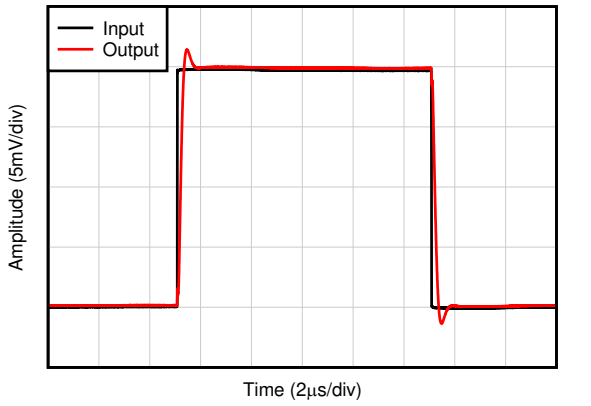
G = –10

図 5-37. Positive Overload Recovery



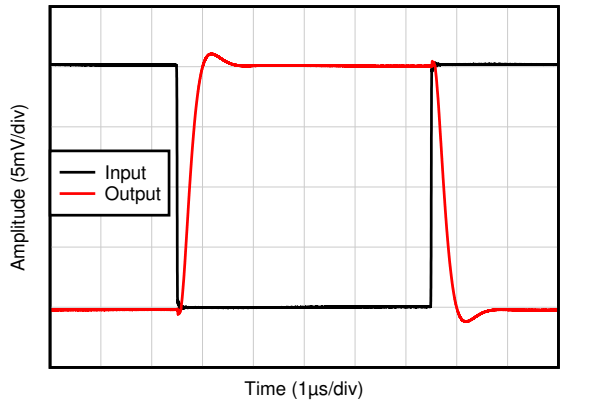
G = –10

図 5-38. Negative Overload Recovery



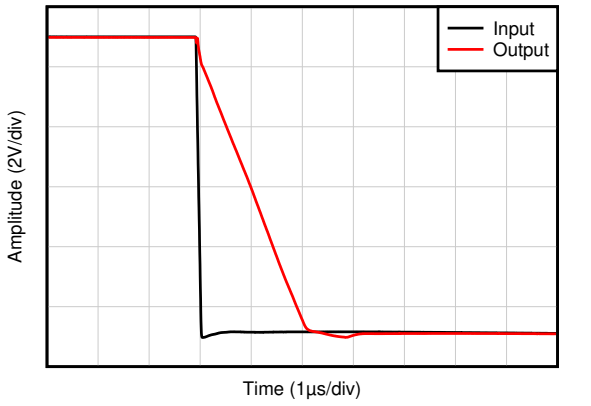
C_L = 20pF, G = 1, 20mV step response

図 5-39. Small-Signal Step Response



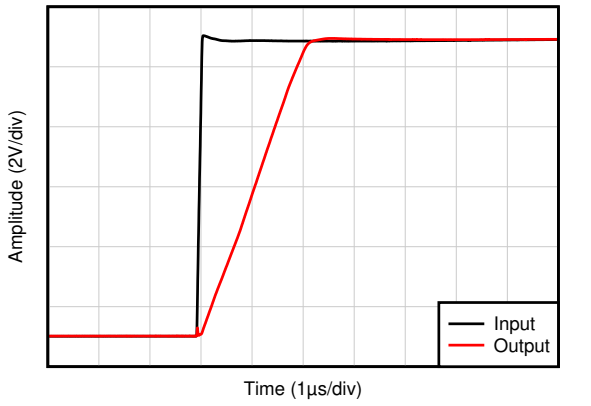
C_L = 20pF, G = –1, 20mV step response

図 5-40. Small-Signal Step Response



C_L = 20pF, G = 1

図 5-41. Large-Signal Step Response (Falling)



C_L = 20pF, G = 1

図 5-42. Large-Signal Step Response (Rising)

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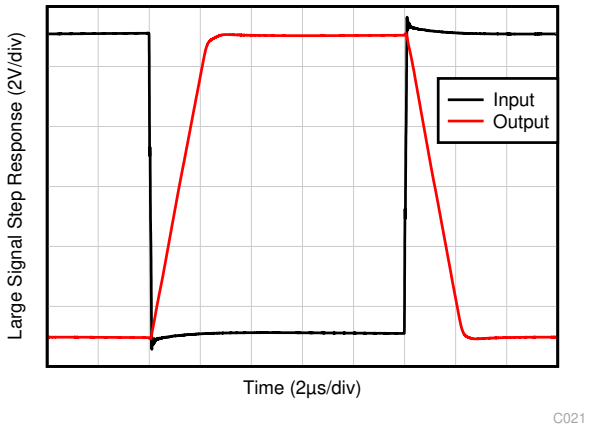
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



C_L = 20pF, G = –1

図 5-43. Large-Signal Step Response

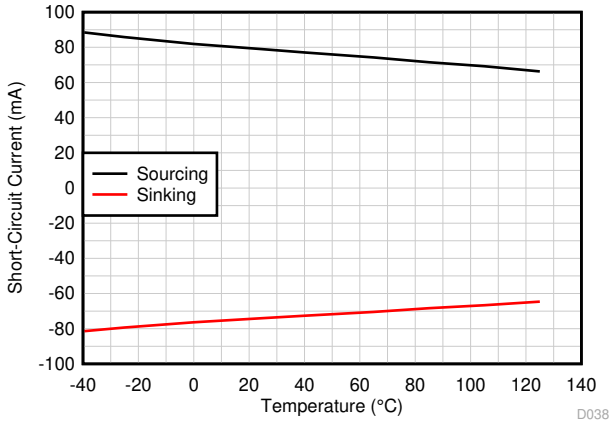


図 5-44. Short-Circuit Current vs Temperature

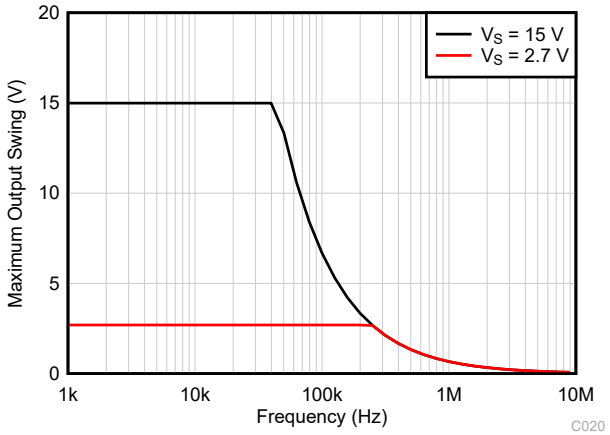


図 5-45. Maximum Output Voltage vs Frequency

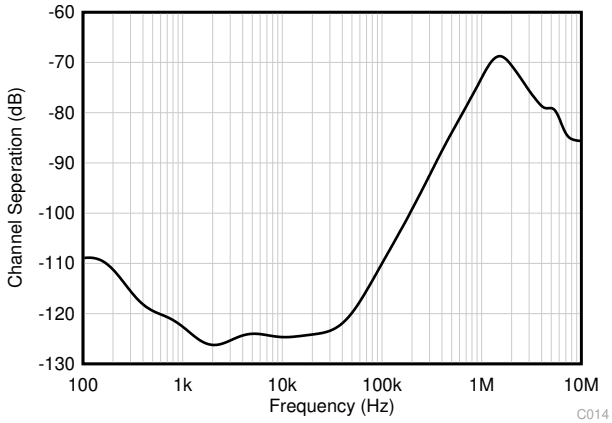


図 5-46. Channel Separation vs Frequency

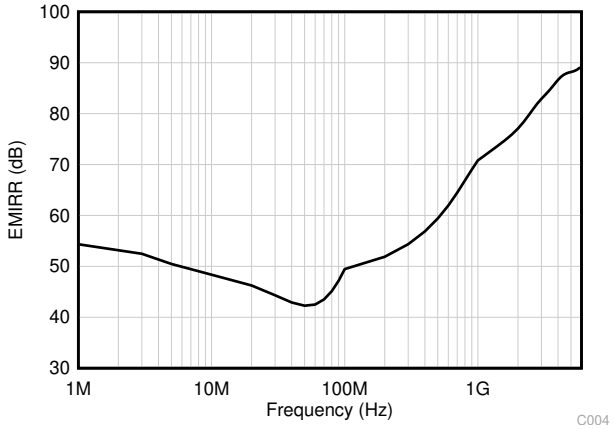


図 5-47. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

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6 Detailed Description

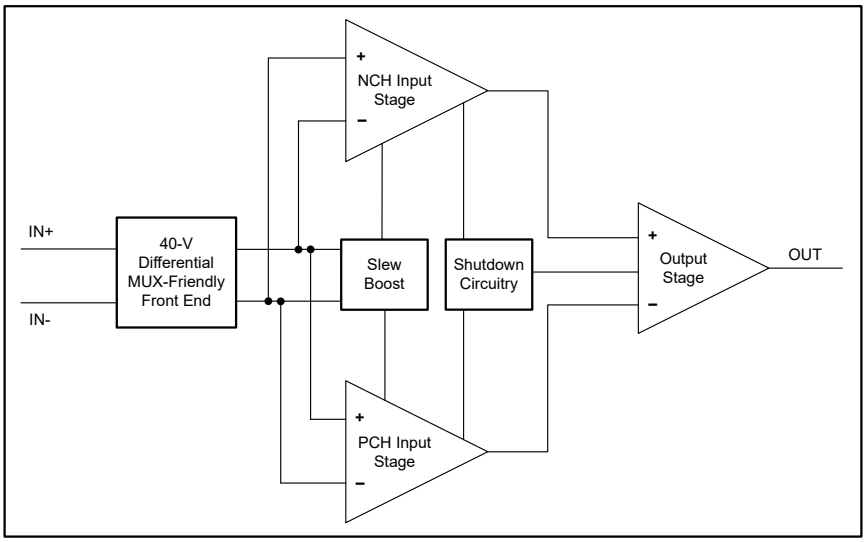
6.1 Overview

The OPAx990-Q1 family (OPA990-Q1, OPA2990-Q1, and OPA4990-Q1) is a family of high voltage (40V) general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input or output, low offset (±300µV, typ), and low offset drift (±0.6µV/°C, typ).

Unique features such as differential and common-mode input voltage range to the supply rail, high short-circuit current (±80mA), and high slew rate (4.5V/µs) make the OPAx990-Q1 an extremely flexible, robust, and high-performance operational amplifier for high-voltage automotive applications.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Input Protection Circuitry

The OPAx990-Q1 uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 図 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 図 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

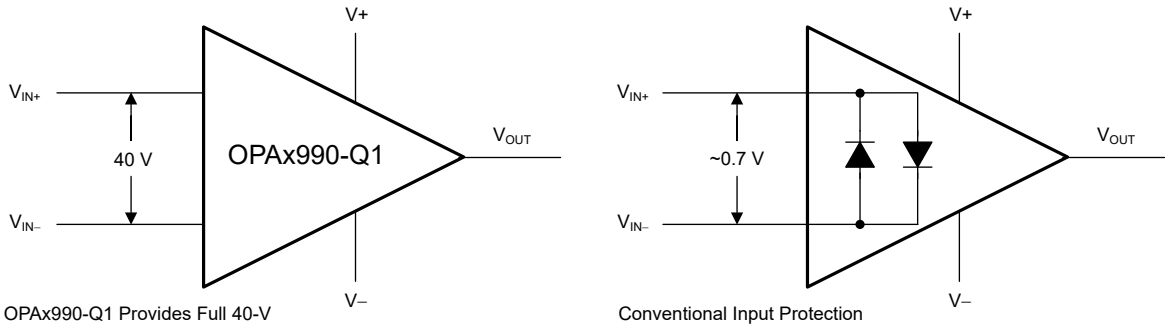

図 6-1. OPAx990-Q1 Input Protection Does Not Limit Differential Input Capability

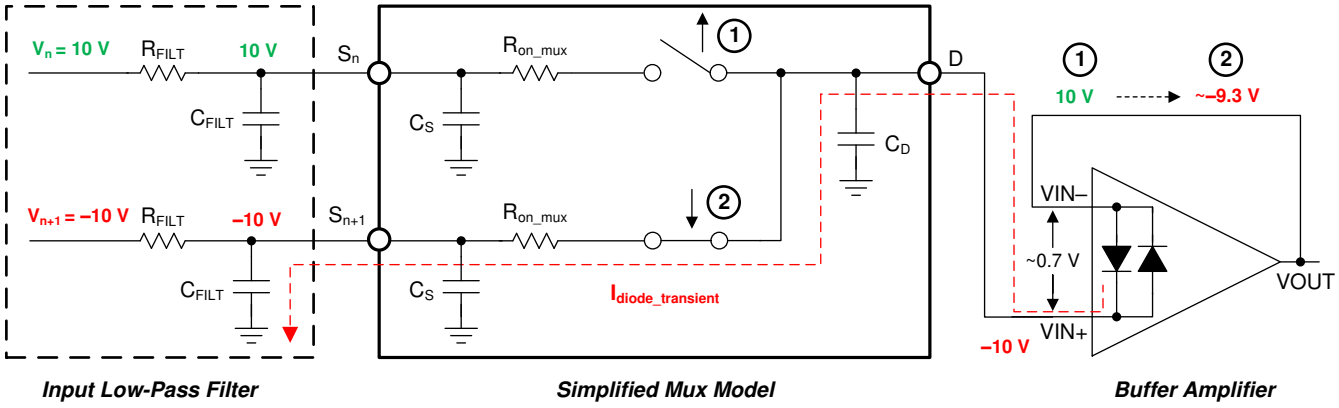

図 6-2. Back-to-Back Diodes Create Settling Issues

The OPAx990-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA990-Q1 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40V, making the device an excellent choice for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; for more information, see the *MUX-Friendly Precision Operational Amplifiers* application brief.

6.3.2 EMI Rejection

The OPAx990-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx990-Q1 benefits from these design improvements. Texas Instruments developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 図 6-3 shows the results of this testing on the OPAx990-Q1. 表 6-1 provides the EMIRR IN+ values for the OPAx990-Q1 at particular frequencies commonly encountered in real-world applications. For detailed information on the topic of EMIRR performance as it relates to op amps, see the *EMI Rejection Ratio of Operational Amplifiers* application report.

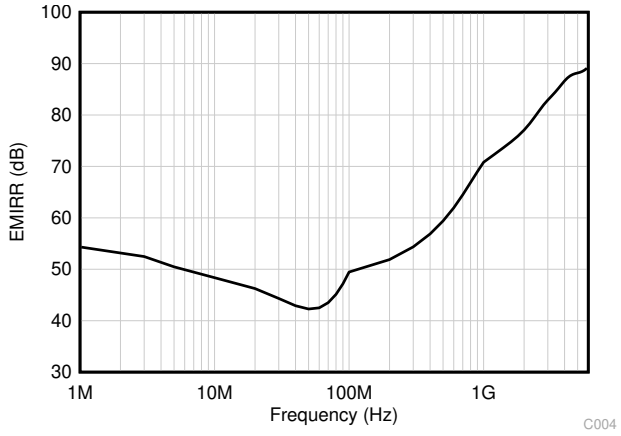

図 6-3. EMIRR Testing

表 6-1. OPA990-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	68.9dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	77.8dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, automotive, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	78.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	87.6dB

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6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx990-Q1 is 150°C. Exceeding this temperature causes damage to the device. The OPAx990-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 図 6-4 shows an application example for the OPA990-Q1 that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature must reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 図 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, then the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

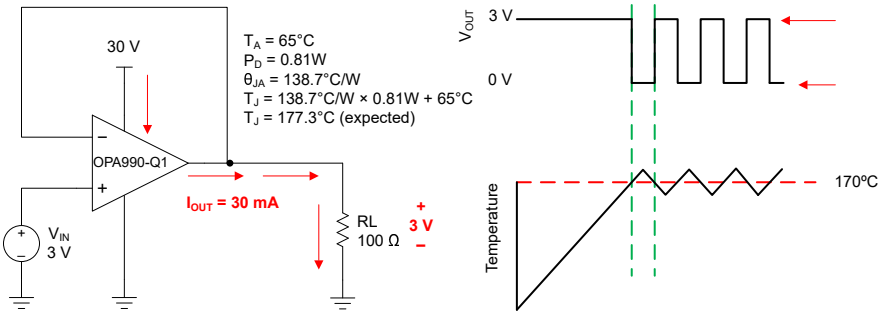

図 6-4. Thermal Protection

6.3.4 Capacitive Load and Stability

The OPAx990-Q1 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. As shown in 図 6-5 and 図 6-6, increasing the gain enhances the ability of the amplifier to drive greater capacitive loads. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

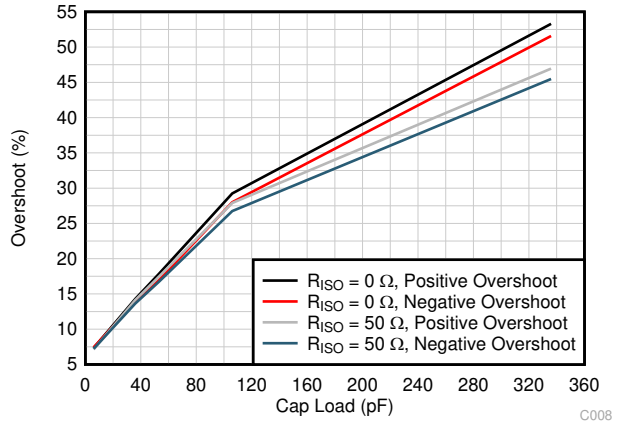

図 6-5. Small-Signal Overshoot vs Capacitive Load (10mV Output Step, G = 1)

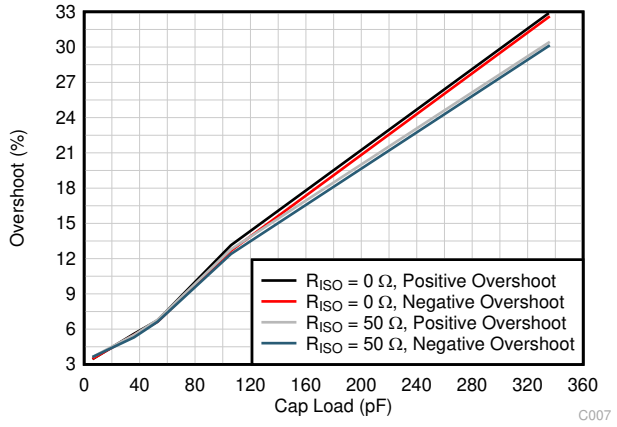

図 6-6. Small-Signal Overshoot vs Capacitive Load (10mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 図 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx990-Q1 an excellent choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 図 6-7 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

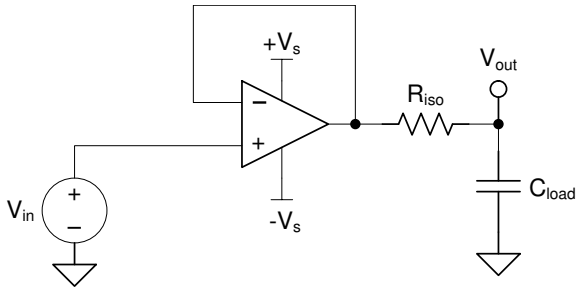

図 6-7. Extending Capacitive Load Drive With the OPA990-Q1

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6.3.5 Common-Mode Voltage Range

The OPAx990-Q1 is a 40V, true rail-to-rail input operational amplifier with an input common-mode range that extends 200 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 図 6-8. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) – 2V to (V+) – 1V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

図 5-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

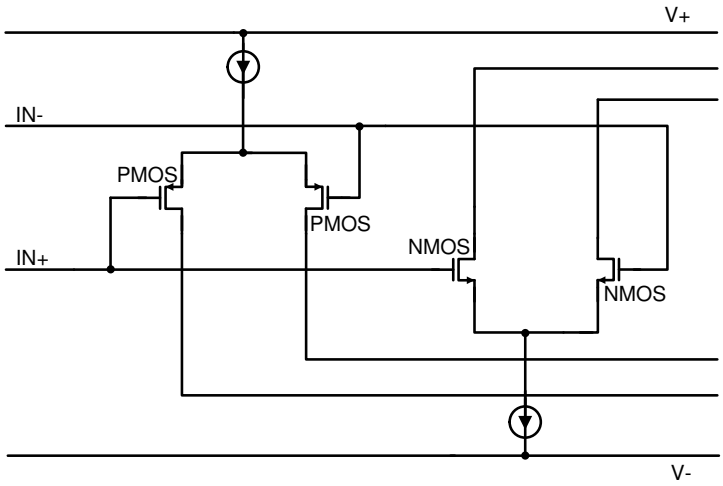

図 6-8. Rail-to-Rail Input Stage

6.3.6 Phase Reversal Protection

The OPAx990-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx990-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 図 6-9. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

ADVANCE INFORMATION

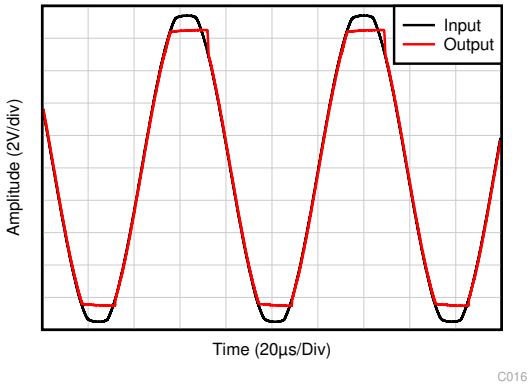

図 6-9. No Phase Reversal

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 図 6-10 shows an illustration of the ESD circuits contained in the OPAx990-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

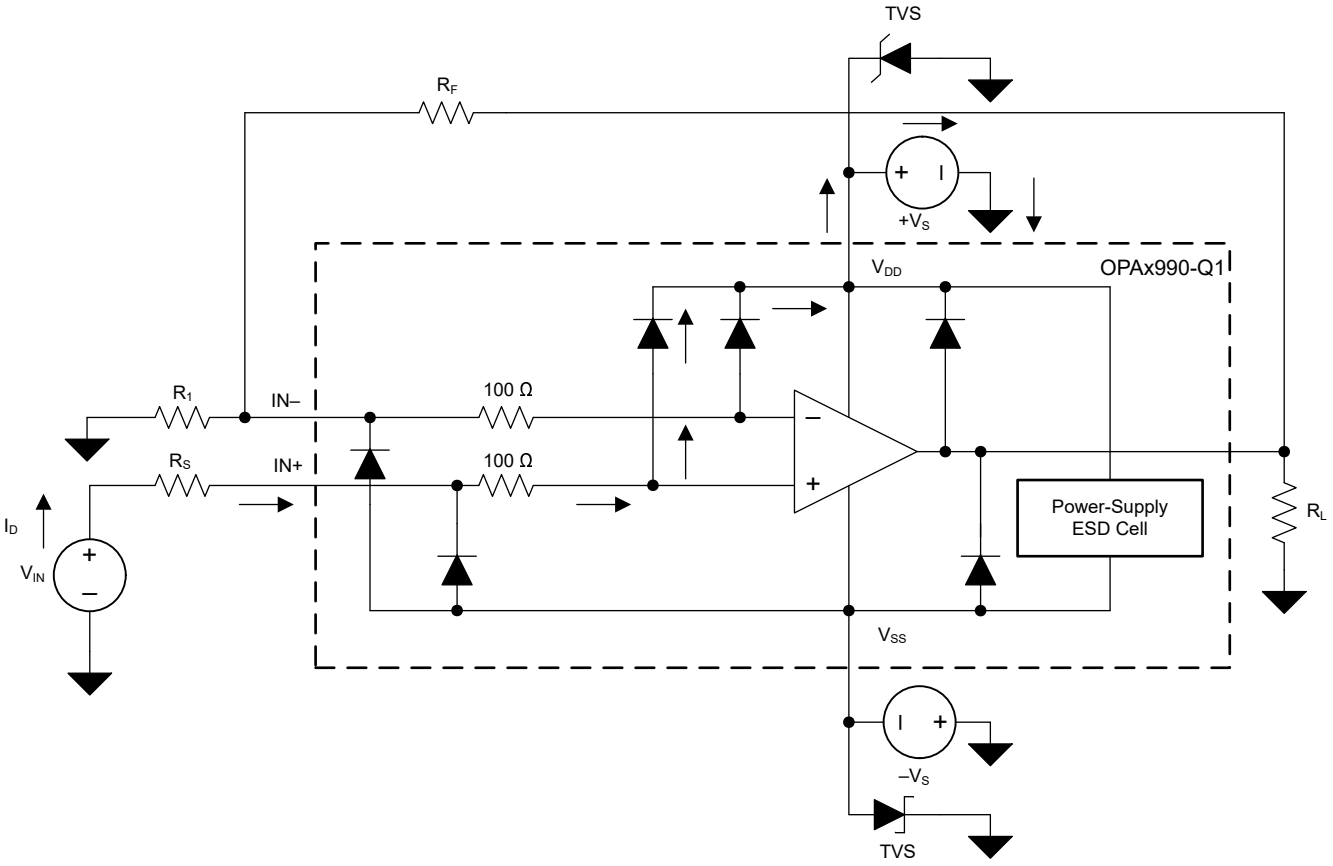

図 6-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and has a very high voltage (for example; 1kV, 100ns), whereas an EOS event is long in duration and has a lower voltage (for example; 50V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx990-Q1 is approximately 600ns.

6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the target value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

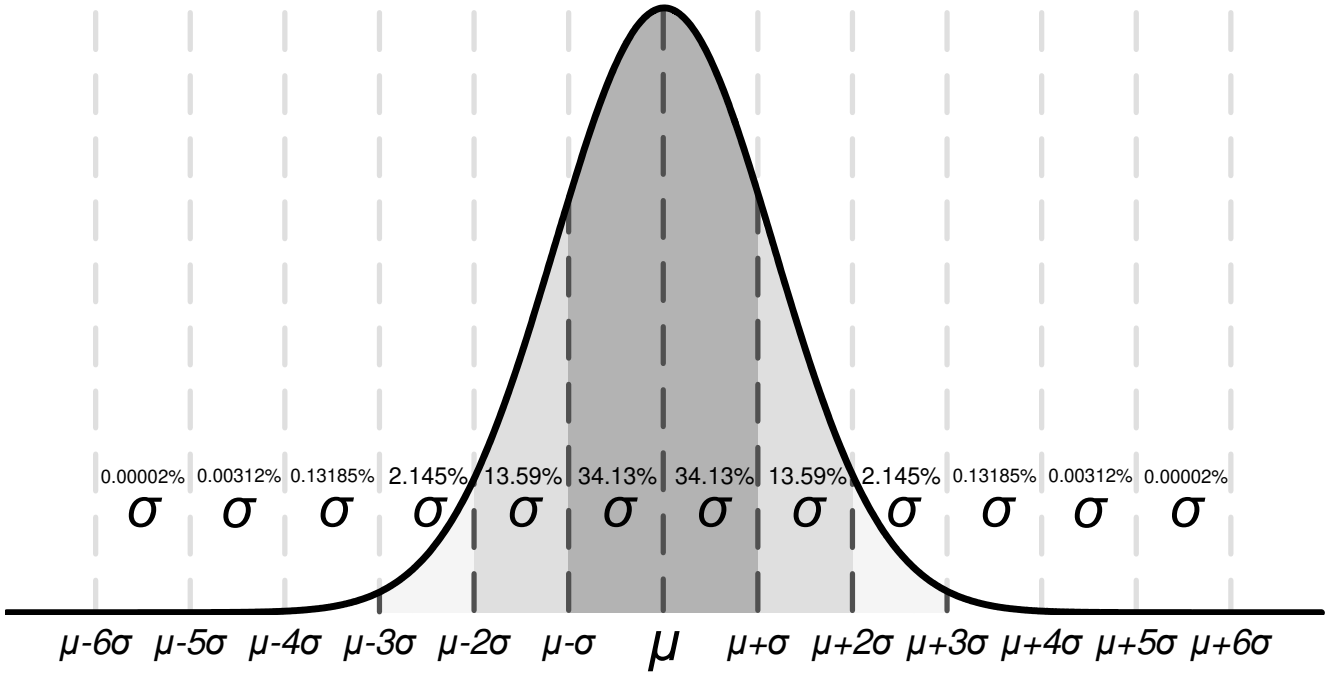

図 6-11. Gaussian Distribution

図 6-11 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ–σ* to *μ+σ*).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

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This chart can be used to calculate approximate probability of a specification in a unit; for example, for OPAx990-Q1, the typical input voltage offset is 300µV, so 68.2% of all OPAx990-Q1 devices are expected to have an offset from –300µV to +300µV. At 4 σ (±1200µV), 99.9937% of the distribution has an offset voltage less than ±1200µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are specified by TI, and units outside these limits will be removed from production material. For example, the OPAx990-Q1 family has a maximum offset voltage of 2.1 mV at 25°C, and even though this corresponds to 7 σ, which is extremely unlikely, any unit with larger offset than 2.1 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the OPAx990-Q1 family does not have a maximum or minimum for offset voltage drift, but based on 図 5-2 and the typical value of 0.6µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6-σ value for offset voltage drift is about 3.6µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should only be used to estimate the performance of a device.

6.4 Device Functional Modes

The OPAx990-Q1 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7V (±1.35V). The maximum power supply voltage for the OPAx990-Q1 is 40V (±20V).

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7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx990-Q1 family offers excellent DC precision and AC performance. These devices operate up to 40V supply rails and offer true rail-to-rail input or output, low offset voltage and offset voltage drift, as well as 1.1MHz bandwidth and high output drive. These features make the OPAx990-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

図 7-1 shows the OPAx990-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in 図 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

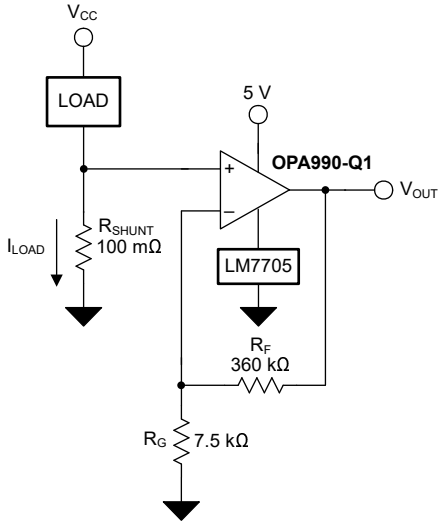

図 7-1. OPAx990-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9V
- Maximum shunt voltage: 100 mV

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7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 図 7-1 is given in 式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Using 式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA990-Q1 to produce an output voltage of 0V to 4.9V. The gain needed by the OPA990-Q1 to produce the necessary output voltage is calculated using 式 3.

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using 式 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. 式 4 is used to size the resistors, R_F and R_G, to set the gain of the OPA990-Q1 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 360 kΩ, R_G is calculated to be 7.5 kΩ. R_F and R_G were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. 図 7-2 shows the measured transfer function of the circuit shown in 図 7-1.

7.2.1.3 Application Curve

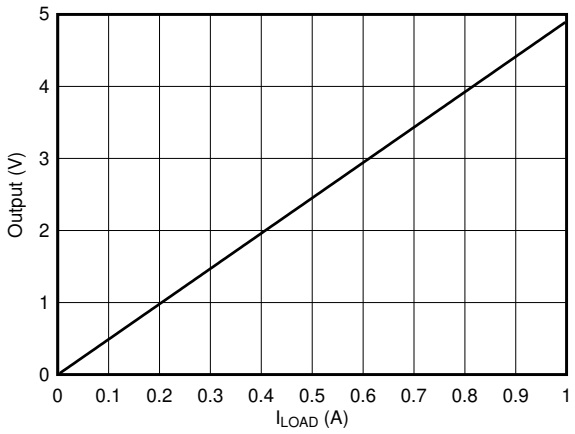

図 7-2. Low-Side, Current-Sense, Transfer Function

7.2.2 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx990-Q1 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. 図 7-3 shows the OPA990-Q1 in a slew-rate limit design.

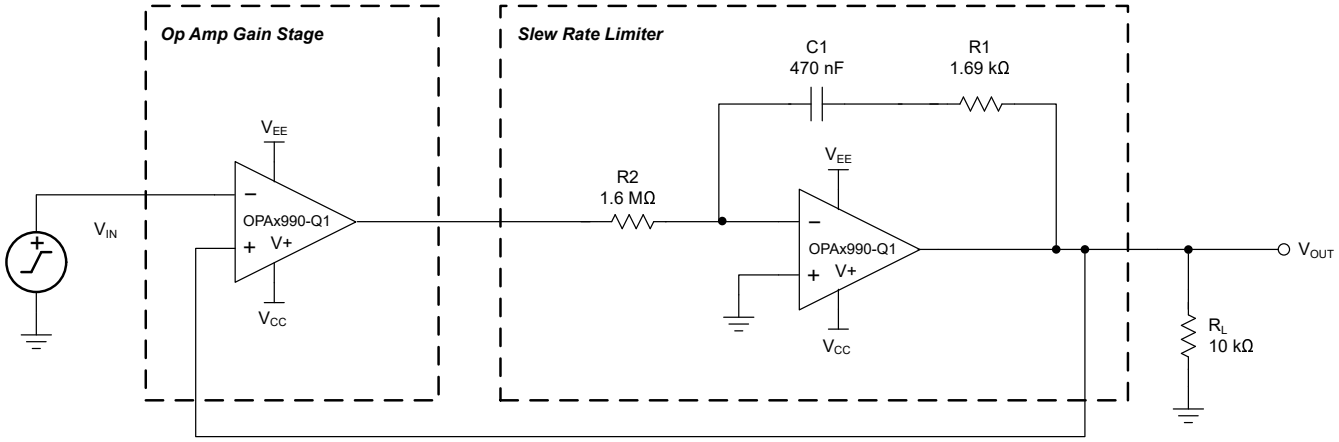

図 7-3. Slew Rate Limiter Uses One Op Amp

7.3 Power Supply Recommendations

The OPAx990-Q1 is specified for operation from 2.7V to 40V (±1.35V to ±20V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions. For parameters that can exhibit significant variance regarding operating voltage or temperature, see the *Typical Characteristics* section.

> **注意**
>
> Supply voltages larger than 40V can permanently damage the device; for more information, see the *Absolute Maximum Ratings* section.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate the digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, then crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 7-5, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

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- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

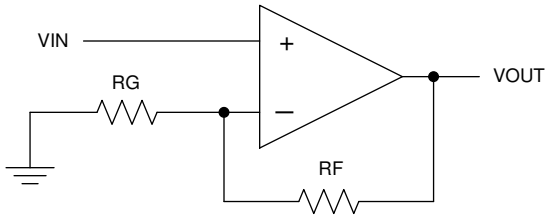

図 7-4. Schematic Representation

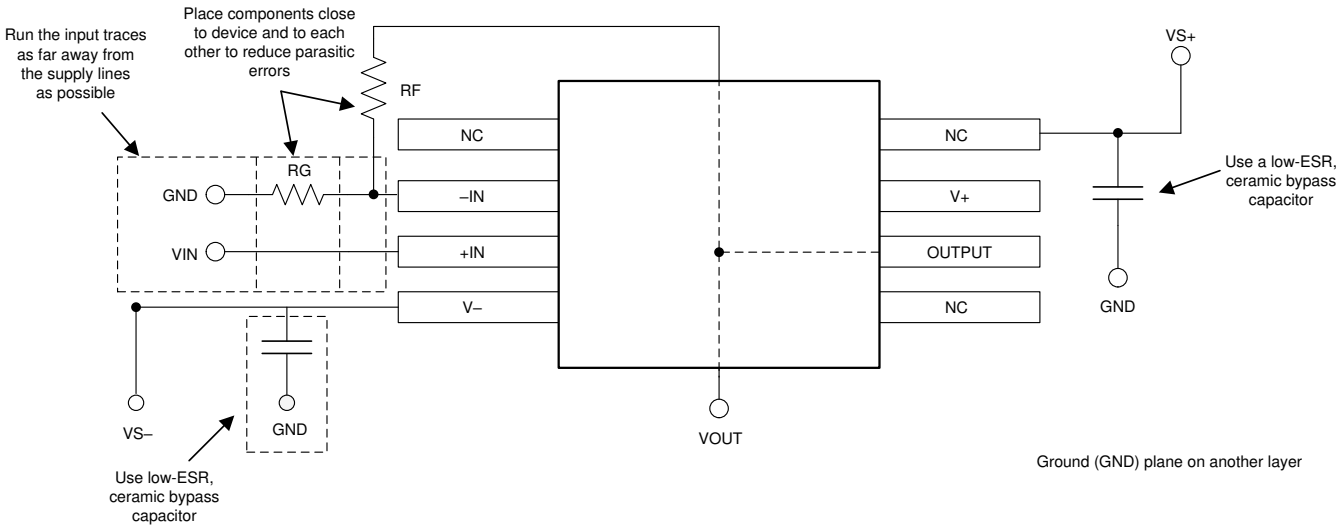

図 7-5. Operational Amplifier Board Layout for Noninverting Configuration

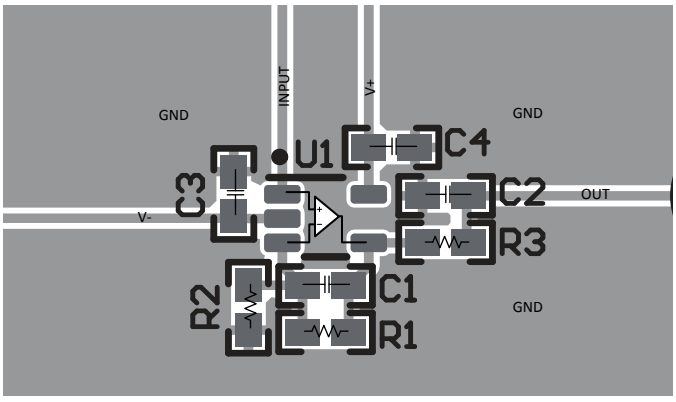

図 7-6. Example Layout for SC70 (DCK) Package

ADVANCE INFORMATION

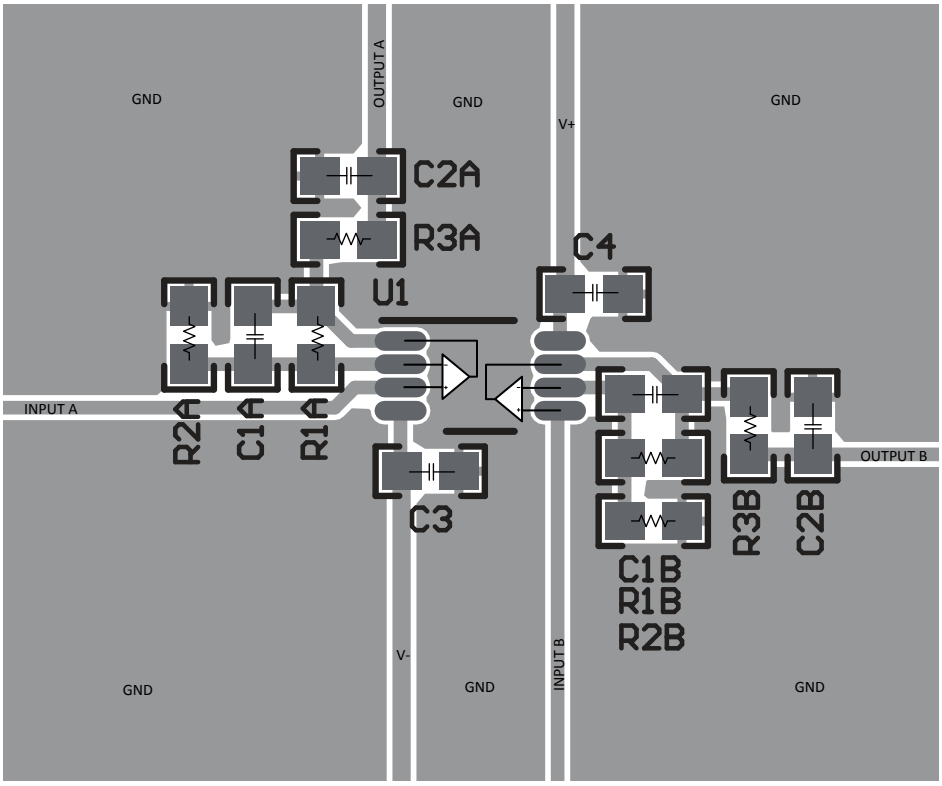

図 7-7. Example Layout for VSSOP-8 (DGK) Package

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *MUX-Friendly, Precision Operational Amplifiers* application brief
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2023) to Revision A (February 2024)	Page
• TSSOP (14) パッケージのステータスをプレビューからアクティブに変更	1

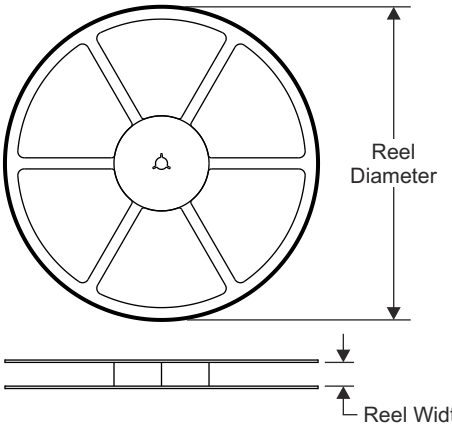
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

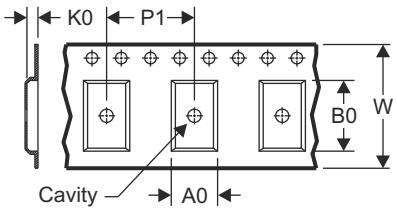
ADVANCE INFORMATION

10.1 Tape and Reel Information

REEL DIMENSIONS

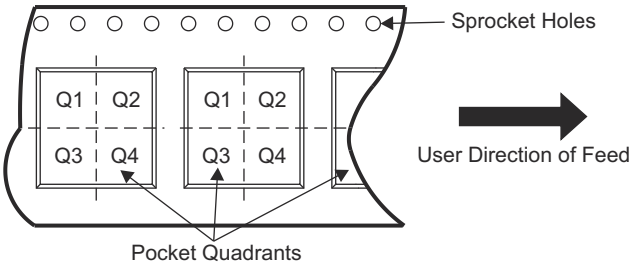


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

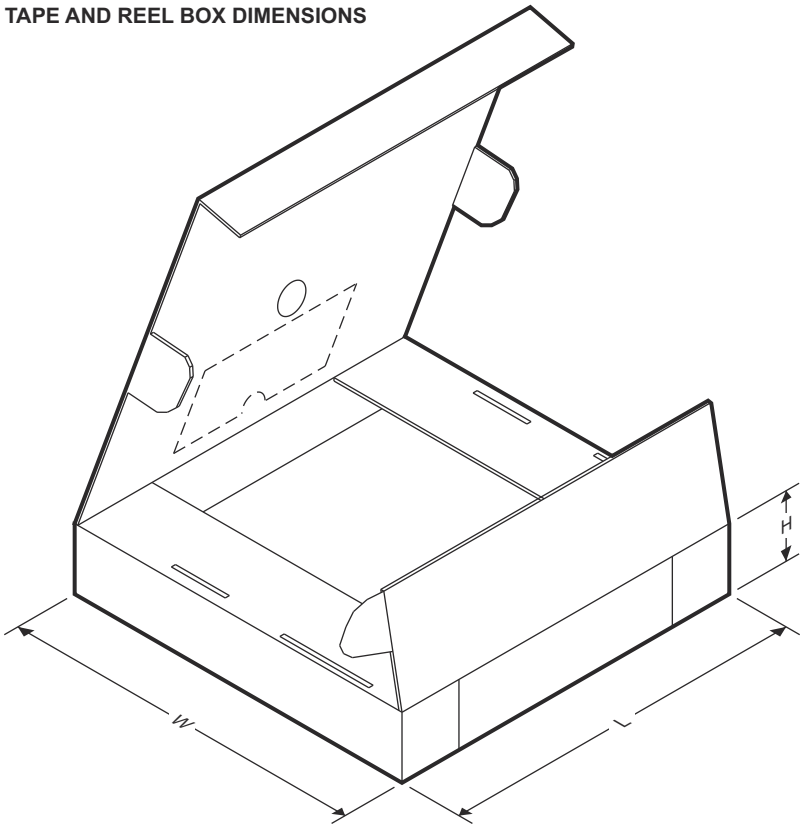
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4990QPWRQ1	TSSOP	PW	14	3000	330	12.4	6.9	5.6	1.6	8	12	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



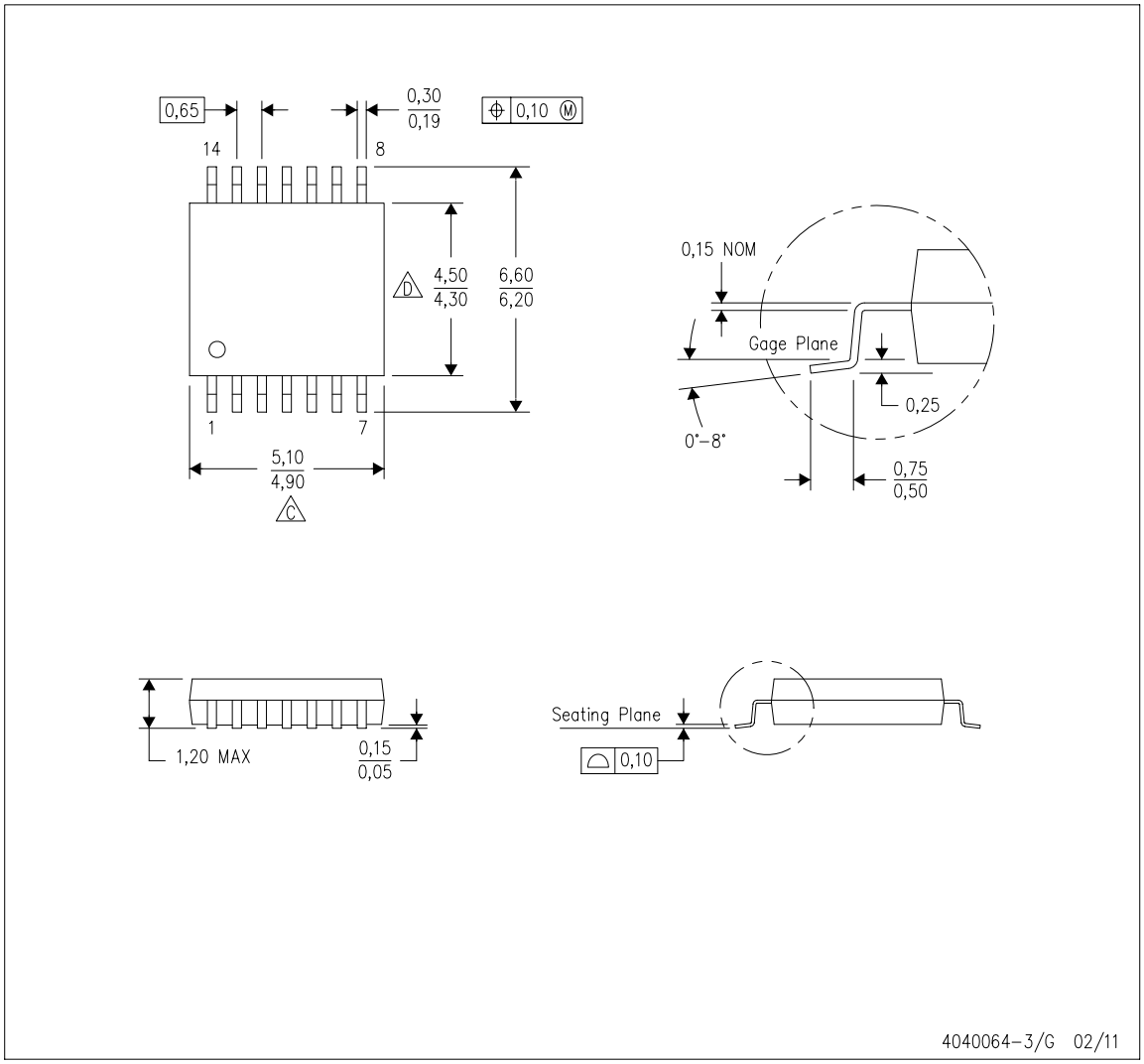
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4990QPWRQ1	TSSOP	PW	14	3000	356	356	35

ADVANCE INFORMATION

10.2 Mechanical Data

MECHANICAL DATA

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

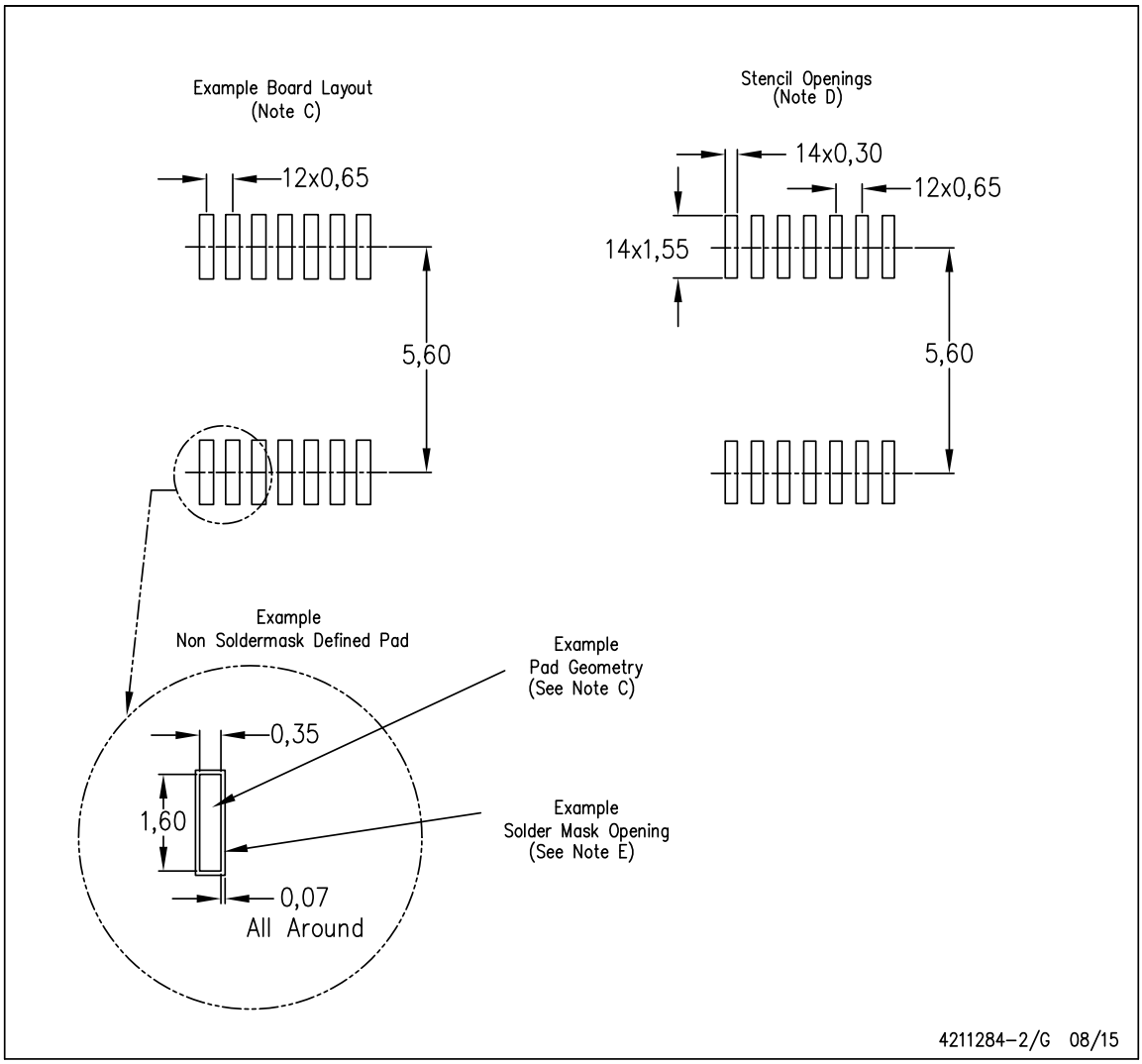


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

ADVANCE INFORMATION

LAND PATTERN DATA

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4990QPWRQ1	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q4990PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA4990-Q1 :

- Catalog : OPA4990

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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