HIGH-VOLTAGE, HIGH-CURRENT OPERATIONAL AMPLIFIER

Check for Samples: OPA549-HiRel

FEATURES

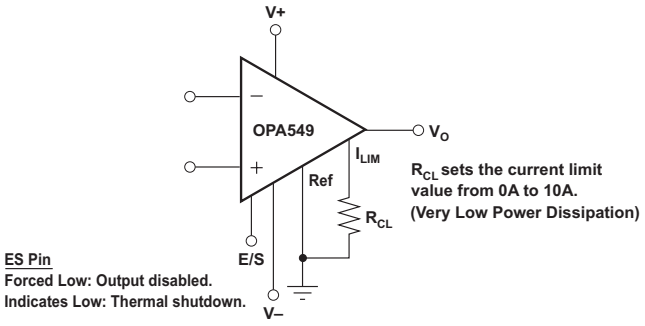
- **High Output Current:**
  - **8-A Continuous**
  - **10-A Peak**
- **Wide Power Supply Range:**
  - **Single Supply: 8 V to 60 V**
  - **Dual Supply: ±4 V to ±30 V**
- **Wide Output Voltage Swing**
- **Fully Protected:**
  - **Thermal Shutdown**
  - **Adjustable Current**
- **Output Disable Control**
- **Thermal Shutdown Indicator**
- **High Slew Rate: 9 V/µs**
- **Control Reference Pin**
- **11-Lead Power Package**

APPLICATIONS

- **Valve, Actuator Drivers**
- **Synchro, Servo Drivers**
- **Power Supplies**
- **Test Equipment**
- **Transducer Excitation**
- **Audio Power Amplifiers**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C), Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**



(1) Additional temperature ranges available - contact factory

DESCRIPTION

The OPA549 is a low-cost, high-voltage and high-current operational amplifier ideal for driving a wide variety of loads. This laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high output voltage and current.

The OPA549 operates from either single or dual supplies for design flexibility. The input common-mode range extends below the negative supply.

The OPA549 is internally protected against over-temperature conditions and current overloads. In addition, the OPA549 provides an accurate, user-selected current limit. Unlike other designs which use a power resistor in series with the output current path, the OPA549 senses the load indirectly. This allows the current limit to be adjusted from 0 A to 10 A with a resistor or potentiometer, or controlled digitally with a voltage-out or current-out digital-to-analog converter (DAC).

The enable/status (E/S) pin provides two functions. It can be monitored to determine if the device is in thermal shutdown, and it can be forced low to disable the output stage and effectively disconnect the load.

The OPA549 is available in an 11-lead power package. Its copper tab allows easy mounting to a heat sink for excellent thermal performance. Operation is specified over the temperature range of −55°C to 125°C.

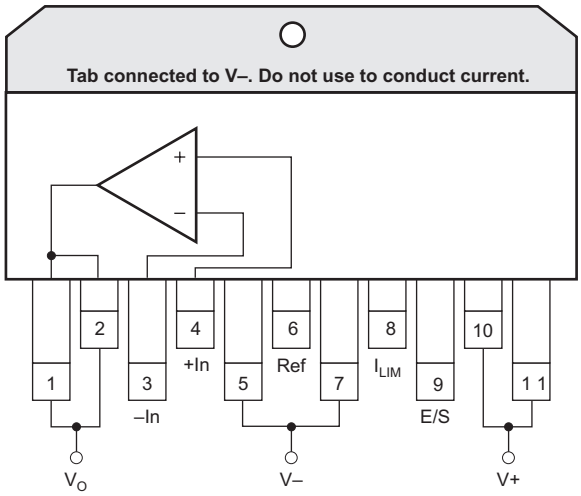
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_{CASE}	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	KVC	OPA549MKVC	OPA549M

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.



Connect both pins 1 and 2 to output.
Connect both pins 5 and 7 to V–.
Connect both pins 10 and 11 to V+.

Figure 1. Connection Diagram

ABSOLUTE MAXIMUM RATINGS(1)

	Output current		See Figure 8
V+ to V-	Supply voltage		60 V
V_I	Input voltage range		(V−) − 0.5 V to (V+) + 0.5 V
	Input voltage reference maximum		(V+) - 8
	Input shutdown voltage		Ref - 0.5 V to V+
T_{OP}	Operating temperature		−55°C to 125°C
T_{stg}	Storage temperature		−55°C to 125°C
T_J	Junction temperature		150°C
	Lead temperature	Soldering, 10 s	300°C
ESD	Electrostatic discharge rating	Human Body Model	2000 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		OPA549 KVC 11 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	21.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	17.4	
θ_{JB}	Junction-to-board thermal resistance(4)	9.2	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	9.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

At T_{CASE} = 25°C, V_S = ±30V, Ref = 0V, and and E/S pin open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = 0 V, I_O = 0 A, T_{CASE} = 25°C		±1	±5	mV
		V_{CM} = 0 V, I_O = 0 A, T_{CASE} = -55°C to 125°C			±7	mV
dV_{OS}/dT	Input offset voltage drift	V_{CM} = 0 V, I_O = 0 A, T_{CASE} = -55°C to 125°C		±20		µV/°C
PSRR	Input offset voltage vs power supply	V_S = ±4 V to ±30 V, Ref = V–, T_{CASE} = -55°C to 125°C		25	100	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current(1)	V_{CM} = 0 V, T_{CASE} = -55°C to 125°C		-100	-500	nA
I_{OS}	Input offset current	V_{CM} = 0 V, T_{CASE} = -55°C to 125°C		±5	±100	nA
NOISE						
e_n	Input voltage noise density	f = 1 kHz		705		nV/√Hz
i_n	Input current noise density	f = 1 kHz		1		pA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	Linear operation; Positive, T_{CASE} = -55°C to 125°C	(V+) – 3	(V+) - 2.3		V
		Linear operation; Negative, T_{CASE} = -55°C to 125°C	(V-) – 0.1	(V-) – 0.2		
CMRR	Common-mode rejection ratio	V_{CM} = (V-) - 0.1 V to (V+) - 3 V, T_{CASE} = -55°C to 125°C	78	95		dB
INPUT IMPEDANCE						
	Differential			10^7 || 6		Ω || pF
	Common-mode			10^9 || 4		Ω || pF

(1) Positive conventional current is defined as flowing into the terminal.

ELECTRICAL CHARACTERISTICS (continued)

At T_{CASE} = 25°C, V_S = ±30V, Ref = 0V, and and E/S pin open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_O = ±25 V, R_L = 1 kΩ, T_{CASE} = -55°C to 125°C	100	110		dB
		V_O = ±25 V, R_L = 4 Ω		100		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			0.9		MHz
SR	Slew rate	G = 1, 50-Vp-p step, R_L = 4 Ω		9		V/µs
	Full-power bandwidth			See Typical Characteristics		
t_S	Settling time	±0.1%, G = -10, 50-V step		20		µs
THD+N	Total harmonic distortion + noise(2)	f = 1 kHz, R_L = 4 Ω, G = 3, Power = 25 W		0.015		%
OUTPUT						
	Voltage output	I_O = 2 A, T_{CASE} = -55°C to 125°C	(V+) - 3.7	(V+) - 2.7		V
		I_O = -2 A, T_{CASE} = -55°C to 125°C	(V-) + 1.8	(V-) + 1.4		
		I_O = 8 A, T_{CASE} = -55°C to 125°C	(V+) - 5.0	(V+) - 4.3		
		I_O = -8 A, T_{CASE} = -55°C to 125°C	(V-) + 4.9	(V-) + 3.9		
		R_L = 8 Ω to V-, T_{CASE} = -55°C to 125°C	(V-) + 0.4	(V-) + 0.1		
	Maximum continuous current output(3)	dc	±8			A
		ac; Waveform cannot exceed 10-A peak		8		A rms
	Output current limit range			0 to ±10		A
	Output current limit equation			I_{LIM} = 15800 x 4.75 V/(7500 Ω + R_{CL})		A
	Output current limit tolerance(4)	R_{CL} = 7.5 kΩ (I_{LIM} = ±5 A), R_L = 4 Ω		±200	±600	mA
C_{LOAD}	Capacitive load drive (stable operation)			See Typical Characteristics		
	Output disabled leakage current	V_O = 0 V, T_{CASE} = -55°C to 125°C	-2000	±200	2000	µA
	Output disabled capacitance			750		pF
OUTPUT ENABLE/STATUS (E/S) PIN						
	Shutdown input mode $V_{E/S}$ high (output enabled)	E/S pin open or forced high	(Ref) + 2.4			V
	Shutdown input mode $V_{E/S}$ low (output disabled)	E/S pin forced low			(Ref) + 0.8	V
	Shutdown input mode $I_{E/S}$ high (output enabled)	E/S pin indicates high		-50		µA
	Shutdown input mode $I_{E/S}$ low (output disabled)	E/S pin indicates low		-55		µA
	Ouput disable time			1		µs
	Output enable time			3		µs
	Thermal shutdown status output (normal operation)	Sourcing 20 µA	(Ref) + 2.4	(Ref) + 3.5		V
	Thermal shutdown status output (thermally shutdown)	Sinking 5 µA, T_J > 160°C		(Ref) + 0.2	(Ref) + 0.8	V
	Junction temperature	Shutdown		160		°C
		Reset from shutdown		140		

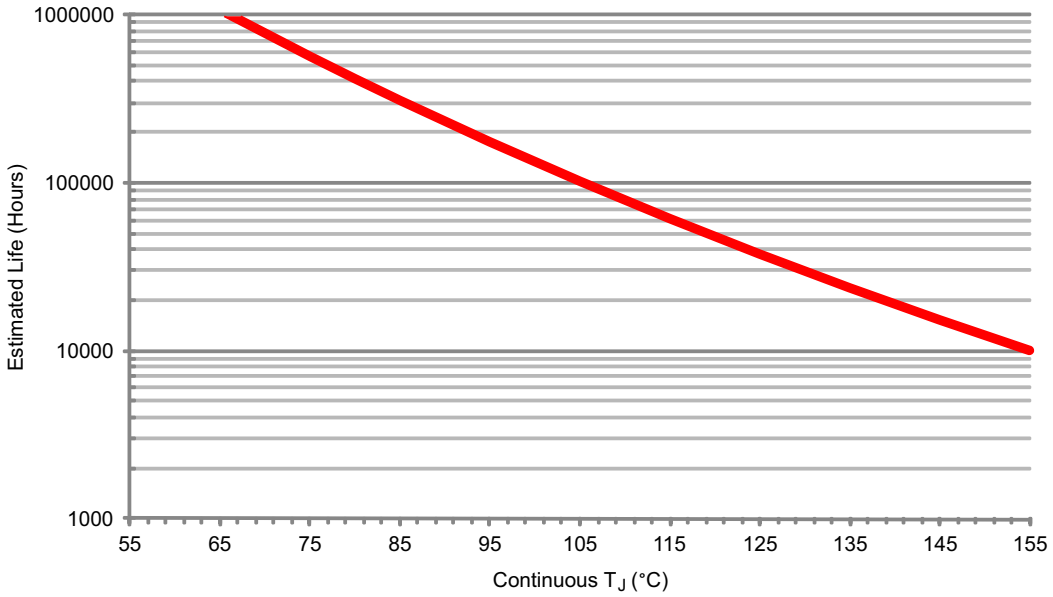
(2) See Total Harmonic Distortion + Noise vs Frequency in the Typical Characteristics section for additional power levels.
(3) See Safe Operating Area (SOA) in the Typical Characteristics section.
(4) High-speed test at T_J = 25°C

ELECTRICAL CHARACTERISTICS (continued)

At T_{CASE} = 25°C, V_S = ±30V, Ref = 0V, and and E/S pin open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ref (REFERENCE PIN FOR CONTROL SIGNALS)						
	Voltage range		V-			V
	Current(5)			-3.5		mA
POWER SUPPLY						
V_S	Specified voltage range	T_{CASE} = -55°C to 125°C		±30		V
	Operating voltage range	(V+) - (V-)	8		60	V
I_Q	Quiescent current	I_{LIM} connected to Ref I_O = 0, T_{CASE} = -55°C to 125°C		±26	±35	mA
		Shutdown mode; I_{LIM} connected to Ref		±6		

(5) Positive conventional current is defined as flowing into the terminal.



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

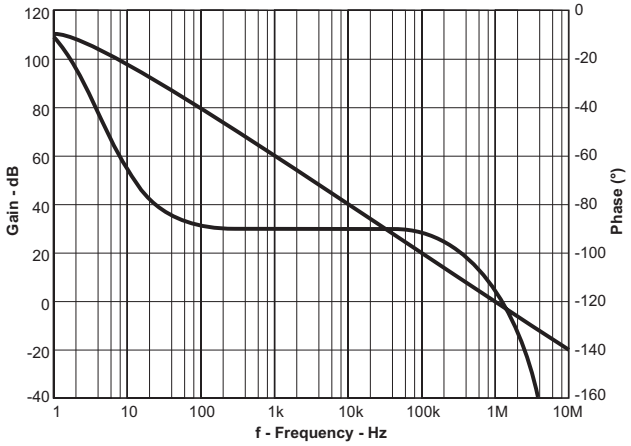
D. This curve represents operation with 8-A continuous output current.

Figure 2. OPA549MKVC Operating Life Derating Chart

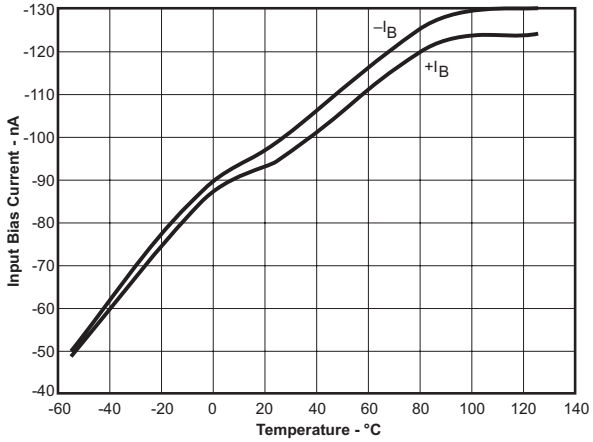
TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

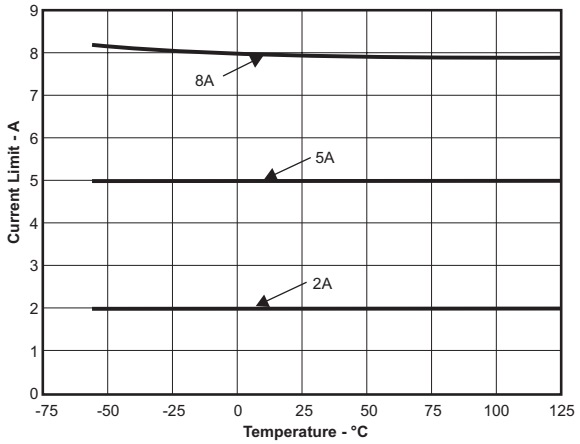
OPEN-LOOP AND PHASE vs FREQUENCY



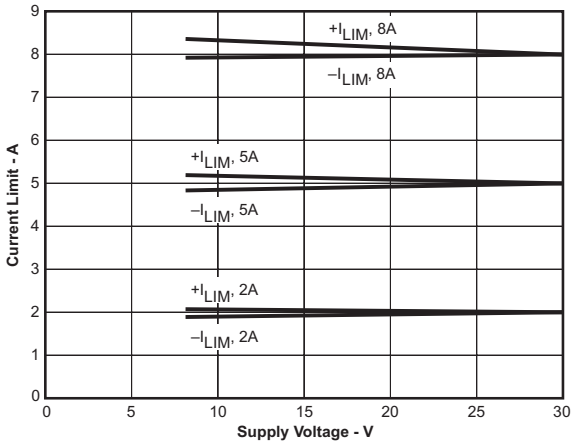
INPUT BIAS CURRENT vs TEMPERATURE



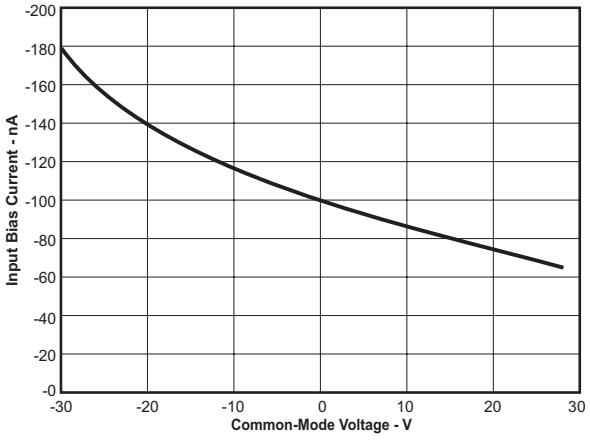
CURRENT LIMIT vs TEMPERATURE



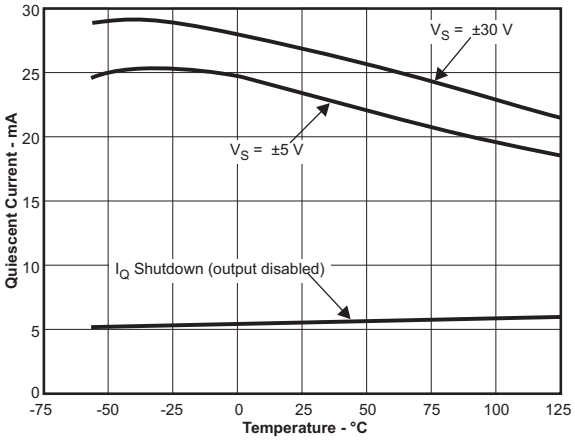
CURRENT LIMIT vs SUPPLY VOLTAGE



INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



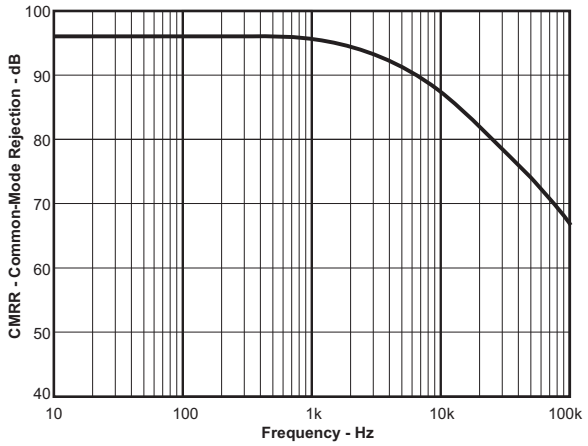
QUIESCENT CURRENT vs TEMPERATURE



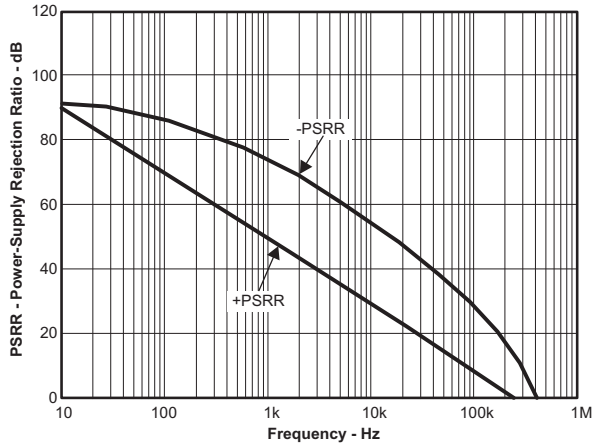
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

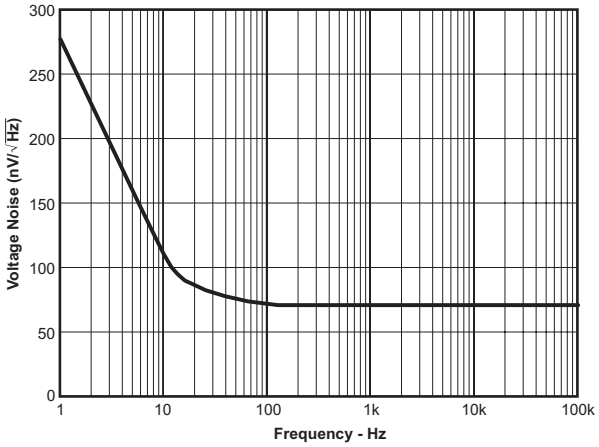
COMMON-MODE REJECTION RATIO vs FREQUENCY



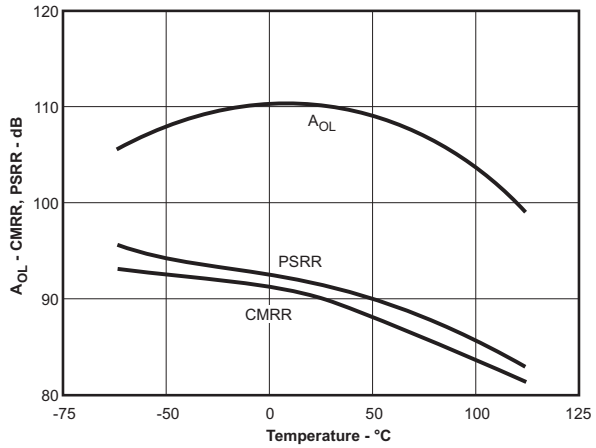
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



VOLTAGE NOISE DENSITY vs FREQUENCY



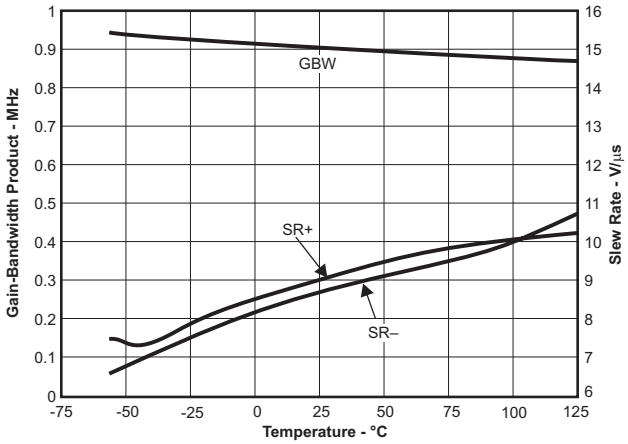
OPEN-LOOP GAIN, COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE



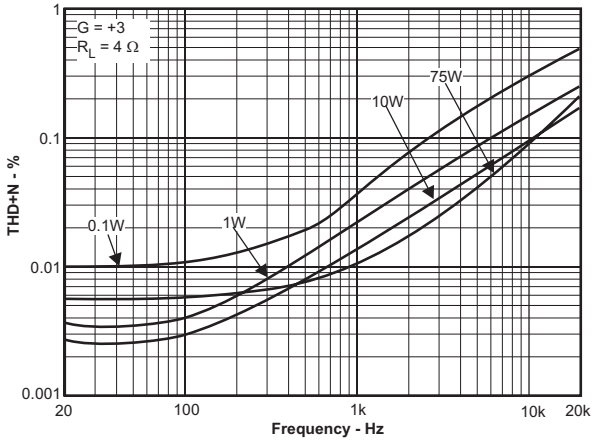
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

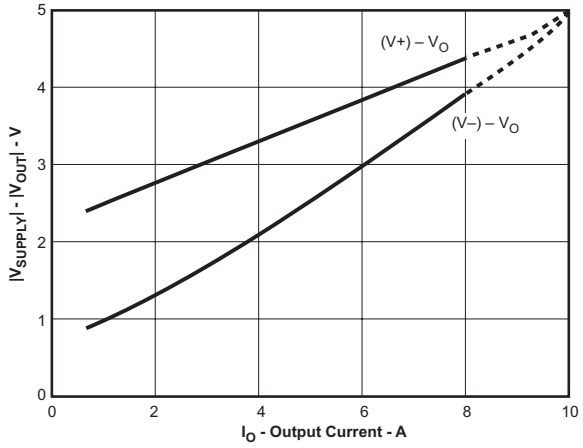
GAIN-BANDWIDTH PRODUCT AND SLEW RATE vs TEMPERATURE



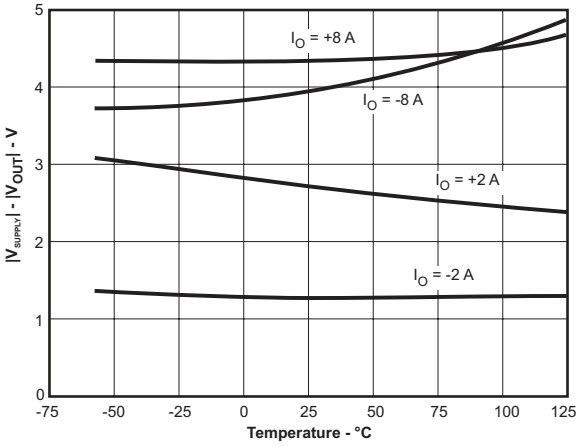
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



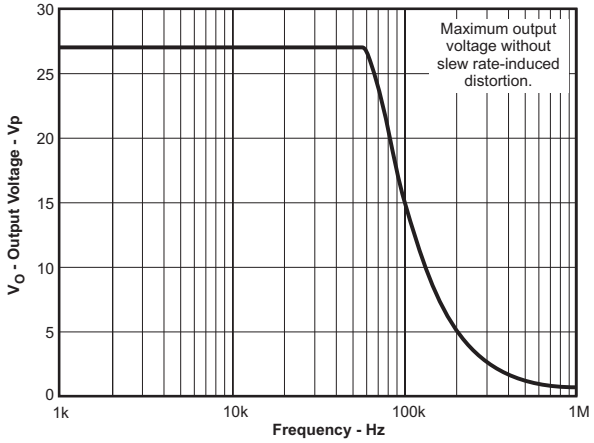
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



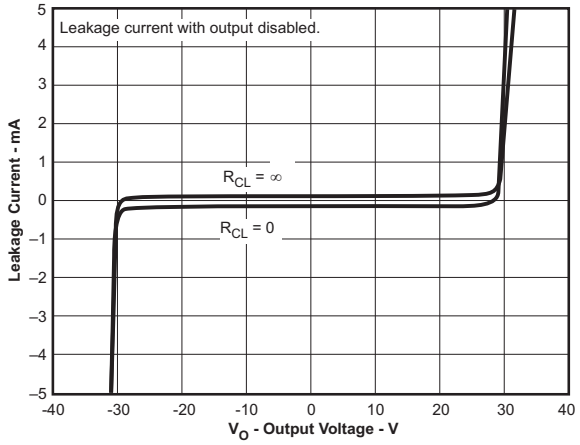
OUTPUT VOLTAGE SWING vs TEMPERATURE



MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



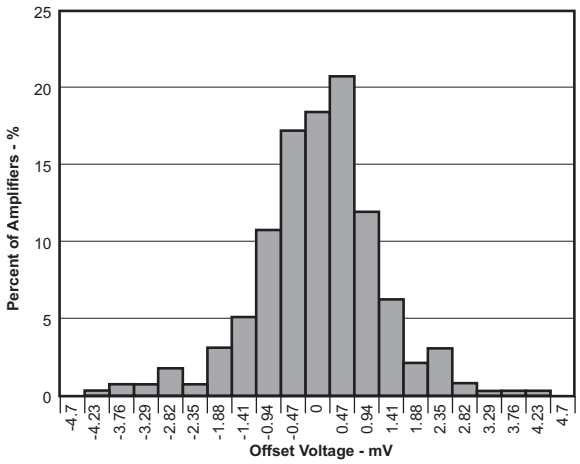
OUTPUT LEAKAGE CURRENT vs APPLIED OUTPUT VOLTAGE



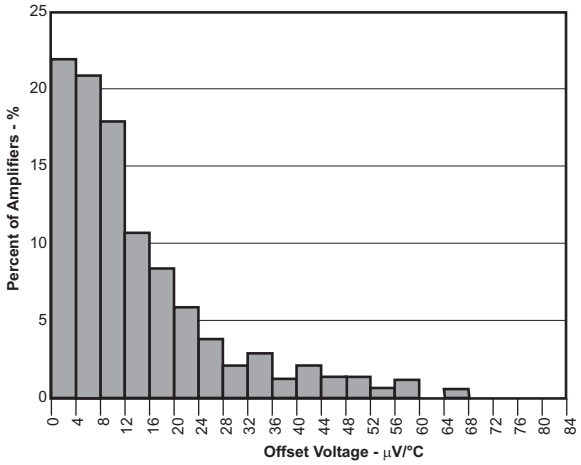
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

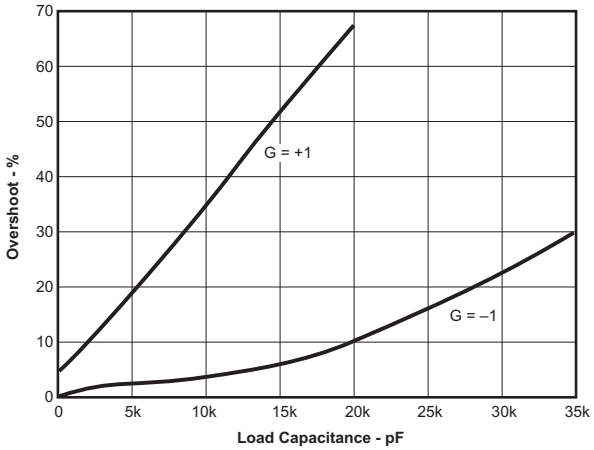
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



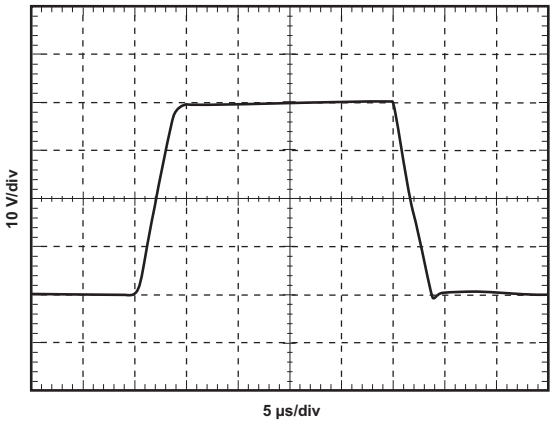
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



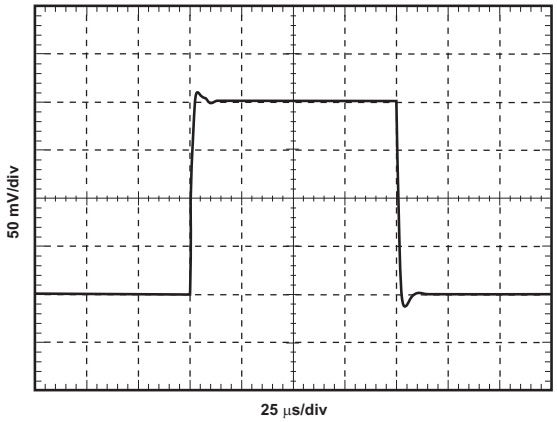
SMALL-SIGNAL OVERSHOOT VS LOAD CAPACITANCE



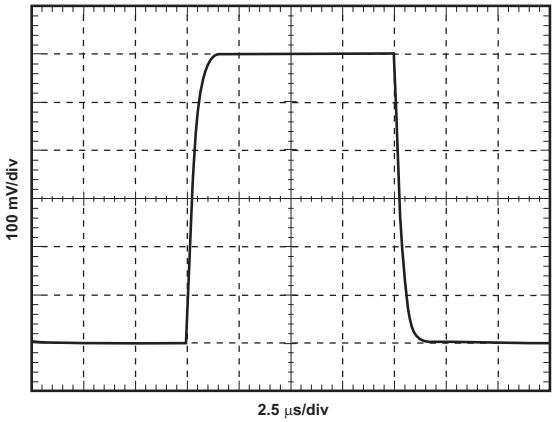
LARGE-SIGNAL STEP RESPONSE
G = 3, C_L = 1000pF



SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 1000pF



SMALL-SIGNAL STEP RESPONSE
G = 3, C_L = 1000pF

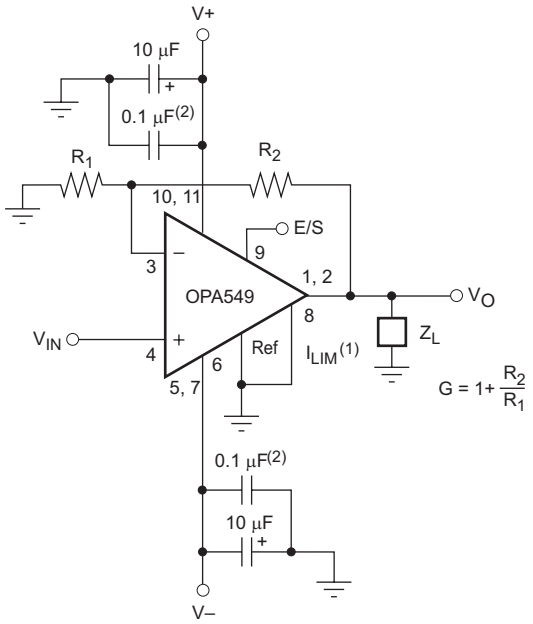


APPLICATION INFORMATION

Figure 3 shows the OPA549 connected as a basic noninverting amplifier. The OPA549 can be used in virtually any operational amplifier configuration.

Power-supply terminals should be bypassed with low series impedance capacitors. The technique shown in Figure 3, using a ceramic and tantalum type in parallel, is recommended. Power-supply wiring should have low series impedance.

Be sure to connect both output pins (pins 1 and 2).



NOTES: (1) I_{LIM} connected to Ref gives the maximum current limit, 10A (peak). (2) Connect capacitors directly to package power-supply pins.

Figure 3. Basic Circuit Connections

Power Supplies

The OPA549 operates from single (8-V to 60-V) or dual (±4-V to ±30-V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics. Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not need to be equal. The OPA549 can operate with as little as 8 V between the supplies and with up to 60 V between the supplies. For example, the positive supply could be set to 55 V with the negative supply at –5 V. Be sure to connect both V– pins (pins 5 and 7) to the negative power supply, and both V+ pins (pins 10 and 11) to the positive power supply. Package tab is internally connected to V–; however, do not use the tab to conduct current.

Control Reference (Ref) Pin

The OPA549 features a reference (Ref) pin to which the I_{LIM} and the E/S pin are referred. Ref simply provides a reference point accessible to the user that can be set to V–, ground, or any reference of the user's choice. Ref cannot be set below the negative supply or above (V+) – 8 V. If the minimum V_S is used, Ref must be set at V–.

Adjustable Current Limit

The OPA549's accurate, user-defined current limit can be set from 0 A to 10 A by controlling the input to the I_{LIM} pin. Unlike other designs, which use a power resistor in series with the output current path, the OPA549 senses the load indirectly. This allows the current limit to be set with a 0-µA to 633-µA control signal. In contrast, other designs require a limiting resistor to handle the full output current (up to 10 A in this case).

Although the design of the OPA549 allows output currents up to 10 A, it is not recommended that the device be operated continuously at that level. The highest rated continuous current capability is 8 A. Continuously running the OPA549 at output currents greater than 8 A will degrade long-term reliability.

Operation of the OPA549 with current limit less than 1 A results in reduced current limit accuracy. Applications requiring lower output current may be better suited to the OPA547 or OPA548.

Resistor-Controlled Current Limit

See Figure 4(a) for a simplified schematic of the internal circuitry used to set the current limit. Leaving the I_{LIM} pin open programs the output current to zero, while connecting I_{LIM} directly to Ref programs the maximum output current limit, typically 10 A.

With the OPA549, the simplest method for adjusting the current limit uses a resistor or potentiometer connected between the I_{LIM} pin and Ref according to Equation 1:

$$R_{CL} = \frac{75kV}{I_{LIM}} - 7.5k\Omega \quad (1)$$

Refer to Figure 4 for commonly used values.

Digitally-Controlled Current Limit

The low-level control signal (0 µA to 633 µA) also allows the current limit to be digitally controlled by setting either a current (I_{SET}) or voltage (V_{SET}). The output current I_{LIM} can be adjusted by varying I_{SET} according to Equation 2:

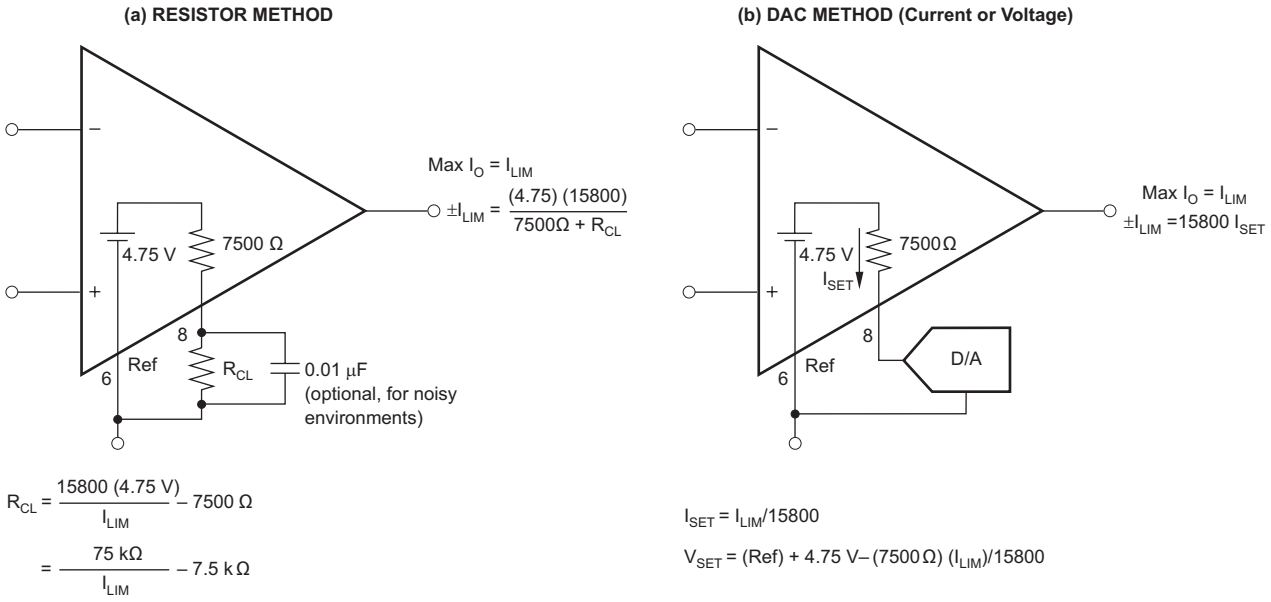
$$I_{SET} = \frac{I_{LIM}}{15800} \quad (2)$$

Figure 4(b) demonstrates a circuit configuration implementing this feature.

The output current I_{LIM} can be adjusted by varying V_{SET} according to Equation 3:

$$V_{SET} = (\mathrm{Ref}) + 4.75\mathrm{V} - \frac{(7500W)(I_{LIM})}{15800} \quad (3)$$

demonstrates a circuit configuration implementing this feature.



OPA549 CURRENT LIMIT: 0 A to 10 A

DESIRED CURRENT LIMIT	RESISTOR(1) (R_{CL})	CURRENT (I_{SET})	VOLTAGE (V_{SET})
0A(2)	I_{LIM} Open	0 µA	(Ref) + 4.75 V
2.5 A	22.6 kΩ	158 µA	(Ref) + 3.56 V
3 A	17.4 kΩ	190 µA	(Ref) + 3.33 V
4 A	11.3 kΩ	253 µA	(Ref) + 2.85 V
5 A	7.5 kΩ	316 µA	(Ref) + 2.38 V
6 A	4.99 kΩ	380 µA	(Ref) + 1.90 V
7 A	3.24 kΩ	443 µA	(Ref) + 1.43 V
8 A	1.87 kΩ	506 µA	(Ref) + 0.95 V
9 A	845 Ω	570 µA	(Ref) + 0.48 V
10 A	I_{LIM} Connected to Ref	633 µA	(Ref)

NOTES: (1) Resistors are nearest standard 1% values. (2) Offset in the current limit circuitry may introduce approximately ±0.25 A variation at low current limit values.

Figure 4. Adjustable Current Limit

Enable/Status (E/S) Pin

The enable/status pin provides two unique functions: 1) output disable by forcing the pin low, and 2) thermal shutdown indication by monitoring the voltage level at the pin. Either or both of these functions can be utilized in an application. For normal operation (output enabled), the E/S pin can be left open or driven high (at least 2.4 V above Ref). A small value capacitor connected between the E/S pin and C_{REF} may be required for noisy applications.

Output Disable

To disable the output, the E/S pin is pulled to a logic low (no greater than 0.8 V above Ref). Typically the output is shut down in 1 µs. To return the output to an enabled state, the E/S pin should be disconnected (open) or pulled to at least 2.4 V above Ref. It should be noted that driving the E/S pin high (output enabled) does not defeat internal thermal shutdown; however, it does prevent the user from monitoring the thermal shutdown status. Figure 5 shows an example implementing this function.

This function not only conserves power during idle periods (quiescent current drops to approximately 6 mA) but also allows multiplexing in multi-channel applications. See Figure 14 for two OPA549s in a switched amplifier configuration. The on/off state of the two amplifiers is controlled by the voltage on the E/S pin. Under these conditions, the disabled device will behave like a 750-pF load. Slewing faster than 3 V/µs will cause leakage current to rapidly increase in devices that are disabled, and will contribute additional load. At high temperature (125°C), the slewing threshold drops to approximately 2 V/µs. Input signals must be limited to avoid excessive slewing in multiplexed applications.

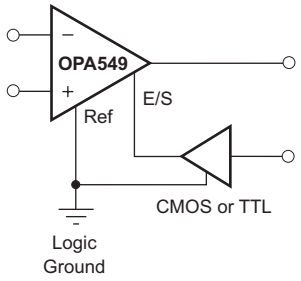


Figure 5. Output Disable

Thermal Shutdown Status

The OPA549 has thermal shutdown circuitry that protects the amplifier from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C and allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. The E/S pin can be monitored to determine if the device is in shutdown. During normal operation, the voltage on the E/S pin is typically 3.5V above Ref. Once shutdown has occurred, this voltage drops to approximately 200 mV above Ref. Figure 6 shows an example implementing this function.

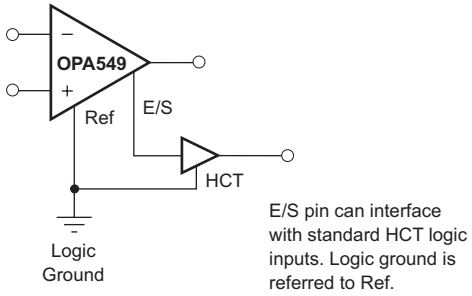


Figure 6. Thermal Shutdown Status

External logic circuitry or an LED can be used to indicate if the output has been thermally shutdown, see Figure 12.

Output Disable and Thermal Shutdown Status

As mentioned earlier, the OPA549's output can be disabled and the disable status can be monitored simultaneously. Figure 7 provides an example of interfacing to the E/S pin.

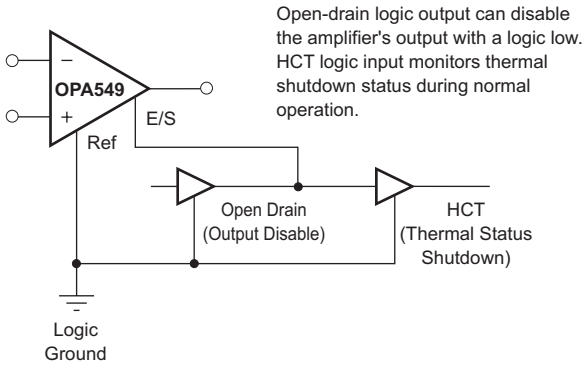


Figure 7. Output Disable and Thermal Shutdown Status

Safe Operating Area

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistor, $V_S - V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The safe operating area (SOA curve, Figure 8) shows the permissible range of voltage and current.

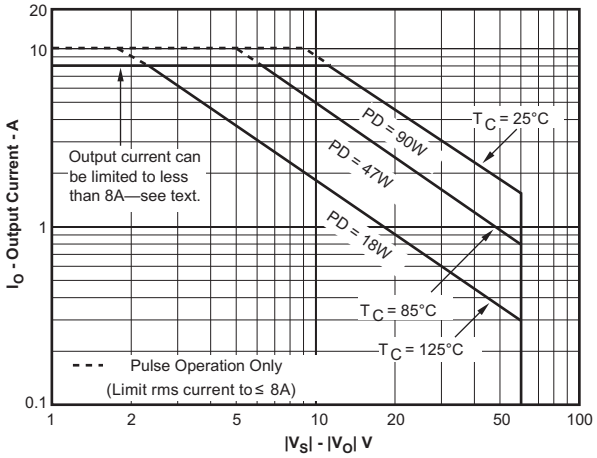


Figure 8. Safe Operating Area

The safe output current decreases as $V_S - V_O$ increases. Output short circuits are a very demanding case for SOA. A short circuit to ground forces the full power-supply voltage (V+ or V–) across the conducting transistor. Increasing the case temperature reduces the safe output current that can be tolerated without activating the thermal shutdown circuit of the OPA549. For further insight on SOA, consult Application Bulletin (SBOA022).

Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower. Application Bulletin (SBOA022) explains how to calculate or measure power dissipation with unusual signals and loads.

Thermal Protection

Power dissipated in the OPA549 will cause the junction temperature to rise. Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C and resets when the die has cooled to 140°C. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink) increase the ambient temperature until the thermal protection is triggered.

Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

The internal protection circuitry of the OPA549 was designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the OPA549 into thermal shutdown will degrade reliability.

Amplifier Mounting and Heat Sinking

Most applications require a heat sink to assure that the maximum operating junction temperature (125°C) is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the Equations:

$$T_J = T_A + P_D\theta_{JA} \quad (4)$$

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA} \quad (5)$$

Where:

- T_J = Junction Temperature (°C)
- T_A = Ambient Temperature (°C)
- P_D = Power Dissipated (W)
- θ_{JC} = Junction-to-Case Thermal Resistance (°C/W)
- θ_{CH} = Case-to-Heat Sink Thermal Resistance (°C/W)
- θ_{HA} = Heat Sink-to-Ambient Thermal Resistance (°C/W)
- θ_{JA} = Junction-to-Air Thermal Resistance (°C/W)

Figure 9 shows maximum power dissipation versus ambient temperature with and without the use of a heat sink. Using a heat sink significantly increases the maximum power dissipation at a given ambient temperature, as shown in Figure 9.

The challenge in selecting the heat sink required lies in determining the power dissipated by the OPA549. For dc output, power dissipation is simply the load current times the voltage developed across the conducting output transistor, $P_D = I_L (V_S - V_O)$. Other loads are not as simple. Consult the SBOA022 Application Report for further insight on calculating power dissipation. Once power dissipation for an application is known, the proper heat sink can be selected.

Heat Sink Selection Example

An 11-lead power ZIP package is dissipating 10 Watts. The maximum expected ambient temperature is 40°C. Find the proper heat sink to keep the junction temperature below 125°C (150°C minus 25°C safety margin).

Combining Equation 4 and Equation 5 gives:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CH} + \theta_{HA}) \quad (6)$$

T_J, T_A, and P_D are given. θ_{JC} is provided in the Specifications Table, 0.1°C/W (dc). θ_{CH} can be obtained from the heat sink manufacturer. Its value depends on heat sink size, area, and material used. Semiconductor package type, mounting screw torque, insulating material used (if any), and thermal joint compound used (if any) also affect θ_{CH}. A typical θ_{CH} for a mounted 11-lead power ZIP package is 0.5°C/W. Now we can solve for θ_{HA}:

$\theta_{HA} = [(T_J - T_A)/P_D] - \theta_{JC} - \theta_{CH}$

$\theta_{HA} = [(125°C - 55°C)/10 W] - 0.1°C/W - 0.5°C/W$

$\theta_{HA} = 6.4°C/W$

To maintain junction temperature below 125°C, the heat sink selected must have a θ_{HA} less than 6.4°C/W. In other words, the heat sink temperature rise above ambient must be less than 64°C (6.4°C/W • 10 W). For example, at 10 W, Thermalloy model number 6396B has a heat sink temperature rise of 56°C (θ_{HA} = 56°C/10 W = 5.6°C/W), which is below the required 66°C required in this example. Thermalloy model number 6399B has a sink temperature rise of 33°C (θ_{HA} = 33°C/10 W = 3.3°C/W), which is also below the required 66°C required in this example. Figure 9 shows power dissipation versus ambient temperature for a 11-lead power ZIP package with the Thermalloy 6396B and 6399B heat sinks.

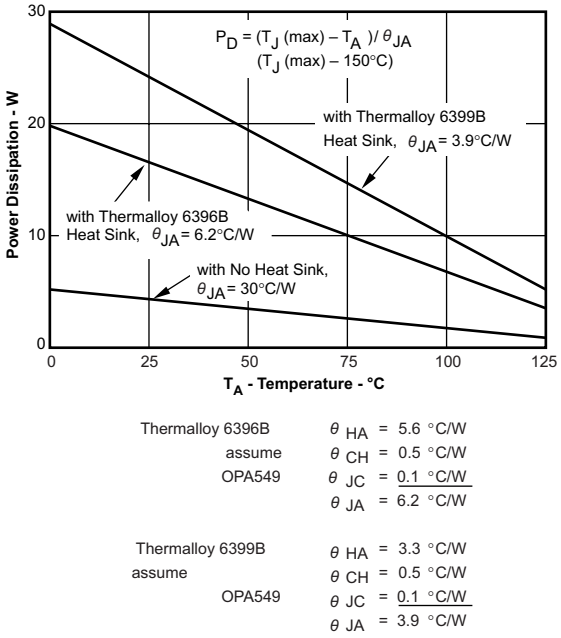


Figure 9. Maximum Power Dissipation vs Ambient Temperature

Another variable to consider is natural convection versus forced convection air flow. Forced-air cooling by a small fan can lower θ_{CA} (θ_{CH} + θ_{HA}) dramatically. Some heat sink manufacturers provide thermal data for both of these cases. Heat sink performance is generally specified under idealized conditions that may be difficult to achieve in an actual application. For additional information on determining heat sink requirements, consult Application Report (SBOA021).

As mentioned earlier, once a heat sink has been selected, the complete design should be tested under worst-case load and signal conditions to ensure proper thermal protection. Any tendency to activate the thermal protection circuitry may indicate inadequate heat sinking.

The tab of the 11-lead power ZIP package is electrically connected to the negative supply, V–. It may be desirable to isolate the tab of the 11-lead power ZIP package from its mounting surface with a mica (or other film) insulator. For lowest overall thermal resistance, it is best to isolate the entire heat sink/OPA549 structure from the mounting surface rather than to use an insulator between the semiconductor and heat sink.

Output Stage Compensation

The complex load impedances common in power op amp applications can cause output stage instability. For normal operation, output compensation circuitry is typically not required. However, for difficult loads or if the OPA549 is intended to be driven into current limit, an R/C network may be required. Figure 10 shows an output R/C compensation (snubber) network which generally provides excellent stability.

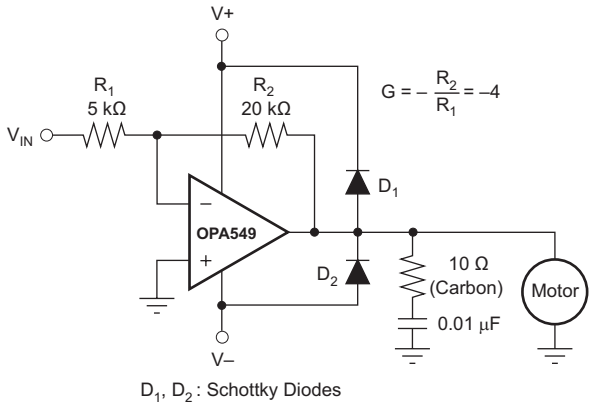


Figure 10. Motor Drive Circuit

A snubber circuit may also enhance stability when driving large capacitive loads (> 1000 pF) or inductive loads (motors, loads separated from the amplifier by long cables). Typically, 3-Ω to 10-Ω resistors in series with 0.01-µF to 0.1-µF capacitors is adequate. Some variations in circuit values may be required with certain loads.

Output Protection

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 10. Schottky rectifier diodes with an 8-A or greater continuous rating are recommended.

Voltage Source Application

Figure 11 illustrates how to use the OPA549 to provide an accurate voltage source with only three external resistors. First, the current limit resistor, R_{CL}, is chosen according to the desired output current. The resulting voltage at the I_{LIM} pin is constant and stable over temperature. This voltage, V_{CL}, is connected to the noninverting input of the op amp and used as a voltage reference, thus eliminating the need for an external reference. The feedback resistors are selected to gain V_{CL} to the desired output voltage level.

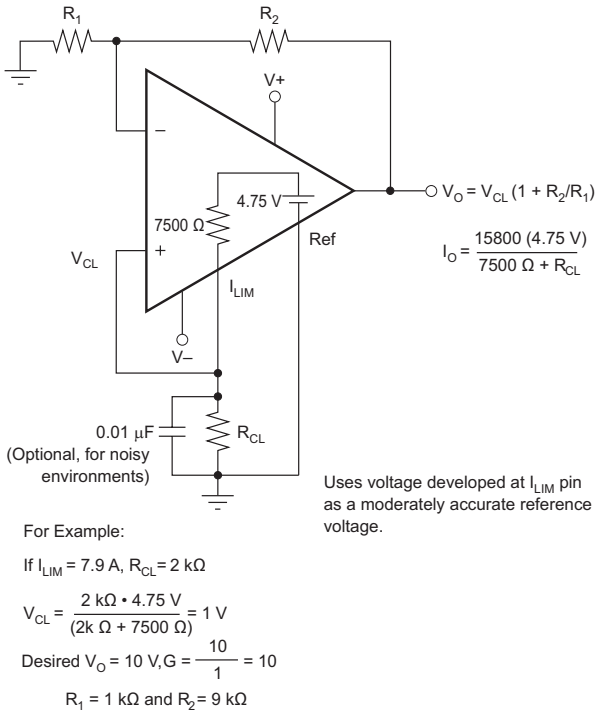


Figure 11. Voltage Source

Programmable Power Supply

A programmable source and sink power supply can easily be built using the OPA549. Both the output voltage and output current are user-controlled. See Figure 12 for a circuit using potentiometers to adjust the output voltage and current while Figure 13 uses DACs. An LED connected to the E/S pin through a logic gate indicates if the OPA549 is in thermal shutdown.

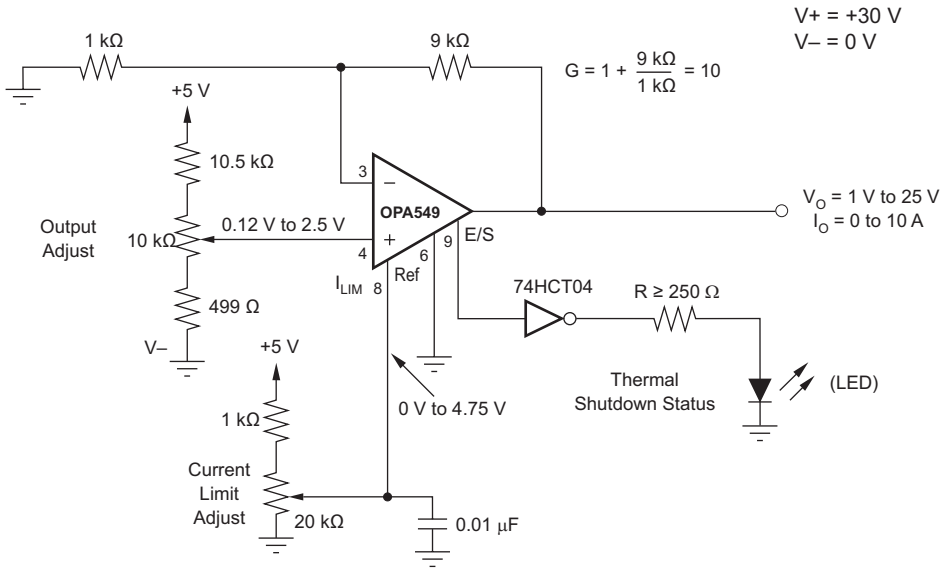
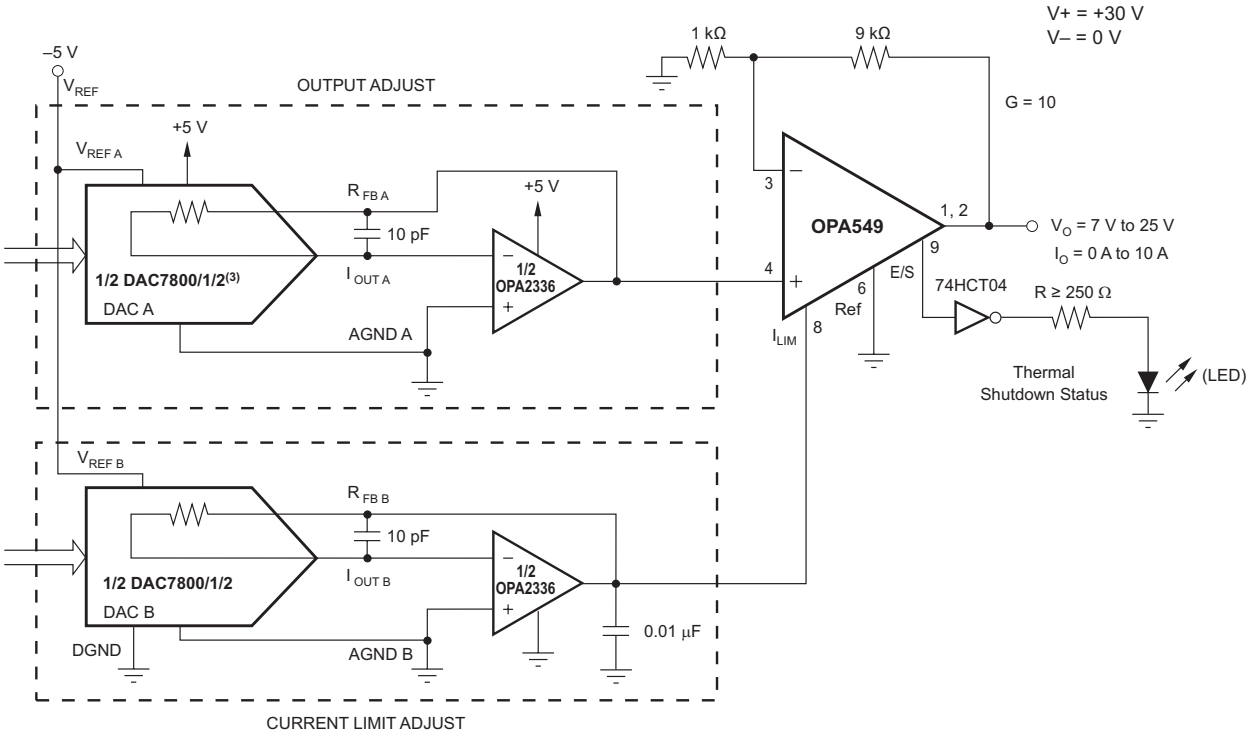
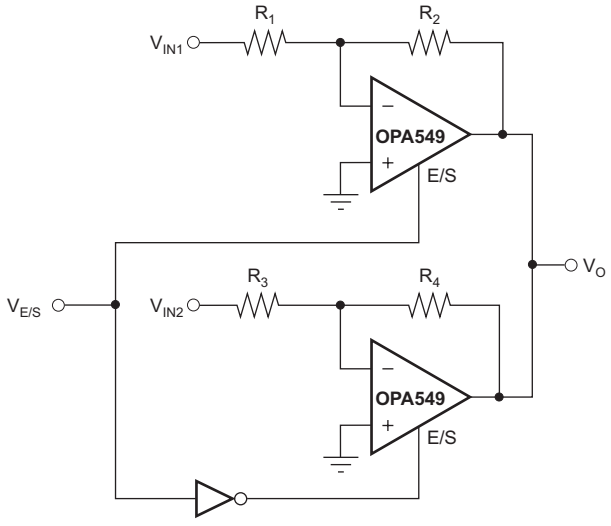


Figure 12. Resistor-Controlled Programmable Power Supply



Choose DAC780X based on digital interface: DAC7800—12-bit interface, DAC7801—8-bit interface + 4 bits, DAC7802—serial interface.

Figure 13. Digitally-Controlled Programmable Power Supply



Limit output slew rates to ≤ 3 V/ µs (see text).

Figure 14. Switched Amplifier

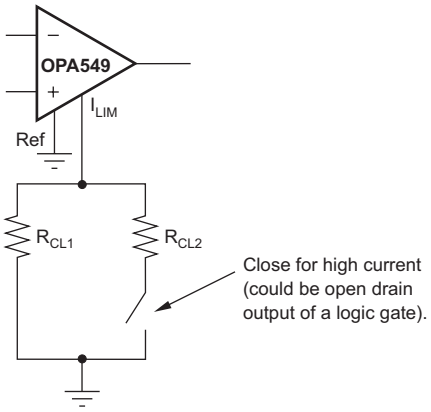


Figure 15. Multiple Current Limit Values

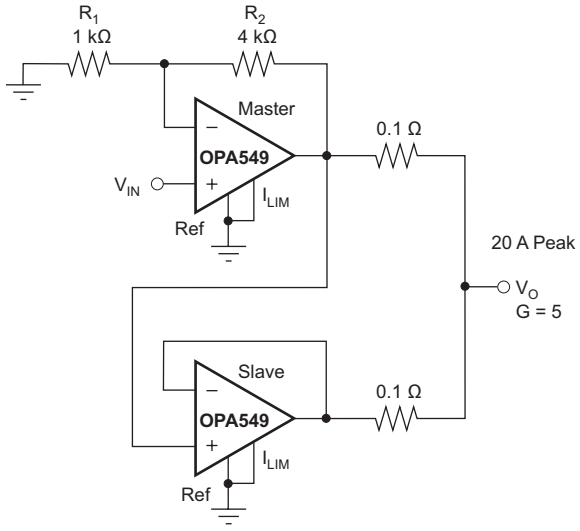


Figure 16. Parallel Output for Increased Output Current

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA549MKVC	ACTIVE	Power Package	KVC	11	25	RoHS & Green	SN	N / A for Pkg Type	-55 to 125	OPA549M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

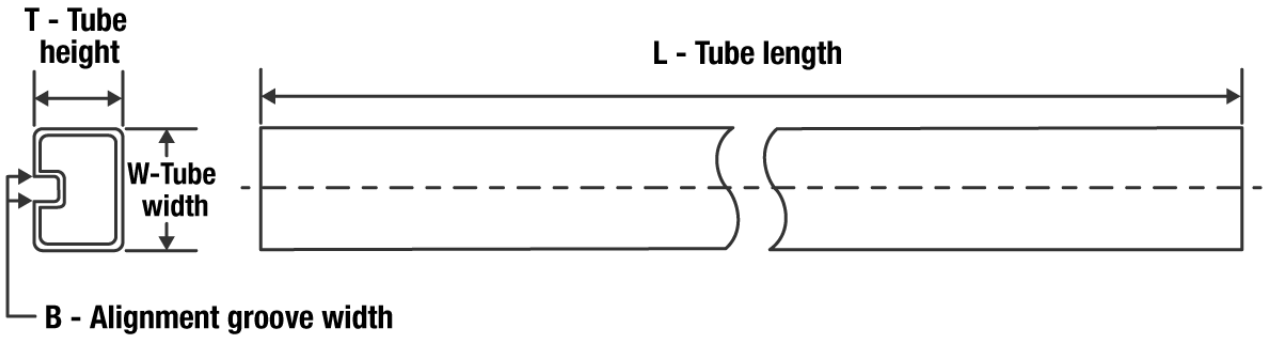
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

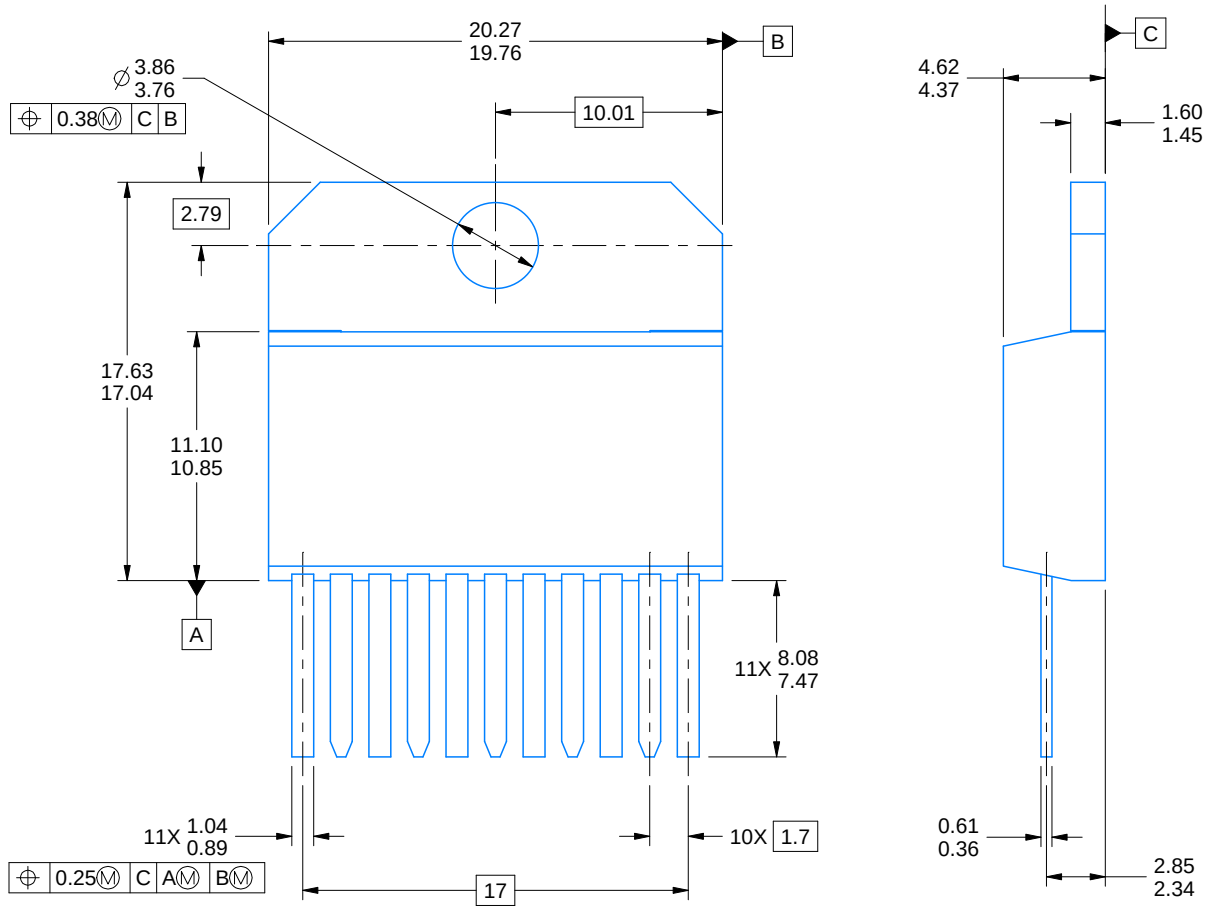
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA549MKVC	KVC	TO-OTHER	11	25	532.13	36.32	13340	NA

PACKAGE OUTLINE

KVC0011A

TO - 4.62 mm max height

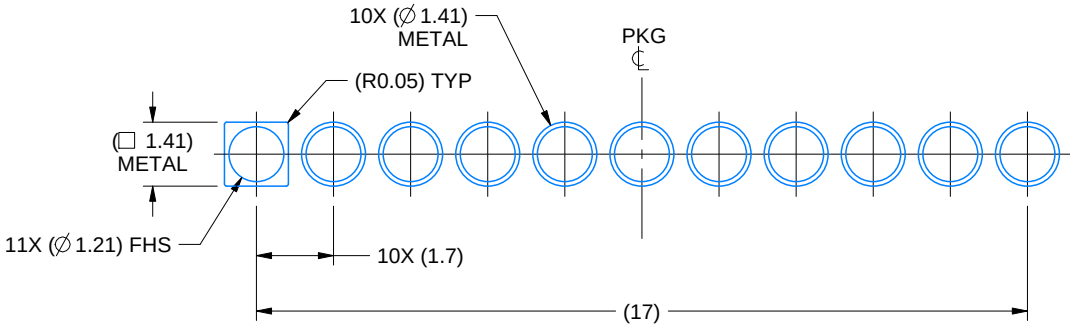
TRANSISTOR OUTLINE



4220628/A 02/2024

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-48-AA. Reference for body dimensions only (excluding lead forming dimensions).



LAND PATTERN EXAMPLE
SCALE: 6X

4220628/A 02/2024

NOTES: (continued)

4. Refer to IPC-7251 which may have alternate design recommendations.

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