

OPAx596 マルチプレクサ対応入力付き、高電圧 (85V)、低消費電力 (420 μ A)、高スルーレート (100V/ μ s) パワー アンプ

1 特長

- 高いスルーレート: 100V/ μ s
- 低消費電力: 420 μ A
- 広い電源電圧範囲:
 - $\pm 4\text{V} \sim \pm 42.5\text{V}$
 - 8V \sim 85V
- MUX 対応入力
- レール ツー レール 入出力
- ゲイン帯域幅: 3.75MHz
- 低ノイズ: 12.8nV/ $\sqrt{\text{Hz}}$
- 低い入力バイアス電流: 5pA
- 大出力負荷ドライブ: $I_O \pm 30\text{mA}$
- 幅広い温度範囲: $-40^\circ\text{C} \sim +125^\circ\text{C}$
- 業界標準の小型パッケージ:
 - DBV (5 ピン SOT-23)
 - DGK (8 ピン VSSOP)

2 アプリケーション

- 半導体試験装置
- LCD テスト
- プログラマブル DC 電源
- CT および PET スキャナ
- ソース メジャー ユニット (SMU)
- 光学モジュール
- 実験室およびフィールド用計測機器

3 概要

OPA596 および OPA2596 (OPAx596) は、高電圧 (85V)、高スルーレート (100V/ μ s)、マイクロパワー (420 μ A)、ユニティゲイン安定のオペアンプです。

OPAx596 を使用すると、高ゲイン構成でシステムの出力電圧を上げることで、半導体試験の出力負荷ドライバやデジタル電源などの次世代の高電圧システムを実現できます。低消費電力と業界標準の小型パッケージにより、サイズに制約のある高密度システムで使用でき、システムの熱管理要件を低減できます。

独自の設計手法により、OPAx596 は最小限の消費電力で非常に高いスルーレートを実現できるため、大信号セトリングタイムが改善され、実効大信号帯域幅が最大化されます。また、これらのデバイスはマルチプレクサ対応入力を備えており、大きな差動電圧 (最大 85V) に対応するため、多重化アプリケーションで従来の入力と比較してセトリング動作を向上させるのに役立ちます。

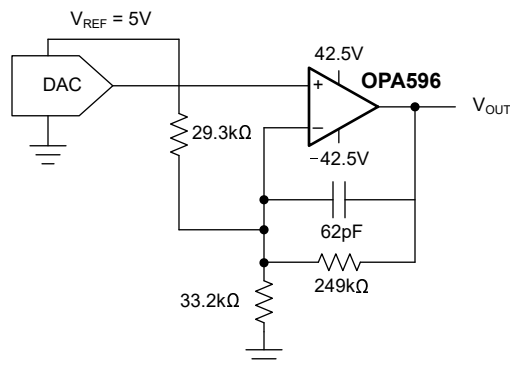
OPAx596 は、業界標準パッケージで供給され、 $-40^\circ\text{C} \sim +125^\circ\text{C}$ の温度範囲全体で動作します。

製品情報

部品番号	チャンネル	パッケージ ⁽¹⁾
OPA596	シングル	DBV (SOT-23, 5)
OPA2596 ⁽²⁾	デュアル	DGK (VSSOP, 8)

(1) 詳細については、[セクション 10](#) を参照してください。

(2) プレビュー情報。



ゲイン付き DAC 出力バッファ



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4 Pin Configuration and Functions

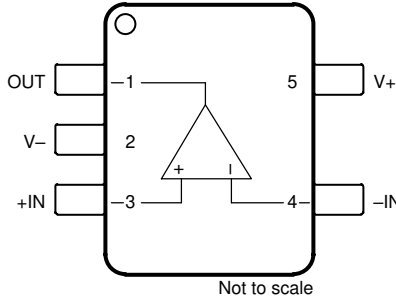


図 4-1. OPA596 DBV Package, 5-Pin SOT-23 (Top View)

表 4-1. Pin Functions: OPA596

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
-IN	4	Input	Inverting input
OUT	1	Output	Output
V+	5	Power	Positive (highest) power supply
V-	2	Power	Negative (lowest) power supply

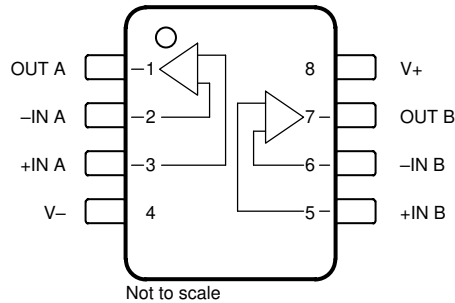


図 4-2. OPA2596 DGK Package, 8-Pin VSSOP (Top View)

表 4-2. Pin Functions: OPA2596

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
-IN A	2	Input	Inverting input, channel A
-IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V-	4	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage	Dual supply	±46.5		V
		Single supply, V _S = (V+) – (V–)	93		
	Signal input pin voltage ⁽²⁾	Common-mode	(V–) – 0.3	(V+) + 0.3	V
		Differential	(V+) – (V–)		
	Input current, all pins ⁽²⁾		±10		mA
I _{SC}	Output short circuit ⁽³⁾		Continuous		
T _J	Junction temperature		150		°C
T _{STG}	Storage temperature		–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
- (3) Short-circuit to ground.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _S	Supply voltage	Dual supply	±4		±42.5	V
		Single supply	8		85	
T _A	Ambient temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA596	OPA2596	UNIT
		DBV (SOT-23)	DGK (VSSOP)	
		5 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	165.4	143.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	99.1	50.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	64.5	78.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	42.6	3.0	°C/W
ψ _{JB}	Junction-to-board characterization parameter	64.2	77.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

at $V_S = 85V (\pm 42.5V)$, $T_A = 25^\circ C$, $R_L = 10k\Omega$ to mid-supply, and $V_{CM} = V_{OUT} = \text{mid-supply}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			± 0.2	± 1	mV
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ C$ to $+125^\circ C$		± 1	± 6	$\mu V/^\circ C$
PSRR	Power supply rejection ratio	$8V \leq V_S \leq 85V$		± 1	± 5	$\mu V/V$
INPUT BIAS CURRENT						
I_B	Input bias current			± 5	± 10	pA
		$T_A = -40^\circ C$ to $+85^\circ C$			± 50	
		$T_A = -40^\circ C$ to $+125^\circ C$				± 1
I_{OS}	Input offset current			± 5	± 10	pA
		$T_A = -40^\circ C$ to $+85^\circ C$				
		$T_A = -40^\circ C$ to $+125^\circ C$				± 1
NOISE						
	Input voltage noise	$f = 0.1\text{Hz}$ to 10Hz		1.4		μV_{PP}
e_n	Input voltage noise density	$f = 100\text{Hz}$		17.8		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		12.9		
		$f = 10\text{kHz}$		12.8		
i_n	Current noise density	$f = 1\text{kHz}$		10		fA/ $\sqrt{\text{Hz}}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage	Linear operation	$(V-) - 0.1$		$(V+) - 3.5$	V
CMRR	Common-mode rejection	$(V-) \leq V_{CM} \leq (V+) - 3.5V$		126	140	dB
			$T_A = -40^\circ C$ to $+125^\circ C$	124	140	
INPUT IMPEDANCE						
	Differential			$100 \parallel 2.5$		M $\Omega \parallel$ pF
	Common-mode			$10 \parallel 5.5$		G $\Omega \parallel$ pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$(V-) + 1V < V_O < (V+) - 1.5V$, $R_L = 10k\Omega$ to mid-supply		134	140	dB
			$T_A = -40^\circ C$ to $+125^\circ C$	120	140	
		$(V-) + 3V < V_O < (V+) - 3.5V$, $R_L = 2k\Omega$ to mid-supply			126	
			$T_A = -40^\circ C$ to $+125^\circ C$		126	
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	$G = 1$		2.25		MHz
		$G = 10$		3		
		$G = 100$		3.75		
SR	Slew rate	$G = \pm 1$, $V_O = 70V$ step		100		V/ μs
t_s	Settling time	To $\pm 0.01\%$, $G = -1$, $V_O = 10V$ step, $C_L = 100\text{pF}$		2		μs
	Overload recovery	$G = -1$		115		ns
THD+N	Total harmonic distortion + noise	$G = +1$, $V_O = 70V_{PP}$, $f = 1\text{kHz}$	$R_L = 10k\Omega$		-102	dB
			$R_L = 2k\Omega$		-95	

5.5 Electrical Characteristics (続き)

 at $V_S = 85V (\pm 42.5V)$, $T_A = 25^\circ C$, $R_L = 10k\Omega$ to mid-supply, and $V_{CM} = V_{OUT} =$ mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail	No load			12	50	mV
		$R_L = 10k\Omega$ to mid-supply			100	435	
		$R_L = 2k\Omega$ to mid-supply			500	2.05	V
I_{SC}	Output current				± 30		mA
C_{LOAD}	Capacitive load drive				1		nF
Z_O	Open-loop output impedance				550		Ω
CURRENT LIMIT							
POWER SUPPLY							
I_Q	Quiescent current	$I_O = 0mA$			420	490	μA
			$T_A = -40^\circ C$ to $+125^\circ C$			500	
TEMPERATURE							
	Overtemperature shutdown	Shutdown temperature			185		$^\circ C$
		Thermal hysteresis			20		

6 Detailed Description

6.1 Overview

The OPAx596 are low power (420 μ A), high-slew rate (100V/ μ s), 85V operational amplifiers (op amps). These op amps use a proprietary design technique to achieve a very high slew capability with minimal power consumption. The OPAx596 is capable of driving \pm 30mA of output current and can swing to within 100mV of either power supply rail.

The amplifiers feature state-of-the-art CMOS technology and advanced design features that help achieve outstanding ac performance and enable small package options. The OPAx596 strengths also include 3.75MHz bandwidth, 12.8nV/ \sqrt Hz noise spectral density, and low input bias current. These features make the OPAx596 an exceptional choice to gain or buffer the output of a digital-to-analog converter (DAC) in digitally programmable power supplies.

6.2 Functional Block Diagram

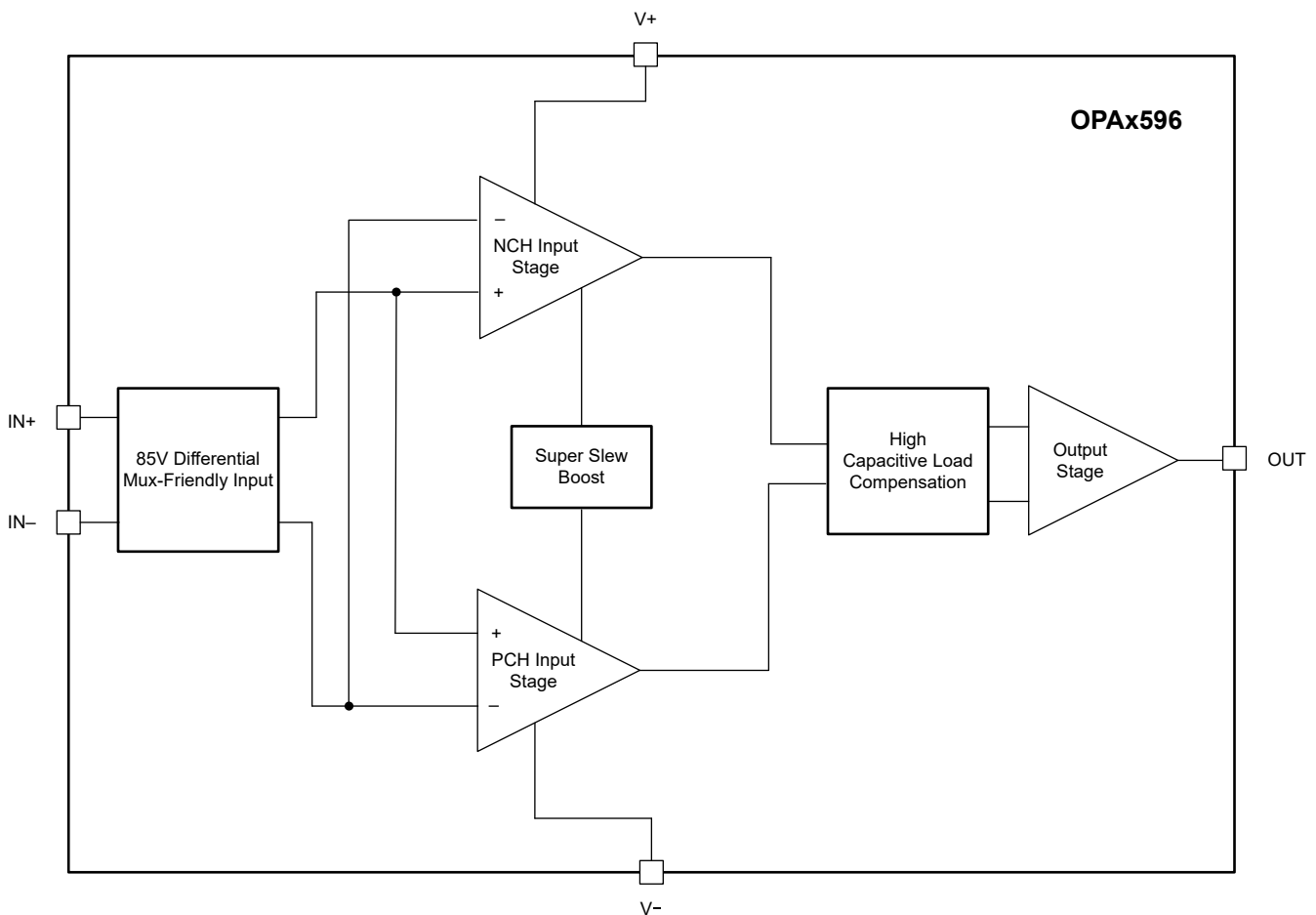


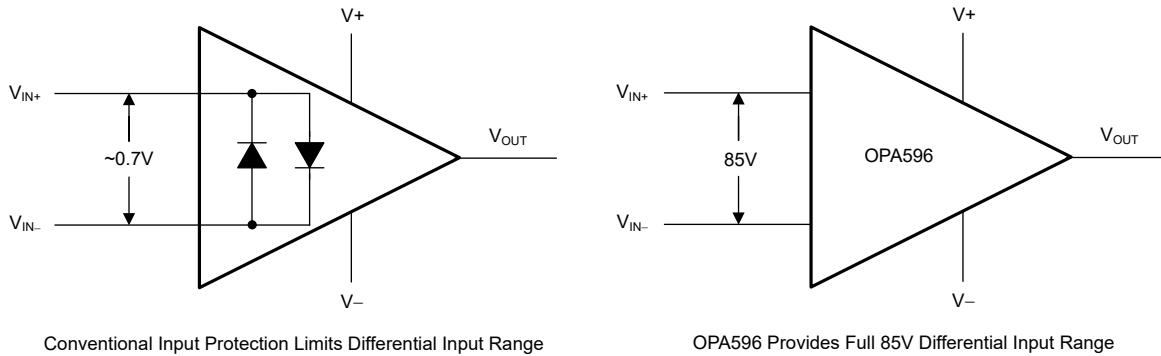
図 6-1. Functional Block Diagram

ADVANCE INFORMATION

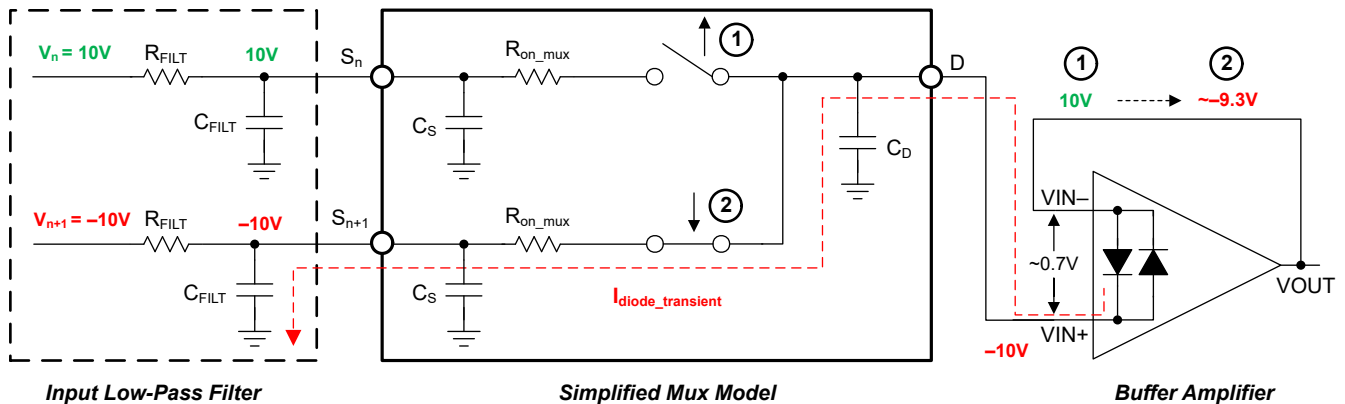
6.3 Feature Description

6.3.1 Mux-Friendly Inputs

The OPAx596 use a unique input architecture to eliminate the need for input protection diodes but still provide robust input protection under transient conditions. Conventional input diode protection schemes shown in [6-2](#) can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in [6-3](#). For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current and result in extended settling time.



6-2. OPA596 Input Protection Does Not Limit Differential Input Capability



6-3. Back-to-Back Diodes Create Settling Issues

The OPAx596 feature a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making these devices an excellent choice for multichannel, high-switched, input applications. The OPAx596 tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 85V, making these devices a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

6.3.2 Thermal Protection

The OPAx596 has a thermal protection feature that prevents damage from self heating. When the junction temperature (T_J) reaches approximately 180°C, the op amp output stage disables. This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive. Thermal protection forces the output to a high-impedance state. The OPAx596 is designed with approximately 30°C of thermal hysteresis and returns to normal operation when the output stage temperature becomes less than approximately 150°C.

This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

6.3.3 Slew Boost

Slew rate is the maximum rate of change of output voltage change with respect to time and is typically specified in units of volts per microsecond, V/ μ s. The OPAx596 can enter a slew condition when a large, rapid moving signal is applied at the input. While slewing, the op amp enters an open loop condition and significant slew induced distortion can be seen on the output signal.

式 1 shows that the slew rate of an op amp is typically determined by the saturation current of the input stage, I_{SAT} , and the compensation capacitor, C_C .

$$SR = \frac{I_{SAT}}{C_C} \quad (1)$$

The slew rate scales with the quiescent current, I_Q , of the op amp. There are several ways that designers have overcome slew rate limitation. For example, decompensation improves slew rate at the expense of stability by lowering C_C . More commonly, modern op amps are equipped with slew boost technology that increases I_{SAT} to overcome the inherent slew rate limitations. Slew boost circuits can vary in implementation, but designers can typically expect about a 4 × improvement over comparable unboosted op amps.

The OPAx596 uses a proprietary design to achieve an unprecedented slew rate to I_Q ratio. The novel slew boost technology in OPAx596 provides a nearly 100 × slew rate improvement over comparable unboosted op amps.

6.3.4 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

6.4 Device Functional Modes

The OPAx596 has a single functional mode and is operational when the power-supply voltage is between 8V ($\pm 4V$) and 85V ($\pm 42.5V$).

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The OPAx596 are low power (420 μ A), high-slew rate (100V/ μ s), 85V power operational amplifiers (op amps). These op amps use a proprietary design technique to achieve a very high slewing capability while consuming minimal power. The low power consumption helps reduce heat generation on the board while the output swings near the supply rail. The high slew reduces slew related distortion at the output when dealing with large peak, high frequency signals.

7.2 Typical Applications

7.2.1 Bridge-Connected Piezoelectric Driver

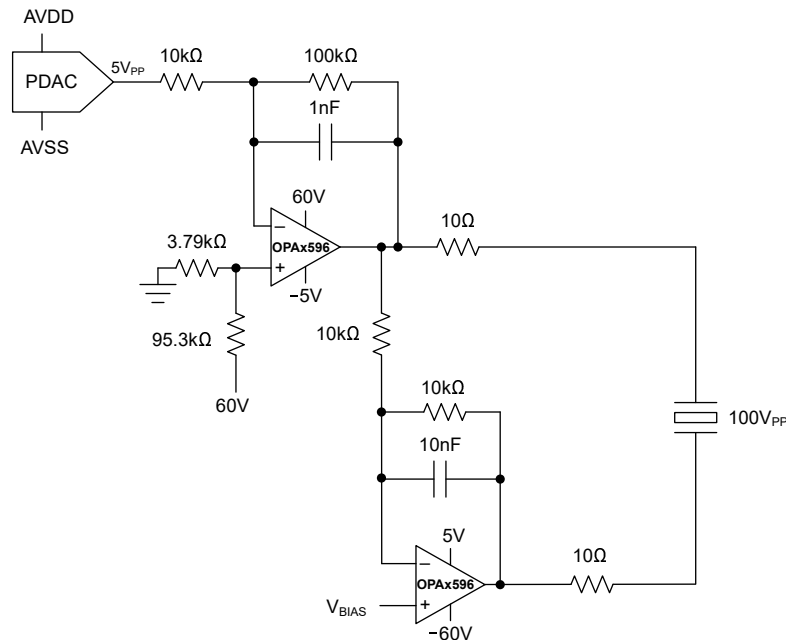


図 7-1. 100V_{PP} Piezoelectric Driver With Bridge Connected Load

7.2.1.1 Design Requirements

The OPAx596 is used to drive a piezoelectric actuator with a 100V operating range at a frequency of 100Hz. The large capacitance inherent to the piezoelectric actuator can cause undesired ringing of the driver amplifier. An inaccurate response of the actuator is possible due in part to amplifier instability. Adequate phase margin for a 500nF equivalent load is necessary for a robust driver circuit for the piezoelectric actuator presented here.

表 7-1. Design Parameters

PARAMETER	VALUE
Positive supply voltage	60V
Negative supply voltage	-5V
Piezoelectric actuator capacitance (1kHz)	500nF
Piezoelectric operating voltage range	0V to 100V
Operating frequency	100Hz
DAC output voltage	5V _{PP}

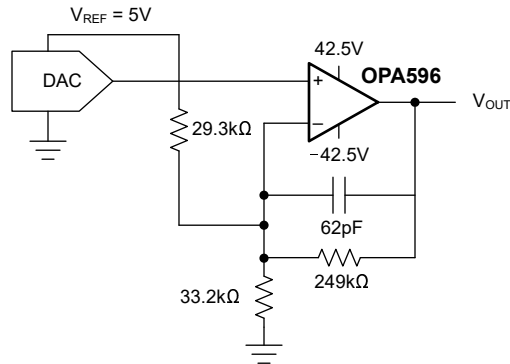
7.2.1.2 Detailed Design Procedure

Piezoelectric actuators offer many benefits over traditional solenoid counterparts. Piezoelectric actuators are more precise, power efficient, and smaller in general when compared to solenoid actuators. One challenge with piezoelectric actuators is that the piezoelectric actuators operate over a very wide voltage range. Driving voltages of more than 60V are not uncommon, and can easily reach hundreds of volts. The OPAx596 operate with a supply voltage of up to 85V.

In this design example, the OPAx596 are used to provide a 100V_{PP} signal to control a high-voltage piezoelectric actuator (see also [図 7-1](#)). The piezoelectric actuator can be modeled as a large capacitor when operated at less than the resonant frequency. The piezoelectric actuator is treated as a floating load driven by two op amps of the OPAx596. The outputs of the op amps are set to be 180° out-of-phase to essentially double the voltage seen by the actuator load.

The signal voltage of the digital-to-analog converter is applied a 10V/V gain by the OPAx596. A simple voltage divider provides a 2.5V reference to level shift the output to create a unipolar driving voltage. An isolation resistor improves phase margin and stability. Add a small 10Ω R_{ISO} at the output of the OPAx596.

7.2.2 DAC Output Gain and Buffer



7.2.2.1 Design Requirements

The OPA596 is designed for use as an output driver stage with gain and provides a wide, bipolar supply voltage. Combined with the small size of the SOT23-5 package and the low power consumption, these features make this device a great choice for high-channel density systems, such as semiconductor test and manufacturing platforms where many channels are present. In this design example, the OPA596 is configured for a gain of approximately 17V/V.

表 7-2. Design Parameters

PARAMETER	VALUE
Supply voltage	-42.5V to +42.5V
Input voltage	0V to 5V
Output voltage	-42.5V to +42.5V
Gain	17V/V

7.2.2.2 Detailed Design Procedure

In this design example, the OPA596 is configured as both a gain stage and output driver. The input signal to the amplifier is 0V to 5V, and the device is configured with a noninverting gain of 17V/V. The DAC reference voltage of 5V is used as a reference to enable a bipolar output swing. This configuration results in an output voltage of -42.5V to +42.5V. This design example is common in many systems that use a DAC to provide the input signal and require a wide output signal with low output current requirements. The OPA596 can swing to either rail while remaining within the thermally specified limits. Such systems include test and measurement platforms and power supplies.

7.2.3 Single-Supply Piezoelectric Driver

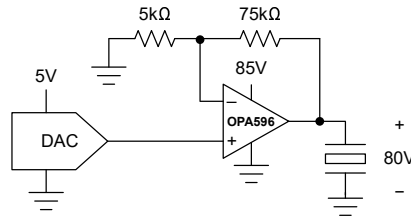


図 7-2. 80V Single-Supply Piezoelectric Driver

7.2.4 High-Side Current Sense

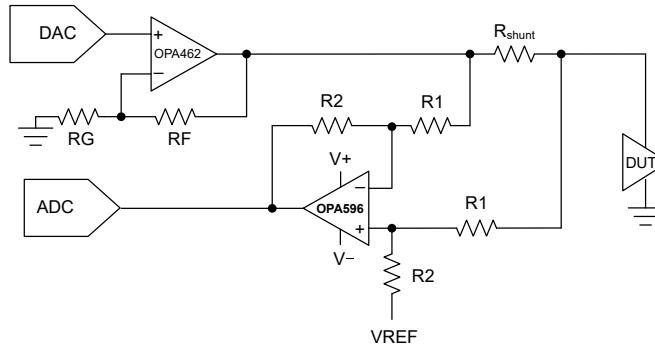


図 7-3. 100V High-Side Current Sense

7.2.5 High-Voltage Instrumentation Amplifier

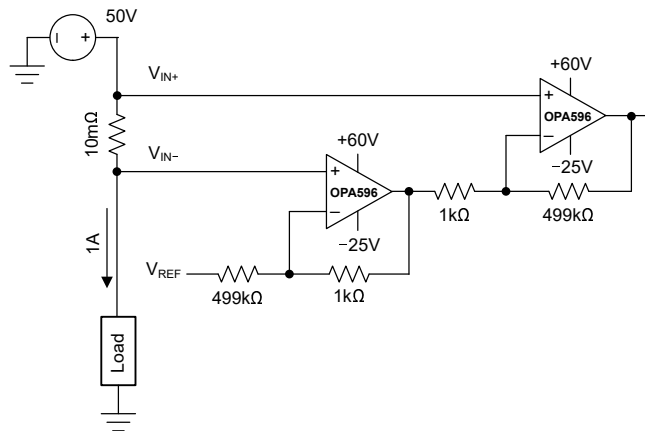


図 7-4. High-Voltage Instrumentation Amplifier

7.2.6 Composite Amplifier

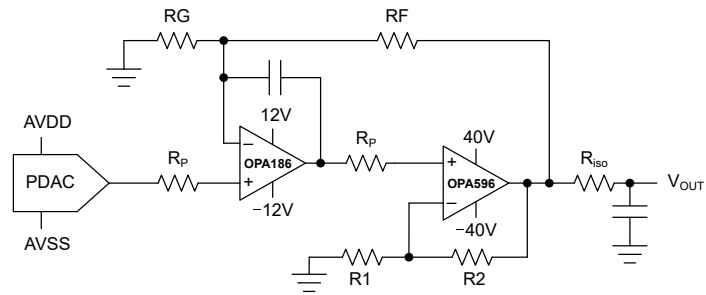


図 7-5. High-Precision, High-Voltage Output Composite Amplifier

ADVANCE INFORMATION

7.3 Power Supply Recommendations

The OPAx596 operates from power supplies up to $\pm 42.5\text{V}$ (85V), and as little as $\pm 4\text{V}$ (8V) with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least $0.1\mu\text{F}$ is required for proper operation. Ensure that the capacitor voltage is rated for high voltage across the full operating temperature range. Some applications do not require an equal positive and negative output voltage swing. The OPAx596 can be powered with asymmetrical supplies.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Connect low-ESR, $0.1\mu\text{F}$ ceramic bypass capacitors between each supply pin and ground. Place the capacitors as close to the device as possible. A single bypass capacitor from $V+$ to ground is sufficient for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.1.1 Thermal Considerations

Through normal operation, the op amps can self-heat. Self-heating is a natural increase in the die junction temperature that occurs in every amplifier. This self-heating is a result of several factors, including quiescent power consumption, package thermal resistance, PCB layout, and device operating conditions.

Operate the OPAX596 within the rated junction temperature, T_J , range to avoid thermal shutdown. Use the 式 2 to determine the estimated T_J

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

In a quiescent state, P_D is given by the product of the power supply and the quiescent current of the op amp. 式 3 shows the calculation of T_J for the OPAX596 assuming an 85V power supply is used and an operating temperature of 25°C.

$$T_J = (85V \times 490\mu A) \times 165.4 \frac{C}{W} + 25^\circ C \quad (3)$$

$$T_J = 31.89^\circ C \quad (4)$$

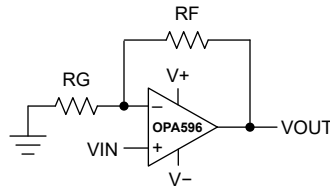
The low power consumption of the OPAX596 causes minimal self-heating even in a small SOT23-5 package as given by 式 4. In a loaded condition, P_D is equal to addition of the quiescent power, P_{DQ} and the power dissipated by the output stage, P_{DL} . The worst-case condition is given when the output voltage is equal to ½ of either supply rail (assuming symmetrical supplies, V+ and V-). In a worst-case condition, P_{DL} is given by 式 5.

$$P_{DL} = \frac{(V+)^2}{4 \times R_L} \quad (5)$$

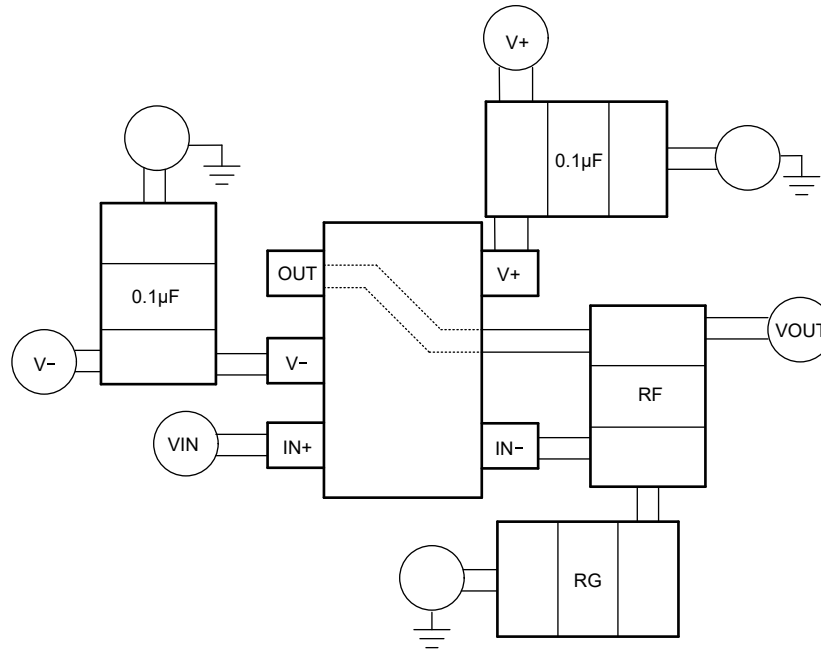
For example, assume the OPAX596 is powered with bipolar ±42.5V power supplies and drives a 5kΩ load, R_L , to ground. The maximum increase in T_J is expected to be about 22°C as given by 式 6. In this example, to keep the op amp within the *Absolute Maximum Ratings*, operate in T_A well under 128°C to account for different factors.

$$\Delta T_J = (41.7mW + 90.3mW) \times 165.4 \frac{C}{W} \quad (6)$$

7.4.2 Layout Example



☒ 7-6. Schematic Representation of Noninverting Configuration



☒ 7-7. Board Layout for Noninverting Configuration of the SOT23-5 Package

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

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8.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

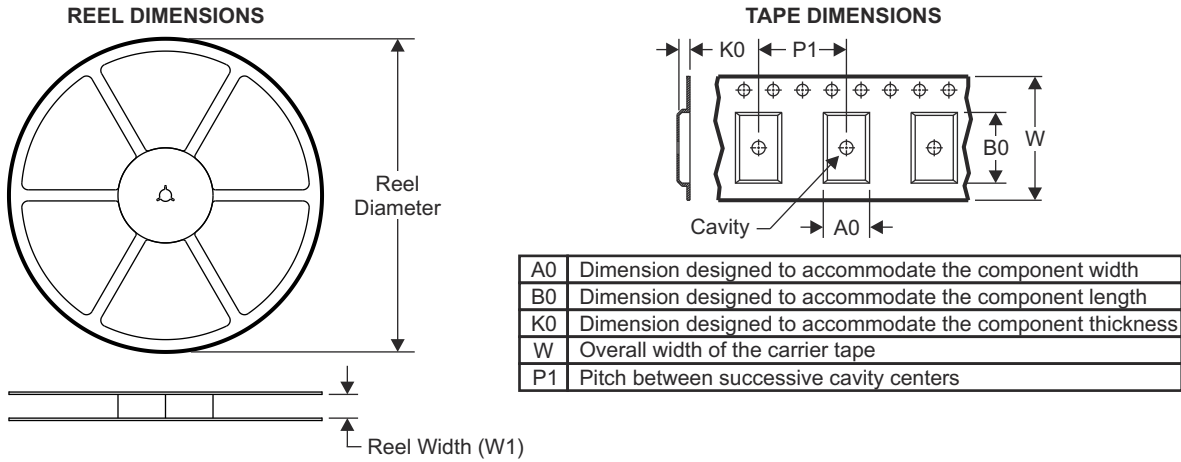
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
June 2024	*	Initial Release

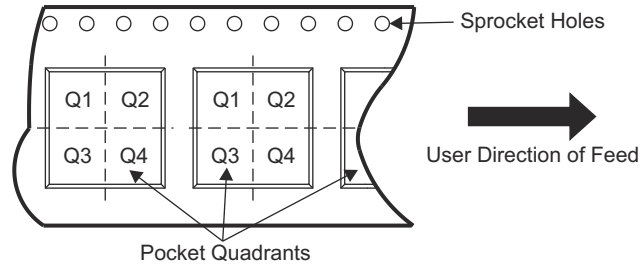
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information



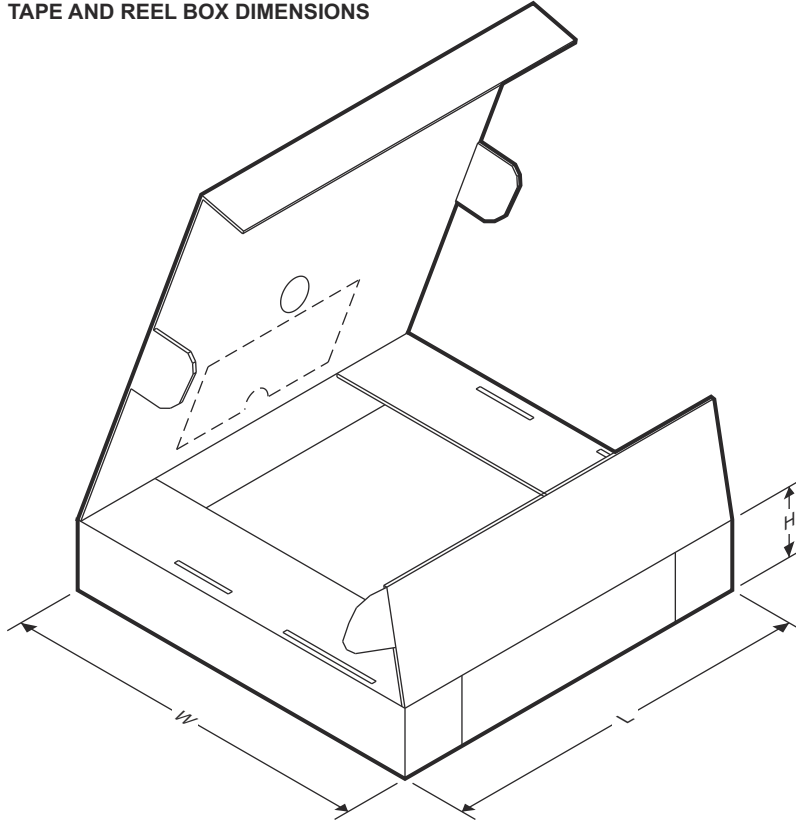
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA596DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA596DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA596DBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA596DBVT	SOT-23	DBV	5	250	223.0	270.0	35.0

ADVANCE INFORMATION

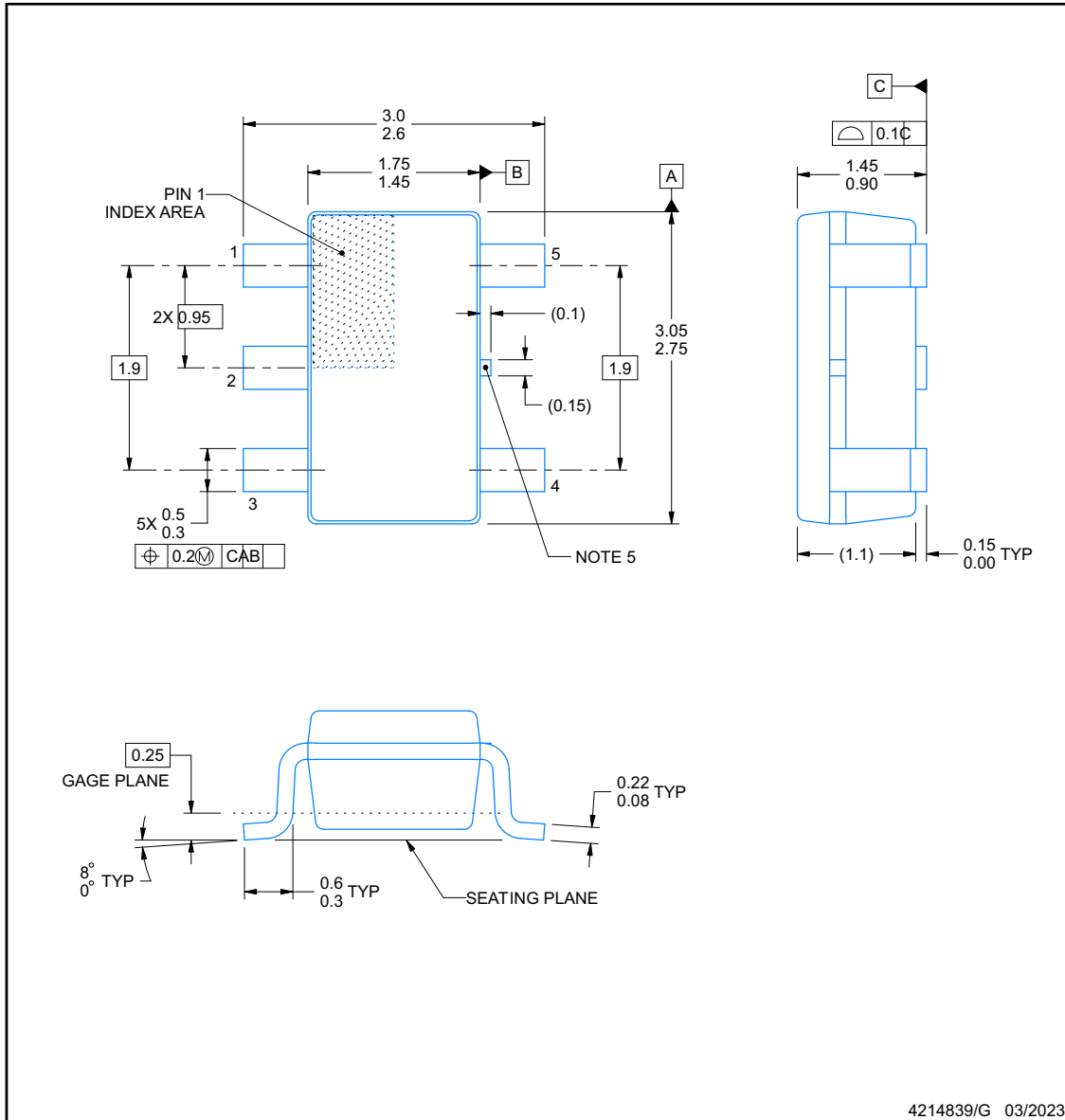


PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

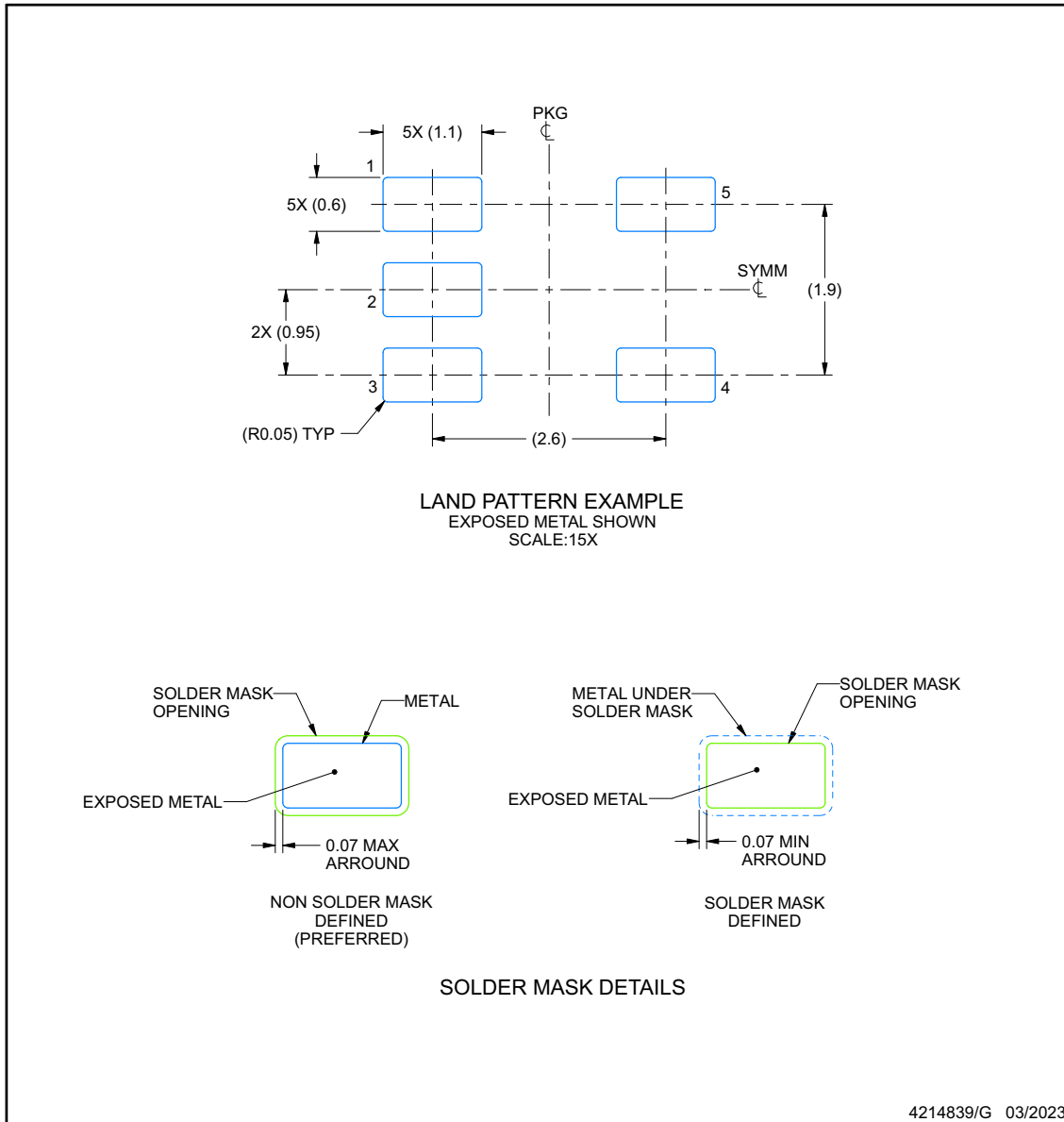
EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

ADVANCE INFORMATION



NOTES: (continued)

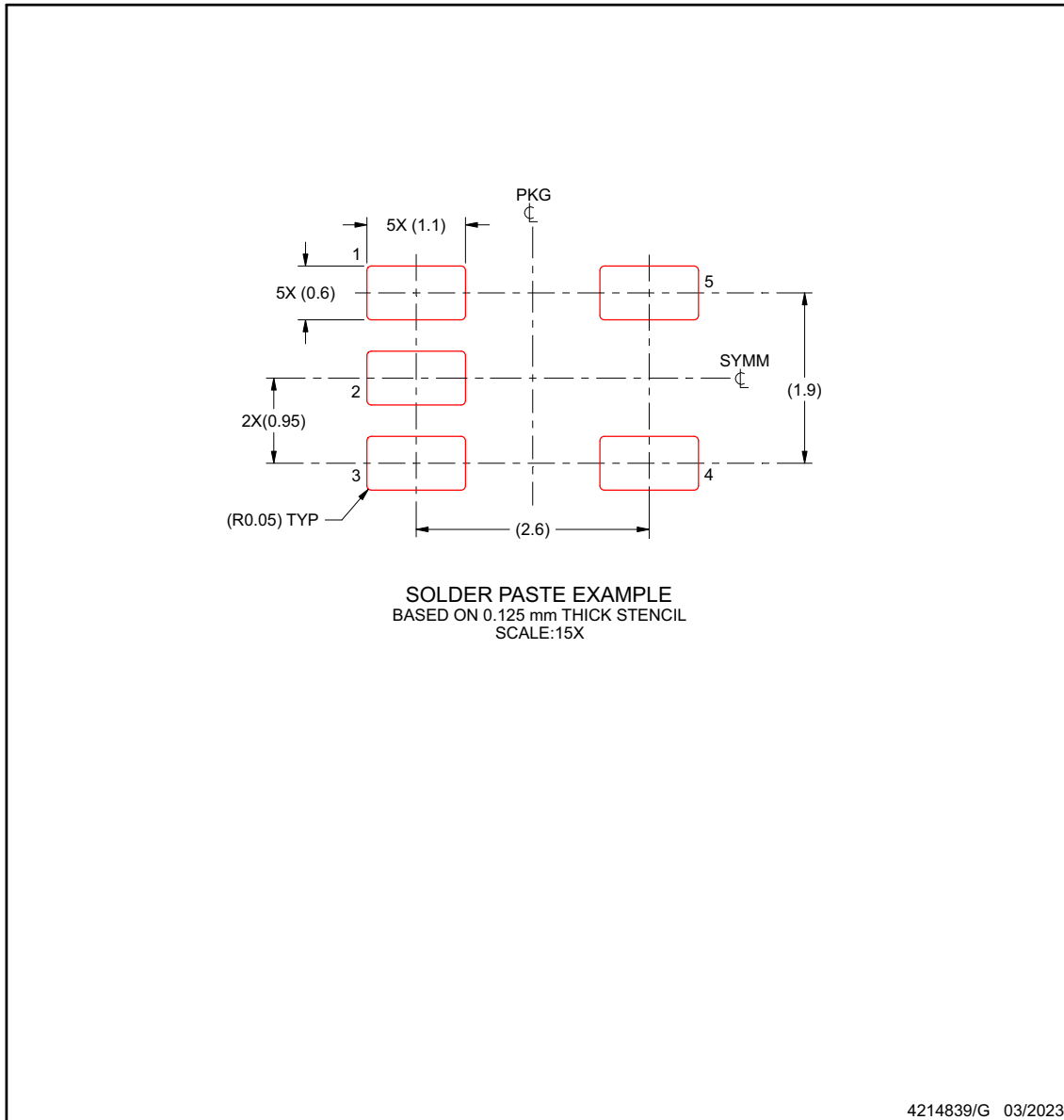
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
POPA596DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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