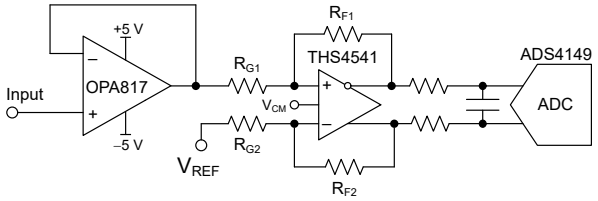
OPA817 800MHz、高精度、ユニティ ゲイン安定、FET 入力オペアンプ

1 特長

- 広い帯域幅:
  - ゲイン帯域幅積:400MHz
  - 帯域幅 (G = 1V/V):800MHz
  - 大信号帯域幅 ($2V_{PP}$):250MHz
  - スルーレート:1000V/µs
- 高精度:
  - 入力オフセット電圧:250µV (最大値)
  - 入力オフセット電圧ドリフト:3.5µV/℃ (最大値)
- 入力電圧ノイズ:4.5nV/√Hz
- 入力バイアス電流:2pA
- 低歪み (R_L = 100Ω、V_O = $2V_{PP}$):
  - 10MHz での HD2、HD3:–86dBc、–100dBc
- 電源電圧範囲:6V～12.6V
- 消費電流:23.5mA
- シャットダウン電流:55µA
- OPA656 の性能アップグレード版

2 アプリケーション

- 高速データ アクイジション (DAQ)
- アクティブ プローブ
- オシロスコープ
- 広帯域のトランスインピーダンス アンプ (TIA)
- ウェハー スキャン機器
- 光通信モジュール
- 光時間領域反射測定法 (OTDR)
- テストおよび測定機器のフロントエンド
- 医療用および化学用分析器



入力インピーダンスの高いデジタイザ用フロントエンド

3 概要

OPA817 は、高速、高精度、広いダイナミック レンジのアプリケーションに適した、ユニティ ゲイン安定の電圧帰還型オペアンプです。

OPA817 は、400MHz の広いゲイン帯域幅と 6V～12.6V の電源電圧範囲を特長とする、低ノイズ接合ゲート電界効果トランジスタ (JFET) 入力段を備えています。1000V/µs という高速スルーレートは、高速デジタイザ、アクティブ プローブ、他の試験 / 測定機器アプリケーションで高インピーダンス バッファとして使用する際、広い大信号帯域幅と低歪みを実現できます。

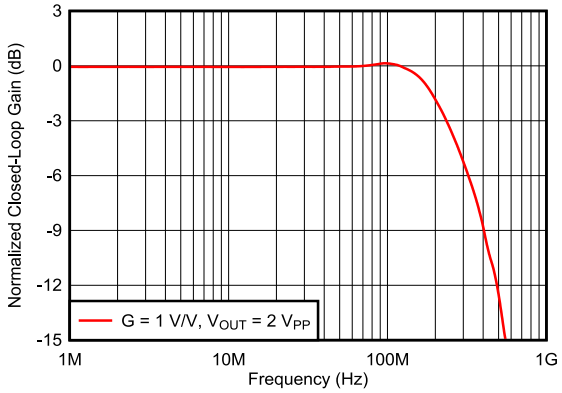
OPA817 は、入力オフセット電圧が ±250µV と非常に低く、オフセット電圧ドリフトは ±3.5µV/℃です。入力バイアス電流がピコアンペア単位であり、また、入力電圧ノイズが低い (4.5nV/√Hz) ため、OPA817 は光学テスト機器、通信機器、医療用および科学用計測機器の広帯域トランスインピーダンス アンプとして優れた選択肢です。

OPA817 は、放熱用の露出サーマル パッドが付いた 8 リードの WSON パッケージで供給されます。このデバイスは、産業用温度範囲の -40℃～+105℃で動作が規定されています。

パッケージ情報

部品番号 (1)	パッケージ (2)	パッケージ サイズ
OPA817	DTK (WSON、8)	3mm × 3mm

(1) セクション 4 を参照してください。
(2) 詳細については、セクション 11 を参照してください。



大信号周波数応答

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Device Comparison Table.....3
5 Pin Configuration and Functions.....3
6 Specifications.....4
6.1 Absolute Maximum Ratings.....4
6.2 ESD Ratings.....4
6.3 Recommended Operating Conditions.....4
6.4 Thermal Information.....4
6.5 Electrical Characteristics.....5
6.6 Typical Characteristics: V_S = ±5 V.....8
7 Detailed Description.....14
7.1 Overview.....14
7.2 Functional Block Diagram.....14
7.3 Feature Description.....15
7.4 Device Functional Modes.....16
8 Application and Implementation.....18
8.1 Application Information.....18
8.2 Typical Applications.....19
8.3 Power Supply Recommendations.....20
8.4 Layout.....20
9 Device and Documentation Support.....23
9.1 Device Support.....23
9.2 Documentation Support.....23
9.3 ドキュメントの更新通知を受け取る方法.....23
9.4 サポート・リソース.....23
9.5 Trademarks.....23
9.6 静電気放電に関する注意事項.....23
9.7 用語集.....23
10 Revision History.....23
11 Mechanical, Packaging, and Orderable Information.....24

4 Device Comparison Table

DEVICE	SUPPLY VOLTAGE (V)	BW (MHz)	INPUT	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	MINIMUM STABLE GAIN (V/V)
OPA817	±6.3	400	FET	1000	4.5	1
OPA818	±6.5	2700	FET	1400	2.2	7
OPA657	±5	1600	FET	700	4.8	7
OPA656	±5	230	FET	290	7	1
OPA659	±6	350	FET	2550	8.9	1
OPA858	±2.5	5500	CMOS	2000	2.5	7
THS4631	±15	210	FET	1000	7	1

5 Pin Configuration and Functions

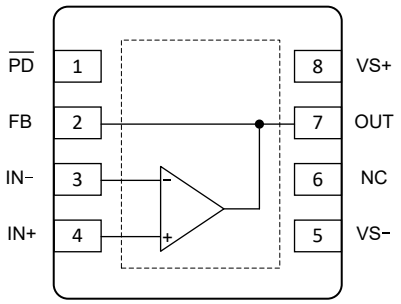


図 5-1. DTK Package, 8-Pin WSON With Thermal Pad (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
FB	2	Output	Feedback resistor connection (optional)
IN–	3	Input	Inverting input
IN+	4	Input	Noninverting input
NC	6	—	No connect (no internal connection to die)
OUT	7	Output	Output of amplifier
$\overline{PD}$	1	Input	Power down Low = amplifier disabled, High = amplifier enabled, Internal 2-MΩ pullup allows floating this pin
VS–	5	Power	Negative power supply
VS+	8	Power	Positive power supply
Thermal pad		—	Electrically isolated from the die substrate. The thermal pad can be connected to any potential between the device power supplies. However, best practice is to connect the thermal pad to a heat-spreading plane, typically ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)		13	V
	Maximum dV_S/dT for supply turn-on and turn-off(2)		1	V/µs
V_I	Input voltage	$V_{S–}$	V_{S+}	V
V_{ID}	Differential input voltage		±V_S	V
I_I	Continuous input current		±10	mA
I_O	Continuous output current(3)		±30	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	105	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) To keep the edge-triggered ESD absorption devices across the supply pins off, do not exceed this specification.
(3) Long-term continuous current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+} – $V_{S–}$	Total supply voltage	6	10	12.6	V
T_A	Ambient temperature	–40	25	105	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA817 DTK (WSON) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	64.9	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	53.0	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	32.8	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	1.3	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	32.8	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A ≈ 25°C, V_S = ±5 V, G = 1 V/V, R_F = 0, R_F = 250 Ω for other gains, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 200 mV_{PP}		800		MHz
		V_{OUT} = 200 mV_{PP}, G = 2 V/V		400		
		V_{OUT} = 200 mV_{PP}, G = 5 V/V		100		
		V_{OUT} = 200 mV_{PP}, G = 10 V/V		40		
GBWP	Gain-bandwidth product	V_{OUT} = 200 mV_{PP}, G = 100 V/V		400		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		250		MHz
		V_{OUT} = 4 V_{PP}		140		
	Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}		100		MHz
SR	Slew rate (10% to 90%)	V_{OUT} = 4–V step		1000		V/µs
	Slew rate (10% to 90%)	V_{OUT} = 1–V step, Gain = 2 V/V		750		
t_R, t_F	Rise, fall time	V_{OUT} = 200–mV step		0.7		ns
	Settling time to 0.1%,	V_{OUT} = 2–V step		6		ns
	Overshoot and undershoot	V_{OUT} = 2–V step		8		%
	Output Overdrive recovery time	V_{OUT} = $V_{S–}$ to V_{S+}, G = 2 V/V,		15		ns
HD2	Second-order harmonic distortion	f = 1 MHz, V_{OUT} = 2 V_{PP}		–110		dBc
		f = 10 MHz, V_{OUT} = 2 V_{PP}		–86		
		f = 50 MHz, V_{OUT} = 2 V_{PP}		–76		
		f = 10 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		–97		
HD3	Third-order harmonic distortion	f = 1 MHz, V_{OUT} = 2 V_{PP}		–120		dBc
		f = 10 MHz, V_{OUT} = 2 V_{PP}		–100		
		f = 50 MHz, V_{OUT} = 2 V_{PP}		–68		
		f = 10 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		–102		
e_N	Input voltage noise	f ≥ 200 kHz		4.5		nV/√Hz
	Voltage noise 1/f corner frequency			2.6		kHz
	Input current noise			18		fA/√Hz
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±1 V	78	85		dB
		T_A = –40°C to +85°C	72			
		T_A = –40°C to +105°C	69			
V_{OS}	Input-referred offset voltage			50	±250	µV
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +105°C			±600	
	Input offset voltage drift	T_A = –40°C to +85°C		1	±3.5	µV/°C
		T_A = –40°C to +105°C		1	±3.5	
I_B	Input bias current			2	±20	pA
		T_A = –40°C to +85°C			±1000	
		T_A = –40°C to +105°C			±1500	
I_{OS}	Input offset current			1	±20	pA
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +105°C			±750	
	Internal feedback trace resistance	Device turned OFF, OUT to FB pin resistance		0.7		Ω

6.5 Electrical Characteristics (続き)

at T_A ≈ 25°C, V_S = ±5 V, G = 1 V/V, R_F = 0, R_F = 250 Ω for other gains, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Most positive input voltage(1)		2.1	2.7		V
		T_A = –40°C to +85°C	2.0			
		T_A = –40°C to +105°C	2.0			
	Most negative input voltage(1)			-3.9	-3.5	V
		T_A = –40°C to +85°C			-3.4	
		T_A = –40°C to +105°C			-3.4	
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V	84	110		dB
		T_A = –40°C to 85°C	83			
		T_A = –40°C to 105°C	82			
	Input impedance common-mode			60 || 2.9		GΩ || pF
	Input capacitance differential mode			0.1		pF
OUTPUT						
V_{OL}	Output voltage, low	no-load		-3.9	-3.6	V
		R_L = 100 Ω		-3.7	-3.4	
		T_A = –40°C to +85°C			-3.3	
		T_A = –40°C to +105°C			-3.2	
V_{OH}	Output voltage, high	no-load	3.7	3.9		V
		R_L = 100 Ω	3.4	3.7		
		T_A = –40°C to +85°C	3.3			
		T_A = –40°C to +105°C,	3.2			
	Linear output drive (sourcing/sinking)	V_{OUT} = ±1 V, ΔV_{OS} < 2 mV	±58	80		mA
		T_A = –40 to 85°C, ΔV_{OS} < 3 mV	±40			
		T_A = –40 to 105°C, ΔV_{OS} < 3 mV	±35			
	Short-circuit current			±100		mA
Z_O	Closed loop output Impedance	f = 100 kHz		0.04		Ω
POWER SUPPLY						
I_Q	Quiescent current			23.5	24.5	mA
		T_A = –40°C to +85°C			24.7	
		T_A = –40°C to +105°C			24.9	
PSRR+	Power-supply rejection ratio	ΔV_{S+} = ±0.5 V	80	100		dB
		T_A = –40°C to +85°C	77			
		T_A = –40°C to +105°C	76			
PSRR-	Power-supply rejection ratio	ΔV_{S-} = ±0.5 V,	80	100		dB
		T_A = –40°C to +85°C	77			
		T_A = –40°C to +105°C	76			

6.5 Electrical Characteristics (続き)

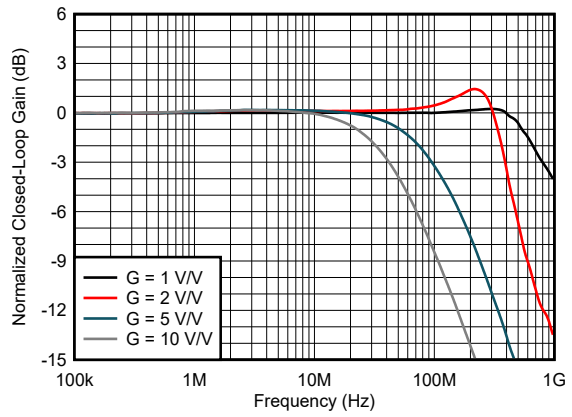
at T_A ≈ 25°C, V_S = ±5 V, G = 1 V/V, R_F = 0, R_F = 250 Ω for other gains, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER DOWN						
	Enable voltage threshold	Specified *on* above (V_{S+}) – 1 V			4	V
	Disable voltage threshold	Specified *off* below (V_{S+}) – 3 V	2			V
	Power-down quiescent current	$\overline{PD}$ ≤ (V_{S+}) – 3V		55	100	µA
	Power-down pin bias current in shutdown mode	$\overline{PD}$ = 0 V to (V_{S+}) – 3 V		9	12	µA
	Power-down pin bias current in active mode	$\overline{PD}$ = (V_{S+}) – 1 V to (V_{S+})		0.5	1	µA
	Turn-on time delay	Time from $\overline{PD}$ voltage exceeds threshold to V_{OUT} = 90% of final value, V_{IN} = 1V		0.3		µs
	Turn-off time delay	Time from $\overline{PD}$ voltage reduces below threshold to I_Q = 10% of active mode value		0.1		µs

(1) Input range for CMRR > 77 dB.

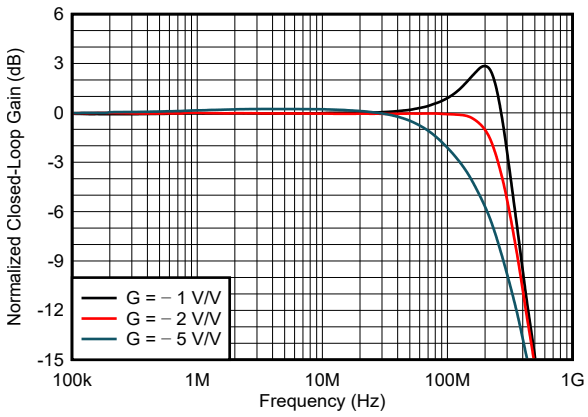
6.6 Typical Characteristics: V_S = ±5 V

at G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 200 mV_{PP}

図 6-1. Noninverting Small-Signal Frequency Response



V_{OUT} = 200 mV_{PP}

図 6-2. Inverting Small-Signal Frequency Response

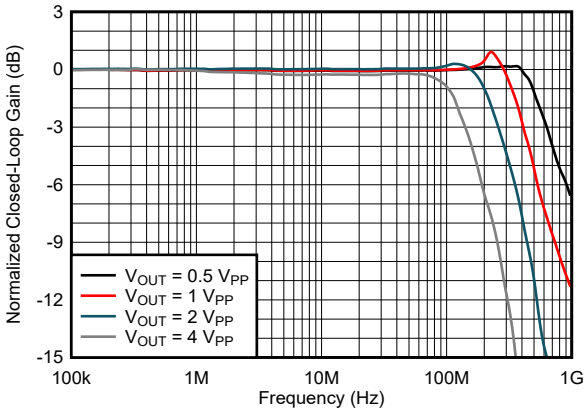


図 6-3. Noninverting Large-Signal Frequency Response

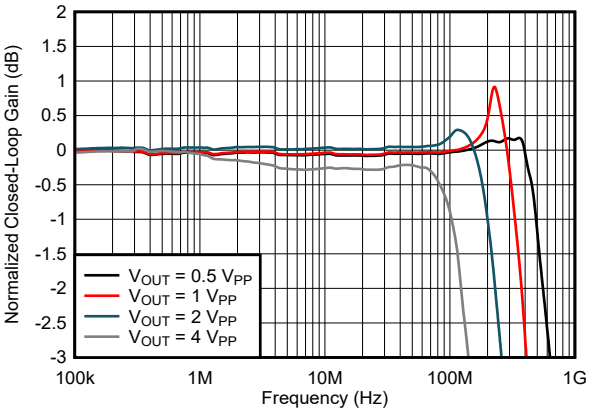
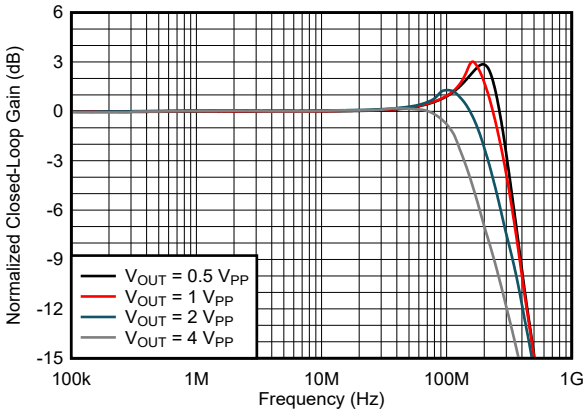
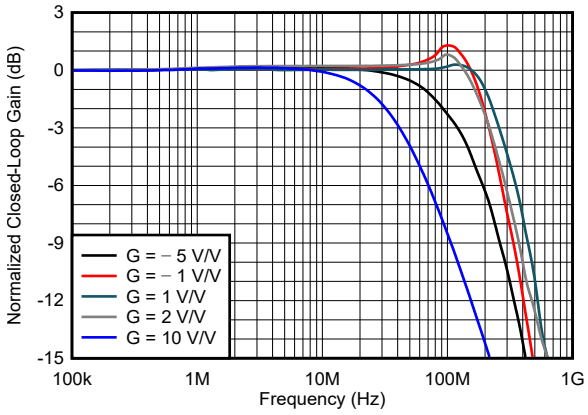


図 6-4. Gain Flatness vs Frequency



G = –1 V/V

図 6-5. Inverting Large-Signal Frequency Response

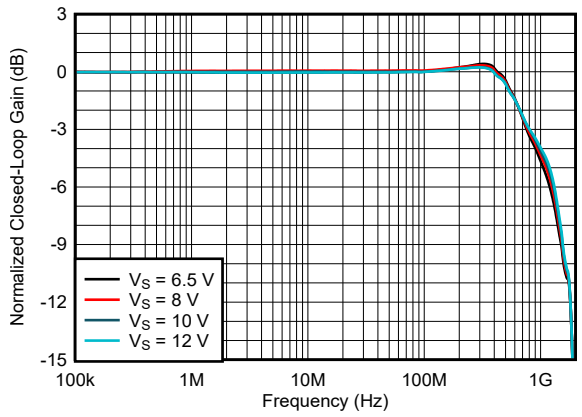


V_{OUT} = 2 V_{PP}

図 6-6. Large-Signal Frequency Response Over Gain

6.6 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 200 mV_{PP}

図 6-7. Noninverting Small-Signal Frequency Response Over Supply

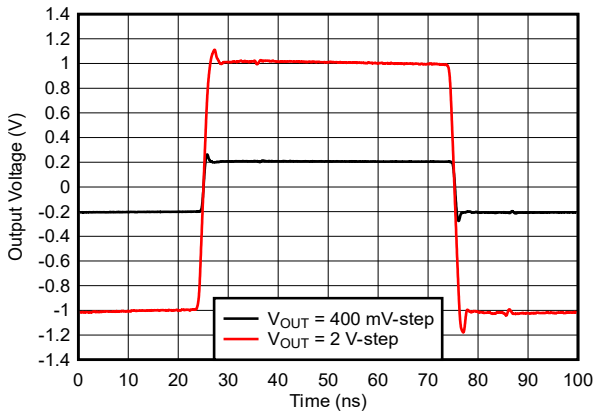
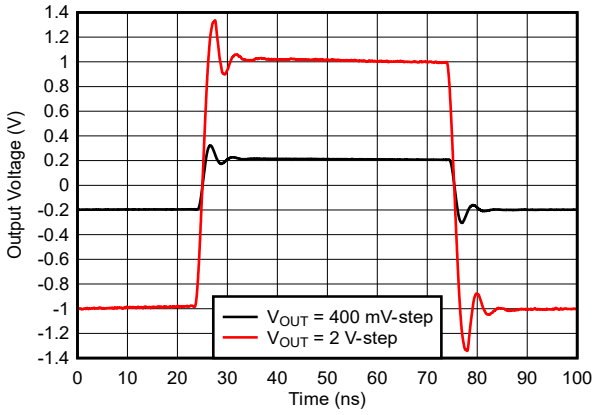
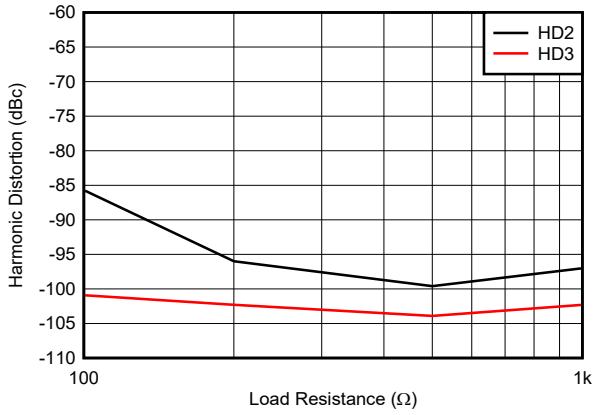


図 6-8. Noninverting Large-Signal Pulse Response



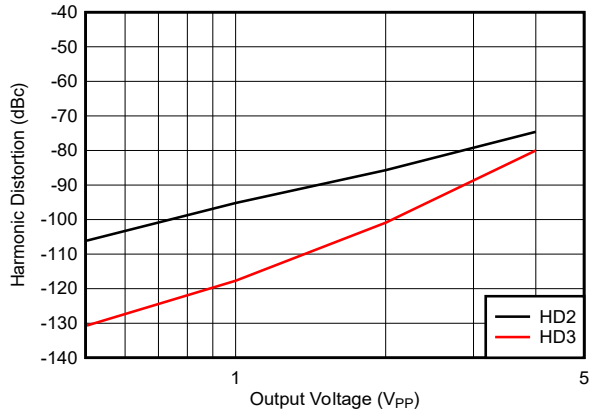
G = –1 V/V

図 6-9. Inverting Large-Signal Pulse Response



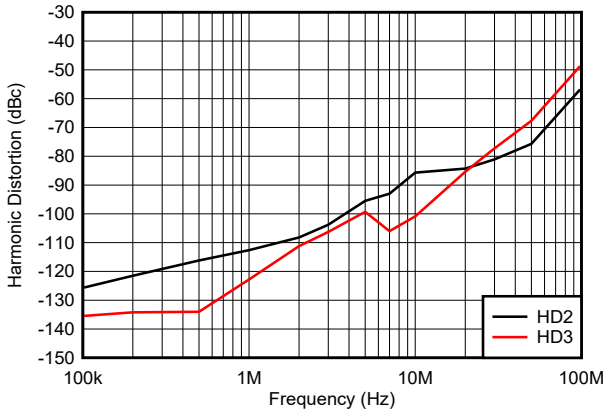
f = 10 MHz V_{OUT} = 2 V_{PP}

図 6-10. Harmonic Distortion vs Load Resistance



f = 10 MHz

図 6-11. Harmonic Distortion vs Output Voltage

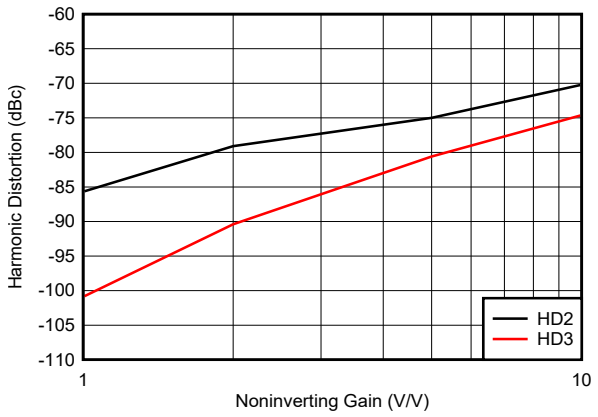


V_{OUT} = 2 V_{PP}

図 6-12. Harmonic Distortion vs Frequency

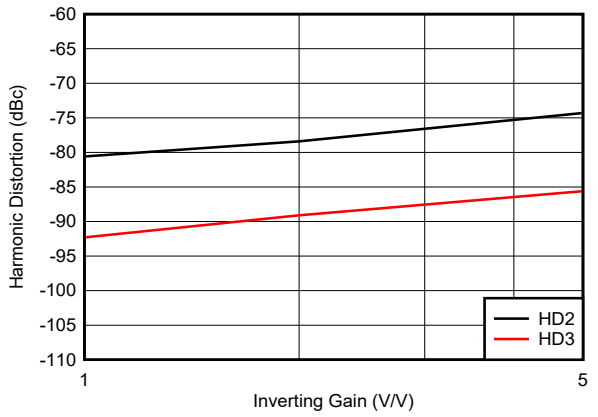
6.6 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



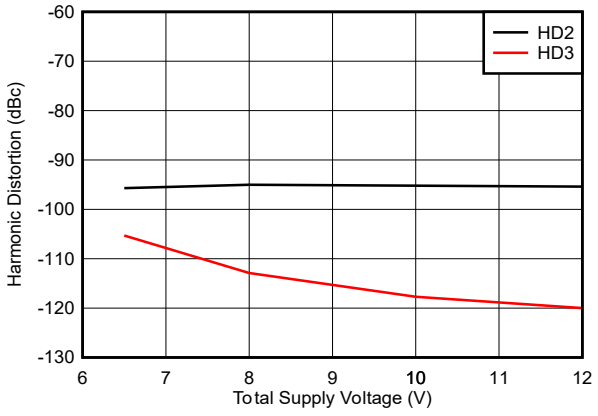
f = 10 MHz V_{OUT} = 2 V_{PP}

図 6-13. Harmonic Distortion vs Noninverting Gain



f = 10 MHz V_{OUT} = 2 V_{PP}

図 6-14. Harmonic Distortion vs Inverting Gain



f = 10 MHz V_{OUT} = 2 V_{PP}

図 6-15. Harmonic Distortion vs Supply Voltage

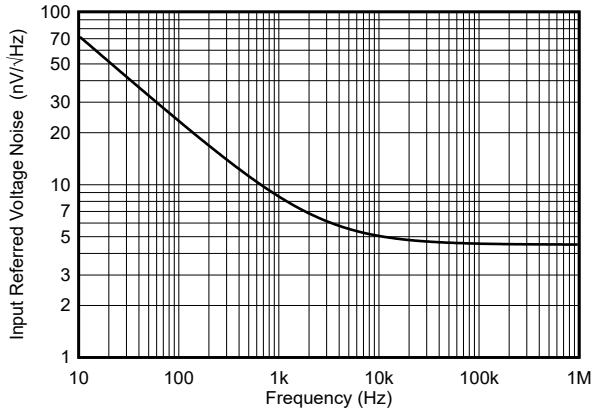


図 6-16. Voltage Noise Density vs Frequency

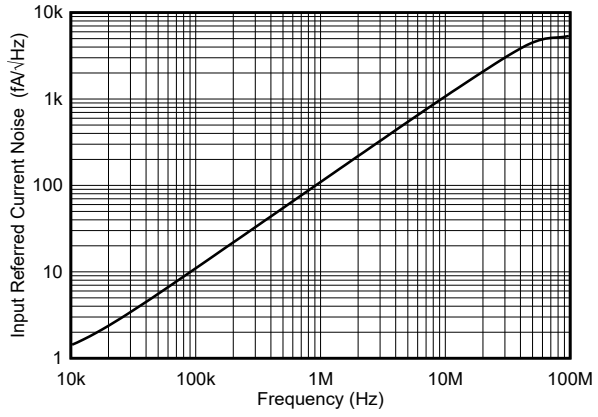


図 6-17. Current Noise Density vs Frequency

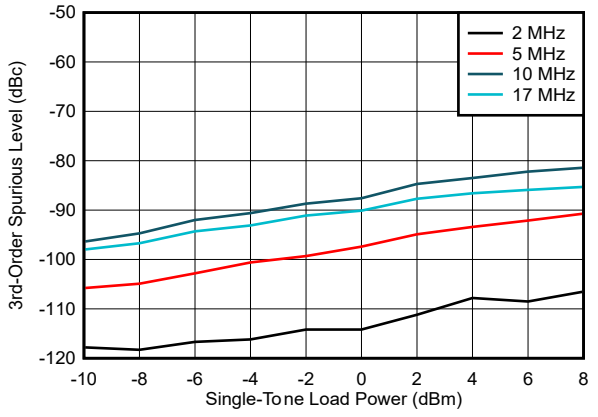


図 6-18. Intermodulation Distortion vs Load Power

6.6 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

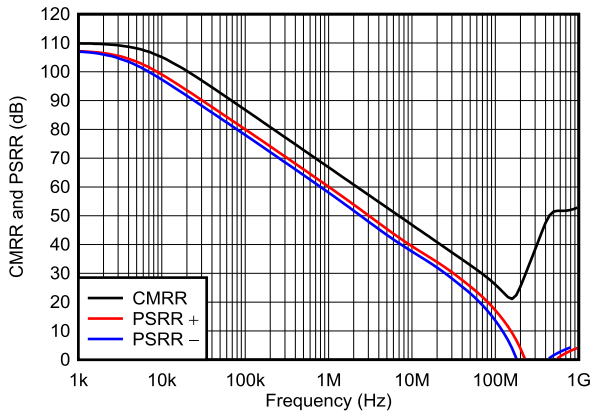


図 6-19. Common-Mode and Power-Supply Rejection Ratio vs Frequency

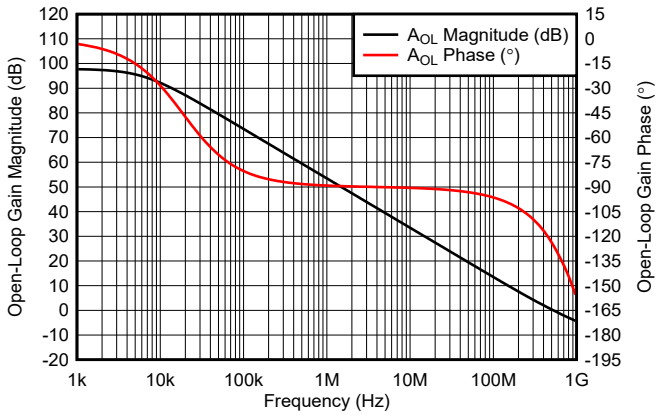


図 6-20. Open-Loop Gain Magnitude and Phase vs Frequency

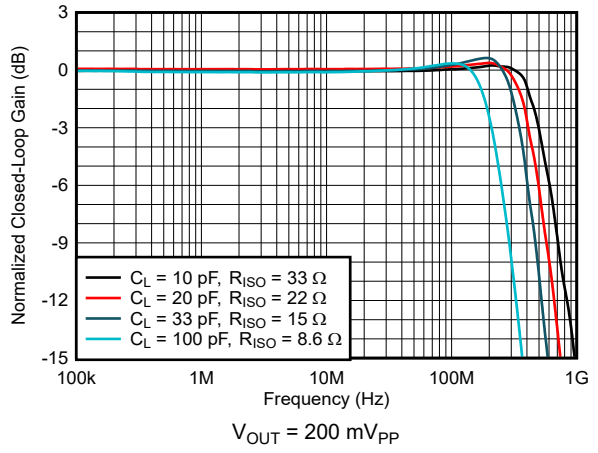


図 6-21. Frequency Response vs Capacitive Load

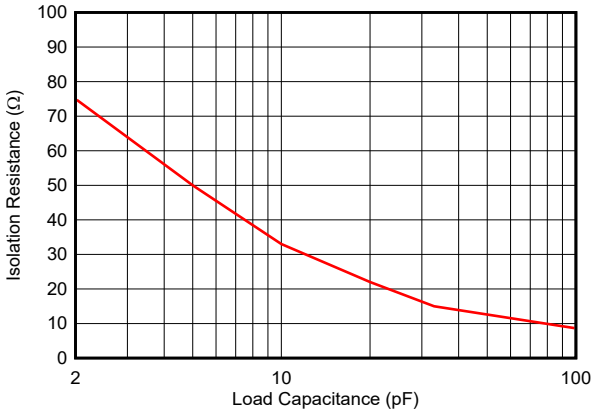


図 6-22. Recommended Isolation Resistor vs Capacitive Load

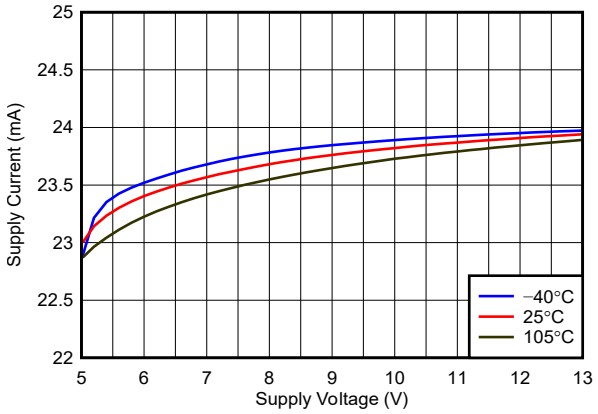


図 6-23. Quiescent Current vs Voltage Supply Over Temperature

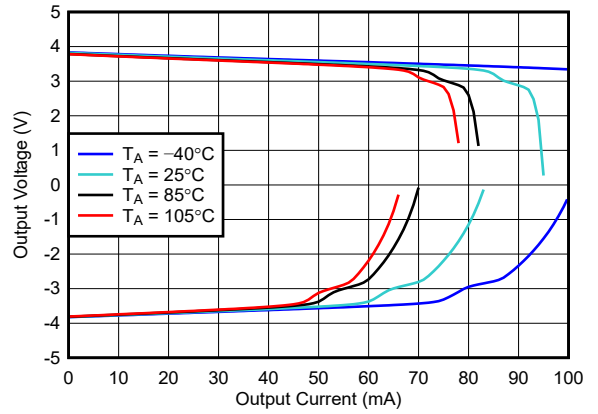
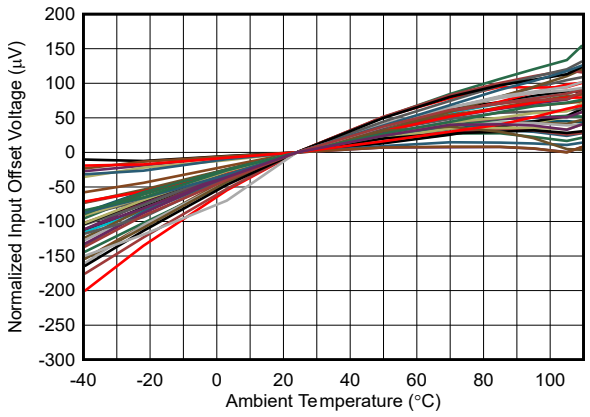


図 6-24. Output Voltage vs Output Current Over Temperature

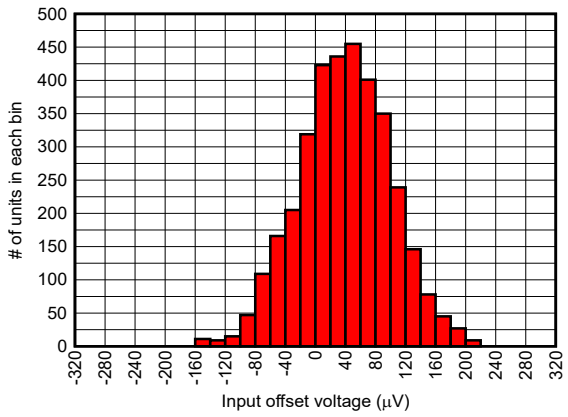
6.6 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



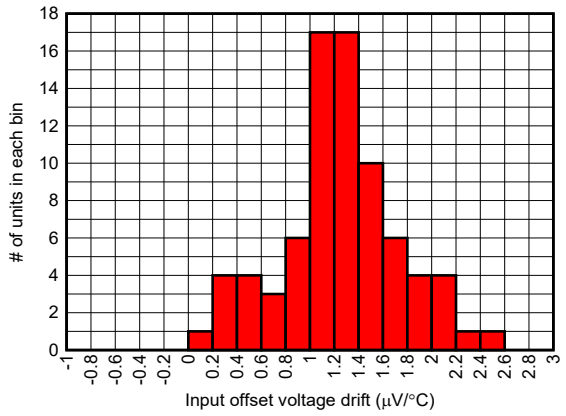
40 units, delta from 25°C

図 6-25. Input Offset Voltage vs Temperature



4000 units, µ = 40 µV, σ = 60 µV

図 6-26. Input Offset Voltage Histogram



40 units, µ = 1.2 µV/°C, σ = 0.5 µV/°C

図 6-27. Input Offset Voltage Drift Histogram

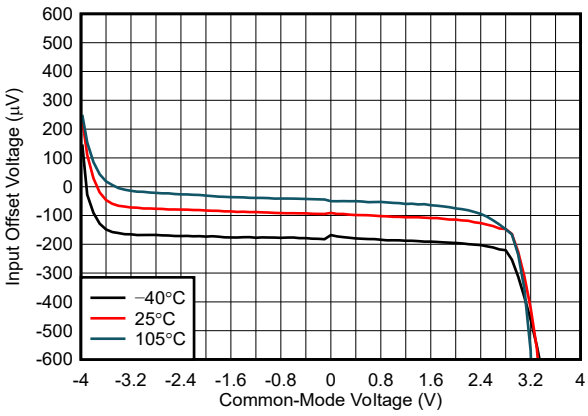
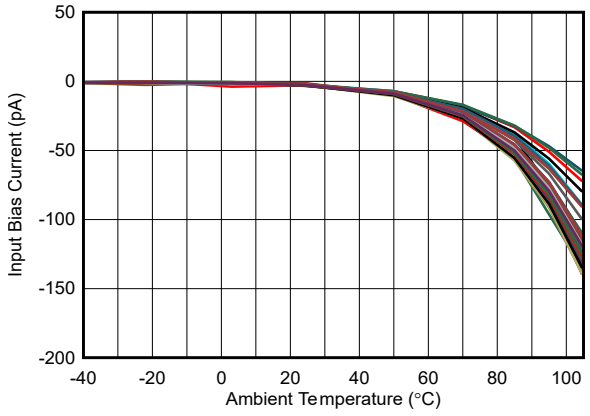
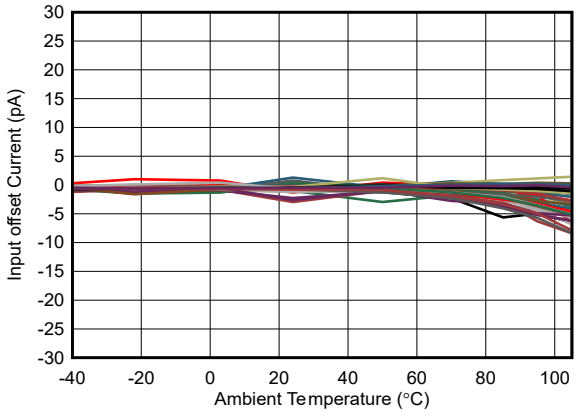


図 6-28. Input Offset Voltage vs Common-Mode Voltage Over Temperature



40 units

図 6-29. Input Bias Current vs Temperature



40 units

図 6-30. Input Offset Current vs Temperature

6.6 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

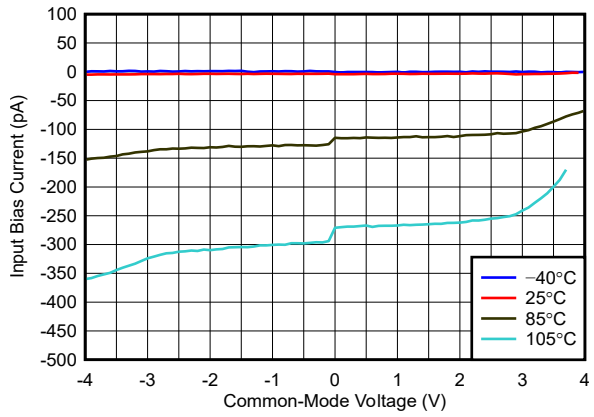
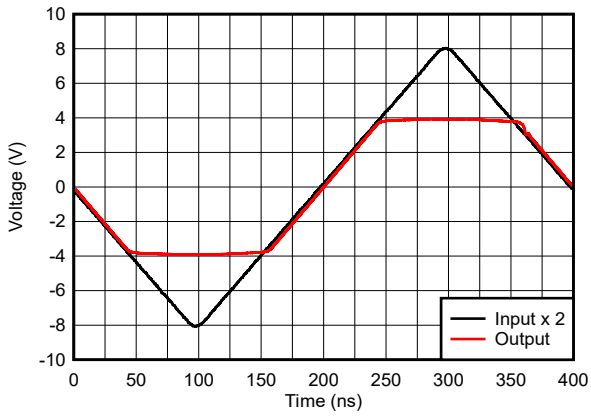
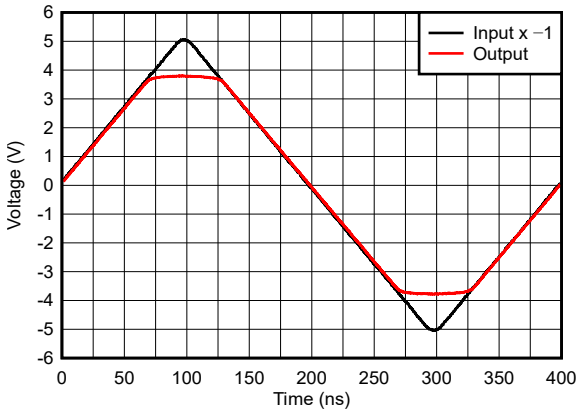


図 6-31. Input Bias Current vs Common-Mode Voltage Over Temperature



G = 2 V/V

図 6-32. Noninverting Output Overdrive Recovery



G = –1 V/V

図 6-33. Inverting Output Overdrive Recovery

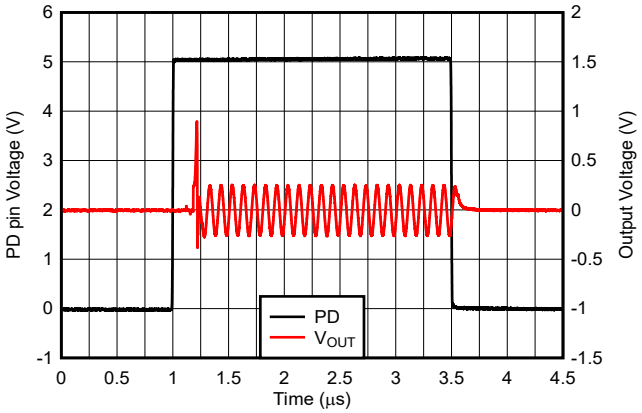


図 6-34. Turn-On and Turn-Off Waveform

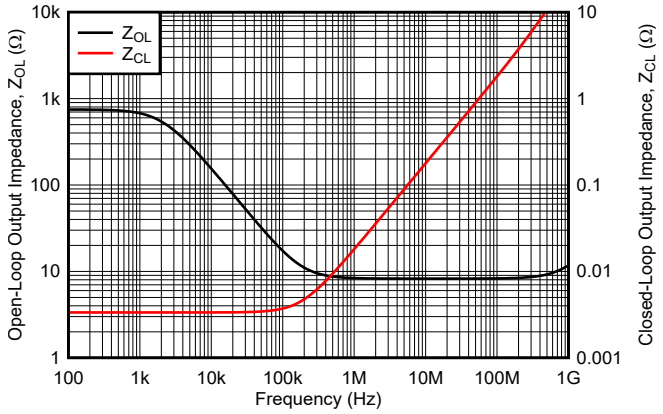


図 6-35. Open-Loop and Closed-Loop Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The OPA817 is a high-voltage, unity-gain-stable, 400-MHz gain-bandwidth product (GBWP), voltage-feedback operational amplifier (op amp) featuring a 4.5-nV/√Hz, low-noise, JFET input stage. The low offset voltage (250 µV maximum), offset voltage drift (3.5 µV/°C maximum), and unity gain bandwidth of 800 MHz makes this device an excellent choice for high-input-impedance, high-speed, data-acquisition front-ends. The high voltage capability combined with 1000 V/µs slew rate enables applications needing wide output swings (9 V_{PP} at V_S = 12 V) for high-frequency signals such as those often found in medical instrumentation, optical front-end, test, and measurement applications. The low noise JFET input with pico-amperes of bias current makes the device attractive in high-gain TIA applications and in test and measurement front-ends. OPA817 also features a power-down mode that disables the core amplifier for power savings.

The OPA817 is built using TI's proprietary high-voltage, high-speed, complementary bipolar SiGe process.

7.2 Functional Block Diagram

The OPA817 is a conventional voltage feedback op amp with two high-impedance inputs and a low-impedance output. 図 7-1 and 図 7-2 shows two standard amplifier configuration examples that are supported for this device. The reference voltage (V_{REF}) level shifts the dc operating point for each configuration, which is typically set to mid-supply in single-supply operation. V_{REF} is typically set to ground in split-supply applications.

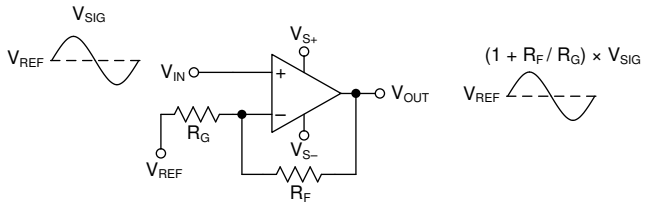


図 7-1. Noninverting Amplifier

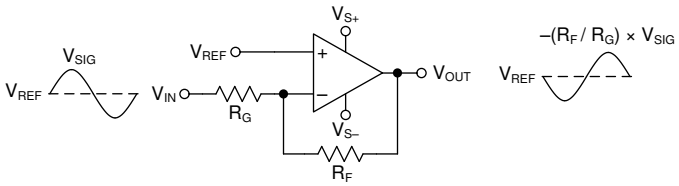


図 7-2. Inverting Amplifier

7.3 Feature Description

7.3.1 Input and ESD Protection

The OPA817 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings*. As 図 7-3 shows, all device pins are protected with internal ESD protection diodes to the power supplies.

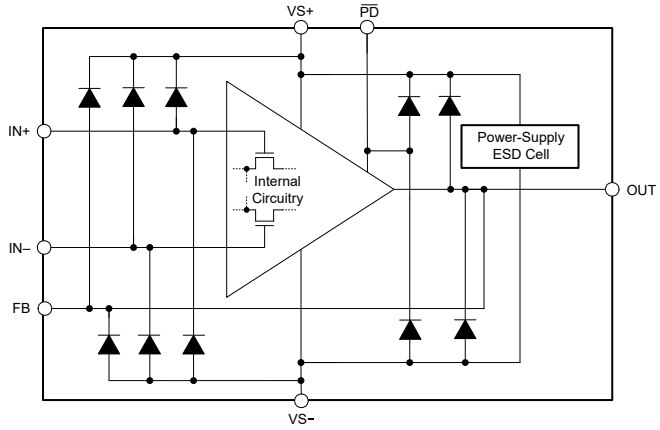


図 7-3. Internal ESD Protection

The diodes provide moderate protection to input overdrive voltages beyond the supplies as well. The protection diodes can typically support a 10-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA817), add current limiting series resistors in series with the two inputs to limit the current. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response. There are no back-to-back ESD diodes between V_{IN+} and $V_{IN–}$. As a result, the differential input voltage between V_{IN+} and $V_{IN–}$ is entirely absorbed by the V_{GS} of the input JFET differential pair and must not exceed the voltage ratings shown in the *Absolute Maximum Ratings*.

7.3.2 Feedback Pin

For high-speed analog design, minimizing parasitic capacitances and inductances is critical to get the best performance from a high-speed amplifier such as the OPA817. Parasitic capacitance and inductance are especially detrimental in the feedback path and at the inverting input, and result in undesired poles and zeroes in the feedback that can result in reduced phase margin or instability. Techniques used to correct this phase margin reduction often result in reduced application bandwidth. To keep system engineers from making these tradeoff choices and to simplify the PCB layout, OPA817 features an FB pin on the same side as the inverting input pin (IN–). 図 7-4 shows how this feature allows for a very short feedback resistor (R_F) connection between the FB and the IN– pin, which minimizes parasitic capacitance and inductance with minimal PCB design effort. Internally the FB pin is connected to OUT pin through metal routing on the silicon. Because of the fixed metal sizing of this connection, the FB pin has limited current carrying capability. Therefore, the specifications in the *Absolute Maximum Ratings* section must be adhered to for continuous operation. For applications requiring high accuracy, the metal routing resistance from OUT to FB can be considered and added to R_F to set the desired gain. For more information, see セクション 6.5.

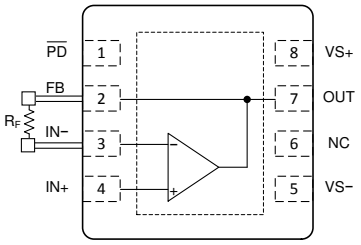


図 7-4. R_F Connection Between FB and IN– Pins

7.3.3 FET-Input Architecture With Wide Gain-Bandwidth Product

図 7-5 shows the open-loop gain and phase response of the OPA817. The GBWP of an op amp is measured in the 20-dB/decade constant slope region of the A_{OL} magnitude plot. The open-loop gain of 60 dB for the OPA817 is along this 20-dB/decade slope, and the corresponding frequency intercept is at 400 kHz. Converting 60 dB to linear units (1000 V/V) and multiplying by the 400-kHz frequency intercept gives a GBWP of 400 MHz for the OPA817. The A_{OL} Bode plot shows that the second pole in the A_{OL} response occurs after A_{OL} magnitude drops to less than 0 dB (1 V/V). The location of second pole results in phase change of less than 180° at 0 dB A_{OL}, indicating that the amplifier is stable in a gain of 1 V/V. Amplifiers such as the OPA817 that are JFET-input, low noise and unity-gain stable can be used as high-input-impedance buffers and gain stages with minimal degradation in SNR. The device has 800 MHz of SSBW in a gain-of-1-V/V configuration with a phase margin of approximately 55°.

The low input offset voltage and offset voltage drift of OPA817 makes the device an excellent amplifier for high-precision, high-input-impedance, wideband, data-acquisition-system front-ends. 図 8-2 shows that the system benefits from the low noise JFET input stage with pico-amperes of input bias current to achieve higher precision at 1-MΩ input impedance setting and higher SNR at 50-Ω input impedance setting simultaneously in a typical data-acquisition front-end circuit.

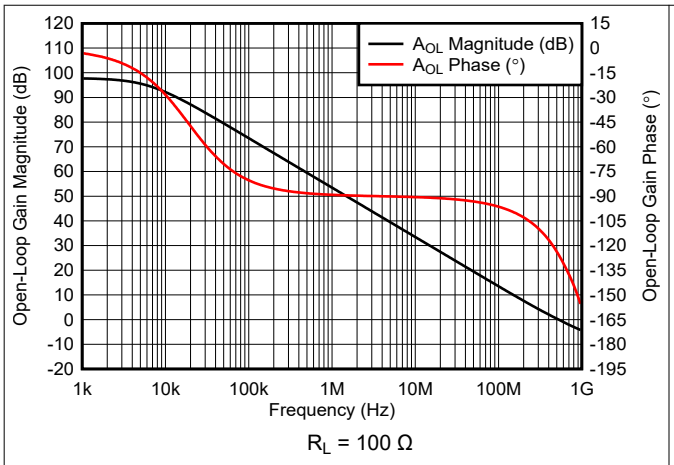


図 7-5. Open-Loop Gain Magnitude and Phase vs Frequency

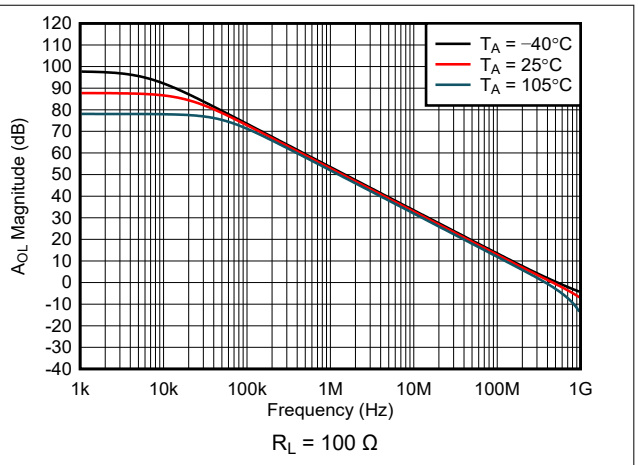


図 7-6. Open-Loop Gain Magnitude vs Temperature

7.4 Device Functional Modes

7.4.1 Power-Down ($\overline{PD}$) Pin

The OPA817 includes a power-down mode for low-power or standby operation and only consumes 55 µA (typical) of current when placed in power-down mode. Low-power systems that are only active for small periods of time benefit from this feature. The OPA817 transitions from low-power mode to active-mode in 300 ns (typical). For power-down pin control thresholds, see also セクション 6.5. An internal pull-up resistor of 2-MΩ provides a weak pull-up to V_{S+} if $\overline{PD}$ is left unconnected. Use an external 1-nF capacitor to V_{S+} to avoid external

noise coupling and false triggering. If the power-down mode is not used in an application, then connect the $\overline{PD}$ pin to V_{S+}.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Wideband, High-Input-Impedance DAQ Front End

The OPA817 features a unique combination of high GBWP, low-input voltage noise, and the dc precision of a trimmed JFET-input stage to provide a high input impedance for a voltage-feedback amplifier. 図 8-2 shows how the very high GBWP of 400 MHz and high large signal bandwidth of 250 MHz can be used to either deliver wide signal bandwidths at high gains or to extend the achievable bandwidth or gain in typical high-speed, high-input impedance data acquisition front-end applications. To achieve the full performance of the OPA817, careful attention to the printed circuit board (PCB) layout and component selection is required as discussed in the following sections of this data sheet. OPA817 also features a wider supply range thereby enabling a wider common-mode input range to support higher input signal swings.

図 8-1 shows the noninverting gain of +2 V/V circuit used as the basis for most of the *Typical Characteristics*. Most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. As 図 8-1 shows, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator, while the 49.9-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in 図 8-1) while output power specifications are at the matched 50-Ω load. As shown in 図 8-1, the total 100-Ω load at the output combined with the 250-Ω total feedback network load presents the OPA817 with an effective output load of 83.3 Ω for the circuit.

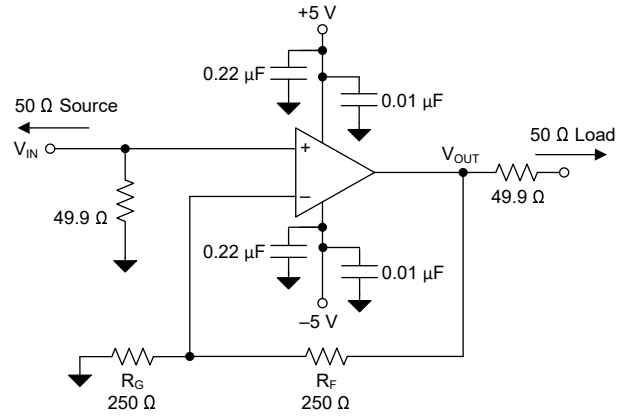


図 8-1. Noninverting G = +2 V/V Configuration and Test Circuit

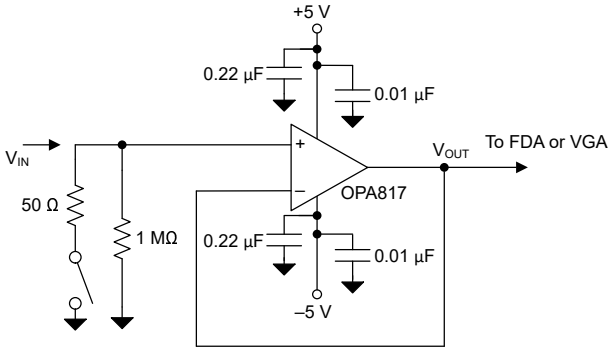


図 8-2. High Input Impedance DAQ Front-End

Voltage-feedback operational amplifiers, unlike current feedback amplifiers, can use a wide range of resistor values to set the gain. As 図 8-1 shows, always keep the parallel combination of R_F || R_G to a lower value to retain a controlled frequency response for the noninverting voltage amplifier. In the noninverting configuration, the parallel combination of R_F || R_G forms a pole with the parasitic input capacitance at the inverting node of the OPA817 (including layout parasitic capacitance). For best performance, ensure that this pole is at a frequency greater than the closed-loop bandwidth for the OPA817.

8.2 Typical Applications

8.2.1 High-Input-Impedance, 200-MHz, Digitizer Front-End Amplifier Design

The OPA817 offers a wide large-signal bandwidth, high-slew rate along with high-input impedance making this device an excellent choice for data-acquisition systems. The trimmed dc precision of the OPA817 enables direct use of the device as a front-end amplifier where low offset and offset voltage drift is needed.

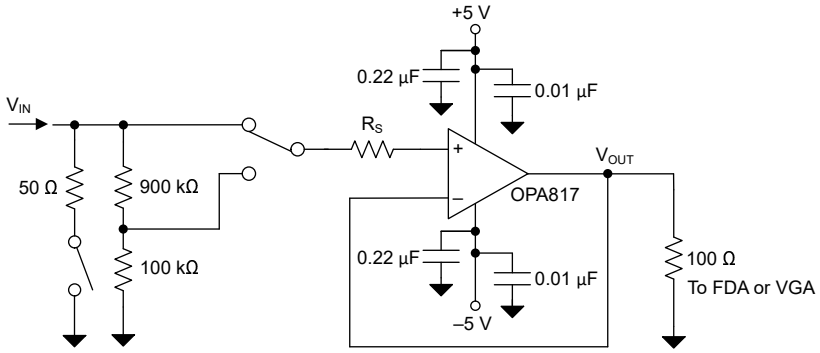


図 8-3. High-Input-Impedance, 200MHz, Digitizer Front-End Amplifier

8.2.1.1 Design Requirements

表 8-1 lists the design requirements for a high-input-impedance, 200-MHz, digitizer front-end amplifier.

表 8-1. Design Requirements

SPECIFICATION	VALUE
Input impedance	1 MΩ / 50Ω
Input range (1 MΩ / 50 Ω)	20 V_{PP} / 2 V_{PP}
Offset drift	3.5 µV/°C maximum
Noise at highest resolution (50 Ω Input)	80 μV_{RMS}

8.2.1.2 Detailed Design Procedure

- **Input Impedance:** The JFET-input stage of the OPA817 offers gigaohms of input impedance, and therefore enables the front-end to be terminated with a 1-MΩ resistor while achieving excellent precision. A 50-Ω resistance can also be switched in offering matched termination for high-frequency signals. The OPA817, therefore, enables the designer to use both 1-MΩ and 50-Ω termination in the same signal chain.
- **Noise**: The total noise of the front-end amplifier is the function of the voltage and current noise of the OPA817, input termination, and the resistors thermal noise. In 50-Ω mode, the dominant noise source, however, is contributed by the voltage noise of the OPA817 as a result of noise being integrated over the complete bandwidth. Thus, the total RMS noise of the front-end amplifier is approximately equal to the voltage noise of OPA817 over 200 MHz.

  The specified input referred voltage noise of the OPA817 is 4.5 nV/√Hz; see also セクション 6.5. The total integrated RMS noise at the input in a bandwidth of 200 MHz is given by the following equation:

$$En_{RMS} = 4.5\ nV/\sqrt{Hz} \times \sqrt{(200\ MHz \times 1.57)} = 80\ \mu V_{RMS}. \quad (1)$$

  The Brickwall correction factor of 1.57 is applied assuming the bandwidth is limited to 200 MHz with a single pole RC-filter before digitizing the signal with the ADC. Detailed calculations can be found at TI Precision Labs – Op Amps: Noise – Spectral Density.

- **Optimizing Overshoot:** The OPA817 features an internal slew-boost circuit to deliver fast rise-time in applications needing high slew rates such as when configured as a transimpedance amplifier. For applications where overshoot needs to be limited, the input slew rates can be limited with introducing a series resistance (R_S) as shown in 図 8-3. The resistance R_S forms a low pass filter with the input capacitance of approximately 2.6 pF at the noninverting pin of the OPA817 limiting the input slew rate to the amplifier. 図 8-4 shows how limiting the input slew rate to the amplifier results in good overshoot performance, and 図 8-5 shows how this achieves a small signal and large signal bandwidth of 200 MHz.

8.2.1.3 Application Curves

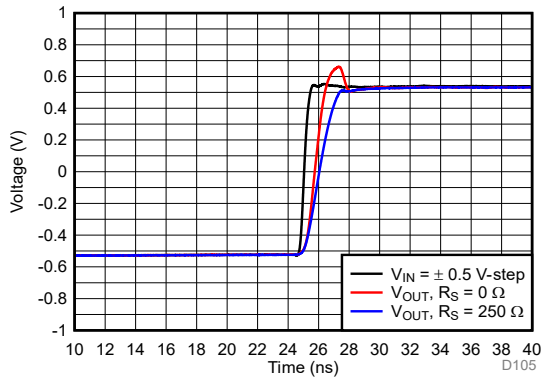


図 8-4. Step Response of Digitizer Front-End

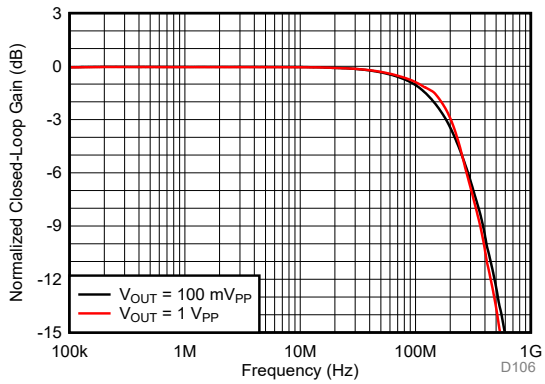


図 8-5. Frequency Response for R_S = 250 Ω

8.3 Power Supply Recommendations

The OPA817 is intended to operate on supplies ranging from 6 V to 12.6 V. OPA817 supports single-supply, split, balanced, and unbalanced bipolar supplies. When operating at supplies below 8 V, consideration must be given to the input common-mode range of the amplifier. Under these supply conditions, the common-mode must be biased appropriately for linear operation. Thus, the limit to lower supply voltage operation is the usable input voltage range for the JFET-input stage.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimized performance with a high-frequency amplifier such as the OPA817 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include the following:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability. On the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional bandlimiting. Ground and power metal planes act as one of the plates of a capacitor while the signal trace metal acts as the other separated by PCB dielectric. To reduce this unwanted capacitance, take care to minimize the routing of the feedback network. A plane cutout around and underneath the inverting input pin on all ground and power planes is recommended. Otherwise, ensure that ground and power planes are unbroken elsewhere on the board.

2. **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency decoupling capacitors.** Use high quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies to maintain a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Use larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, on the supply pins. Place these capacitors further from the device and share the capacitors among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high frequency performance of the OPA817.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound type resistors in a high frequency application. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistor, if any, as close as possible to the inverting input and the output pin, respectively. Place other network components, such as noninverting input termination resistors, close to the package. Even with a low parasitic capacitance at the noninverting input, high external resistor values can create significant time constants that can degrade performance. When OPA817 is configured as a conventional voltage amplifier, keep the resistor values as low as possible and consistent with the load driving considerations. Decrease the resistor values to keep the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.
4. **Heat dissipation is important for a high voltage device like the OPA817** . For good thermal relief, connect the thermal pad to a heat-spreading plane that is preferably on the same layer as the OPA817, or connected by as many vias as possible if the plane is on a different layer. Have at least one heat-spreading plane on the same layer as the OPA817 that makes direct connection to the thermal pad with wide metal for good thermal conduction when operating at high ambient temperatures. If more than one heat-spreading plane is available, then connect the heat-spreading planes by a number of vias to further improve the thermal conduction.

8.4.1.1 Thermal Considerations

The OPA817 does not require a heat sink or airflow in most applications. The maximum allowed junction temperature sets the maximum allowed internal power dissipation as described in the following paragraph. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced bipolar supplies). Under this condition $P_{DL} = V_S{}^2 / (4 \times R_L)$ where R_L includes feedback network loading.

The power in the output stage and not into the load determines internal power dissipation.

As a worst-case example, compute the maximum T_J using the OPA817 in the circuit of 図 8-1 operating at the maximum specified ambient temperature of +105°C and driving a grounded 100-Ω load.

$P_D = 10\ V \times 23.5\ mA + 5^2 / (4 \times (100\ \Omega \parallel 500\ \Omega)) \cong 310\ mW$

Maximum $T_J = 105°C + (0.310\ W \times 64.9°C/W) = 125.1°C$.

All actual applications operate at lower internal power and junction temperature.

8.4.2 Layout Example

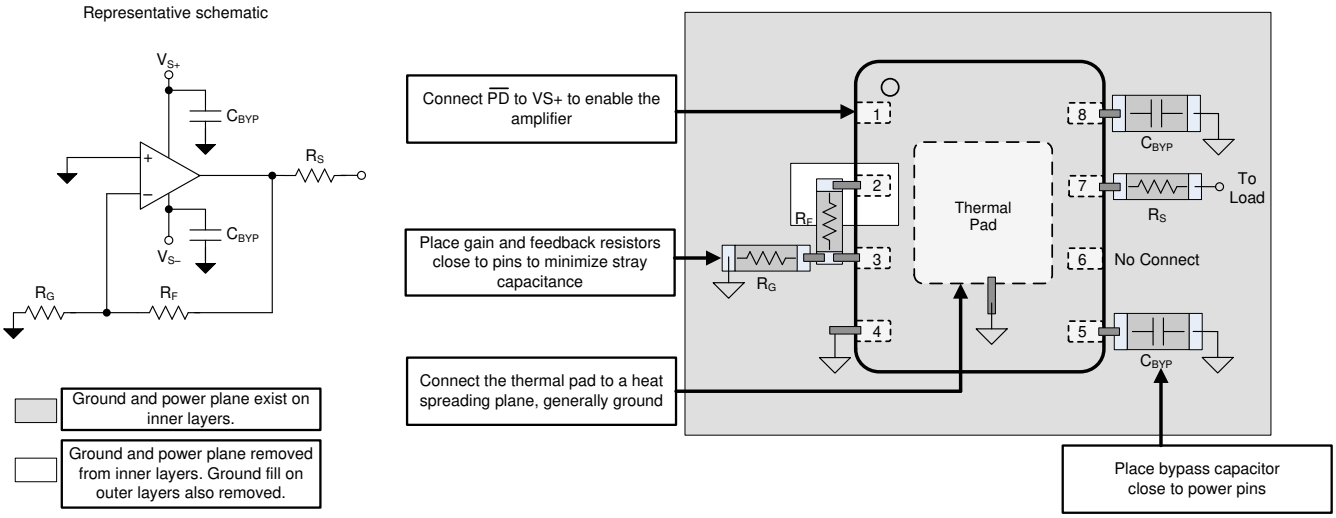


図 8-6. Layout Recommendation

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

- Texas Instruments, *Wide Bandwidth Optical Front-end Reference Design*

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA817EVM User's Guide*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *Maximizing the Dynamic Range of Analog TIA Front-End* technical brief
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2022) to Revision B (December 2024)	Page
• Changed PD pin description to fix incorrect high and low settings	3

Changes from Revision * (July 2022) to Revision A (December 2022)	Page
• データシートのステータスを以下のように変更:「事前情報」から「*量産データ*」	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA817DTKR	ACTIVE	WSON	DTK	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	817	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

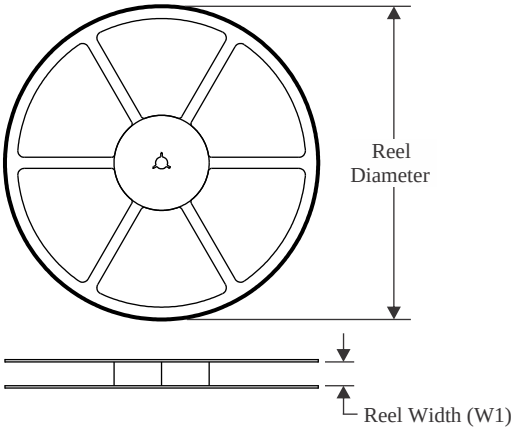
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

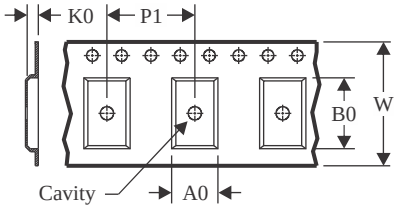
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

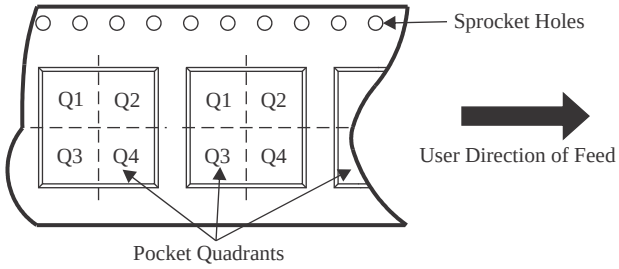


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

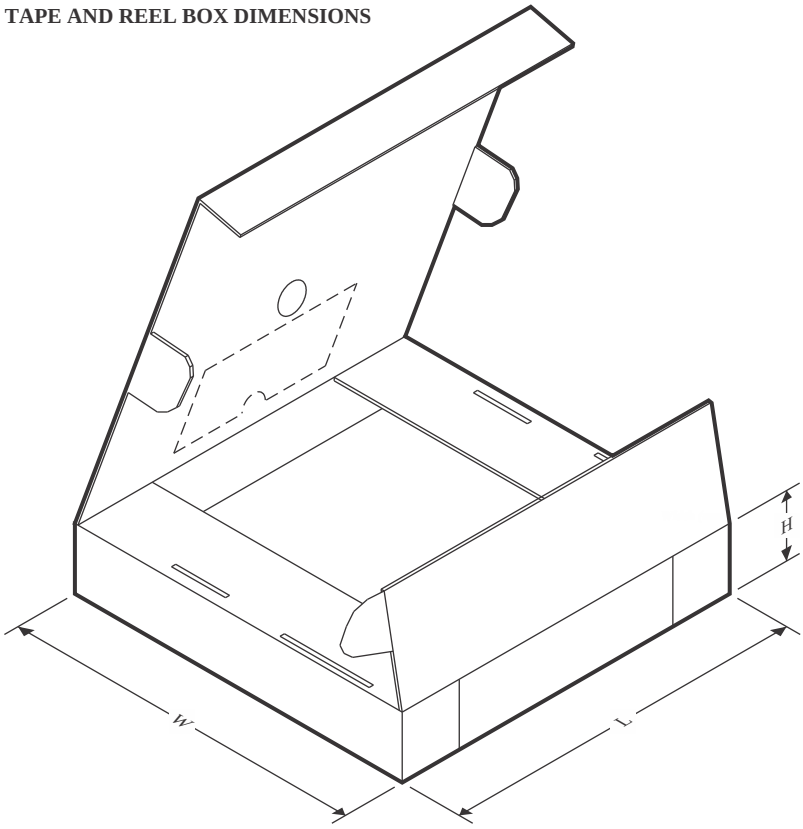
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA817DTKR	WSON	DTK	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

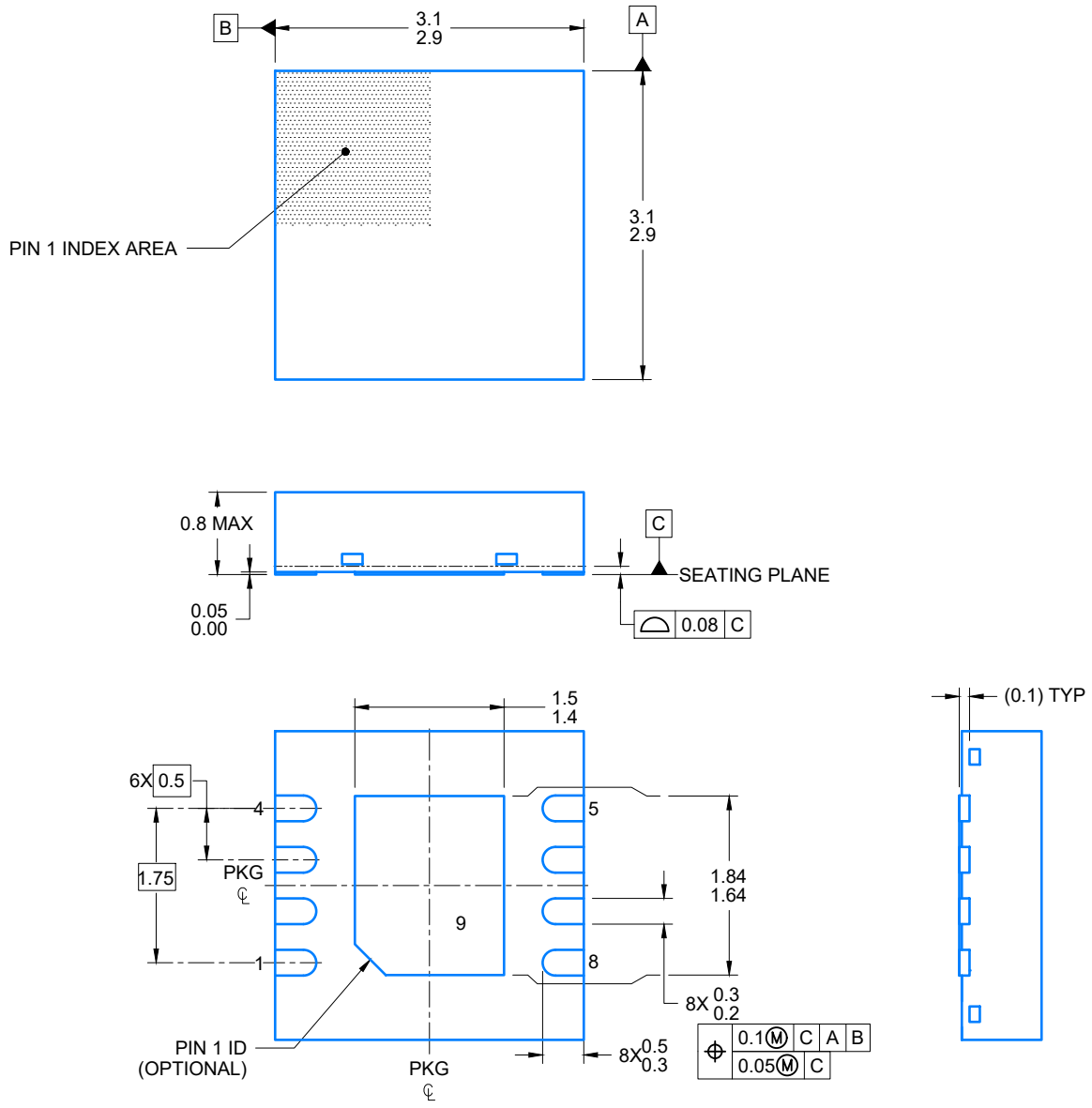
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA817DTKR	WSON	DTK	8	3000	367.0	367.0	35.0

PACKAGE OUTLINE

DTK0008A

WQFN - 0.8 mm max height

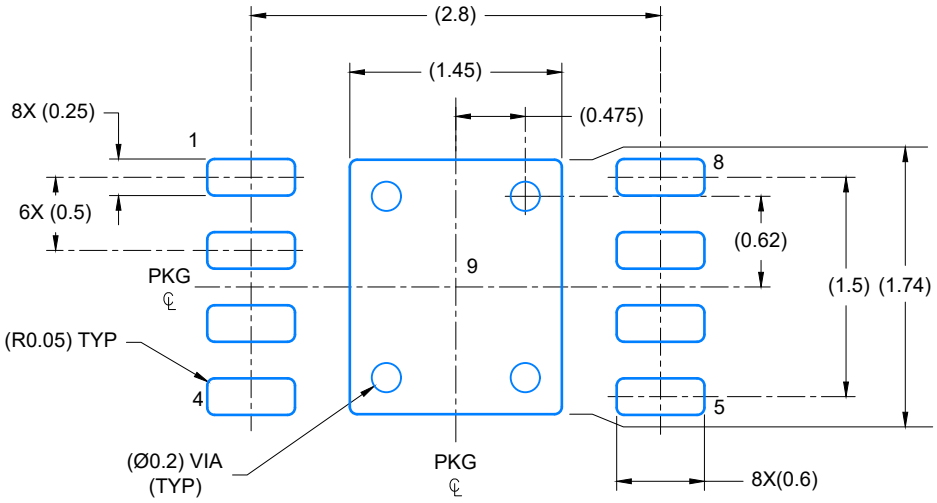
PLASTIC QUAD FLATPACK- NO LEAD



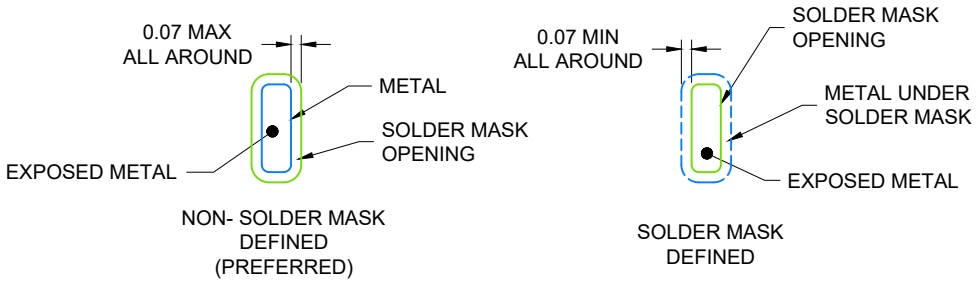
4224357 / A 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

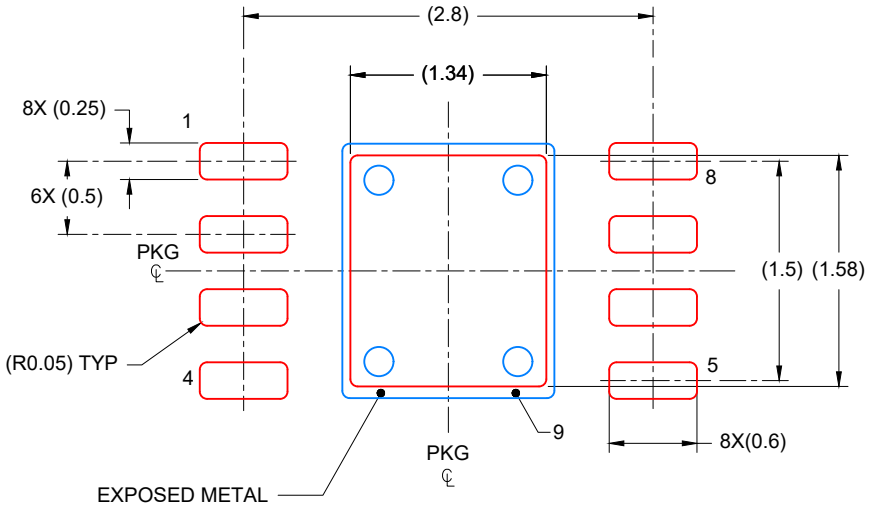


SOLDER MASK DETAILS

4224357 / A 07/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 9: 84%
SCALE: 20X

4224357 / A 07/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265