TEXAS INSTRUMENTS
PCA9536
JAJSOE5H – APRIL 2006 – REVISED MARCH 2022

PCA9536 リモート 4 ビット I²C および SMBus I/O エクスパンダ、構成レジスタ付き

1 特長

- テキサス・インスツルメンツの NanoFree™ パッケージで提供
- 低いスタンバイ消費電流：1μA 以下
- I²C からパラレル・ポートへのエクスパンダ
- 2.3V～5.5V の動作電源電圧範囲
- 5V 許容の I/O ポート
- 400kHz の高速 I²C バス
- 入力 / 出力構成レジスタ
- 極性反転レジスタ
- パワーオン・リセット内蔵
- 電源オン時のグリッチなし
- 電源投入時はすべてのチャネルが入力に構成された状態
- SCL/SDA 入力にノイズ・フィルタ
- 大電流の最大駆動能力を持つラッチ付き出力により、LED を直接駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン・モデル (A115-A)
  - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- パーソナル・エレクトロニクス
  - ウェアラブル
  - 携帯電話 / スマートフォン
  - ゲーム機
- サーバー
- ルーター

3 概要

この 2 線式双方向バス (I²C) 用 4 ビット I/O エクスパンダは、2.3V～5.5V の V_{CC} で動作するように設計されています。I²C インターフェイス [シリアル・クロック (SCL)、シリアル・データ (SDA)] により、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張に使用できます。

PCA9536 は、構成 (入力または出力選択)、入力ポート、出力ポート、極性反転 (アクティブ HIGH またはアクティブ LOW) 用の 4 ビット・レジスタを搭載しています。電源オン時、I/O は V_{CC} への弱いプルアップを備えた入力として構成されます。ただし、システム・コントローラが I/O 構成ビットに書き込むことにより、I/O を入力または出力とすることができます。PCA9536 に外部から信号が印加されていない場合、内部プルアップ抵抗により、電圧レベルは 1 すなわち HIGH になります。それぞれの入力または出力のデータは、対応する入力または出力ポート・レジスタに保存されます。入力ポート・レジスタの極性は、極性反転レジスタで反転できます。システム・コントローラはすべてのレジスタを読み出すことができます。

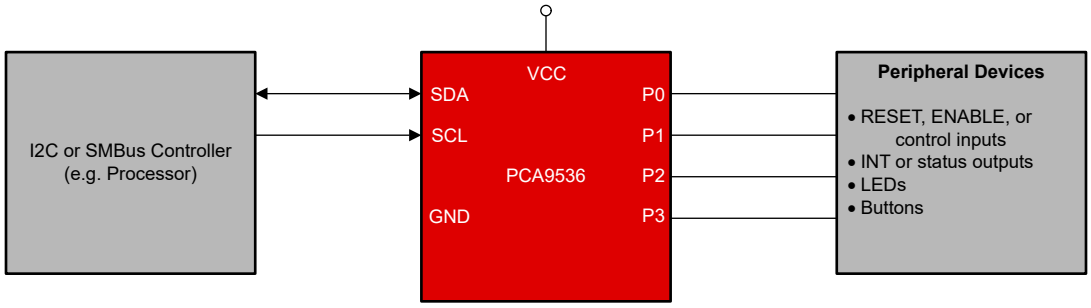
タイムアウトまたはその他の不適切な動作が発生した場合、システム・コントローラは、パワーオン・リセット機能を利用して PCA9536 をリセットできます。これにより、レジスタはデフォルト状態になり、I²C/SMBus ステート・マシンは初期化されます。

本デバイスの出力 (ラッチ付き) は、LED を直接駆動できるように大電流駆動能力を備えていますが、消費電流は小さくなっています。

デバイス情報

部品番号	パッケージ(1)	本体サイズ (公称)
PCA9536	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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Table of Contents

4 Revision History

Changes from Revision G (June 2014) to Revision H (March 2022) — **Page**

- I2C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更 ... 1
- DSBGA (YZP) パッケージの情報を削除 ... 1
- 表紙に「*概略回路図*」を追加 ... 1
- Removed packaging information from the *Absolute Maximum Ratings* table ... 4
- Added T_{stg} to the *Absolute Maximum Ratings* table ... 4
- Added the *Thermal Information* table ... 4
- Deleted V_{POR} from the Electrical Characteristics ... 5
- Added V_{PORR} and V_{PORF} to the Electrical Characteristics ... 5
- Changed the I_{CC} stand by mode current max values for 5.5 V from 1 to 1.8 µA; 3.6 V from 0.9 to 1.2 µA; and 2.7 V from 0.8 to 1 µA in the Electrical Characteristics ... 5
- Changed the $t_{vd(data)}$ and $\mathbf{t_{vd(ack)}}$ MAX values from: 1 µs to: 3.45 µs in the *Standard Mode* timing ... 6
- Changed the t_{icr}, t_{ocf}, and t_{ocf} MIN values in the *Fast Mode* timing ... 6
- Added the Overview section ... 12
- Added the *Device Functional Modes* section ... 13
- Added *Detailed Design Procedure* section ... 20
- Added *Application Curves* section ... 21
- Added the *Layout* section ... 23

Changes from Revision F (September 2008) to Revision G (June 2014) — **Page**

- Added Power-On Reset Errata section ... 22

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5 Pin Configuration and Functions

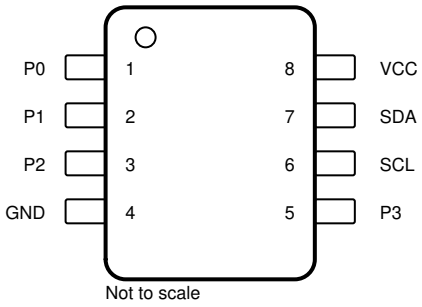

図 5-1. D Package, 8-Pin SOIC (Top View)

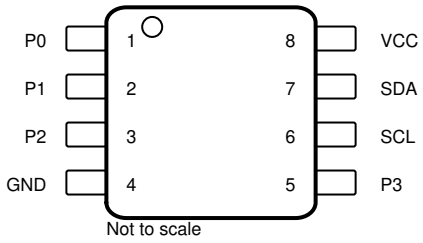

図 5-2. DGK Package, 8-Pin VSSOP, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	P0	I/O	P-port input-output. Push-pull design structure
2	P1	I/O	P-port input-output. Push-pull design structure
3	P2	I/O	P-port input-output. Push-pull design structure
4	GND	—	Ground
5	P3	I/O	P-port input-output. Push-pull design structure
6	SCL	I/O	Serial clock bus. Connect to V_{CC} through a pullup resistor
7	SDA	I/O	Serial data bus. Connect to V_{CC} through a pullup resistor
8	V_{CC}	—	Supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage (2)		–0.5	6	V
V_O	Output voltage (2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–200	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	5.5	V
		P3–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		P3–P0	–0.5	0.8	
I_{OH}	High-level output current	P3–P0		–10	mA
I_{OL}	Low-level output current	P3–P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 8 PINS	DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.9	183.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.6	76.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.3	104.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32.3	18.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.6	103.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2		0	V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND, I_O = 0			1.2	1.6	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	10		mA
	P-port(3)	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	32		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	44		
I_I	SCL, SDA	V_I = V_{CC} or GND	2.3 V to 5.5 V			±1	µA
I_{IH}	P-port	V_I = V_{CC}	2.3 V to 5.5 V			1	µA
I_{IL}	P-port	V_I = GND	2.3 V to 5.5 V			–100	µA
I_{CC}	Operating mode	V_I = V_{CC}, I_O = 0, I/O = inputs, f_{scl} = 400 kHz	5.5 V		73	150	µA
			3.6 V		9	50	
			2.7 V		7	30	
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{scl} = 100 kHz	5.5 V		14	25	
			3.6 V		9	20	
			2.7 V		6	15	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		225	350	
			3.6 V		175	250	
			2.7 V		125	200	
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		0.25	1.8	
			3.6 V		0.2	1.2	
			2.7 V		0.1	1	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			0.35	mA
		Every LED I/O at V_I = 4.3 V, f_{scl} = 0 kHz	5.5 V			0.4	
C_i	SCL	V_I = V_{CC} or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	V_{IO} = V_{CC} or GND	2.3 V to 5.5 V		5	6.5	pF
	P-port				7.5	9.5	

(1) All typical values are at nominal supply voltage (2.5-, 3.3-, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be limited externally to a maximum of 25 mA, and the P-port (P3–P0) must be limited to a maximum current of 100 mA.

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6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

		MIN	MAX	UNIT
Standard Mode				
f_{scl}	I²C clock frequency	0	100	kHz
t_{sch}	I²C clock high time	4		µs
t_{scl}	I²C clock low time	4.7		µs
t_{sp}	I²C spike time		50	ns
t_{sds}	I²C serial-data setup time	250		ns
t_{sdh}	I²C serial-data hold time	0		ns
t_{icr}	I²C input rise time		1000	ns
t_{icf}	I²C input fall time		300	ns
t_{ocf}	I²C output fall time, 10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between Stop and Start	4.7		µs
t_{sts}	I²C Start or repeated Start condition setup time	4.7		µs
t_{sth}	I²C Start or repeated Start condition hold time	4		µs
t_{sps}	I²C Stop condition setup time	4		µs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load		400	pF
Fast Mode				
f_{scl}	I²C clock frequency	0	400	kHz
t_{sch}	I²C clock high time	0.6		µs
t_{scl}	I²C clock low time	1.3		µs
t_{sp}	I²C spike time		50	ns
t_{sds}	I²C serial-data setup time	100		ns
t_{sdh}	I²C serial-data hold time	0		ns
t_{icr}	I²C input rise time	20(1)	300	ns
t_{icf}	I²C input fall time	20x(Vdd/5.5V) (1)	300	ns
t_{ocf}	I²C output fall time, 10-pF to 400-pF bus	20x(Vdd/5.5V) (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start	1.3		µs
t_{sts}	I²C Start or repeated Start condition setup time	0.6		µs
t_{sth}	I²C Start or repeated Start condition hold time	0.6		µs
t_{sps}	I²C Stop condition setup time	0.6		µs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load		400	pF

(1) C_b = Total capacitive load of one bus in pF

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
STANDARD MODE and FAST MODE						
t_{pv}	Output data valid	SCL	P3–P0		200	ns
t_{ps}	Input data setup time	P-port	SCL	100		ns
t_{ph}	Input data hold time	P-port	SCL	1		µs

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6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

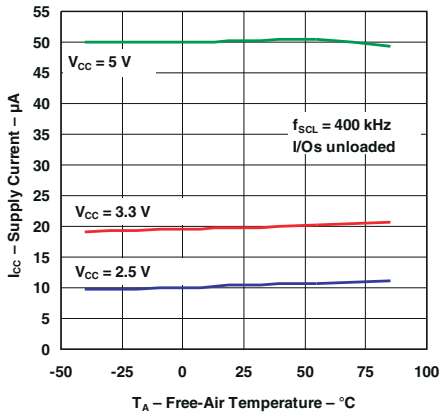

図 6-1. Supply Current vs Temperature

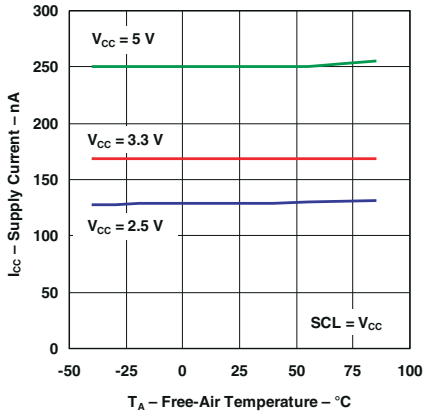

図 6-2. Quiescent Supply Current vs Temperature

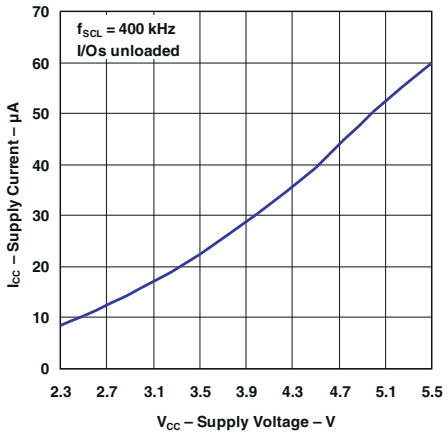

図 6-3. Supply Current vs Supply Voltage

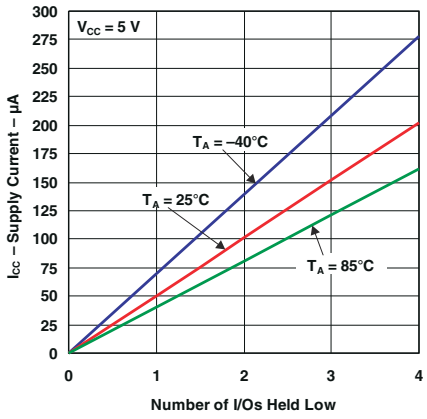

図 6-4. Supply Current vs Number of I/Os Held Low

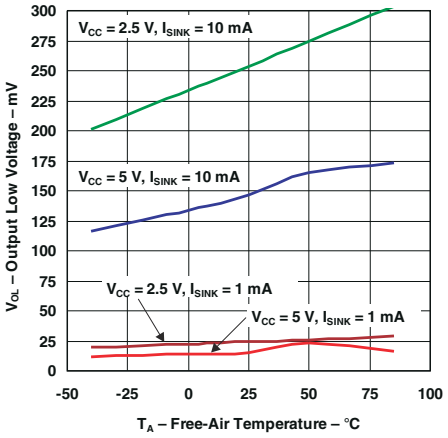

図 6-5. I/O Output Low Voltage vs Temperature

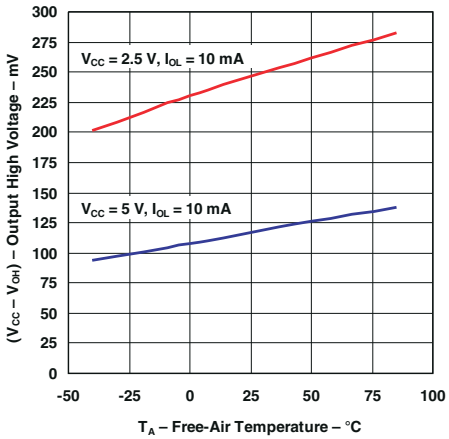

図 6-6. I/O Output High Voltage vs Temperature

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6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

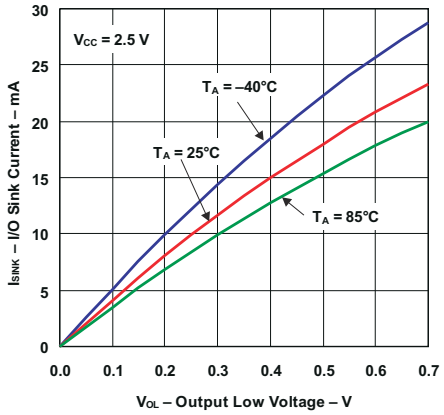

図 6-7. I/O Sink Current vs Output Low Voltage

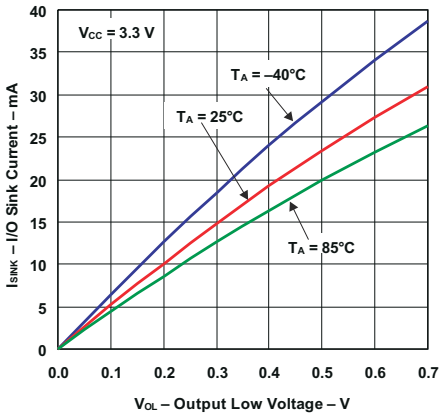

図 6-8. I/O Sink Current vs Output Low Voltage

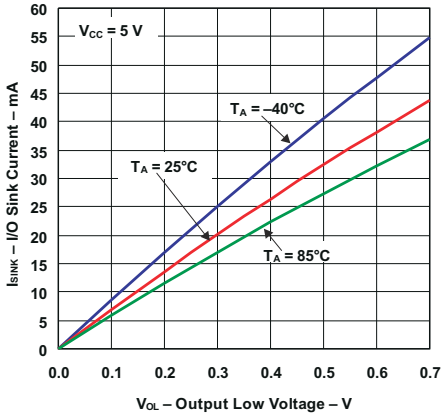

図 6-9. I/O Sink Current vs Output Low Voltage

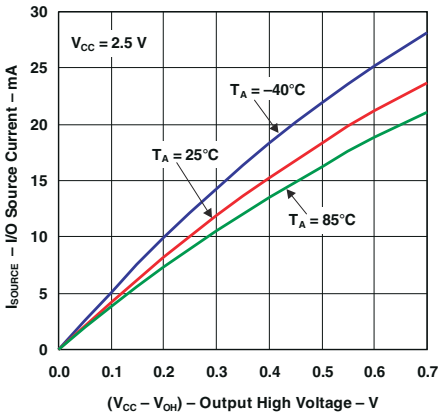

図 6-10. I/O Source Current vs Output High Voltage

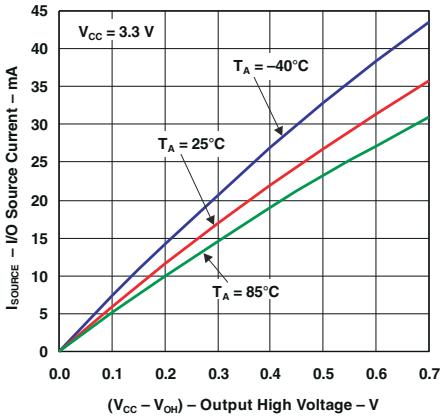

図 6-11. I/O Source Current vs Output High Voltage

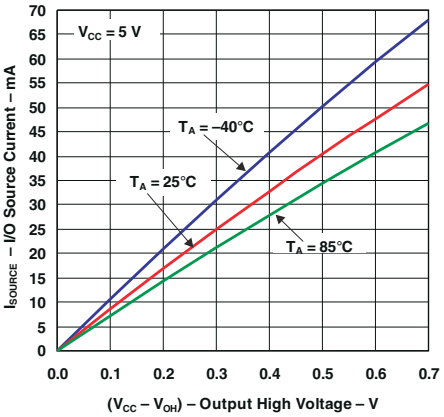

図 6-12. I/O Source Current vs Output High Voltage

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6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

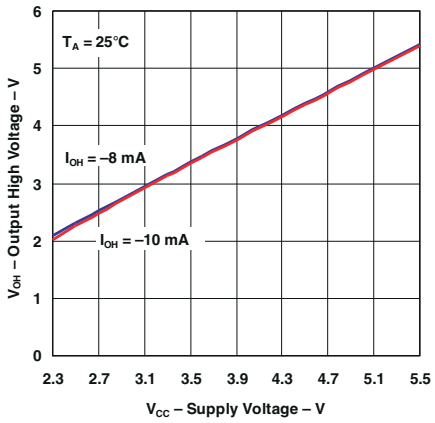
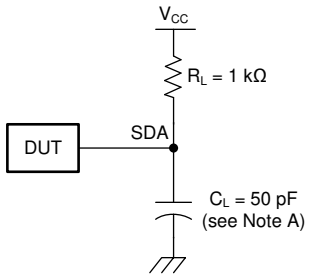
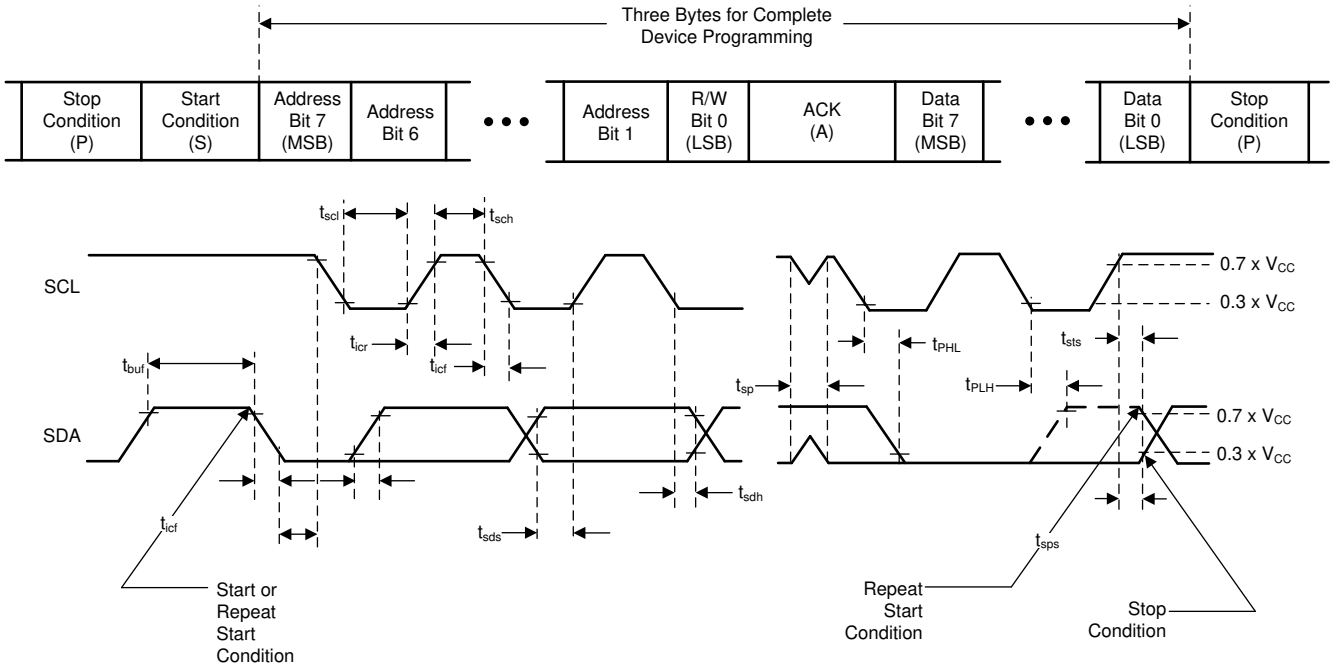


図 6-13. Output High Voltage vs Supply Voltage

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

A. C_L include probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

図 7-1. I²C Interface Load Circuit and Voltage Waveforms

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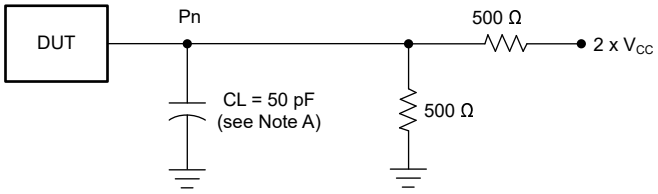
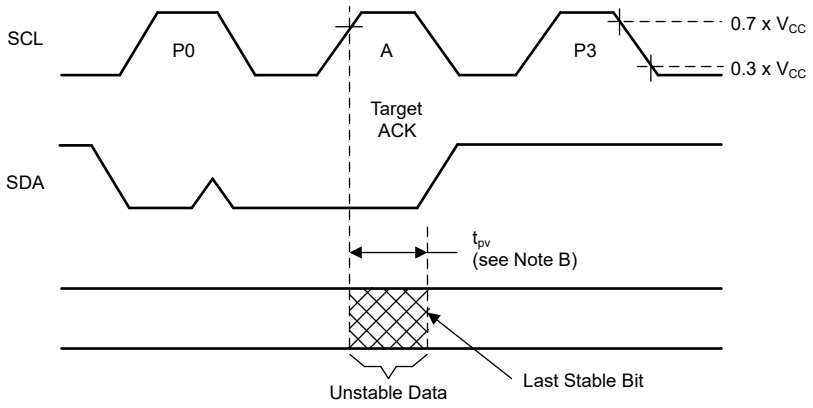
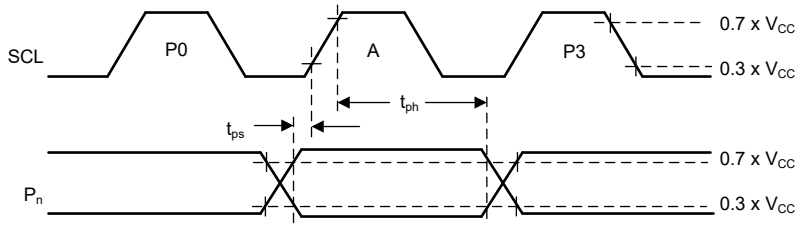


P-PORT LOAD CONFIGURATION



WRITE MODE (R/W = 0)



READ MODE (R/W = 1)

A. C_L include probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 7-2. P-Port Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

The PCA9536 device is a 4-bit I/O expander for the I^2C bus and is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families through the I^2C interface.

The PCA9536 consists of a configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system controller enables the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register and the system controller reads all registers.

The device outputs (latched) have high-current drive capability for directly driving LEDs.

8.2 Functional Block Diagram

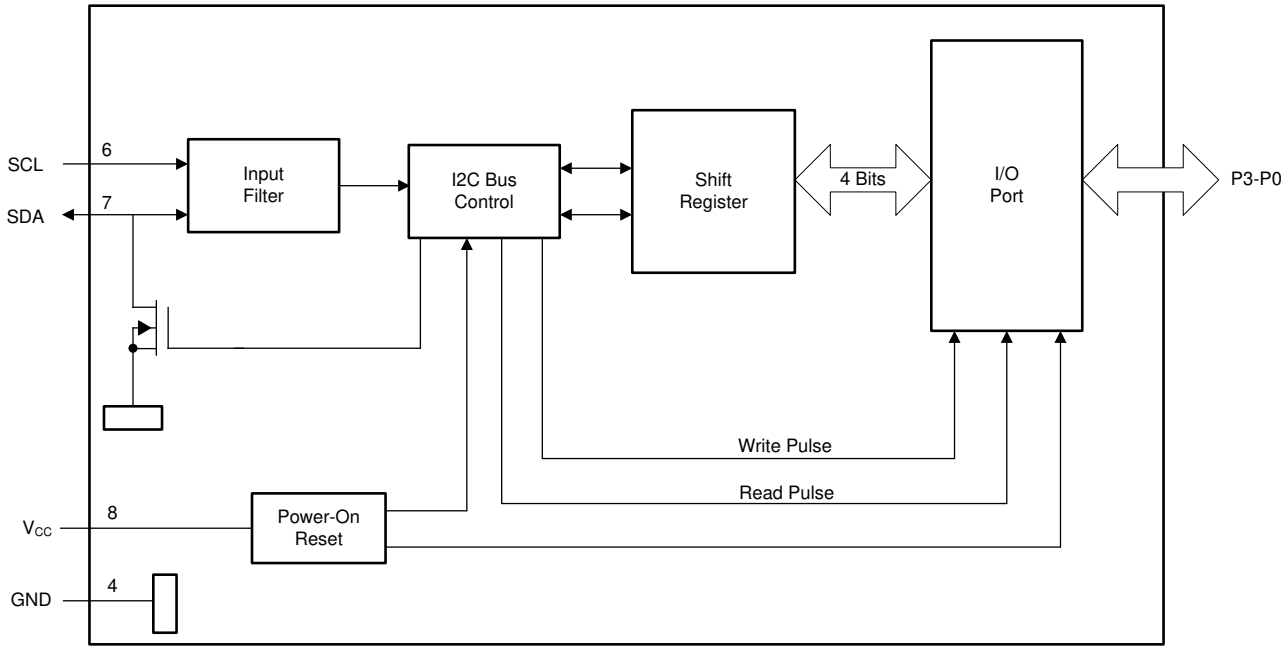

図 8-1. Logic Diagram

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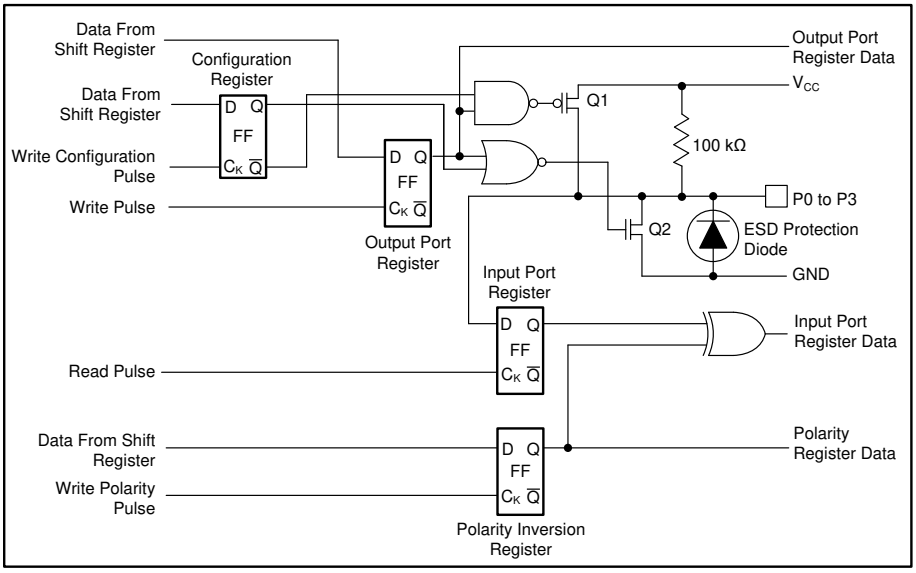

図 8-2. Simplified Schematic Of P0 To P3

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in 図 8-2) are off, creating a high-impedance input with a weak pullup (100 kΩ typical) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9536 in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released and the PCA9536 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Refer to the *セクション 10.1* section.

8.4.2 Powered-Up

When power has been applied to V_{CC} above V_{PORR}, and the POR has taken place, the device is in a functioning mode. In this state, the device is ready to accept any incoming I^2C requests and monitors for changes on the input ports.

8.5 Programming

8.5.1 I^2C Interface

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by a controller sending a Start condition, which is a high-to-low transition on the SDA input and output while the SCL input is high (see 図 8-3). After the Start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$).

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After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input and output during the high of the ACK-related clock pulse.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 図 8-4).

A Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high, is sent by the controller (see 図 8-3).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 8-5). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. This is done by the controller receiver, by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

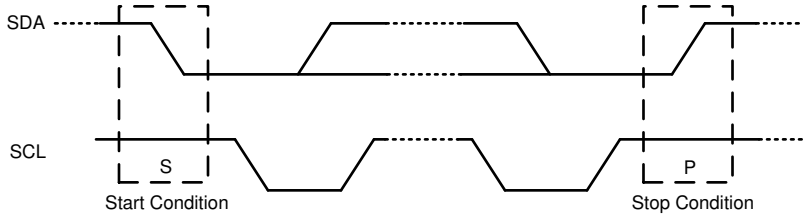

図 8-3. Definition of Start and Stop Conditions

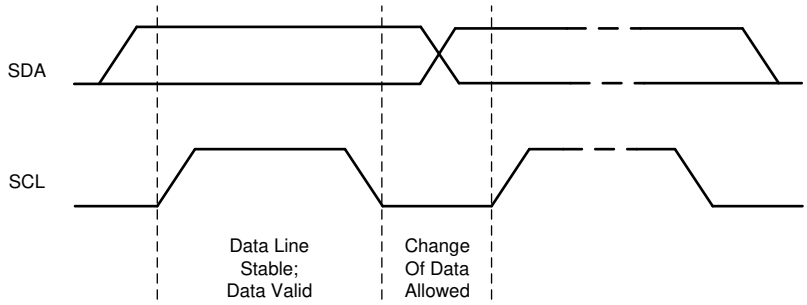

図 8-4. Bit Transfer

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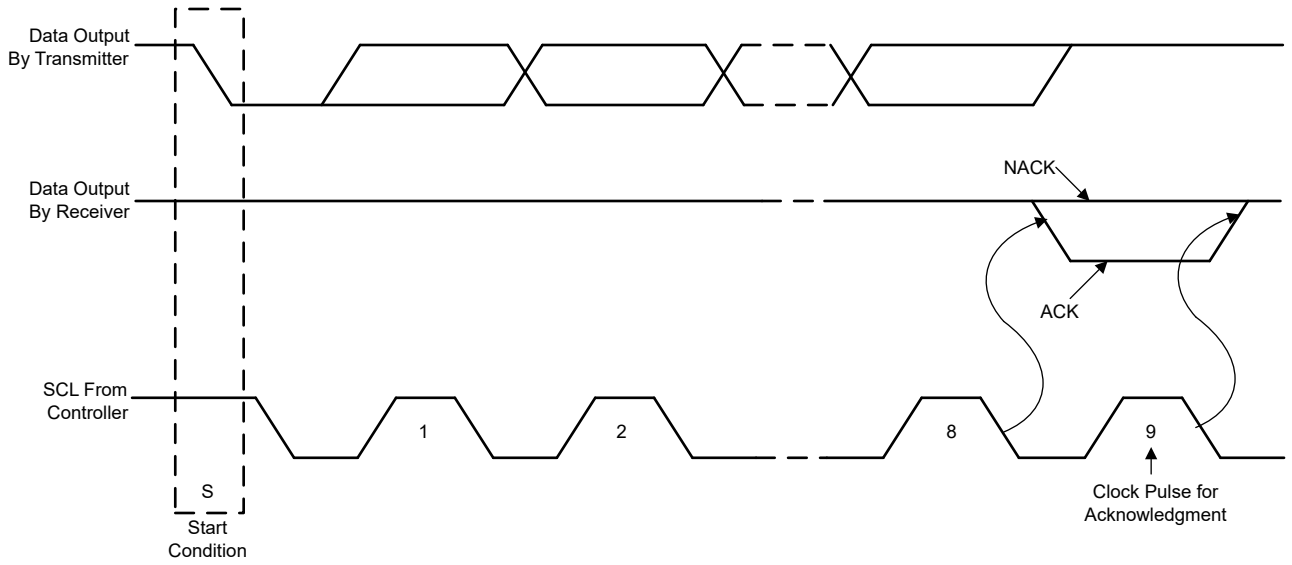

図 8-5. Acknowledgment on the I²C Bus

8.6 Register Maps

表 8-1 shows the PCA9536 interface definition.

表 8-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C target address	H	L	L	L	L	L	H	R/ $\overline{W}$
Px I/O data bus	Does not affect operation of the PCA9536				P3	P2	P1	P0
	P7	P6	P5	P4				

8.6.1 Device Address

図 8-6 shows the address byte of the PCA9536.

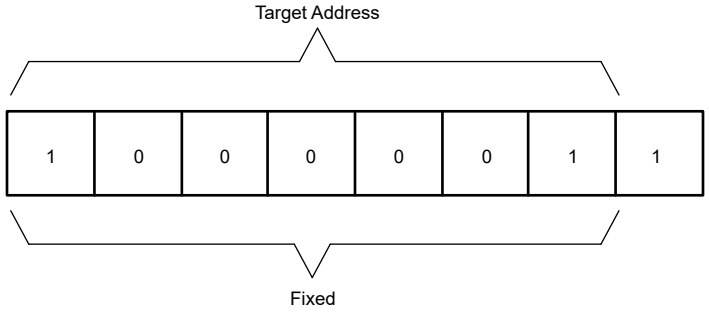

図 8-6. PCA9536 Address

The target address equates to 65 (decimal) and 41 (hexadecimal).

The last bit of the target address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

8.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the PCA9536. Two bits of this data byte state the operation (read or write) and

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the internal register (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the addressed register is continuosly accessed by reads until a new command byte is sent.

図 8-7 shows the PCA9536 control register bits and 表 8-2 shows the command byte.

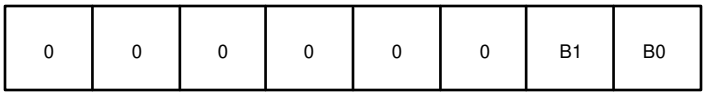

図 8-7. Control Register Bits

表 8-2. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0×00	Input Port	Read byte	1111 XXXX
0	1	0×01	Output Port	Read/write byte	1111 1111
1	0	0×02	Polarity Inversion	Read/write byte	0000 0000
1	1	0×03	Configuration	Read/write byte	1111 1111

8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level. See 表 8-3.

Before a read operation, a write transmission is sent with the command byte to instruct the I^2C device that the Input Port register will be accessed next.

表 8-3. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
	Not Used							
DEFAULT	1	1	1	1	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. The bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See 表 8-4.

表 8-4. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained. See 表 8-5.

表 8-5. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
	Not Used							
DEFAULT	0	0	0	0	0	0	0	0

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The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See 表 8-6.

表 8-6. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

8.6.4 Bus Transactions

Data is exchanged between the controller and PCA9536 through write and read commands.

8.6.4.1 Writes

Data is transmitted to the PCA9536 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see 図 8-8 and 図 8-9).

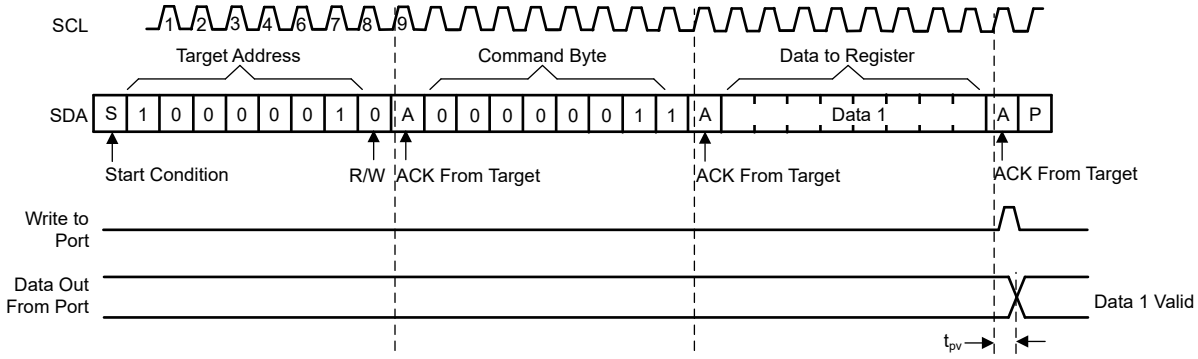

図 8-8. Write to Output Port Register

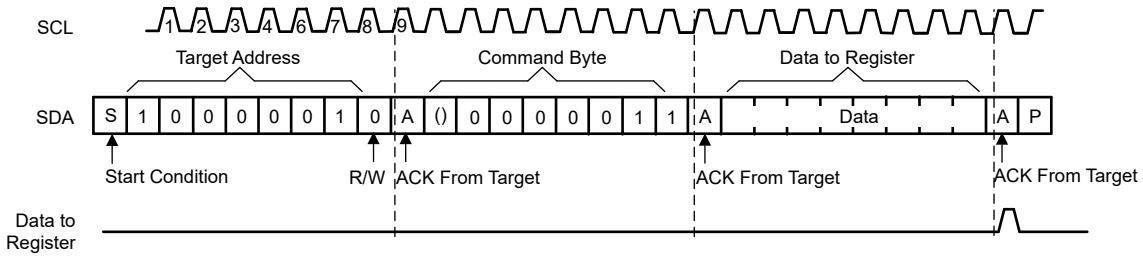

図 8-9. Write to Configuration or Polarity Inversion Registers

8.6.4.2 Reads

The bus controller first must send the PCA9536 address with the LSB set to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9536 (see 図 8-10 and 図 8-11). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus controller must not acknowledge the data.

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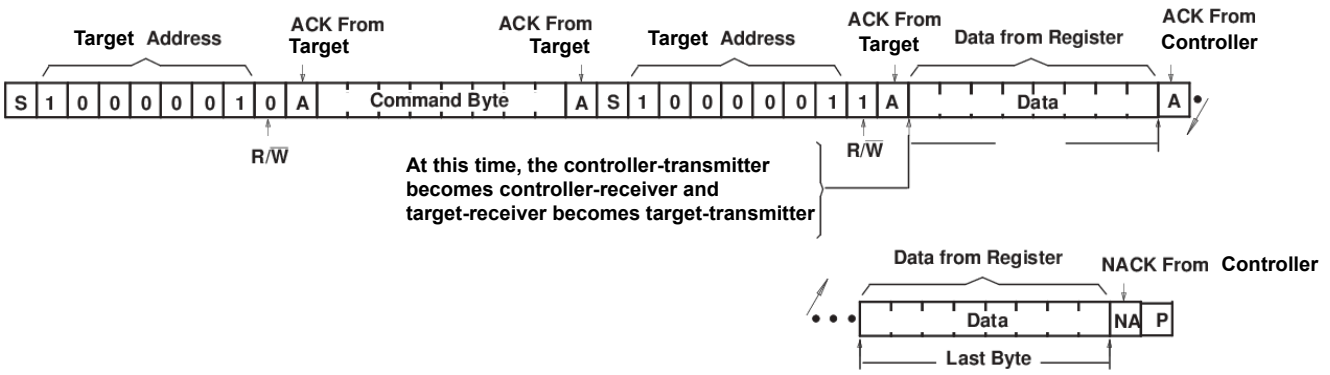
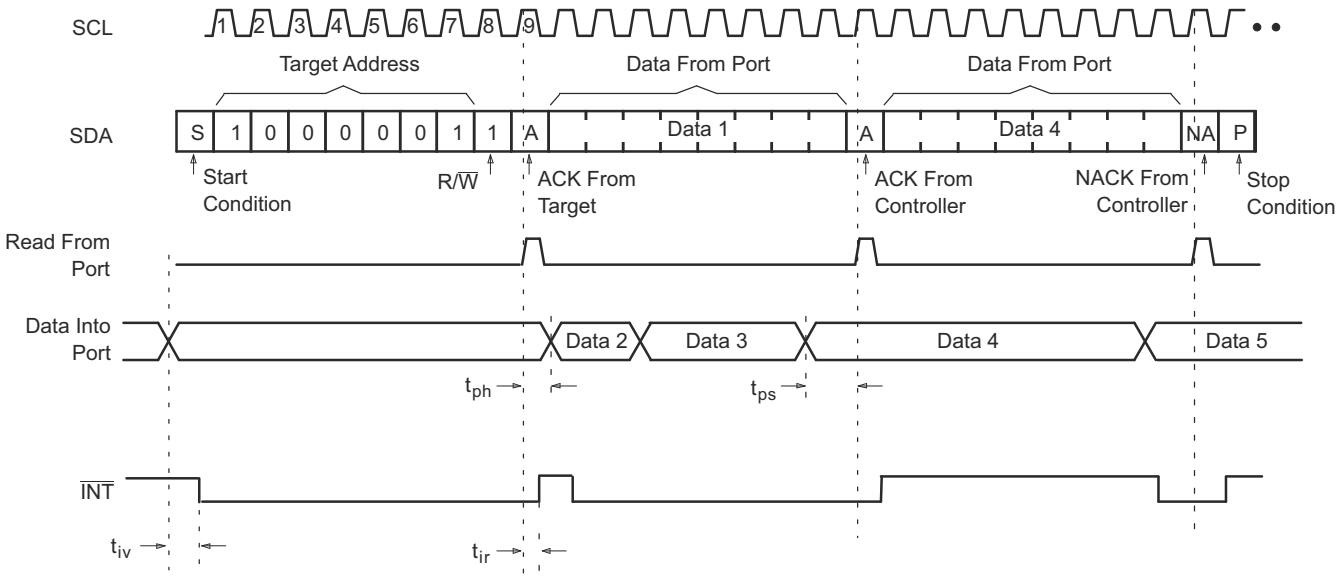


図 8-10. Read From Register



A. This figure assumes that the command byte previously has been programmed with 00h.
B. Transfer of data can be stopped at any moment by a Stop condition.
C. This figure eliminates the command byte transfer, a restart, and the target address call between the initial target address call and actual data transfer from the P-port (see 図 8-10).

図 8-11. Read Input Port Register

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9 Application Information Disclaimer

Note

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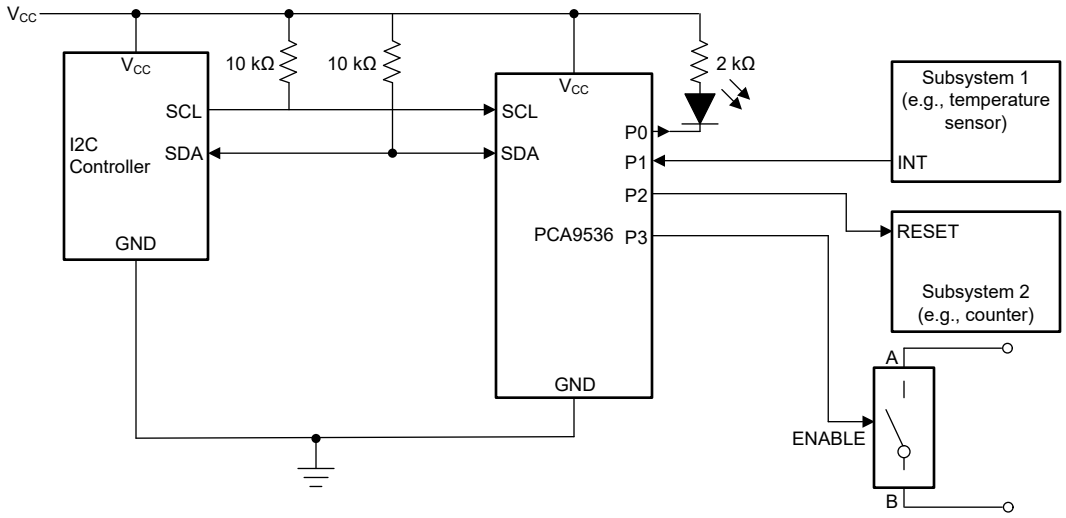
9.1 Application Information

9.2 Typical Application

図 9-1 shows an application in which the PCA9536 can be used.



A. Device address is 10000001.
B. P0, P2, and P3 are configured as outputs.
C. P1 is configured as an input.

図 9-1. Typical Application

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in 図 9-1. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off. 図 9-2 shows a high-value resistor in parallel with the LED. 図 9-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

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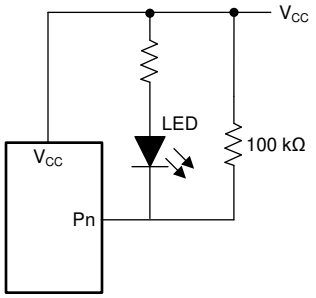

図 9-2. High-Value Resistor in Parallel with the LED

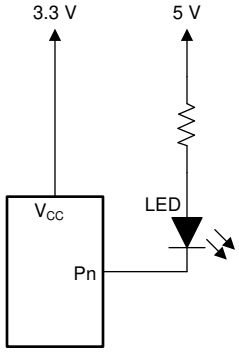

図 9-3. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in 式 1:

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in 式 2:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9536, C_i for SCL or C_{io} for SDA, the capacitance of wires,connections or traces, and the capacitance of additional targets on the bus.

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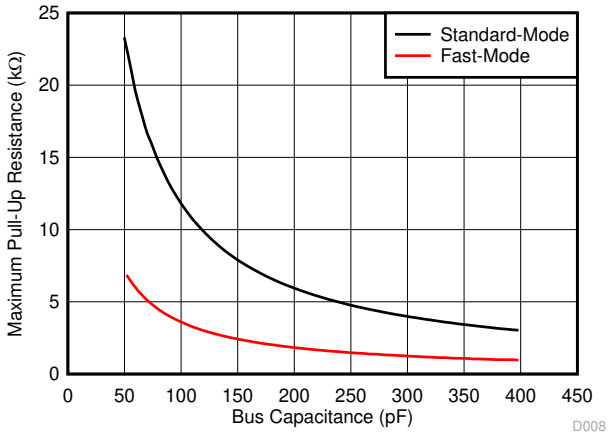
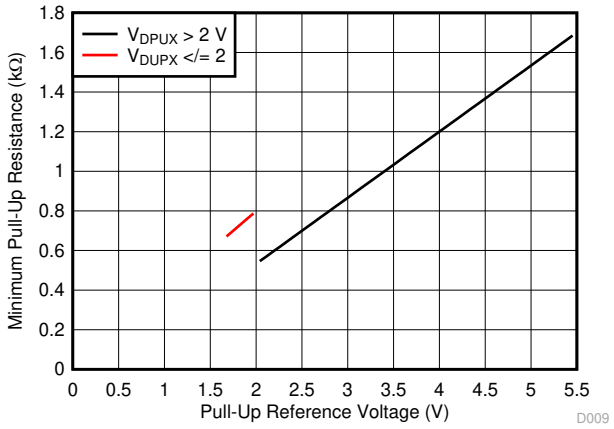
9.2.3 Application Curves



Standard-mode: f_{SCL} = 100 kHz, t_r = 1 µs

Fast-mode: f_{SCL} = 400 kHz, t_r = 300 ns

図 9-4. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

図 9-5. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-up Reference Voltage (V_{CC})

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10 Power Supply Recommendations

10.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed in 図 10-1.

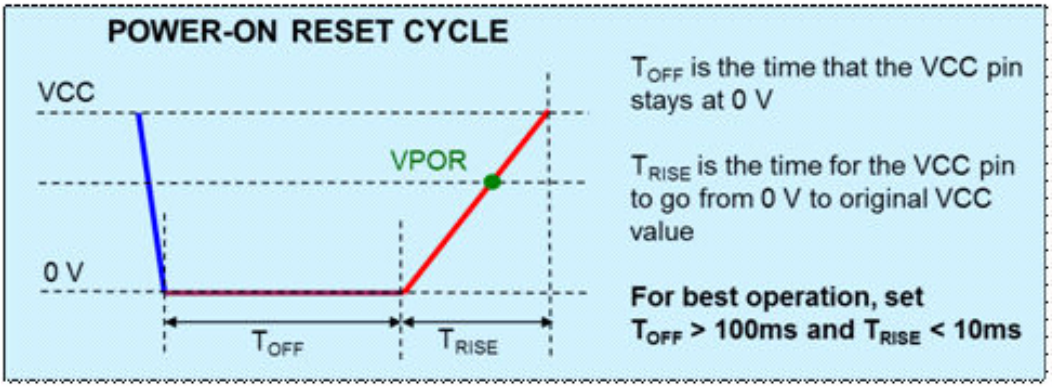

図 10-1. Power-On Reset Cycle

10.2 System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

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11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCA9536, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the PCA9536 as possible.

For the layout example provided, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a 4-layer board is preferable for boards with higher density signal routing. On a 4-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated.

11.2 Layout Example

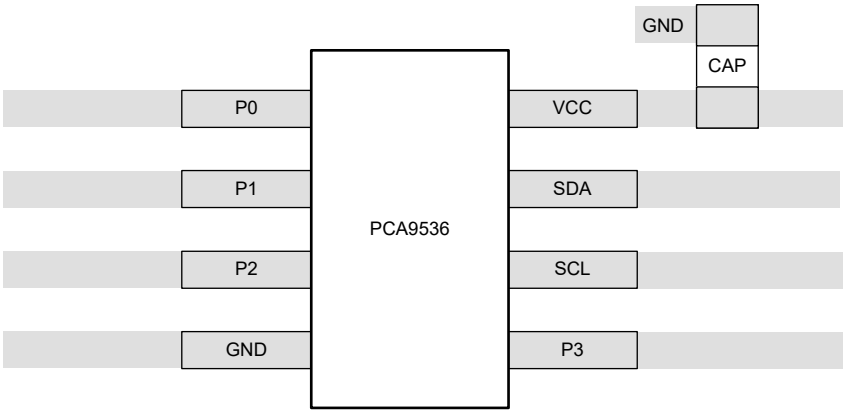

図 11-1. Layout Example (DGK)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *I2C Bus Pull-Up Resistor Calculation*
- *Maximum Clock Frequency of I2C Bus Using Repeaters*
- *Introduction to Logic*
- *Understanding the I2C Bus*
- *Choosing the Correct I2C Device for New Designs*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9536D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	PD536	
PCA9536DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7CF, 7CL)	Samples
PCA9536DGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7CF, 7CL)	Samples
PCA9536DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples
PCA9536DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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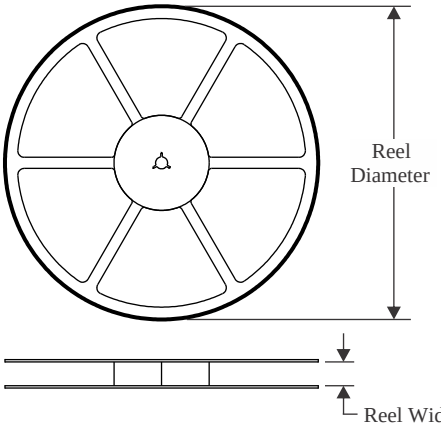
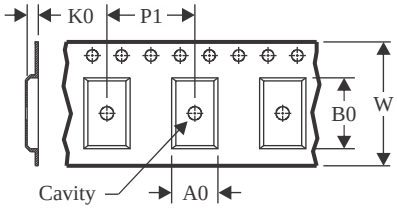
TAPE AND REEL INFORMATION

REEL DIMENSIONS

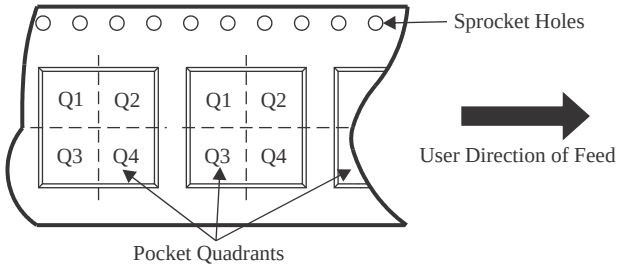


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

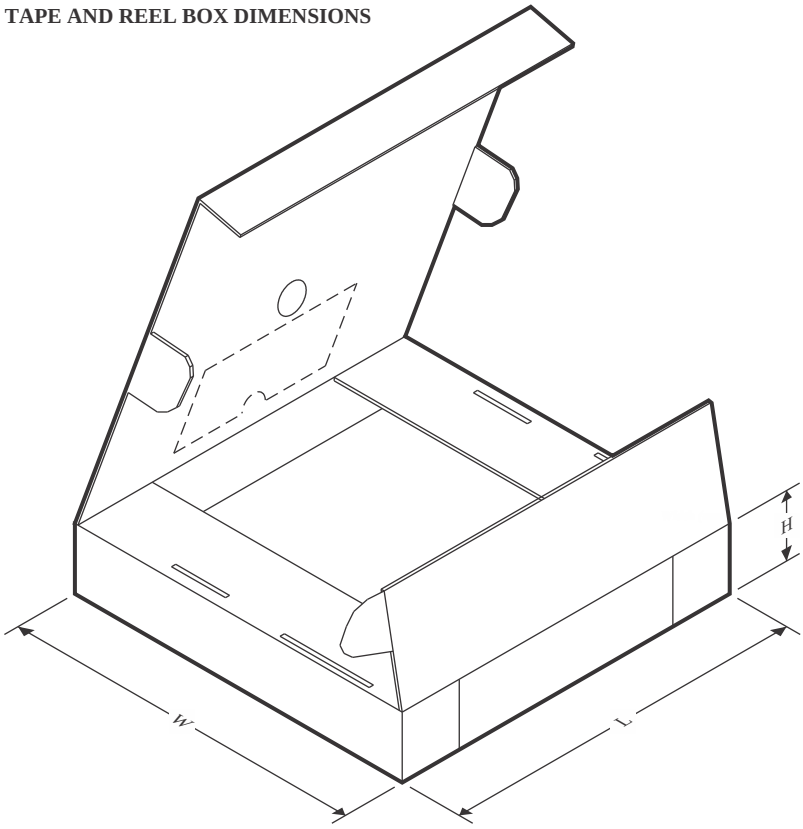
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

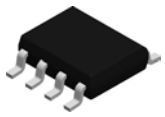
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9536DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
PCA9536DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9536DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
PCA9536DR	SOIC	D	8	2500	356.0	356.0	35.0

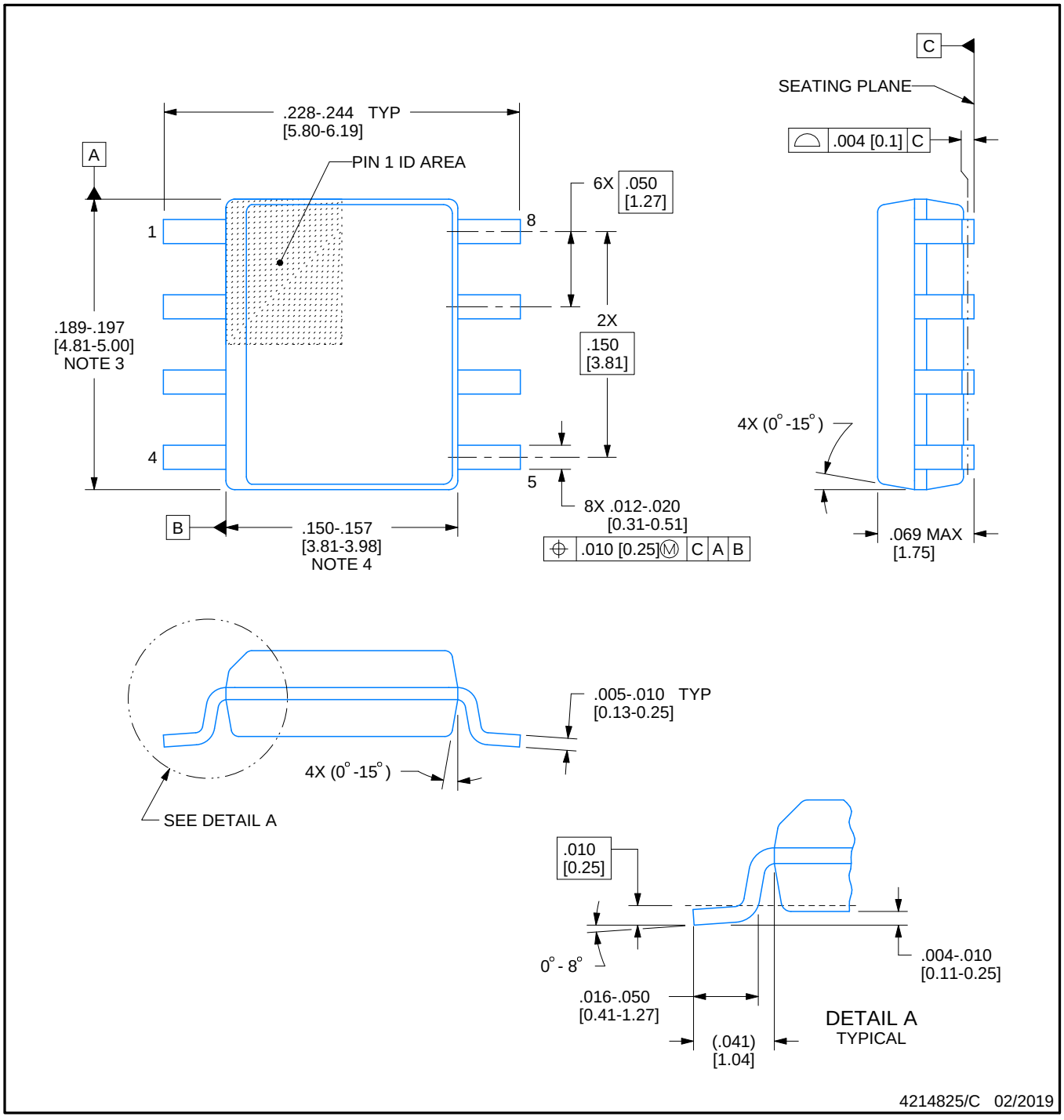


PACKAGE OUTLINE

D0008A

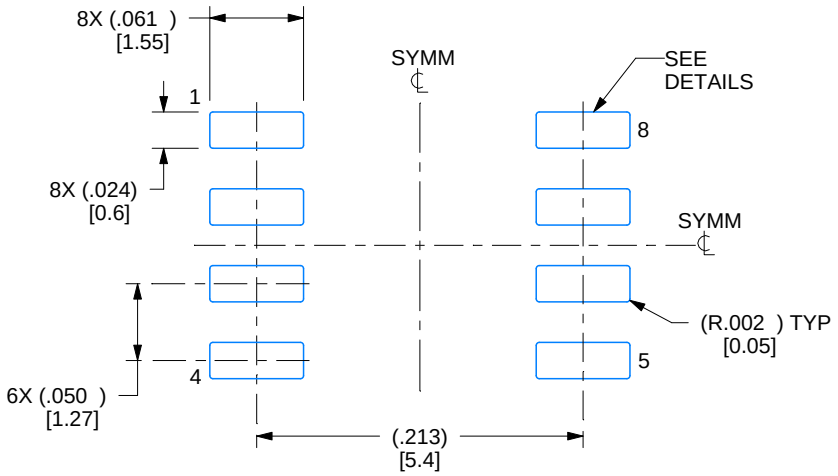
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

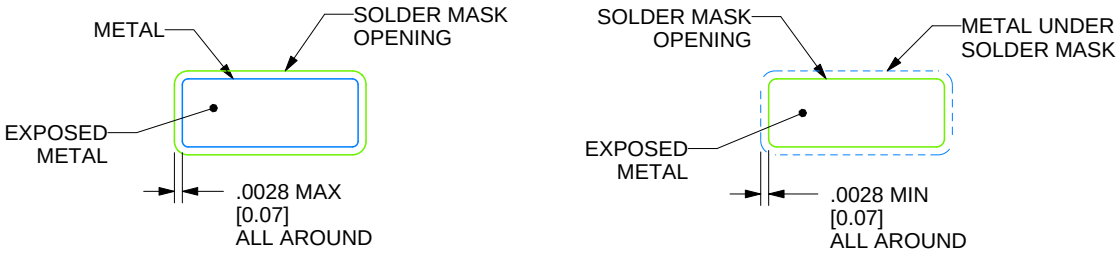


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

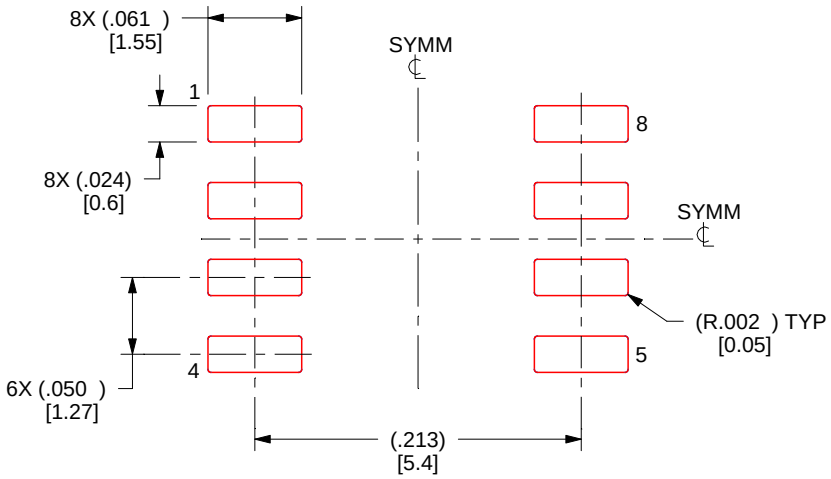
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

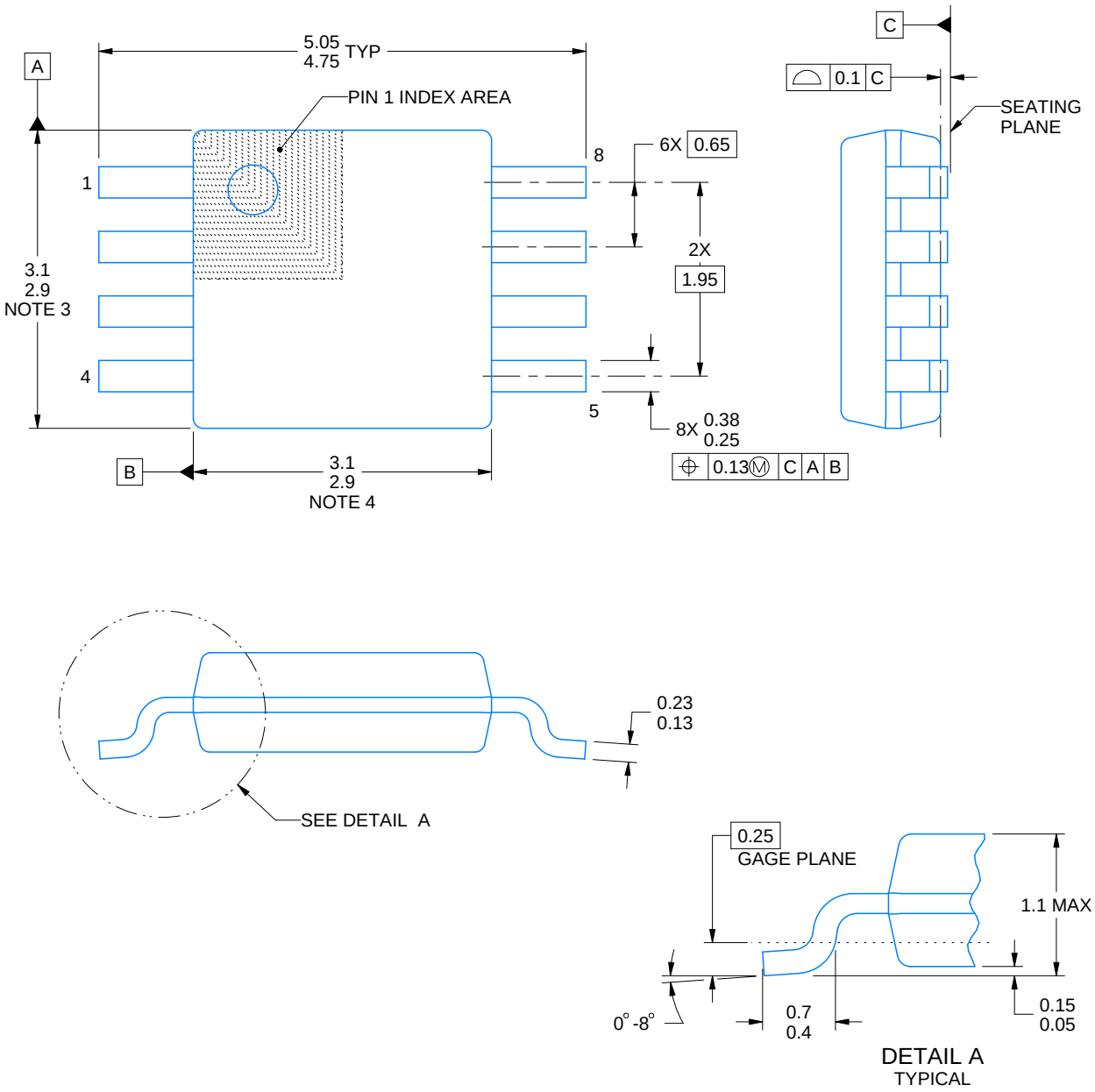
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

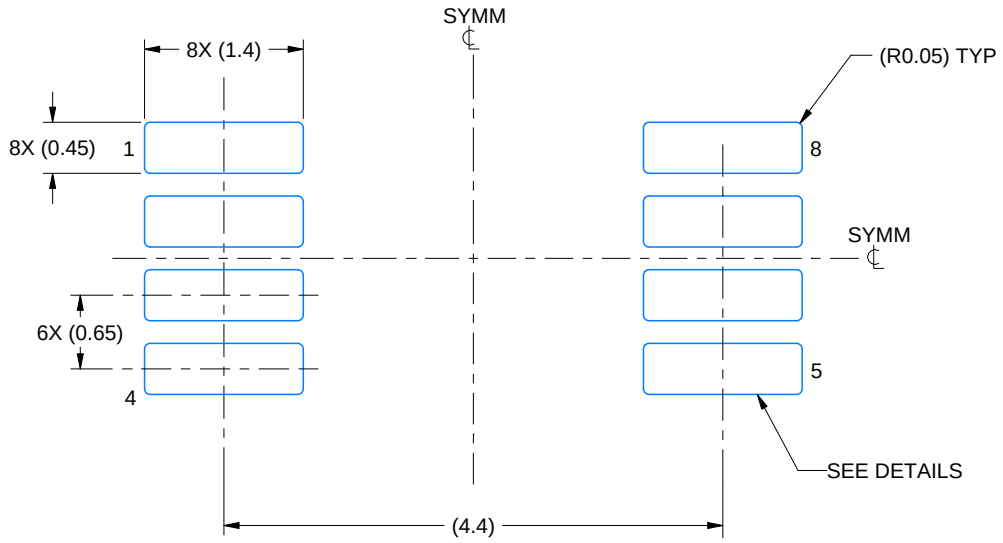
SMALL OUTLINE PACKAGE



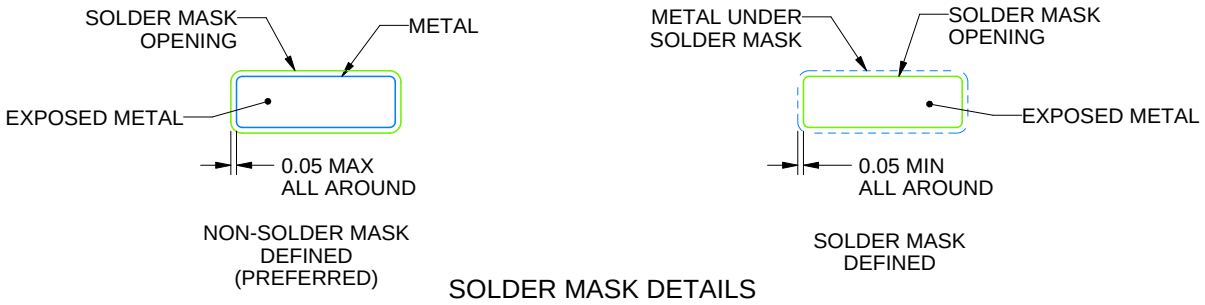
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

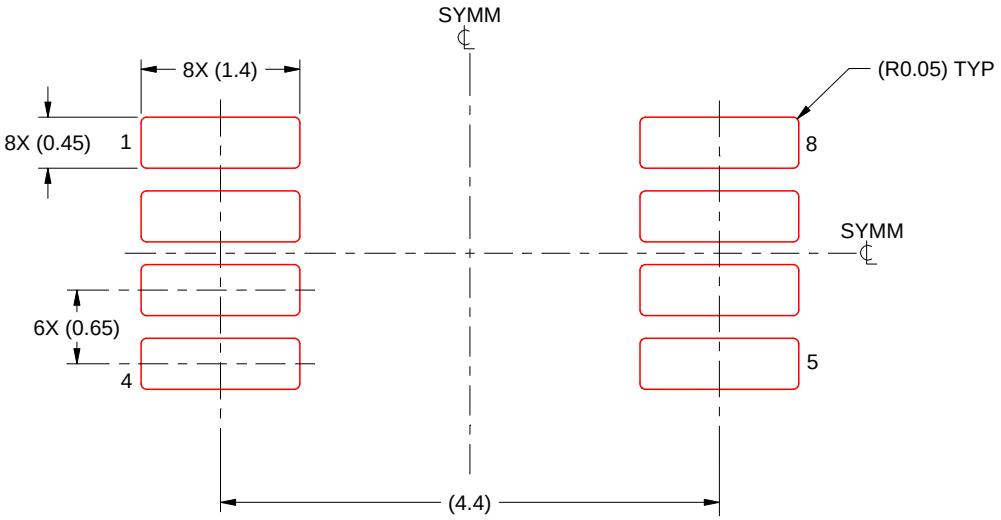


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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