

## PCF8574A リモート 8 ビット I/O エクスパンダ、I<sup>2</sup> バス対応

### 1 特長

- 低いスタンバイ時消費電流: 10 $\mu$ A 以下
- I<sup>2</sup>C からパラレル・ポートへのエクスパンダ
- オープンドレイン割り込み出力
- ほとんどのマイクロコントローラと互換
- 大電流の駆動能力を持つラッチ付き出力により、LED を直接駆動
- JESD 78, Class II 準拠で 100mA 超のラッチアップ性能

### 2 アプリケーション

- テレコム・シェルター: フィルタ・ユニット
- サーバー
- ルーター (テレコム・スイッチング機器)
- パーソナル・コンピュータ
- パーソナル・エレクトロニクス
- 産業用オートメーション
- GPIO が制限されたプロセッサを使用する製品

### 3 概要

この 8 ビット I/O エクスパンダは 2 線式双方向バス (I<sup>2</sup>C) 用で、2.5V~6V の V<sub>CC</sub> で動作するように設計されています。

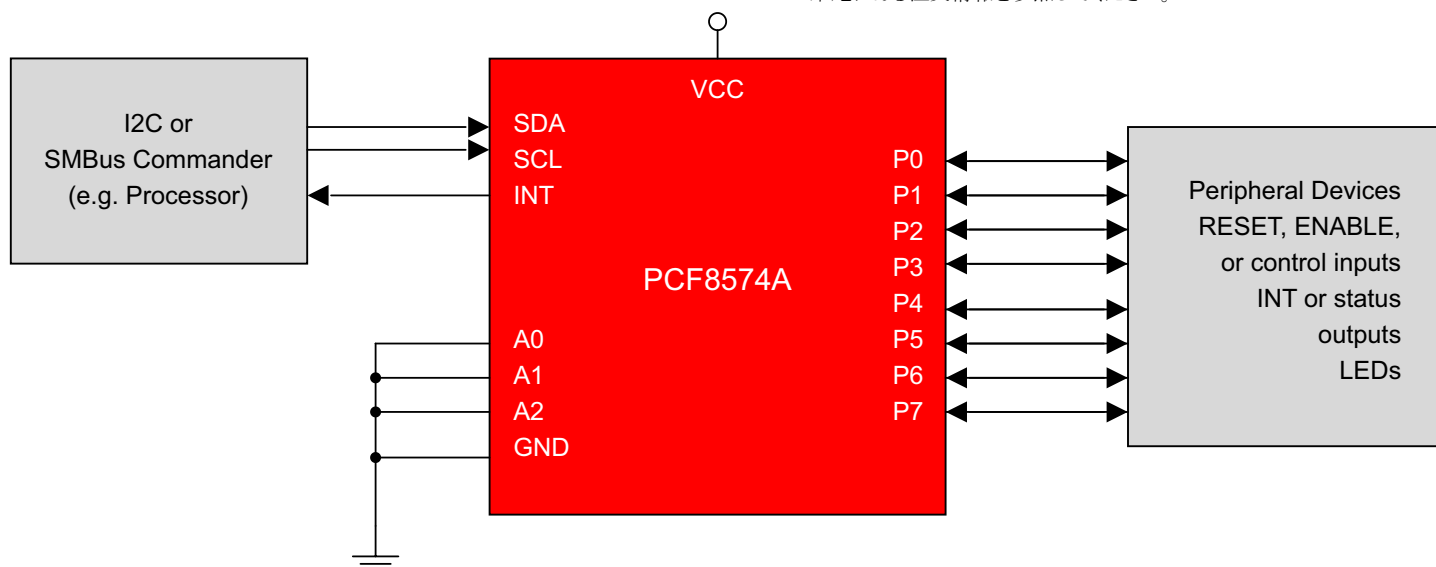
PCF8574A デバイスは、I<sup>2</sup>C インターフェイス [シリアル・クロック (SCL)、シリアル・データ (SDA)] により、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張に使用できます。

このデバイスには 8 ビット、疑似双方向の I/O ポート (P0~P7) があり、大電流駆動能力を持つラッチ付き出力により LED を直接駆動できます。それぞれの疑似双方向 I/O は、データ方向制御信号を使用せずに、入力または出力として使用できます。電源投入時、I/O は HIGH になります。このモードでは、V<sub>CC</sub> への電流源のみがアクティブになります。

#### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
PCF8574A	VQFN (20)	4.50mm × 3.50mm
	PDIP (16)	19.30mm × 6.35mm
	SOIC (16)	10.30mm × 7.50mm
	TSSOP (20)	6.50mm × 4.40mm
	TVSOP (20)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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## 4 Revision History

Changes from Revision F (January 2015) to Revision G (August 2021)	Page
• 旧式の用語を使用している場合、文書全体にわたってコマンドおよびレスポンドに変更.....	1
• Changed the <i>Thermal Information</i> table.....	5
• Changed <a href="#">☒ 7-2</a> Responder address from: S0100 To: S0111.....	9
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• Changed Note B from: configured as 0100000to: configured as 0111000.....	16
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• Added Junction temperature to the <i>Absolute Maximum Ratings</i> .....	4
• Changed Supply Current (A) To: Supply Current (μA) and f <sub>SCL</sub> = 400 kHz to f <sub>SCL</sub> = 100 kHz in <a href="#">☒ 6-1</a> .....	7
• Changed Supply Current (A) To: Supply Current (μA) in <a href="#">☒ 6-2</a> .....	7
• Changed Supply Current (A) To: Supply Current (μA) and f <sub>SCL</sub> = 400 kHz to f <sub>SCL</sub> = 100 kHz in <a href="#">☒ 6-3</a> .....	7
Changes from Revision D (October 2005) to Revision E (January 2015)	Page
• 「アプリケーション」セクション、「製品情報」表、「端子機能」表、「ESD 定格」表、「熱に関する情報」表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• 「注文情報」表を削除.....	1

## 5 Pin Configuration and Functions

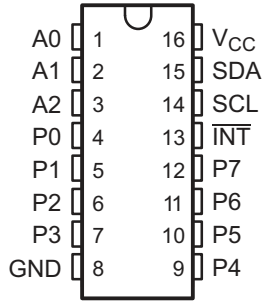


图 5-1. DW or N Package 16 Pins Top View

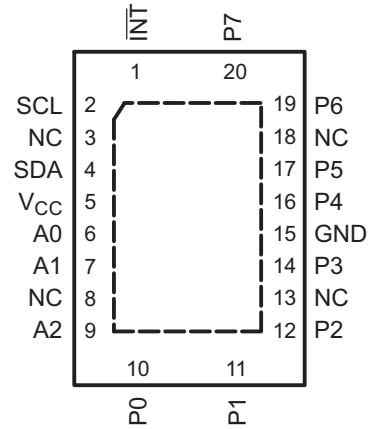


图 5-2. RGY Package 20 Pins Top View

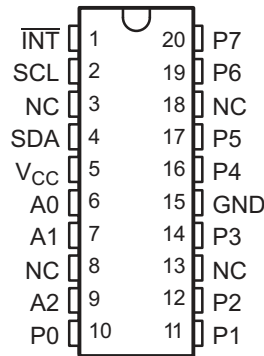


图 5-3. DGV or PW Package 20 Pins Top View

表 5-1. Pin Functions

NAME	PIN			TYPE	DESCRIPTION
	RGY	DGV or PW	DW or N		
A[0..2]	6, 7, 9	6, 7, 9	1, 2, 3	I	Address inputs 0 through 2. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.
GND	15	15	8	—	Ground
INT	1	1	13	O	Interrupt output. Connect to V <sub>CC</sub> through a pullup resistor.
NC	3, 8, 13, 18	3, 8, 13, 18	-	—	Do not connect
P[0..7]	10, 11, 12, 14, 16, 17, 19, 20	10, 11, 12, 14, 16, 17, 19, 20	4, 5, 6, 7, 9, 10, 11, 12	I/O	P-port input/output. Push-pull design structure.
SCL	2	2	14	I	Serial clock line. Connect to V <sub>CC</sub> through a pullup resistor
SDA	4	4	15	I/O	Serial data line. Connect to V <sub>CC</sub> through a pullup resistor.
V <sub>CC</sub>	5	5	16	—	Voltage supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-20	mA
I <sub>OK</sub>	Input/output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±400	µA
I <sub>OL</sub>	Continuous output low current	V <sub>O</sub> = 0 to V <sub>CC</sub>	50	mA
I <sub>OH</sub>	Continuous output high current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-4	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.5	6	V
V <sub>IH</sub>	High-level input voltage	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Low-level input voltage	-0.5	0.3 × V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-1	mA
I <sub>OL</sub>	Low-level output current		25	mA
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PCF8574					UNIT
		DGV	DW	N	PW	RGY	
		20 PINS	16 PINS	16 PINS	20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	112.2	79.7	48.3	99.5	41.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	35.2	42.5	35.6	34.5	42.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.4	44.4	28.2	50.5	16.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	14.8	20.5	2.0	0.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.8	43.8	28.1	49.9	16.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	2.5 V to 6 V	-1.2			V
V <sub>POR</sub>	Power-on reset voltage <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	6 V		1.3	2.4	V
I <sub>OH</sub>	P port	V <sub>O</sub> = GND	2.5 V to 6 V	30		300	μA
I <sub>OHT</sub>	P-port transient pullup current	High during acknowledge, V <sub>OH</sub> = GND	2.5 V		-1		mA
I <sub>OL</sub>	SDA	V <sub>O</sub> = 0.4 V	2.5 V to 6 V	3			mA
	P port	V <sub>O</sub> = 1 V	5 V	10	25		
	INT	V <sub>O</sub> = 0.4 V	2.5 V to 6 V	1.6			
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V			±5	μA
	INT					±5	
	A0, A1, A2					±5	
I <sub>IHL</sub>	P port	V <sub>I</sub> ≥ V <sub>CC</sub> or V <sub>I</sub> ≤ GND	2.5 V to 6 V			±400	μA
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 100 kHz	6 V		40	100	μA
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0			2.5	10	
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V		1.5	7	pF
C <sub>io</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The power-on reset circuit resets the I<sup>2</sup>C-bus logic with V<sub>CC</sub> < V<sub>POR</sub> and sets all I/Os to logic high (with current source to V<sub>CC</sub>).

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#))

		MIN	MAX	UNIT
f <sub>scl</sub>	I <sup>2</sup> C clock frequency		100	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		100	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1	μs
t <sub>icf</sub>	I <sup>2</sup> C input fall time		0.3	μs
t <sub>ocf</sub>	I <sup>2</sup> C output fall time (10-pF to 400-pF bus)		300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	4		μs
t <sub>sps</sub>	I <sup>2</sup> C stop-condition setup	4		μs
t <sub>vd</sub>	Valid-data time	SCL low to SDA output valid		3.4 μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF

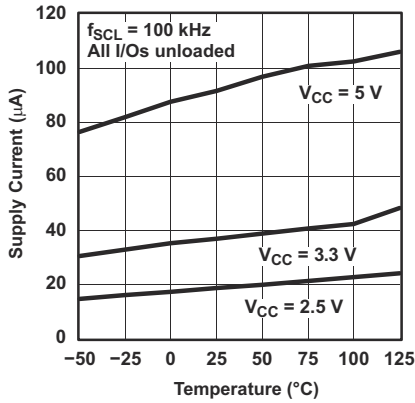
## 6.7 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see [7-2](#))

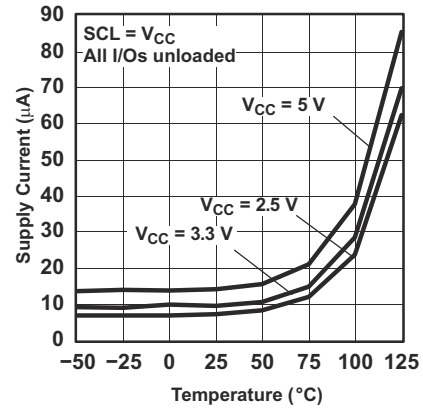
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pv</sub>	Output data valid	SCL		4	μs
t <sub>su</sub>	Input data setup time	P port	0		μs
t <sub>h</sub>	Input data hold time	P port	4		μs
t <sub>iv</sub>	Interrupt valid time	P port		4	μs
t <sub>ir</sub>	Interrupt reset delay time	SCL		4	μs

## 6.8 Typical Characteristics

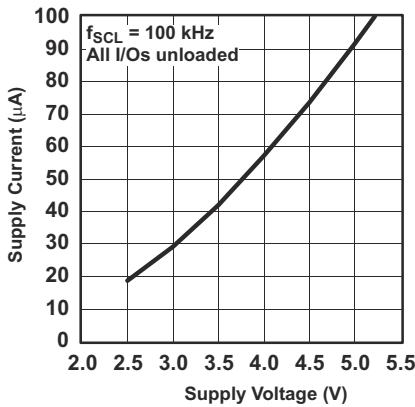
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



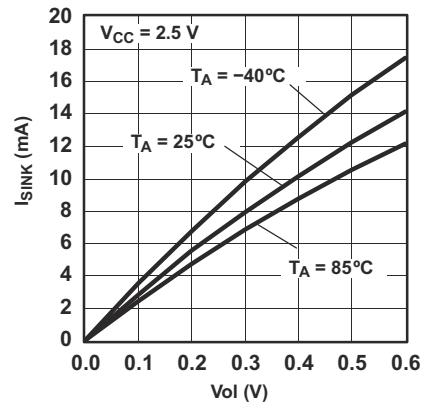
6-1. Supply Current vs Temperature



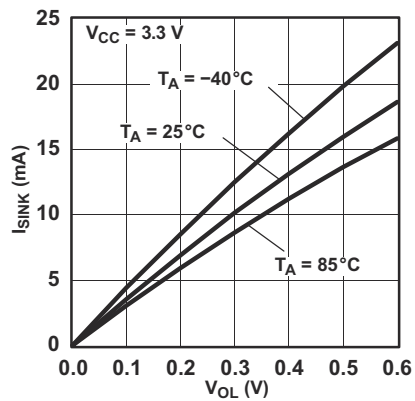
6-2. Standby Supply Current vs Temperature



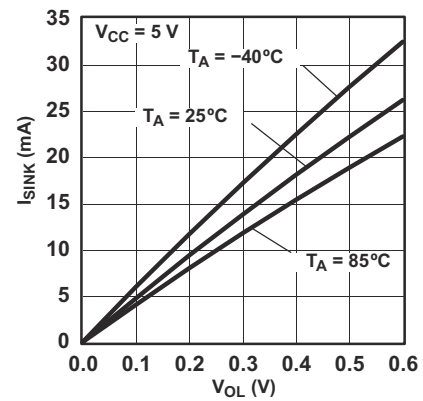
6-3. Supply Current vs Supply Voltage



6-4. I/O Sink Current vs Output Low Voltage



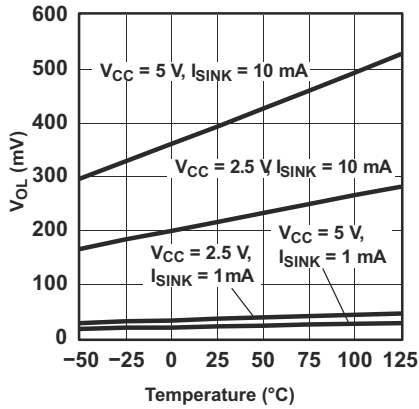
6-5. I/O Sink Current vs Output Low Voltage



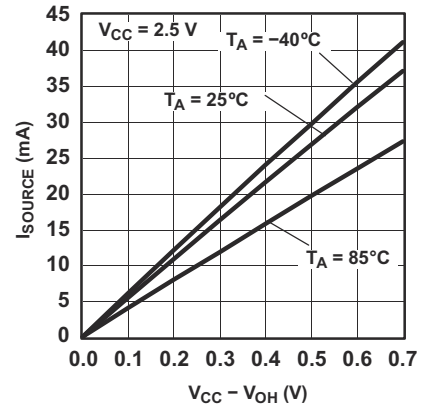
6-6. I/O Sink Current vs Output Low Voltage

## 6.8 Typical Characteristics (continued)

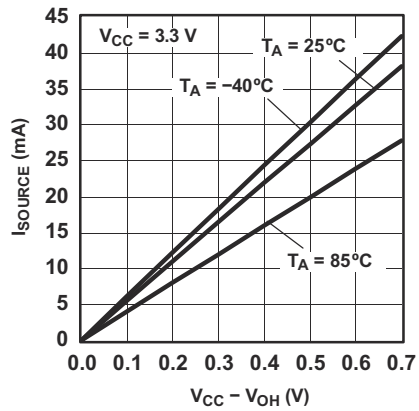
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



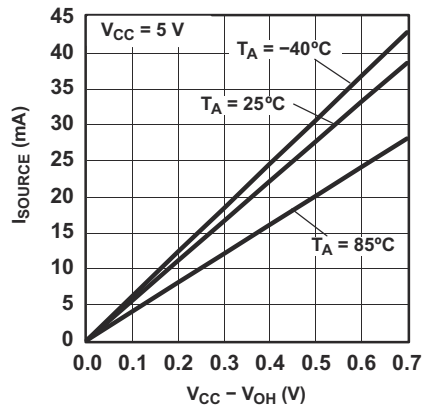
6-7. I/O Output Low Voltage vs Temperature



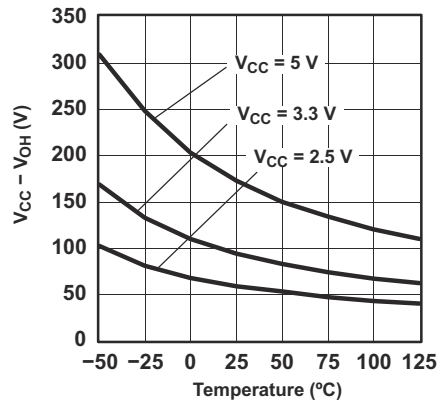
6-8. I/O Source Current vs Output High Voltage



6-9. I/O Source Current vs Output High Voltage



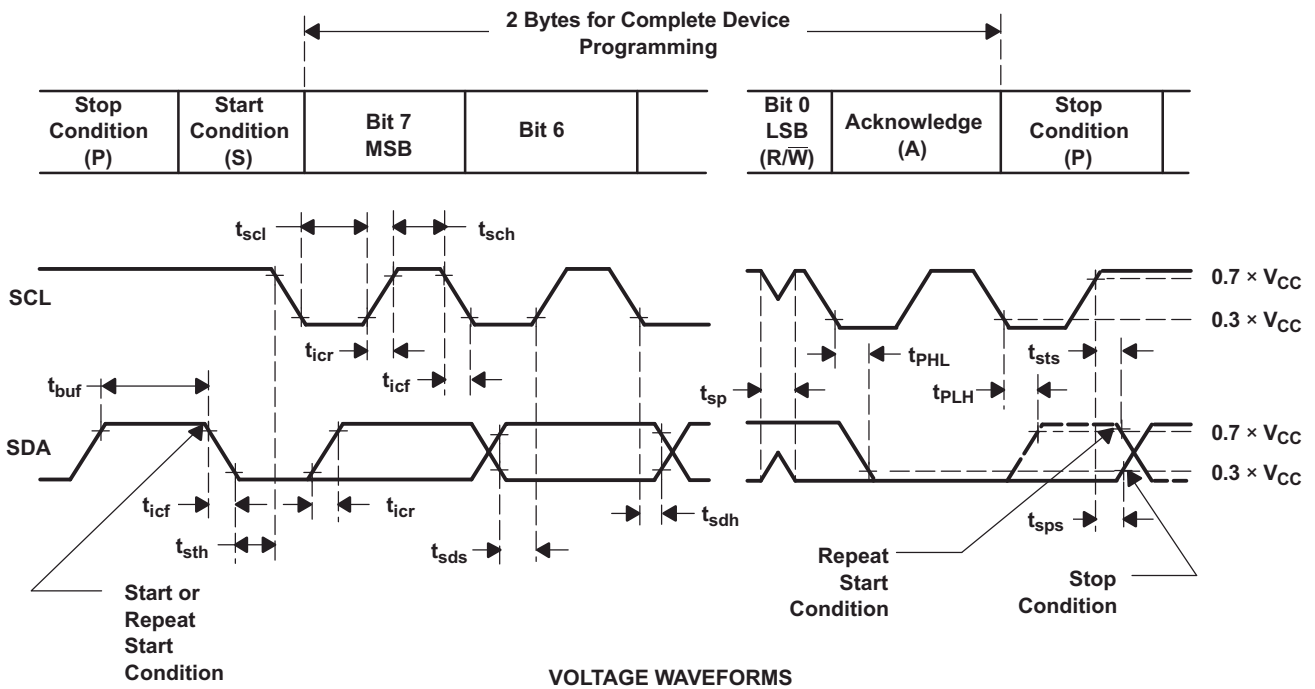
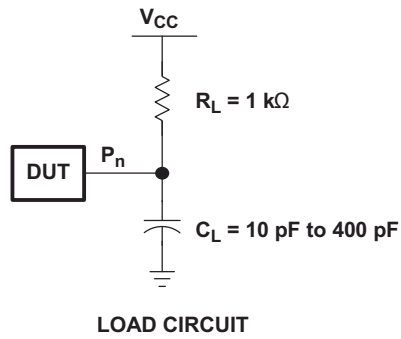
6-10. I/O Source Current vs Output High Voltage



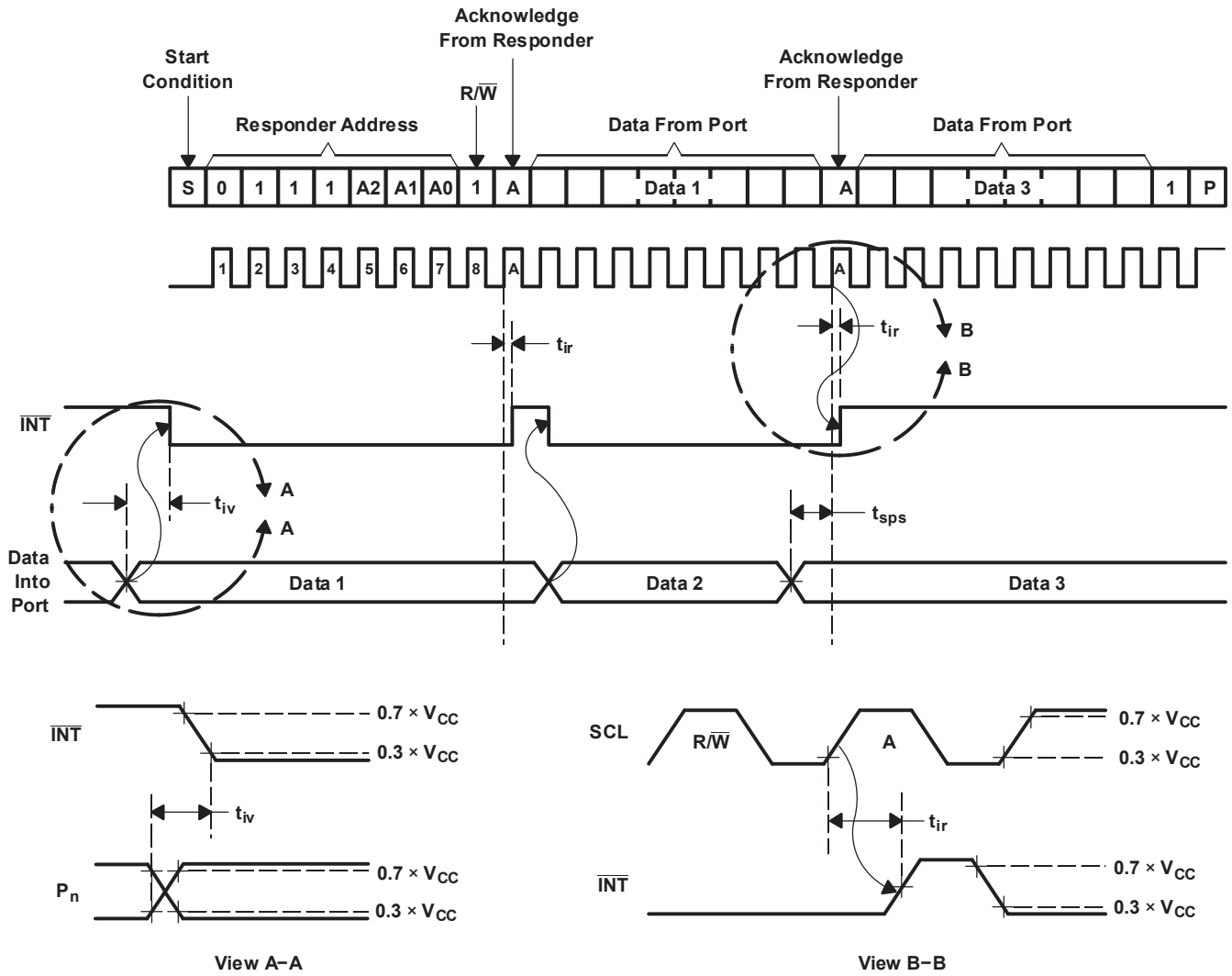
6-11. I/O High Voltage vs Temperature



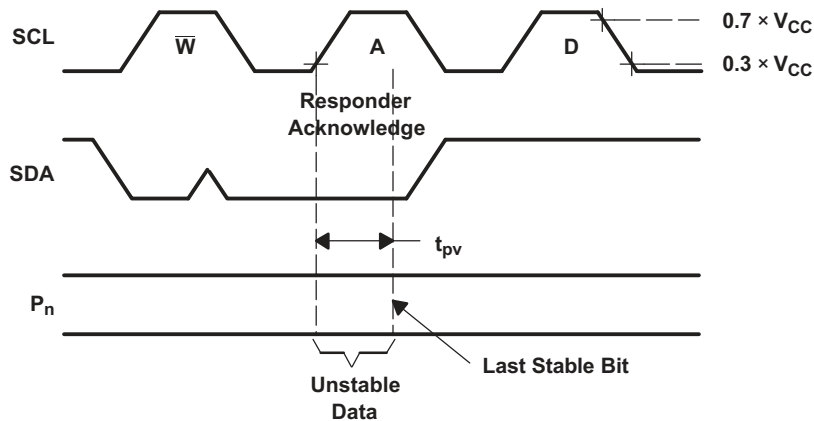
## 7 Parameter Measurement Information



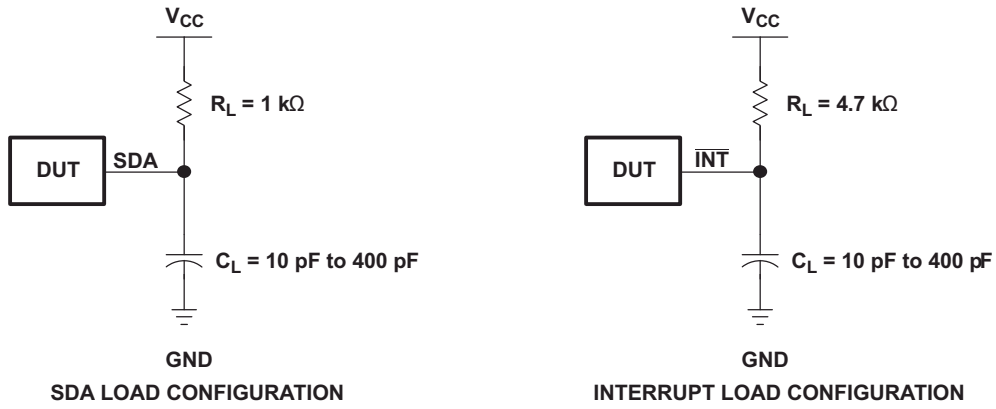
7-1. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms



7-2. Interrupt Voltage Waveforms



7-3. I<sup>2</sup>C Write Voltage Waveforms



7-4. Load Circuits

## 8 Detailed Description

### 8.1 Overview

The PCF8574A device provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

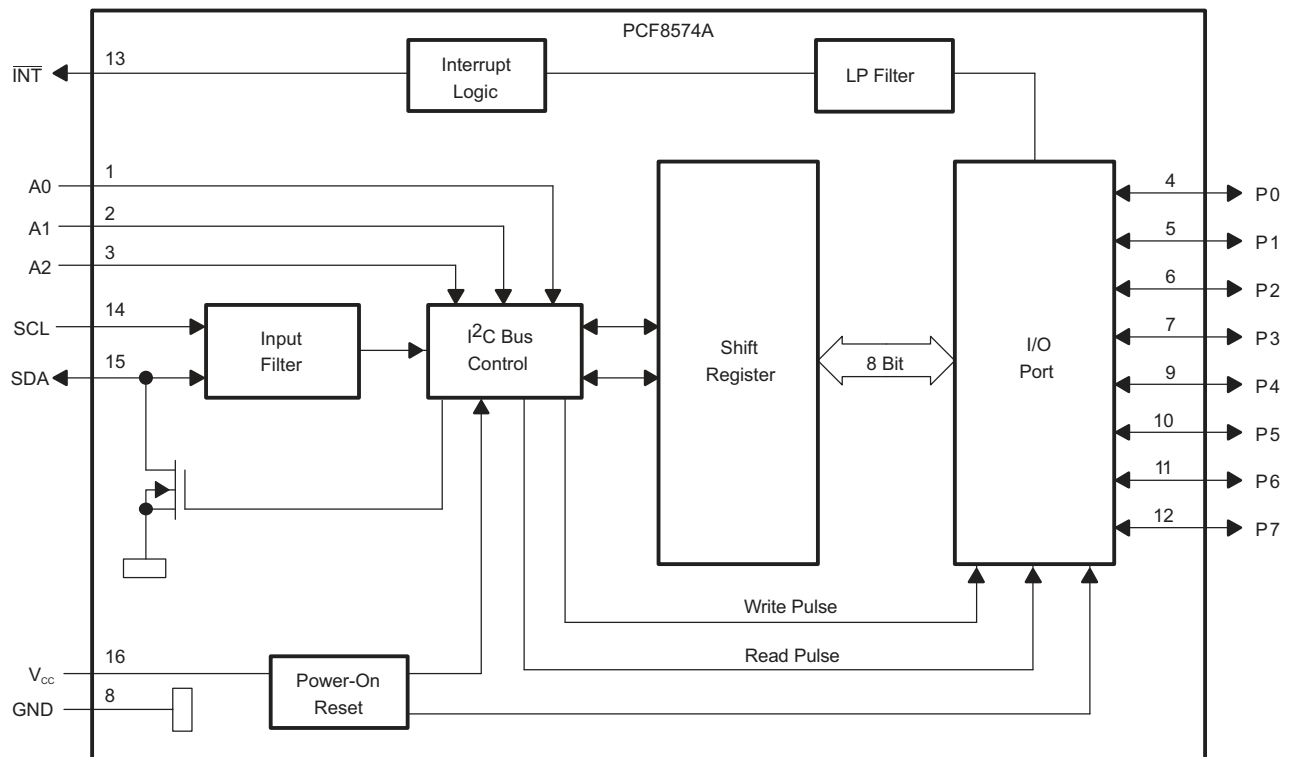
The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V<sub>CC</sub> is active. An additional strong pullup to V<sub>CC</sub> allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

The PCF8574A device provides an open-drain output (  $\overline{\text{INT}}$  ) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time,  $t_{iv}$ ,  $\overline{\text{INT}}$  is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal, or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as  $\overline{\text{INT}}$ . Reading from, or writing to, another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Therefore, the PCF8574A device can remain a simple responder device.

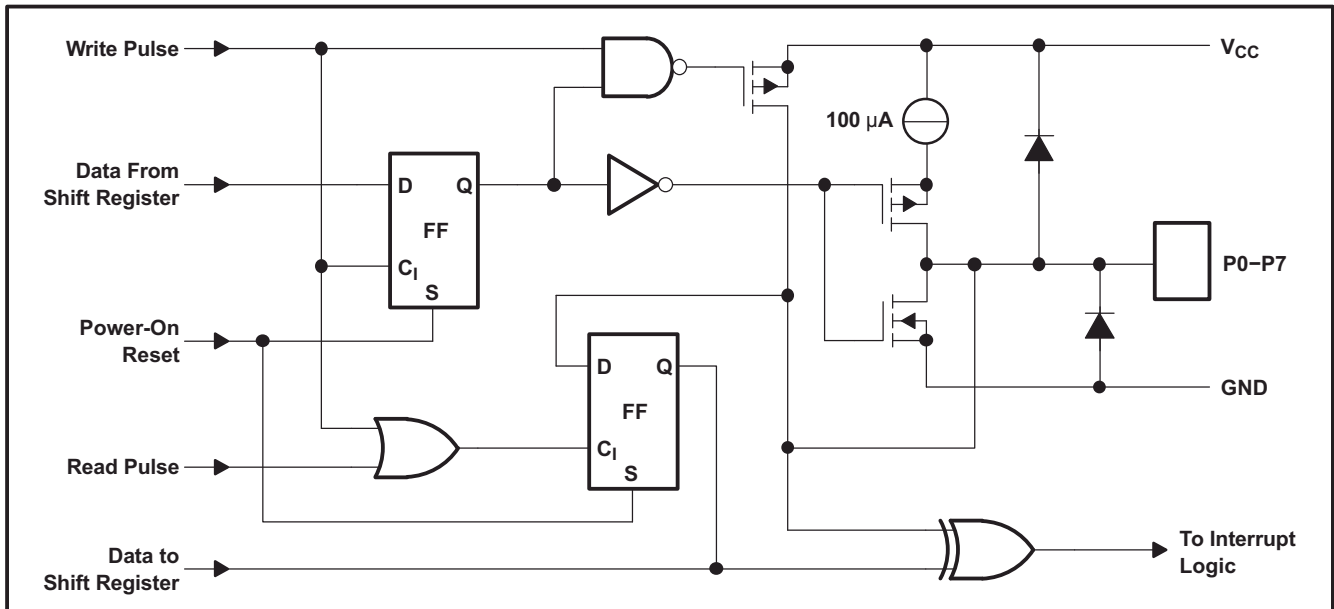
### 8.2 Functional Block Diagram

#### 8.2.1 Simplified Block Diagram of Device



Pin numbers shown are for the DW and N packages.

## 8.2.2 Simplified Schematic Diagram of Each P-Port Input/Output



## 8.3 Feature Description

### 8.3.1 I<sup>2</sup>C Interface

I<sup>2</sup>C communication with this device is initiated by a commander sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit ( $R/\bar{W}$ ). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the responder device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the  $R/\bar{W}$  bit is high, the data from this device are the values read from the P port. If the  $R/\bar{W}$  bit is low, the data are from the commander, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the commander, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time,  $t_{pv}$ , after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the commander.

### 8.3.2 Interface Definition

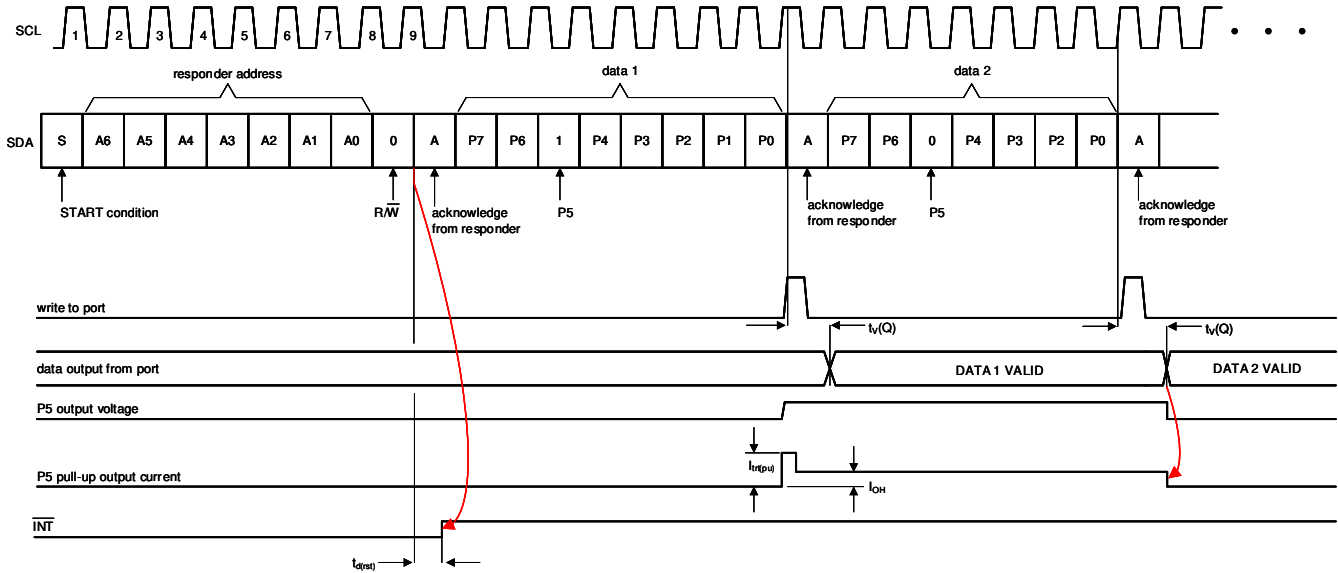
BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C responder address	L	H	H	H	A2	A1	A0	$R/\bar{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

### 8.3.3 Address Reference

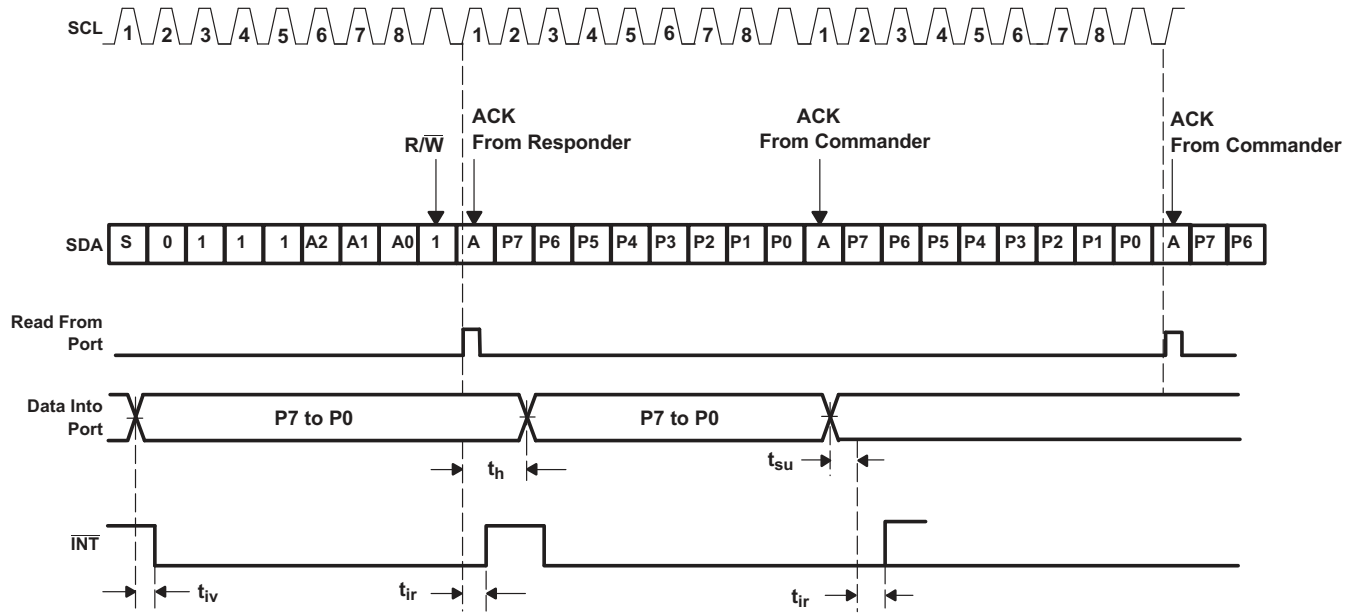
INPUTS			I <sup>2</sup> C BUS responder 8-BIT READ ADDRESS	I <sup>2</sup> C BUS responder 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	113 (dec), 71 (hex)	112 (dec), 70 (hex)
L	L	H	115 (dec), 73 (hex)	114 (dec), 72 (hex)
L	H	L	117 (dec), 75 (hex)	116 (dec), 74 (hex)
L	H	H	119 (dec), 77 (hex)	118 (dec), 76 (hex)
H	L	L	121 (dec), 79 (hex)	120 (dec), 78 (hex)
H	L	H	123 (dec), 7B (hex)	122 (dec), 7A (hex)
H	H	L	125 (dec), 7D (hex)	124 (dec), 7C (hex)
H	H	H	127 (dec), 7F (hex)	126 (dec), 7E (hex)

### 8.4 Device Functional Modes

☒ 8-1 and ☒ 8-2 show the address and timing diagrams for the write and read modes, respectively.



☒ 8-1. Write Mode (Output)



- A. A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

### 8-2. Read Mode (Input)

## 9 Application Information Disclaimer

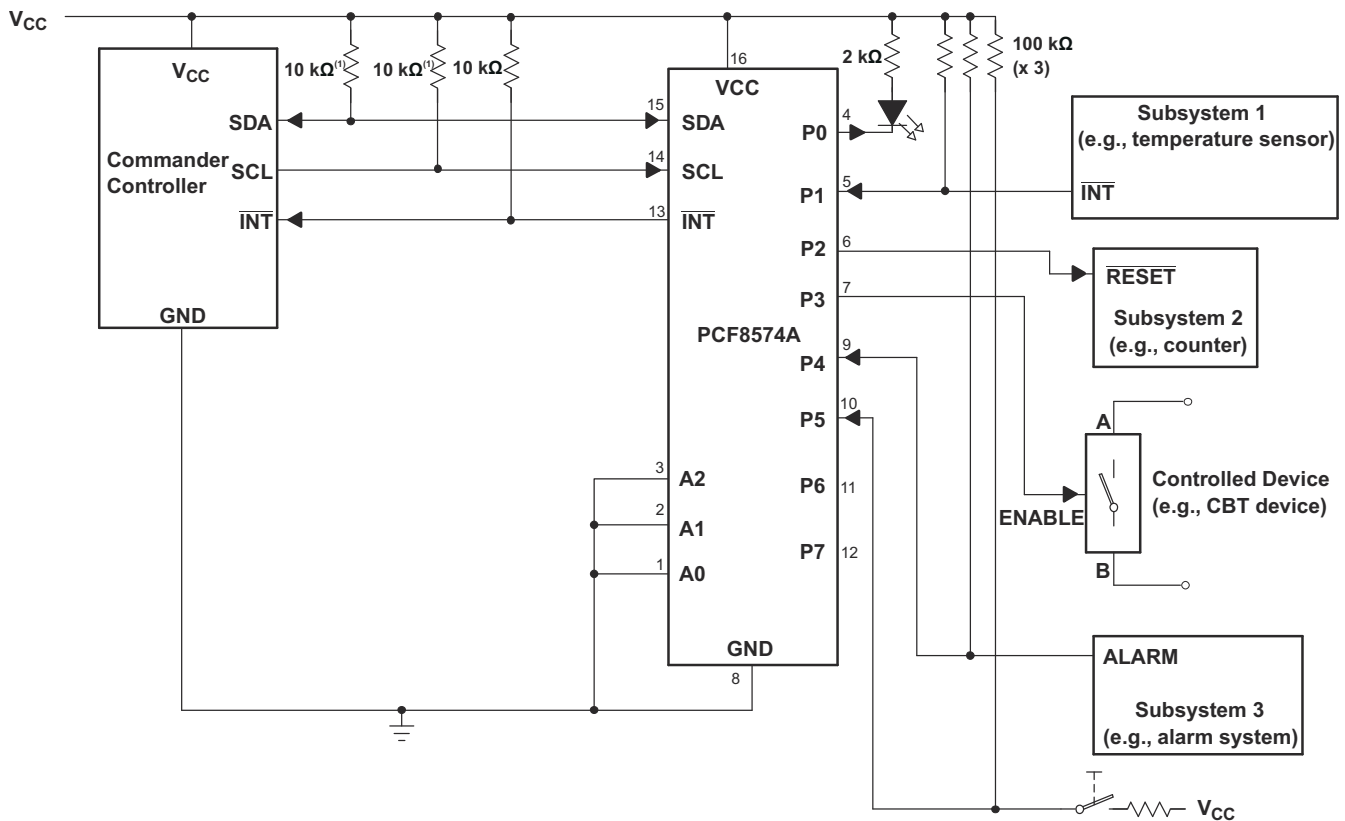
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

Figure 9-1 shows an application in which the PCF8574A device can be used.

### 9.2 Typical Application



- The SCL and SDA pins must be pulled up to V<sub>CC</sub> because if SCL and SDA are pulled up to an auxiliary power supply that could be powered on while V<sub>CC</sub> is powered off, then the supply current, I<sub>CC</sub>, will increase as a result.
- Device address is configured as 0111000 for this example.
- P0, P2, and P3 are configured as outputs.
- P1, P4, and P5 are configured as inputs.
- P6 and P7 are not used and must be configured as outputs.

Figure 9-1. Application Schematic

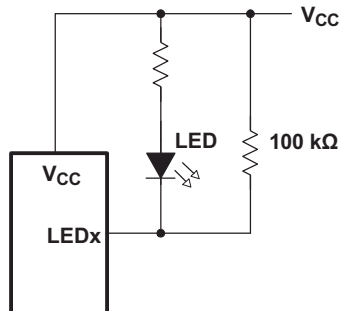


## 9.2.1 Design Requirements

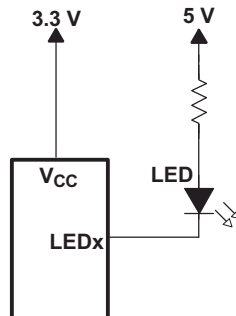
### 9.2.1.1 Minimizing $I_{CC}$ When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to  $V_{CC}$  through a resistor as shown in [Figure 11-1](#). For a P-port configured as an input,  $I_{CC}$  increases as  $V_I$  becomes lower than  $V_{CC}$ . The LED is a diode, with threshold voltage  $V_T$ , and when a P-port is configured as an input the LED will be off but  $V_I$  is a  $V_T$  drop below  $V_{CC}$ .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to  $V_{CC}$  when the P-ports are configured as input to minimize current consumption. [Figure 9-2](#) shows a high-value resistor in parallel with the LED. [Figure 9-3](#) shows  $V_{CC}$  less than the LED supply voltage by at least  $V_T$ . Both of these methods maintain the I/O  $V_I$  at or above  $V_{CC}$  and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.



**Figure 9-2. High-Value Resistor in Parallel With LED**



**Figure 9-3. Device Supplied by a Lower Voltage**

### 9.2.2 Detailed Design Procedure

The pull-up resistors,  $R_p$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all responders on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

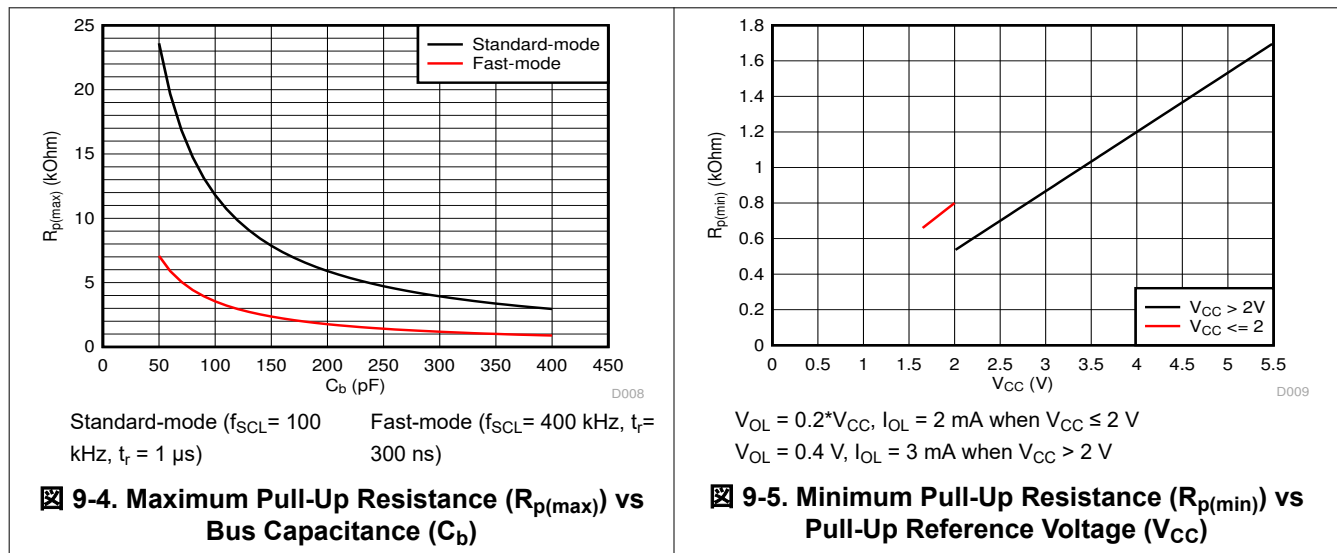
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL}$  = 400 kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8574A device,  $C_i$  for SCL or  $C_{i0}$  for SDA, the capacitance of wires/connections/traces, and the capacitance of additional responders on the bus.

### 9.2.3 Application Curves

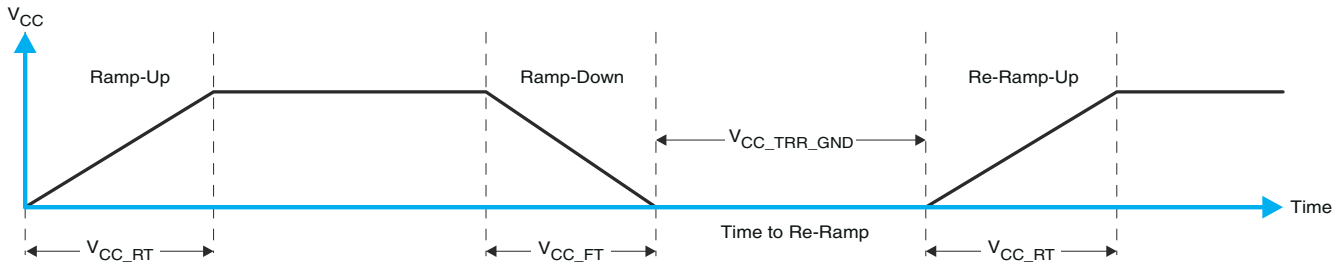


## 10 Power Supply Recommendations

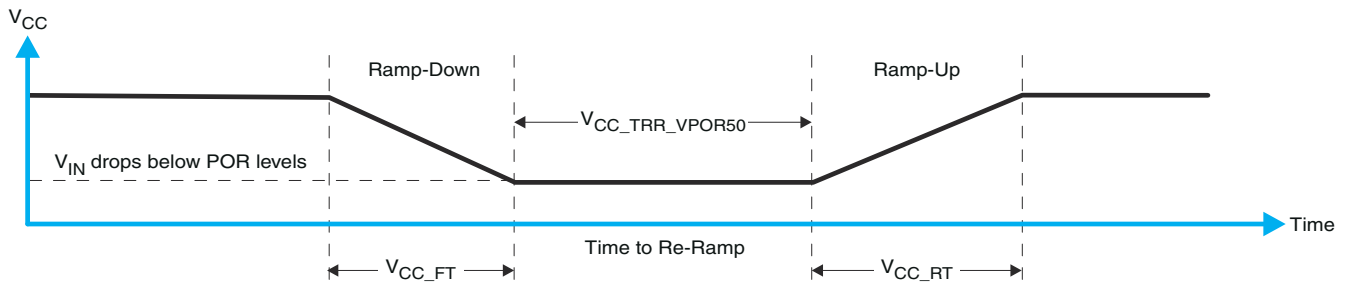
### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCF8574A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 10-1](#) and [Figure 10-2](#).



**Figure 10-1.  $V_{CC}$  is Lowered Below 0.2 V or 0 V and Then Ramped Up to  $V_{CC}$**



**Figure 10-2.  $V_{CC}$  is Lowered Below the POR Threshold, Then Ramped Back Up to  $V_{CC}$**

[Table 10-1](#) specifies the performance of the power-on reset feature for PCF8574A for both types of power-on reset.

**Table 10-1. Recommended Supply Sequencing and Ramp Rates<sup>(1)</sup>**

PARAMETER			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See <a href="#">Figure 10-1</a>	1		100	ms
$V_{CC\_RT}$	Rise rate	See <a href="#">Figure 10-1</a>	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when $V_{CC}$ drops to GND)	See <a href="#">Figure 10-1</a>	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV)	See <a href="#">Figure 10-2</a>	0.001			ms
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s	See <a href="#">Figure 10-3</a>			1.2	V
$V_{CC\_GW}$	Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCx}$	See <a href="#">Figure 10-3</a>				$\mu$ s
$V_{PORF}$	Voltage trip point of POR on falling $V_{CC}$		0.767		1.144	V
$V_{PORR}$	Voltage trip point of POR on rising $V_{CC}$		1.033		1.428	V

(1)  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 10-3](#) and [Table 10-1](#) provide more information on how to measure these specifications.

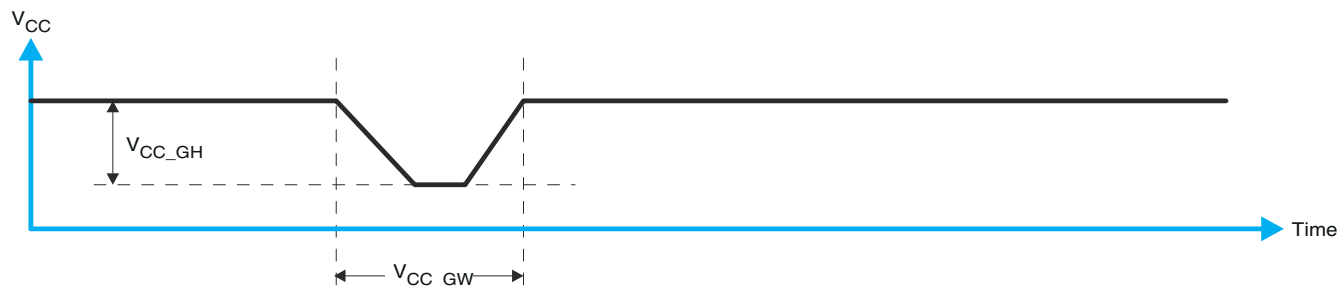


图 10-3. Glitch Width and Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. 图 10-4 和 表 10-1 provide more details on this specification.

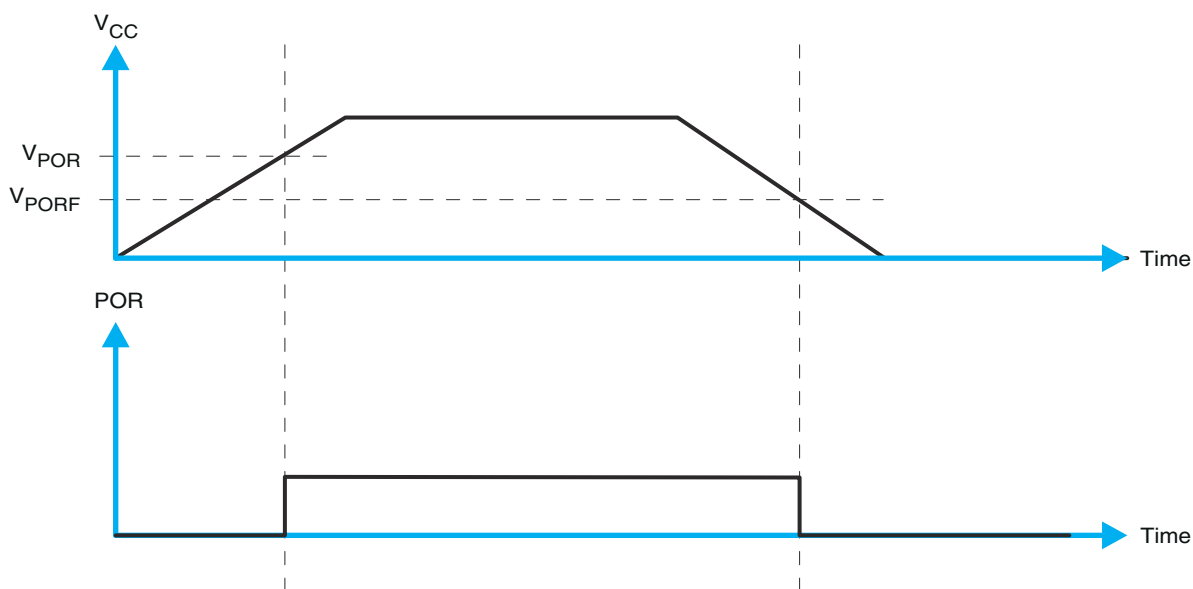


图 10-4.  $V_{POR}$

## 11 Layout

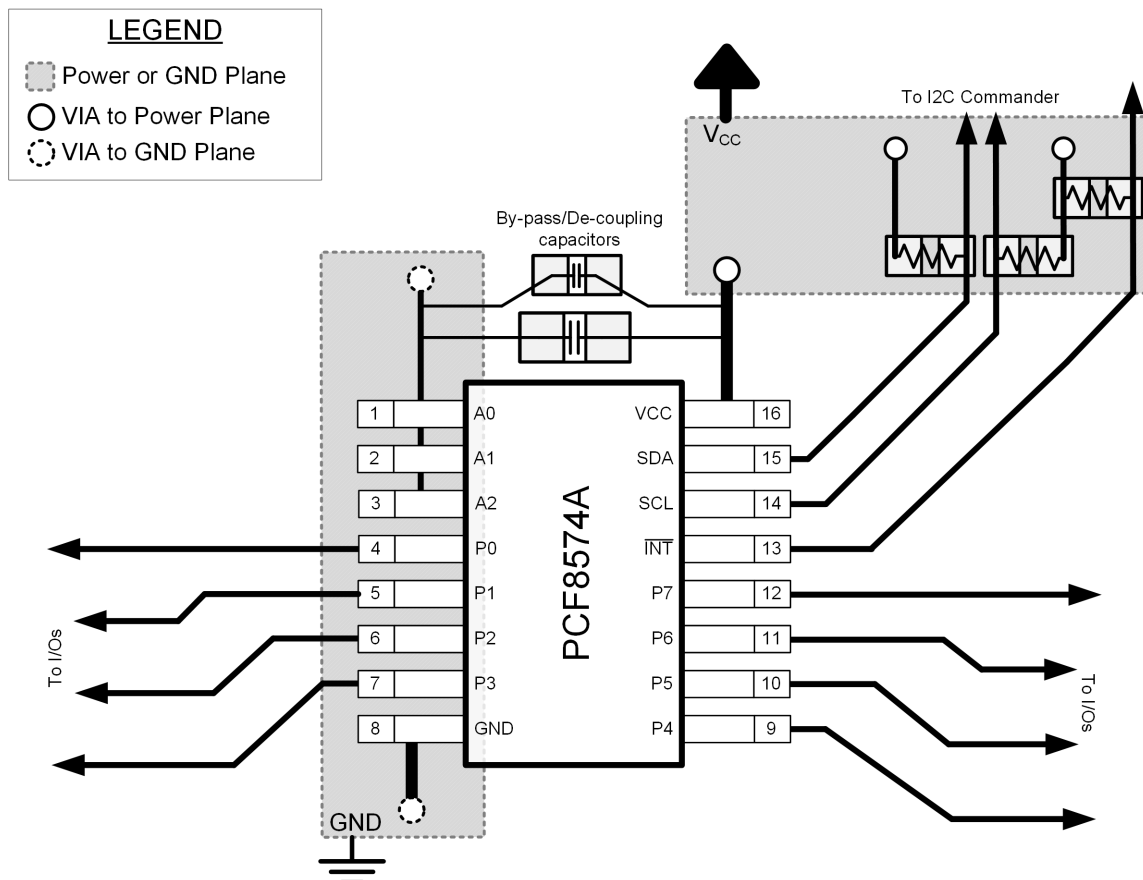
### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of PCF8574A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the  $V_{CC}$  pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8574A device as possible. These best practices are shown in [11-1](#).

For the layout example provided in [11-1](#), it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power ( $V_{CC}$ ) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to  $V_{CC}$  or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in [11-1](#).

### 11.2 Layout Example



**11-1. Layout Example for PCF8574A**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.6 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8574ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574ADWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	Samples
PCF8574AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574AN	Samples
PCF8574ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574AN	Samples
PCF8574APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8574ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8574ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCF8574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
PCF8574ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8574ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
PCF8574ADWR	SOIC	DW	16	2000	350.0	350.0	43.0
PCF8574APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
PCF8574ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
PCF8574AN	N	PDIP	16	25	506	13.97	11230	4.32
PCF8574ANE4	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0020A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

**RGY 20**

**VQFN - 1 mm max height**

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:18X



4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



DW0016A

# PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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