PGA280 ゼロドリフト、高電圧、プログラマブル・ゲイン計測アンプ

1 特長

- 広い入力範囲：±15.5V (±18V 電源の場合)
- バイナリ・ゲイン・ステップ：128V/V～1/8V/V
- 追加の倍率：1V/V および 1⅜V/V
- 小さいオフセット電圧：3µV (G = 128 の場合)
- オフセット電圧の長期的ドリフトがほぼゼロ
- ゲイン・ドリフトがほぼゼロ：0.5ppm/°C
- 優れた直線性：1.5ppm
- 優れた CMRR：140dB
- 高い入力インピーダンス
- 非常に小さい 1/f ノイズ
- 差動信号出力
- 過負荷検出
- 入力構成スイッチ・マトリクス
- 断線テスト電流
- 拡張可能な SPI™、チェックサム付き
- 汎用 I/O ポート
- TSSOP-24 パッケージ

2 アプリケーション

- アナログ入力モジュール
- データ・アクイジション (DAQ)
- 航空機のエンジン制御
- バッテリ試験装置

3 概要

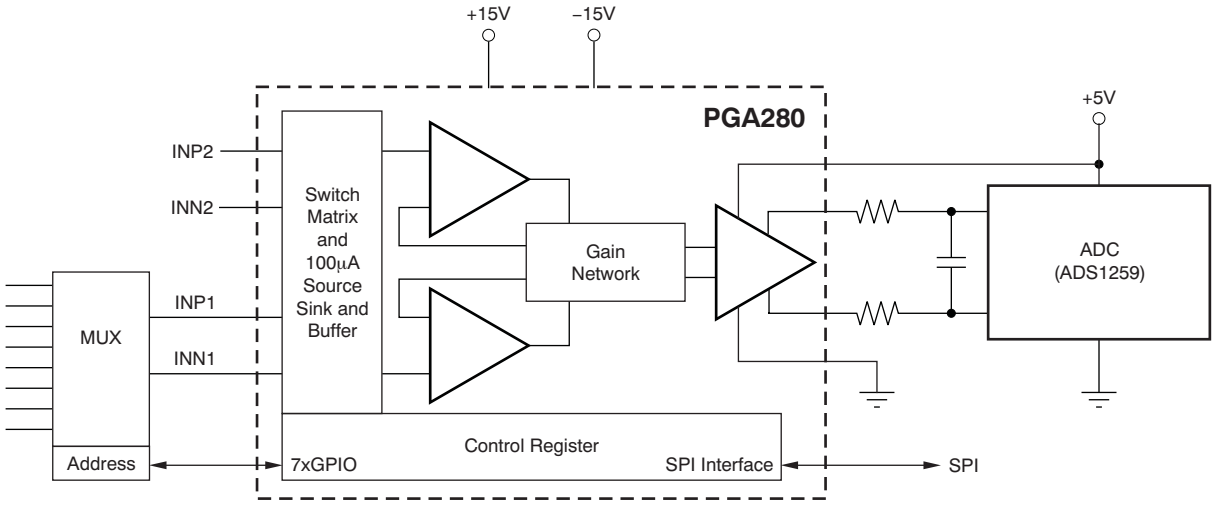
PGA280 は、ゲインをデジタル制御でき、信号整合性テスト機能を備えた高精度計装アンプです。このデバイスは、低オフセット電圧、ほぼゼロのオフセットおよびゲイン・ドリフト、および優れた直線性を提供し、1/f ノイズはほとんどありません。また、優れた同相除去と電源除去により、精度の高い、高分解能の測定をサポートします。36V 電源への対応と、高インピーダンスの広い入力範囲は、汎用的な信号測定の要件を満たしています。

特殊な回路により、マルチプレクサ (MUX) のスイッチングによる突入電流を防止します。また、入力スイッチ・マトリクスにより、再構成とシステム・レベル診断 (過負荷条件の表示) を簡単に実行できます。

デバイスの比較

特長	製品名
23 ビット分解能、ΔΣ アナログ / デジタル・コンバータ	ADS1259
チョッパ安定化計装アンプ、RR I/O、5V 単一電源	INA333
高精度 PGA、G = 1、10、100、1000	PGA204
高精度 PGA、JFET 入力、G = 1、2、4、8	PGA206

代表的なアプリケーション



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (September 2009) から Revision B に変更 **Page**

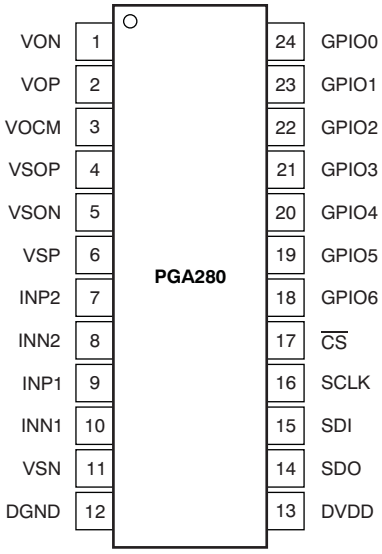
- Added *Timing Characteristics: Serial Interface* table and serial timing diagram ... 8
- Changed text from "This interface allows.clock rates up to 10 Mhz." to "... 16 MHz" in last paragraph of *SPI and Register Description* section ... 27

5 概要（続き）

構成可能な汎用入出力 (GPIO) を使用すると、複数の制御および通信機能を利用できます。SPI は、より多くのデバイスと通信するように拡張でき、4 つの ISO カプラーのみで絶縁できます。PGA280 は TSSOP-24 パッケージで供給され、–40℃～+105℃で動作が規定されています。提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

6 Pin Configuration and Functions

TSSOP-24
PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		DESCRIPTION	PIN		DESCRIPTION
NO.	NAME		NO.	NAME	
1	VON	Inverting signal output	13	DVDD	Digital supply
2	VOP	Noninverting signal output	14	SDO	SPI slave data output
3	VOCM	Input, output common-mode voltage	15	SDI	SPI slave data input
4	VSOP	Positive supply for output	16	SCLK	SPI clock input
5	VSON	Negative supply for output, AGND	17	$\overline{CS}$	SPI chip select input; active low
6	VSP	Positive high-voltage supply	18	GPIO6	GPIO 6, SYNC (in), OSC (out), $\overline{ECS}$6
7	INP2	AUX input, noninverting	19	GPIO5	GPIO 5, BUFA (out), $\overline{ECS}$5
8	INN2	AUX input, inverting	20	GPIO4	GPIO 4, BUFT (in), $\overline{ECS}$4
9	INP1	Signal input, noninverting	21	GPIO3	GPIO 3, EF (out), $\overline{ECS}$3
10	INN1	Signal input, inverting	22	GPIO2	GPIO 2, $\overline{ECS}$2, MUX2
11	VSN	Negative high-voltage supply	23	GPIO1	GPIO 1, $\overline{ECS}$1, MUX1
12	DGND	Digital ground	24	GPIO0	GPIO 0, $\overline{ECS}$0, MUX0

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage	VSN to VSP	40	V
	VSON to VSOP, and DGND to DVDD	6	V
Signal input terminals, voltage(2)		VSN – 0.5 to VSP + 0.5	V
Signal input terminals, current(2)		±10	mA
Output short-circuit(3)		Continuous	
Operating temperature		–55 to +140	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
ESD ratings	Human body model (HBM)	2000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Terminals are diode-clamped to the power-supply (VON and VOP) rails. Signals that can swing more than 0.5V beyond the supply rails must be current-limited.
(3) Short-circuit to VSON or VSOP, respectively, DGND or DVDD.

7.2 Electrical Characteristics

at T_A = 25°C, VSP = 15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = 3 V, DGND = 0 V, R_L = 2.5 kΩ to VSOP/2 = VOCM, G = 1 V/V, using internal clock, BUF inactive, V_{CM} = 0 V, and differential input and output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, RTI(1)	Gain = 1 V/V, 1.375 V/V			±50	±250	µV
		Gain = 128 V/V			±3	±15	
dV_{OS}/dT	vs temperature(2)	T_A = –40°C to +105°C	Gain = 1 V/V		±0.2	±0.6	µV/°C
			Gain = 128 V/V		±0.03	±0.17	
PSR	vs power supply, RTI	VSP – VSN = 10 V and 36 V, gain = 1 V/V, 128 V/V			±0.3	±3	µV/V
dV_{OS}/df	vs external clock, RTI(3)	0.8 MHz to 1.2 MHz, gain = 1 V/V			±0.05		µV/kHz
		0.8 MHz to 1.2 MHz, gain = 128 V/V			±0.001		
	Long-term stability(4)	Gain = 128 V/V			3.5		nV/month
	Input impedance	Single-ended and differential			> 1		GΩ
	Input capacitance, IN1 / IN2	Single-ended			12 / 8		pF
	Input voltage	Gain = 1 V/V, gain = 128 V/V, T_A = –40°C to +105°C		(VSN) + 2.5		(VSP) – 2.5	V
CMR	Common-mode rejection, RTI	Gain = 1 V/V			±0.3	±3	µV/V
		Gain = 128 V/V			±0.08	±0.8	
		Gain = 128 V/V, T_A = –40°C to +105°C			±0.1	±1.5	
SINGLE-ENDED OUTPUT CONNECTION							
V_{OS}	Offset voltage, RTI, SE out	Gain = 1 V/V, 1.375 V/V, SE			±120		µV
		Gain = 1V/V			±3		
dV_{OS}/dT	vs temperature, SE out	Gain = 1 V/V, SE, T_A = –40°C to +105°C			0.6		µV/°C
		Gain = 64 V/V, SE, T_A = –40°C to +105°C			0.05		

(1) RTI: Referred to input.
(2) Specified by design; not production tested.
(3) See *Application Information* section and typical characteristic graphs.
(4) 300-hour life test at +150°C demonstrated randomly distributed variation in the range of measurement limits.

Electrical Characteristics (continued)

at T_A = 25°C, VSP = 15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = 3 V, DGND = 0 V, R_L = 2.5 kΩ to VSOP/2 = VOCM, G = 1 V/V, using internal clock, BUF inactive, V_{CM} = 0 V, and differential input and output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT(3)							
I_B	Bias current	Gain = 1 V/V			±0.3	±1	nA
		Gain = 128 V/V			±0.8	±2	
		Gain = 1 V/V, gain = 128 V/V, T_A = –40°C to +105°C			±0.6	±2	
I_{OS}	Offset current	Gain = 1 V/V, gain = 128 V/V			±0.1	±0.5	nA
		Gain = 1 V/V, gain = 128 V/V, T_A = –40°C to +105°C			±0.9	±2	
NOISE							
e_{NI}	Voltage noise, RTI; target	f = 0.01 Hz to 10 Hz	R_S = 0 Ω, G = 128 V/V		420		nV_{PP}
			R_S = 0 Ω, G = 1 V/V		4.5		μV_{PP}
		f = 1 kHz	R_S = 0 Ω, G = 128 V/V		22		nV/√Hz
			R_S = 0 Ω, G = 1 V/V		240		nV/√Hz
I_N	Current noise, RTI	f = 0.01 Hz to 10 Hz	R_S = 10 MΩ, G = 128 V/V		1.7		pA_{PP}
		f = 1 kHz	R_S = 10 MΩ, G = 128 V/V		90		fA/√Hz
GAIN (Output Swing = ±4.5 V)(5)							
	Range of input gain				⅛ to 128		V/V
	Range of output gain				1 and 1⅜		V/V
	Gain error, all binary steps	All gains			±0.03	±0.15	%
	vs temperature(2) (6)	No load, all gains except G = 128 V/V, T_A = –40°C to +105°C			–0.5	±2	ppm/°C
		No load, G = 128 V/V, T_A = –40°C to +105°C			–1	±3	ppm/°C
	Gain step matching(3) (gain to gain)	No load, all gains		See Typical Characteristics			
	Nonlinearity	No load, all gains(7)			1.5	10	ppm
	Nonlinearity over temperature(2)	No load, all gains, T_A = –40°C to +105°C			3		ppm
OUTPUT							
	Voltage output swing from rail(3)	T_A = –40°C to +105°C	VSOP = 5 V, load current 2 mA		40	100	mV
			VSOP = 2.7 V, load current 1.5 mA			100	mV
	Capacitive load drive				500		pF
I_{SC}	Short-circuit current	To VSOP/2, gain = 1.375 V/V		7	15	25	mA
	Output resistance	Each output VOP and VON			200		mΩ
VOCM							
	VOCM supply voltage	VSP – 2 V > VOCM, T_A = –40°C to +105°C		(VSON) + 0.1		(VSOP) – 0.1	V
I_B	Bias current into VOCM				3	100	nA
	VOCM input resistance				1		GΩ
INTERNAL OSCILLATOR							
	Frequency of internal clock(2)(3)			0.8	1	1.2	MHz
	Ext. oscillator frequency			0.8	1	1.2	MHz

(5) Gains smaller than ½ are measured with smaller output swing.
(6) See Figure 11 for typical gain error drift of various gain settings.
(7) Only G = 1 is production tested.

Electrical Characteristics (continued)

at T_A = 25°C, VSP = 15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = 3 V, DGND = 0 V, R_L = 2.5 kΩ to VSOP/2 = VOCM, G = 1 V/V, using internal clock, BUF inactive, V_{CM} = 0 V, and differential input and output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBP	Gain bandwidth product(3)	G > 4			6		MHz
SR	Slew rate(3), 4-V_{PP} output step	G = 1, C_L = 100 pF, BUF On			1		V/µs
		G = 8, C_L = 100 pF			2		V/µs
		G = 128, C_L = 100 pF			1		V/µs
t_S	Settling time(3)	To 0.01%	G = 8, V_O = 8-V_{PP} step		20		µs
			G = 128, V_O = 8-V_{PP} step		40		µs
		To 0.001%	G = 8, V_O = 8-V_{PP} step		30		µs
			G = 128, V_O = 8-V_{PP} step		40		µs
	Overload recovery, input(3)	0.5 V over supply, G = ⅛ to 128			8		µs
	Overload recovery, output(3)	±5.5-V_P input, G = 1 V/V			6		µs
INPUT MULTIPLEXER (Two-Channel)							
	Crosstalk, INP1 to INP2	At dc, gain = 128 V/V			< –130		dB
	Series-resistance(3)—see Figure 44				600		Ω
	Switch on-resistance(3)				450		Ω
	Current source and sink(3)	To GND		70	95	125	µA
INPUT CURRENT BUFFER (BUF)							
V_{OS}	Offset voltage(3)	Buffer active			15		mV
DIGITAL I/O (Supply: 2.7 V to 5.5 V)							
	Input (logic low threshold)			0		(DVDD)x0.2	V
	Input (logic high threshold)			0.8x(DVDD)		DVDD	V
	Output (logic low)	I_{OUT} = 4 mA, sink				0.7	V
	Output (logic high)	I_{OUT} = 2 mA, source		DVDD – 0.5			V
	SCLK, frequency					10	MHz
POWER SUPPLY: Input Stage (VSN – VSP)							
	Specified voltage	T_A = –40°C to +105°C		10		36	V
	Operating voltage				10 to 38		V
I_Q	Quiescent current	T_A = –40°C to +105°C	VSP		2.4	3	mA
			VSN		2.1	3	mA
POWER SUPPLY: Output Stage (VSOP – VSON)							
	Specified voltage	VSP – 1.5 V ≥ VSOP, T_A = –40°C to +105°C		2.7		5.5	V
	Voltage for VSOP, upper limit	(VSP – 2 V) > VOCM, (VSP – 5 V) > VSON			(VSP)		V
	Voltage for VSON	(VSP – 2 V) > VOCM, VSP ≥ VSOP			(VSN) to (VSP) – 5		V
I_Q	Quiescent Current	VSOP, T_A = –40°C to +105°C			0.75	1	mA
POWER SUPPLY: Digital (DVDD – DGND)							
	Specified voltage	T_A = –40°C to +105°C		2.7		5.5	V
	Voltage for DVDD, upper limit				(VSP) – 1		V
	Voltage for DGND, lower limit				(VSN)		V
I_Q	Quiescent current(3)	Static condition, no external load, DVDD = 3 V, T_A = –40°C to +105°C			0.07	0.13	mA
TEMPERATURE							
	Specified temperature			–40		105	°C
	Operating temperature			–55		140	°C
θ_{JA}	Thermal resistance	SSOP, High-K board, JESD51			80		°C/W

7.3 Timing Requirements: Serial Interface

at T_A = –40°C to +105°C, DVDD = 2.7 V to 5.5 V, and C_{LOAD} on SDO = 20 pF (unless otherwise specified)

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			16	MHz
t_{CLK}	Serial clock time period	62.5			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to first SCLK capture (falling) edge	0			ns
t_{HT_CKCS}	Delay time: last SCK capture (falling) to $\overline{CS}$ rising	0			ns
t_{SU_CKDI}	Setup time: SDI data valid to SCLK capture (falling) edge	5			ns
t_{HT_CKDI}	Hold time: SCLK capture (falling) edge to previous data valid on SDI	10			ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to SDO going to Hi-Z			25	ns
t_{D_CKDO}	Delay time: SCLK rising edge to (next) data valid on SDO			25	ns

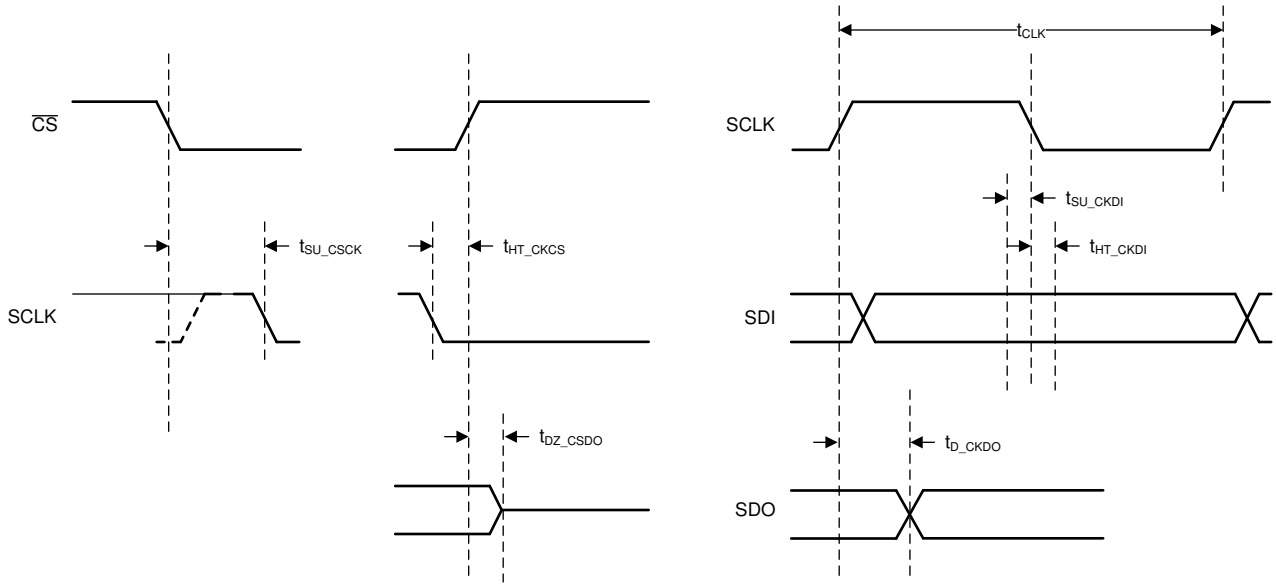


Figure 1. Serial Timing Diagram

7.4 Typical Characteristics

At T_A = +25°C, VSP = +15V, VSN = –15V, VSON = 0V, VSOP = 5V, DVDD = +3V, DGND = 0V, R_L = 2.5kΩ to VSOP/2 = VOCM, G = 1V/V, using internal clock, BUF inactive, V_{CM} = 0V, and differential input and output, unless otherwise noted.

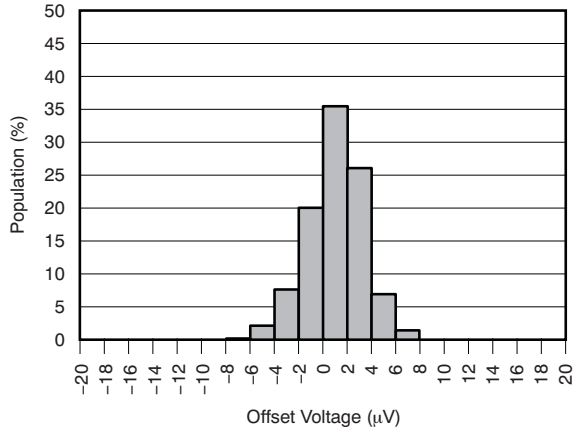


Figure 2. Offset Voltage Production Distribution (G = 128)

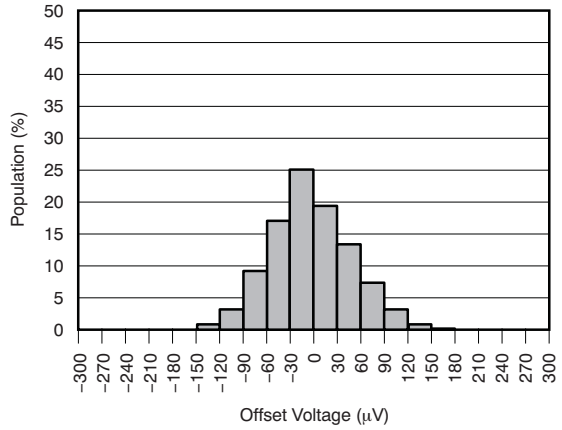


Figure 3. Offset Voltage Production Distribution (G = 1)

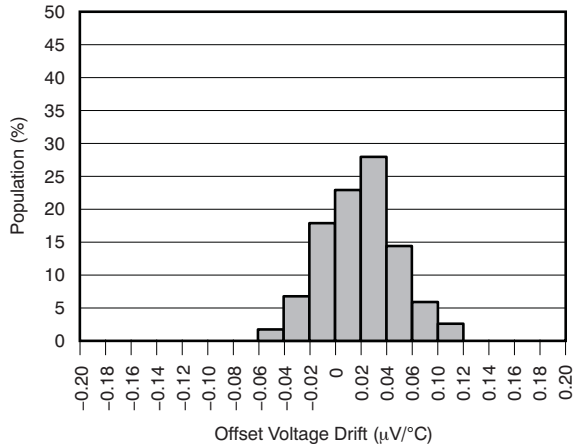


Figure 4. Offset Voltage Drift Distribution (G = 128)

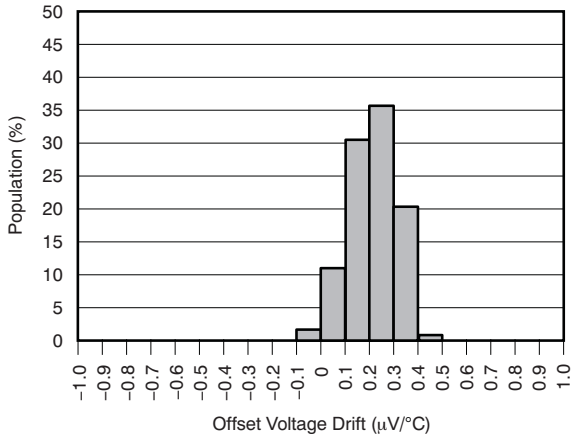


Figure 5. Offset Voltage Drift Distribution (G = 1)

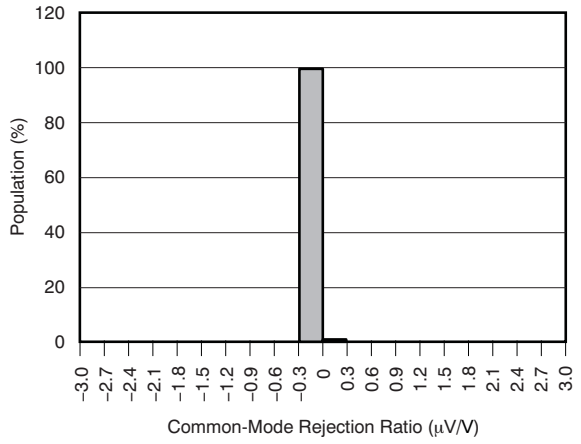


Figure 6. Common-Mode Rejection Distribution (G = 128)

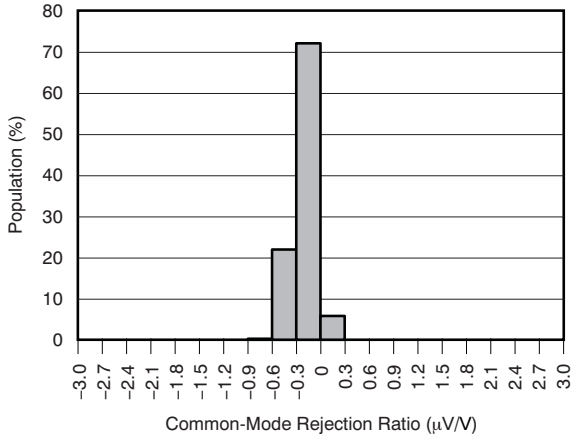


Figure 7. Common-Mode Rejection Distribution (G = 1)

Typical Characteristics (continued)

At T_A = +25°C, VSP = +15V, VSN = –15V, VSON = 0V, VSOP = 5V, DVDD = +3V, DGND = 0V, R_L = 2.5kΩ to VSOP/2 = VOCM, G = 1V/V, using internal clock, BUF inactive, V_{CM} = 0V, and differential input and output, unless otherwise noted.

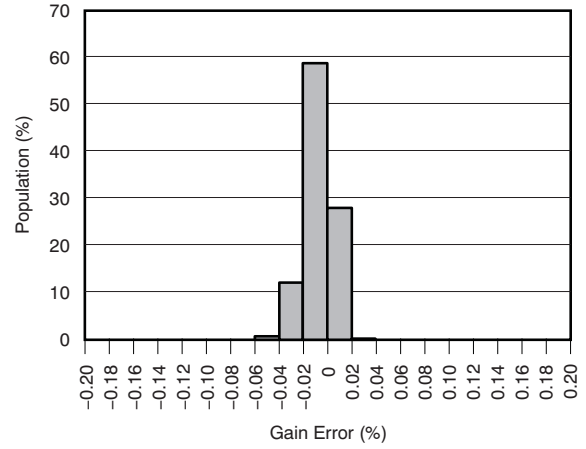


Figure 8. Gain-Error Distribution (G = 128)

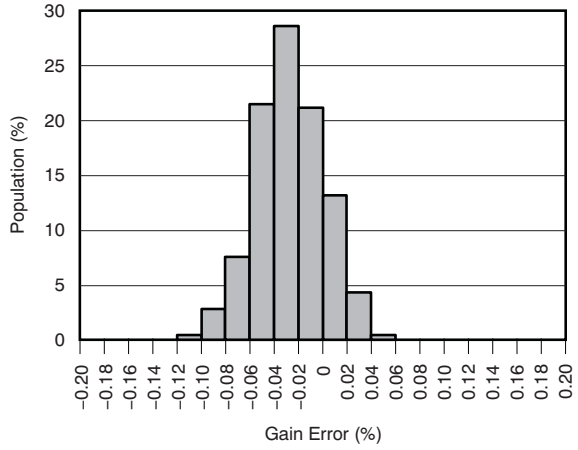


Figure 9. Gain-Error Distribution (G = 1)

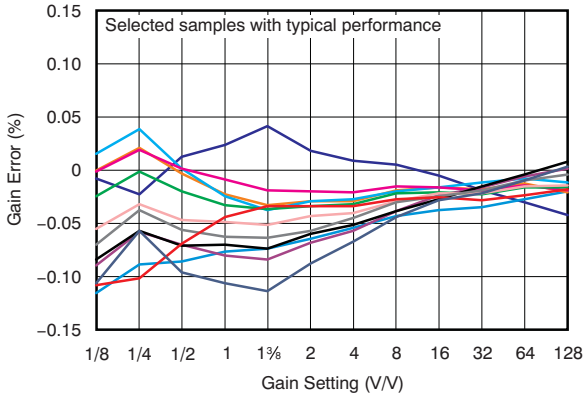


Figure 10. Gain Error vs Gain Setting

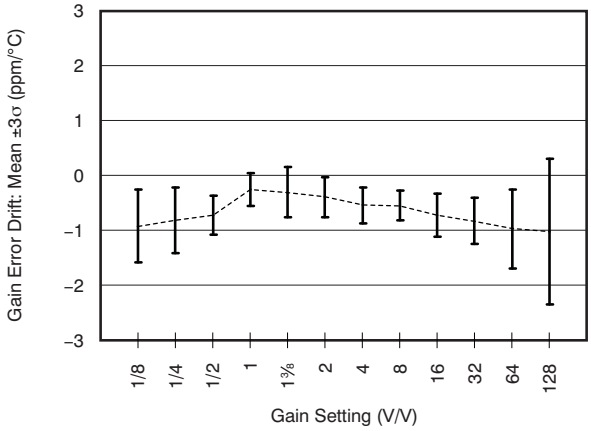


Figure 11. Gain-Error Drift Distribution vs Gain Setting (Mean With ±3 σ)

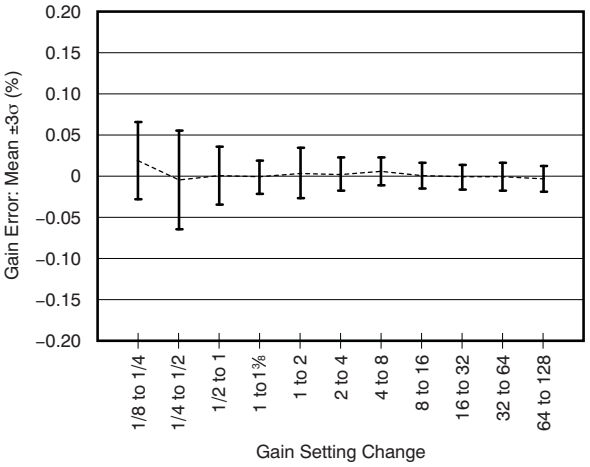


Figure 12. Maximum Gain-Error Deviation Between Sequential Gain Settings (Mean With ±3 σ)

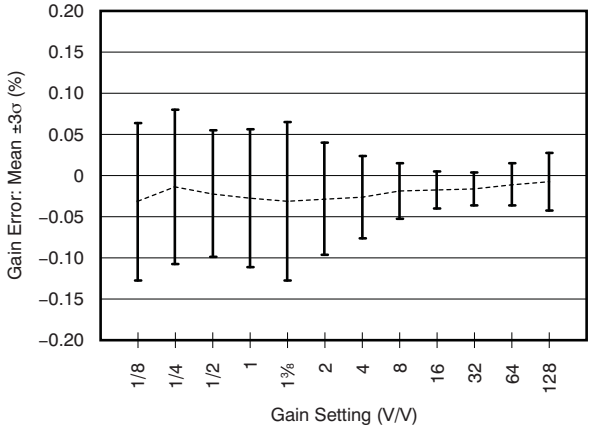


Figure 13. Gain-Error Distribution vs Gain Setting (Mean With ±3σ)

Typical Characteristics (continued)

At T_A = +25°C, VSP = +15V, VSN = –15V, VSON = 0V, VSOP = 5V, DVDD = +3V, DGND = 0V, R_L = 2.5kΩ to VSOP/2 = VOCM, G = 1V/V, using internal clock, BUF inactive, V_{CM} = 0V, and differential input and output, unless otherwise noted.

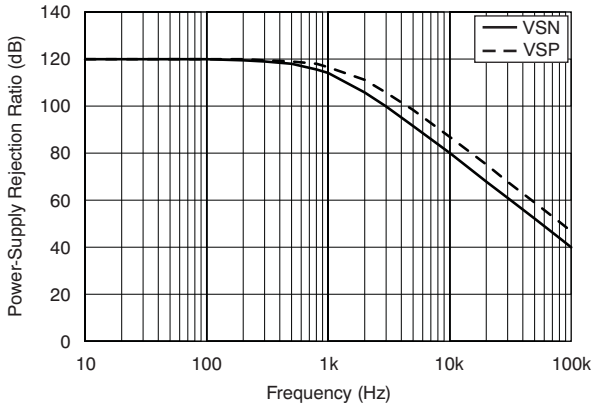


Figure 14. Power-Supply Rejection vs Frequency

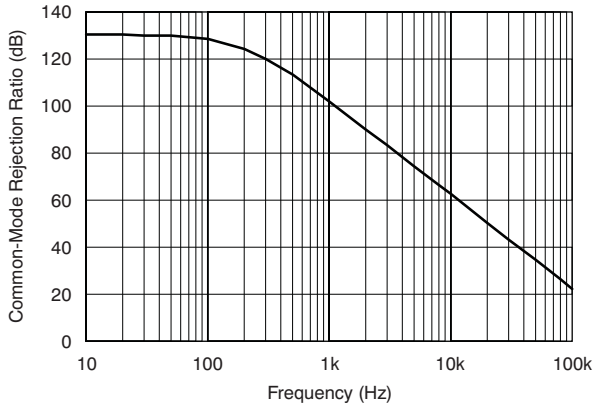


Figure 15. Common-Mode Rejection vs Frequency

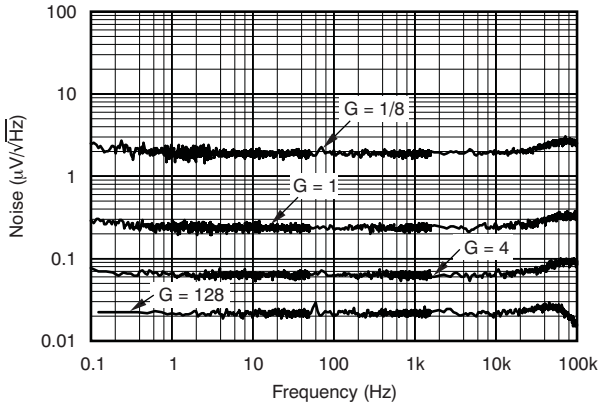


Figure 16. Input-Referred Noise Spectrum

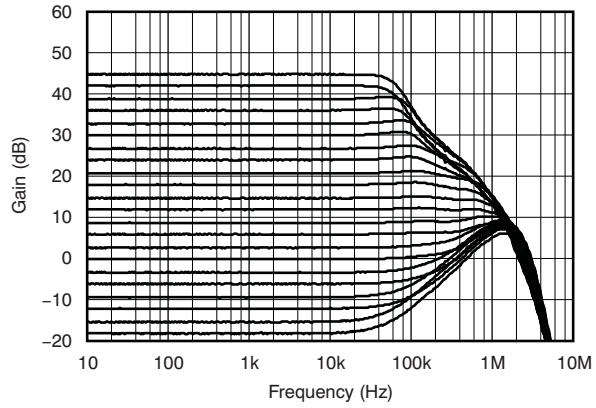


Figure 17. Small-Signal Gain vs Frequency

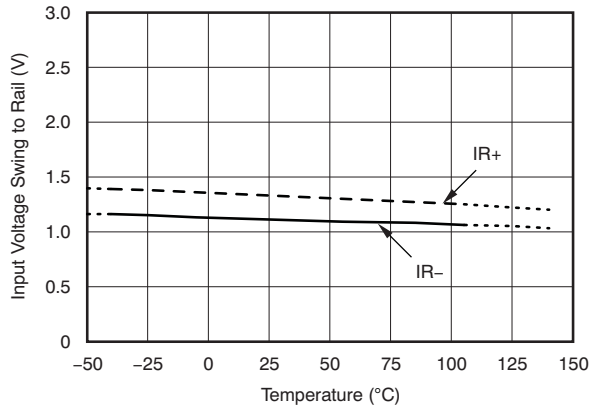


Figure 18. Input Voltage Range Limits vs Temperature

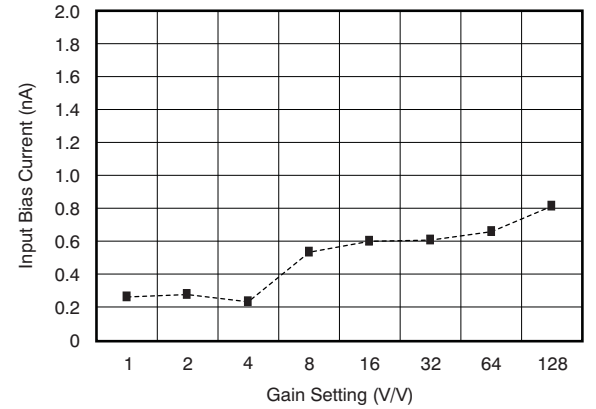


Figure 19. Bias Current vs Gain Setting

Typical Characteristics (continued)

At T_A = +25°C, VSP = +15V, VSN = –15V, VSON = 0V, VSOP = 5V, DVDD = +3V, DGND = 0V, R_L = 2.5kΩ to VSOP/2 = VOCM, G = 1V/V, using internal clock, BUF inactive, V_{CM} = 0V, and differential input and output, unless otherwise noted.

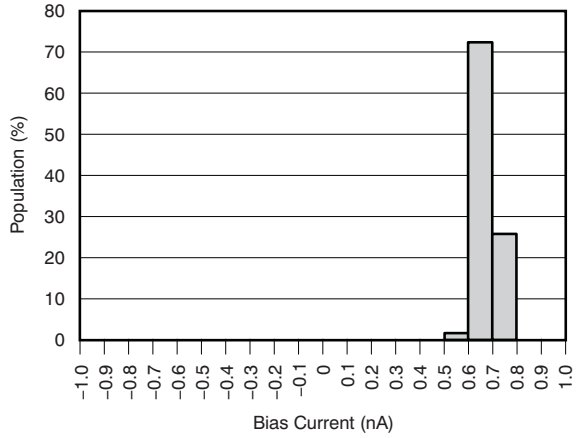


Figure 20. Input Bias Current Distribution (G = 128)

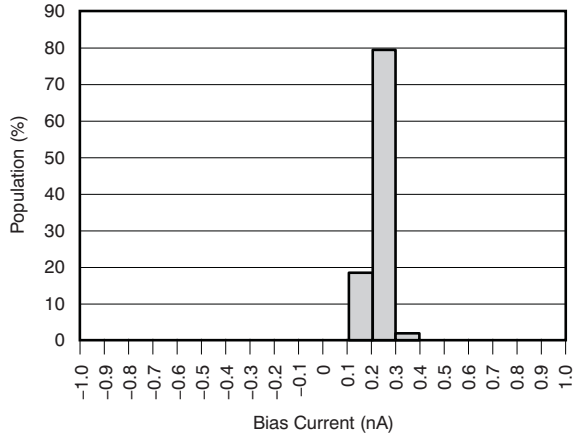


Figure 21. Input Bias Current Distribution (G = 1)

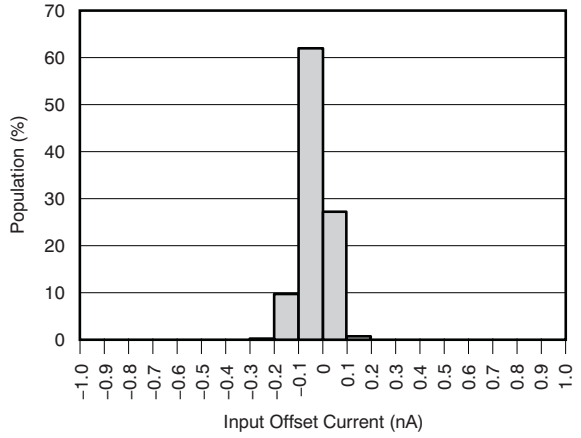


Figure 22. Input Offset Current Distribution (G = 1, G = 128)

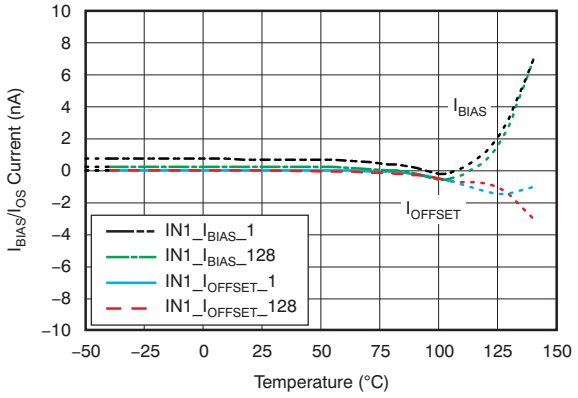


Figure 23. Input Bias Current and Input Offset Current vs Temperature

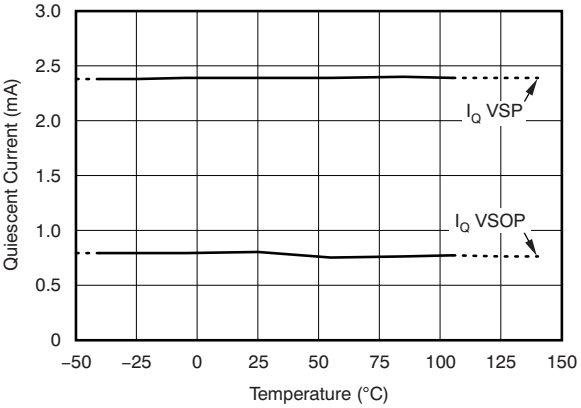


Figure 24. Quiescent Current From Supplies (VSP and VSOP) vs Temperature

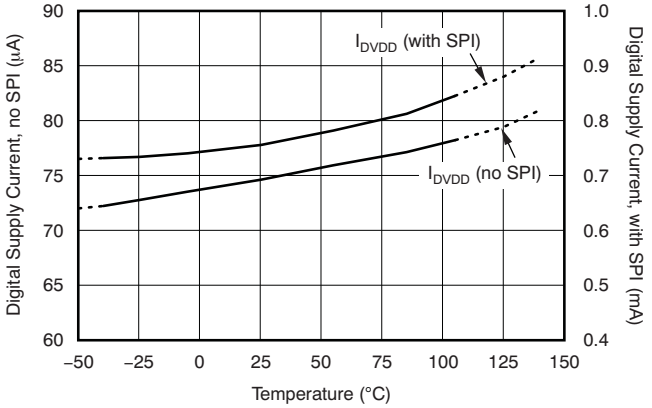


Figure 25. Digital Supply Current With and Without SPI Communication vs Temperature

Typical Characteristics (continued)

At T_A = +25°C, VSP = +15V, VSN = –15V, VSON = 0V, VSOP = 5V, DVDD = +3V, DGND = 0V, R_L = 2.5kΩ to VSOP/2 = VOCM, G = 1V/V, using internal clock, BUF inactive, V_{CM} = 0V, and differential input and output, unless otherwise noted.

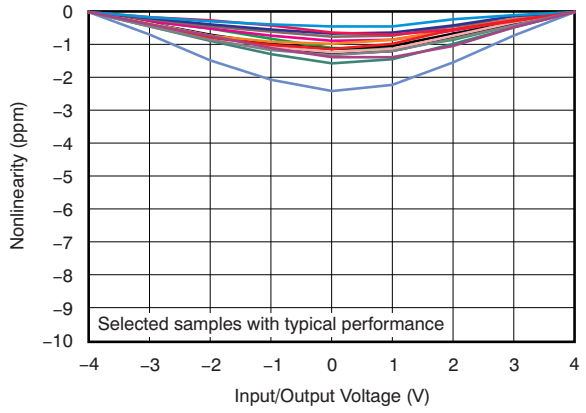


Figure 26. Gain Nonlinearity With End-Point Calibration (G = 1)

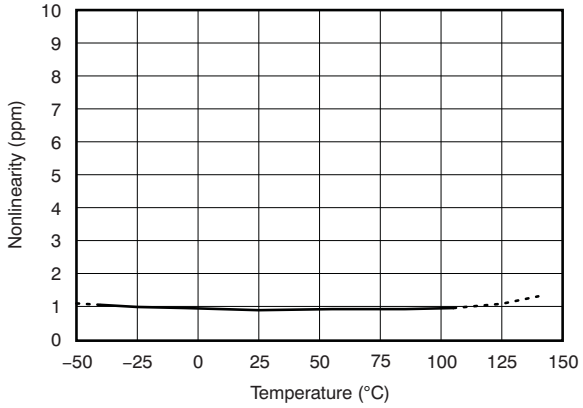


Figure 27. Gain Nonlinearity vs Temperature

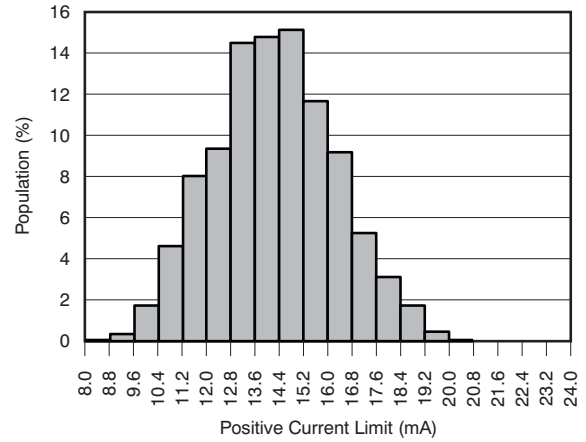


Figure 28. Positive Output Current Limit Distribution

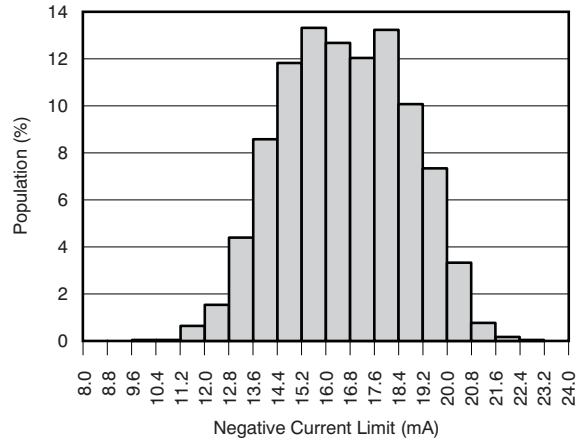


Figure 29. Negative Output Current Limit Distribution

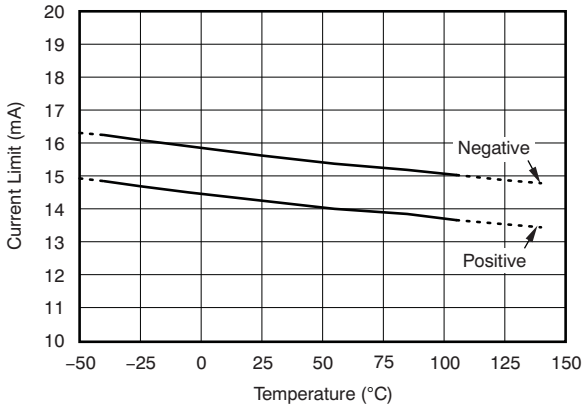


Figure 30. Output Current Limit vs Temperature

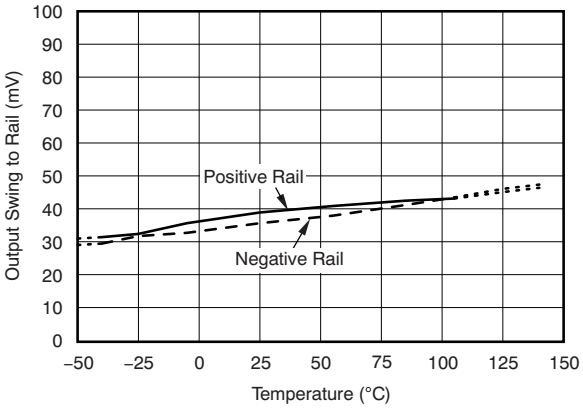


Figure 31. Output Swing To Rail vs Temperature (VSOP – VSON = 5 V)

Typical Characteristics (continued)

At T_A = +25°C, VSP = +15V, VSN = –15V, VSON = 0V, VSOP = 5V, DVDD = +3V, DGND = 0V, R_L = 2.5kΩ to VSOP/2 = VOCM, G = 1V/V, using internal clock, BUF inactive, V_{CM} = 0V, and differential input and output, unless otherwise noted.

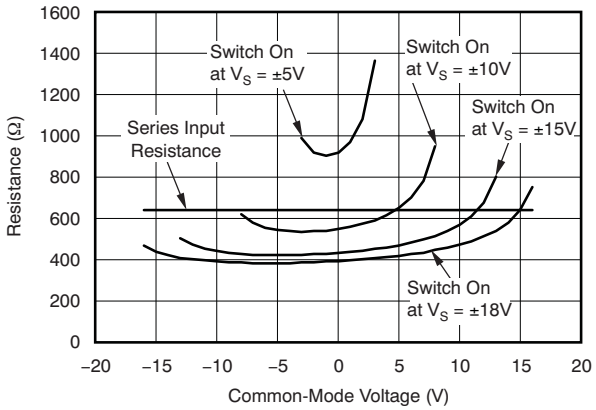


Figure 32. Switch-On Resistance and Series Input Resistance vs Common-Mode Voltage at Various Supply Voltages

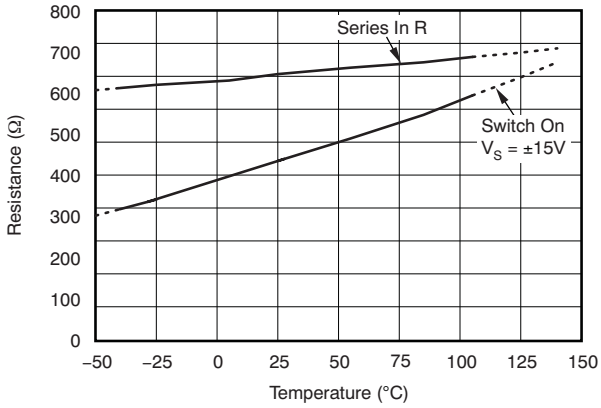


Figure 33. Switch-On Resistance and Series Input Resistance vs Temperature

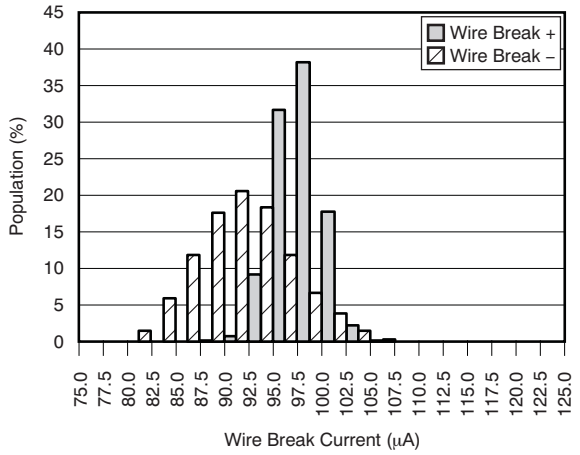


Figure 34. Wire Break Current Distribution

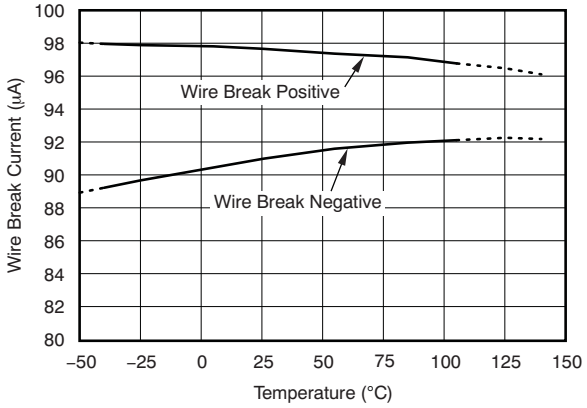


Figure 35. Wire Break Current Magnitude vs Temperature

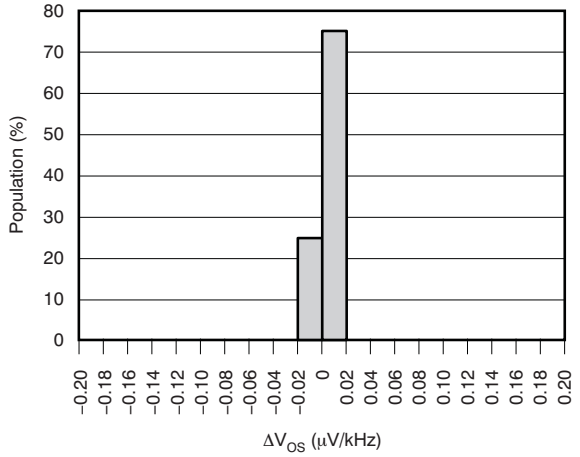


Figure 36. Influence of External Clock Frequency to VOS Performance (G = 128)

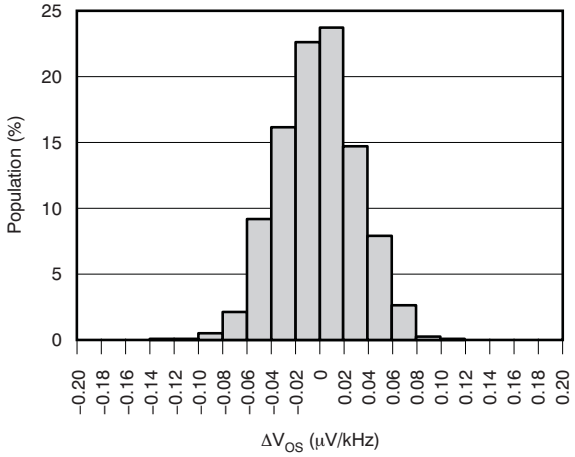


Figure 37. Influence of External Clock Frequency to VOS Performance (G = 1)

Typical Characteristics (continued)

At T_A = +25°C, VSP = +15V, VSN = –15V, VSON = 0V, VSOP = 5V, DVDD = +3V, DGND = 0V, R_L = 2.5kΩ to VSOP/2 = VOCM, G = 1V/V, using internal clock, BUF inactive, V_{CM} = 0V, and differential input and output, unless otherwise noted.

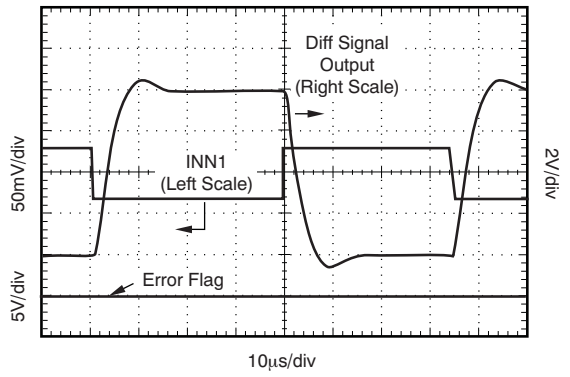


Figure 38. Step Response (G = 128)

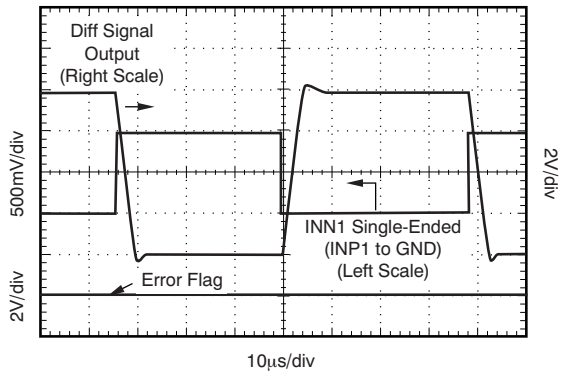


Figure 39. Step Response (G = 8)

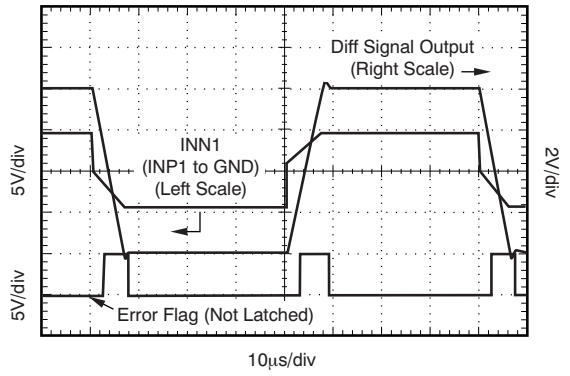


Figure 40. Step Response (G = 1)

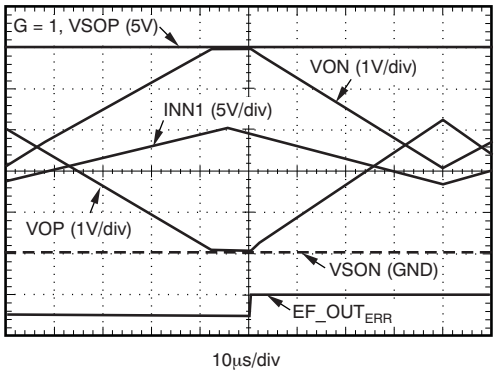


Figure 41. Output Overload Recovery

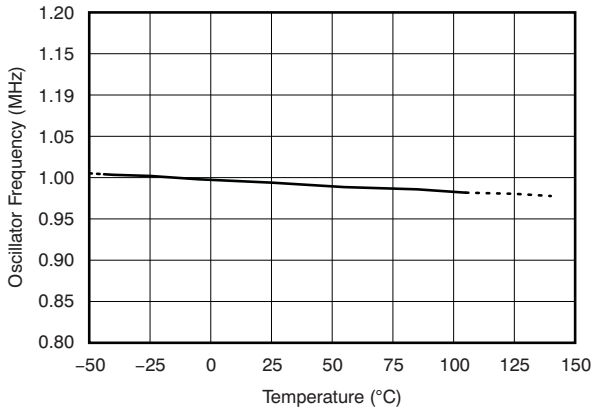


Figure 42. Oscillator Frequency vs Temperature

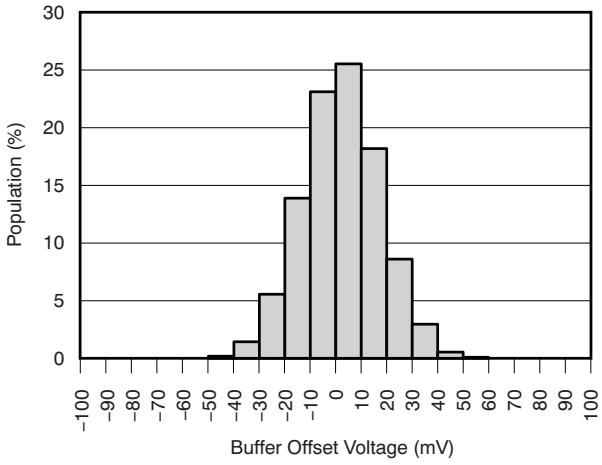


Figure 43. Input Current Buffer Offset Voltage Distribution

8 Detailed Description

8.1 Overview

The PGA280 is a universal high-voltage instrumentation amplifier with digital gain control. This device offers excellent dc precision and long-term stability using modern chopper technology with internal filters that minimize chopper-related noise. The input gain extends from ⅛ V/V (attenuation) to 128 V/V in binary steps. The output stage offers a gain multiplying factor of 1 V/V and 1⅜ V/V for optimal gain adjustment. The output stage connects to the low-voltage (5 V or 3 V) supply. .

A signal multiplexer provides two differential inputs. Several signal switches allow signal diagnosis of wire break, input disconnect, single-ended (versus differential), and shorted inputs.

The supply voltage of up to ±18 V offers a wide common-mode range with high input impedance; therefore, large common-mode noise signals and offsets can be suppressed.

A pair of high-speed current buffers can be activated to avoid inrush currents during fast signal transients, such as those generated from switching the signal multiplexers. This feature minimizes discharge errors in passive signal input filters in front of the multiplexer.

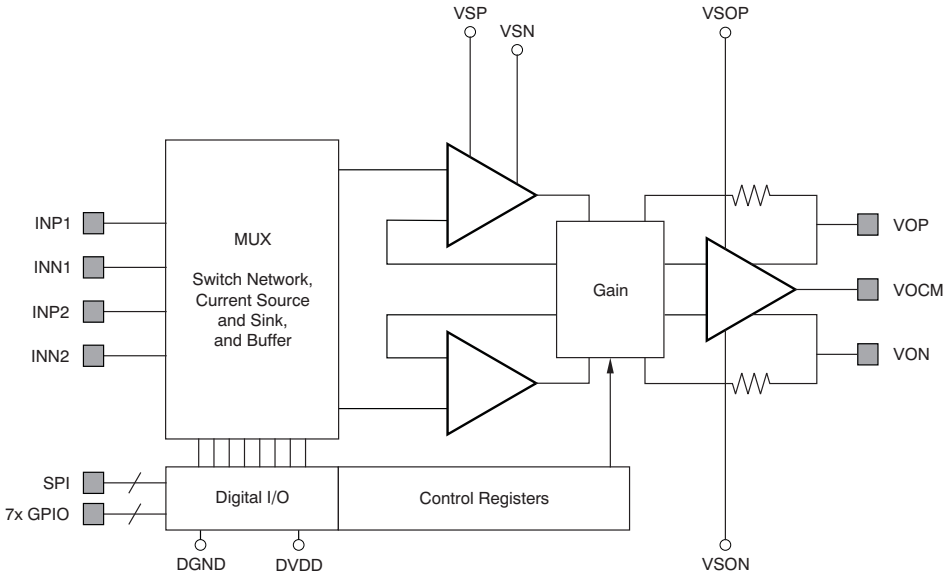
The fully differential signal output matches the inputs of modern high-resolution and high-accuracy analog-to-digital converters (ADCs), including delta-sigma (ΔΣ) as well as successive-approximation response (SAR) converters. The supply voltage for the output stage is normally connected together with the converter supply, thus preventing signal overloads from the high-voltage analog supply.

Internal error detection in the input and output stage provides individual information about the signal condition. Integrating ADCs may hide momentary overloads. Together with the input switch matrix, extensive signal and error diagnosis is made possible.

The serial peripheral interface (SPI) provides write and read access to internal registers. These registers control gain, the current buffer, input switches, and the general-purpose input/output (GPIO) or special function pins, as well as configuration and diagnostics.

The GPIO port controls the multiplexer (MUX) and switches and indicates internal conditions. The GPIO port can also be individually configured for output or input. A special $\overline{CS}$ mode for the GPIO extends the communication to other external SPI devices, such as data converters or shift registers. This special function is intended for SPI communication via a minimum number of isolation couplers. Additional proof for communication integrity is provided by an optional checksum byte following each communication block.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Functional Blocks

Both high-impedance input amplifiers are symmetrical, and have low noise and excellent dc precision. These amplifiers are connected to a resistor network and provide a gain range from 128 V/V down to an attenuation of ⅛. The PGA280 architecture rejects common-mode offsets and noise over a wide bandwidth.

The PGA280 features additional current buffers placed in front of the precision amplifier that can be activated on demand. When activated, these additional current buffers avoid problems that result from input current during dynamic overloads, such as the fast signal transient that follows the channel switching from a multiplexer. Without the use of the additional current buffers, the fast signal transient would overload the precision amplifiers and high bias currents could flow into the protection clamp until the amplifiers recover from the overload. This momentary current can influence the signal source or passive filters in front of the multiplexer and generate long settling tails. Activating this current buffer avoids such an overload current pulse. The buffer disconnects automatically after an adjustable time. For continuous signal measurement, the additional current buffers are not used.

The switches in the input provide signal diagnostic capability and offer an auxiliary input channel (INP2 and INN2; see Figure 44). Both channels can be switched to diagnose or test conditions, such as a ground-referred, single-ended voltage measurement for either input. In this mode, each of the signal inputs can be observed to analyze common-mode offsets and noise.

The primary input channel [INP1 and INN1] provides switches and current sources for a wire break test. Any switch can short both inputs, and can also discharge a filter capacitor after a wire break test, for example.

The signal inputs are diode-clamped to the supply rails. External resistors can be placed in series to the inputs to provide overvoltage protection. Limit current into the input pins to ≤ 10 mA.

The output stage offers a fully-differential signal around the output reference pin, VOCM. The VOCM pin is a high-impedance input and expects an external voltage, typically close to midsupply. The 3-V or 5-V supply of the converter or amplifier, following the PGA280 outputs, is normally connected to VSOP and VSON; this configuration shares a common supply voltage and protects the circuit from overloads. The fully-differential signal avoids coupling of noise and errors from the supply and ground, and allows large signal swing without the risk of nonlinearities that arise when driving near the supply rails.

The PGA280 signal path has several test points for critical overload conditions. The input amplifiers detect signal overvoltage and overload as a result of high gain. The output stage also detects clipping. These events are filtered with adjustable suppression delays and then stored for readout. A GPIO pin can be dedicated for external indication either as an interrupt or in a monitor mode.

A serial peripheral interface (SPI) controls the gain setting and switches, as well as the operation modes and the GPIO port pins. The SPI allows read and write access to the internal registers. These registers contain conditions, flags, and settings, as described in the *SPI and Register Description* section. They represent the gain setting for the input stage from 128V/V to the attenuation of ⅛ V/V in binary steps and the output stage gain of 1 V/V and 1.375 V/V (1⅜). The input MUX and switches and the input buffers are also controlled by registers. Internal error conditions are stored and may be masked to activate an external pin in the GPIO port.

This GPIO port can be configured individually for either input or output or for a special function. In special function mode, the port indicates an error condition, generates $\overline{CS}$ signal, controls an external MUX, and connects to the buffer control and oscillator.

The port pin can act as a $\overline{CS}$ for an external SPI device. This mode connects other SPI devices [such as an analog-to-digital (A/D) converter] to the primary four-wire SPI. This feature is especially desirable when using galvanically-isolated SPI communication. An optional checksum byte further improves communications integrity.

Feature Description (continued)

8.3.1.1 Input Switch Network

Figure 44 shows the arrangement of the input switches. They are controlled individually via the digital SPI. The switches B1b, B2b, A1b, and A2b are controlled automatically with the buffer (BUF) operation.

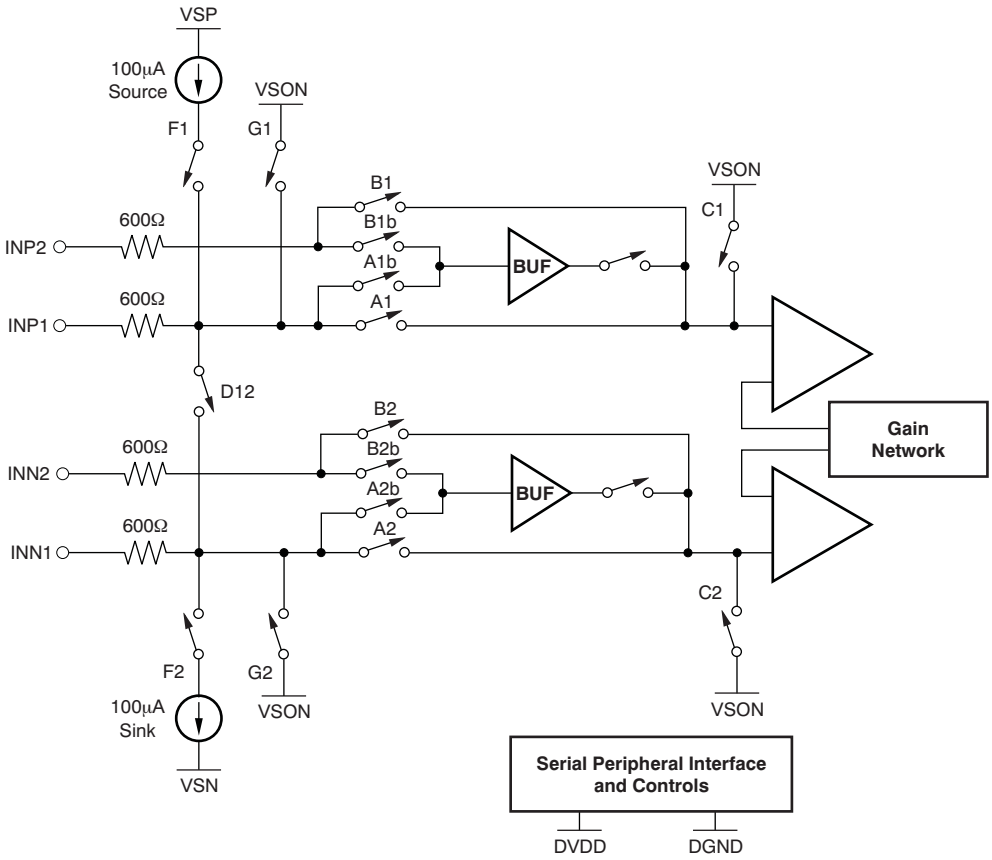


Figure 44. Input Switch Diagram

Switches A and B select the signal input. Input 1 (INP1 and INN1) provides two current sources and two switches that connect to VSON (which is typically the analog ground). This configuration is intended for wire break diagnosis. D12 can discharge an external capacitor or generate a starting condition.

Switches C1 and C2 are used to measure the input voltage referred to GND (VSON); for example, with A1 and C2 closed. This scheme measures the voltage signal connected to the input pin (INP1) referred to a common ground. The BUF output is protected against a short to VSON. See the *SPI and Register Description* section for more information about switch control.

Feature Description (continued)

8.3.1.2 Input Amplifier, Gain Network, and Buffer

The high-precision input amplifiers present very low dc error and drift as a result of a modern chopper technology with an embedded synchronous filter that removes virtually all chopping noise. This topology reduces flicker noise to a minimum and therefore enables the precise measurement of small dc-signals with high resolution, accuracy, and repeatability. The chopper frequency of 250 kHz is derived from an internal 1-MHz clock. An external clock can also be connected, if desired.

The gain network for the binary gain steps connects to the input amplifiers, thus providing the best possible signal-to-noise ratio (SNR) and dc accuracy up to the highest gains. Gain is controlled by Register 0. This register can control the gain and address for an external MUX in one byte. Selectable gains (in V/V) are : 128, 64, 32, 16, 8, 4, 2, 1, ½, ¼, and ⅛. The gain is set to 1/8 V/V after device reset or power-on.

Programmable gain amplifiers such as the PGA280 use internal resistors to set the gain. Consequently, quiescent current is increased by the current that passes through these resistors. The largest amplitude could increase the supply current by ±0.4 mA. In maximum overload, gain of 128 V/V and each or the inputs connected to the opposite supply voltage, a current of approximately 27 mA was measured. External resistors in series with the input pins that are normally present avoid this extreme condition. This current is only limited by the internal 600 Ω and the switch-on resistance (see Figure 44).

8.3.1.3 Current Buffer

Designed for highest accuracy and low noise, both amplifier inputs are protected from dynamic overvoltages through clamps. The amplifier fast input slew rate (approximately 1 V/µs) normally prevents these clamps from turning on, provided adequate signal filtering is placed before the input. However, the fast channel switching-transient of a multiplexer or switch is much steeper, and cannot be filtered; this type of transient generates a dynamic overload. The current buffers (BUF) prevent this dynamic overload condition of the input.

With the buffers not activated, Figure 45 indicates the clamp current flowing as a result of a fast signal change. The ramp in the signal, measured at the input pins (INP1), is the resulting voltage drop across the 1.5-kΩ resistor. In the example measurement, this resistor is placed between the signal generator and the input pin of the PGA280.

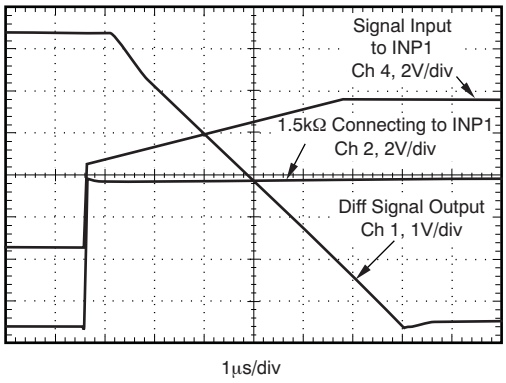
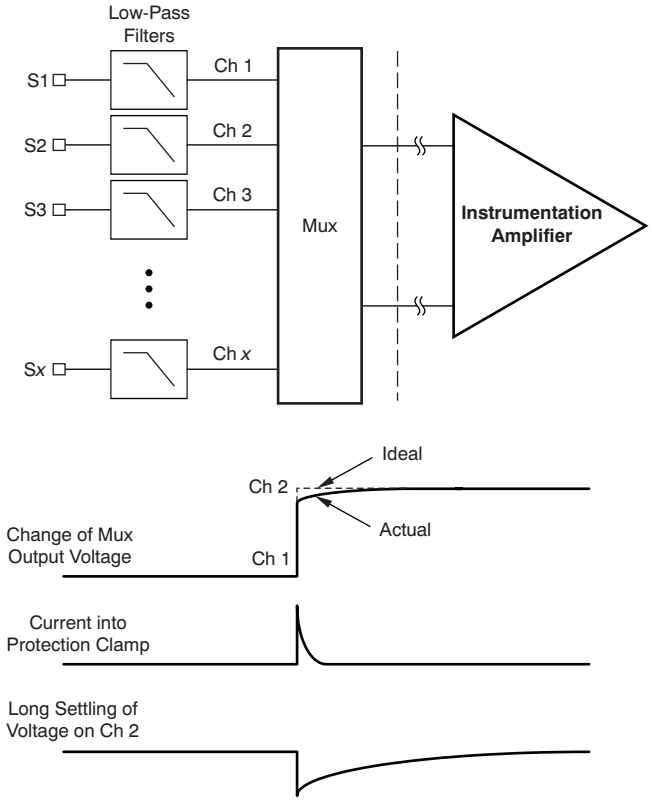


Figure 45. Buffer OFF: Input Clamp Current Flowing

Feature Description (continued)

Figure 46 shows a typical block diagram for multiplexed data acquisition. The transient from channel 1 to channel 2 , shown as a voltage step, dynamically overloads the amplifier. A current pulse results from the input protection clamp. Without the activation of the buffers (see BUF, Figure 44), the clamp current charges the filter and the signal source. Input low-pass filters are often set to settling times in the millisecond range; therefore, discharge currents from dynamic overload would produce long settling delays.



NOTE: Current from the protection clamp into the signal source and filter produces a long settling delay.

Figure 46. Typical Block Diagram for Multiplexed Data Acquisition

Feature Description (continued)

Together with the switching command of the multiplexer or internal switching, the current buffers (BUF) can be activated to prevent such clamp currents. The buffers do not have clamps as long as the signal remains within the supply boundaries. Figure 47 shows an example of the input signal settling for both conditions: without and with the buffer activated.

Without the buffer, there is an obvious long settling, depending on signal and filter impedance. With the buffer activated, only the amplifier has to settle and no distorting current is reflected into the signal source and filter; no glitch is visible in this plot. The plot shows the resulting settling of the input signal for a positive and a negative signal step as indicated in Figure 46; also shown are the SPI signal and the BUFA signal.

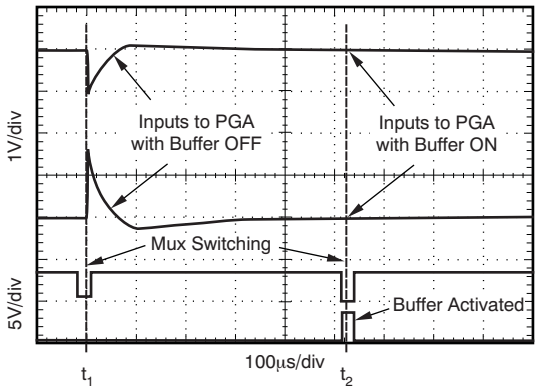


Figure 47. Example for Amplifier Settling Without (t_1) and With (t_2) Buffer (BUF) Activated

The buffers turn off automatically after a preset time (see Register 3, BUFTIM). They are activated from bit 5 (T) within the command byte. They can also be triggered by an external pin (BUFTin on GPIO4). The BUFA bit is active in conjunction with the buffer, indicating that the buffer is busy (see Figure 55).

Error detection circuits observe the signal path for signal overvoltage (IOVerr), amplifier output clipping (IARerr), and gain overload (GAINerr). The Input Clamp Activation indicator ICAerr indicates that current was conducted into the dynamic clamp circuit. These indicators help prevent misinterpretation of the analog signal and diagnose critical input signal conditions, such as those that occur with integrating analog-to-digital converters that may hide momentary overloads and present inaccurate results.

The buffers (BUF) prevent current flowing from the signal source with a compromise of offset voltage. As soon as the buffers are turned off, the amplifiers settle back to high precision. For signal measurement without (multiplexer) switching transients, the buffer is not used.

8.3.1.4 Input Protection

The input terminals are protected with internal diodes connected to VSP and VSN. If the input signal voltage exceeds the power-supply voltage (VSP and VSN), limit the current to less than 10 mA to protect the internal clamp diodes. This current-limiting can generally be accomplished with a series input resistor.

8.3.1.5 EMI Susceptibility

Amplifiers vary in susceptibility to electromagnetic interference (EMI), but good layout practices play a critical role. EMI can generally be identified as a variation in offset voltage shifts. The PGA280 has been specifically designed to minimize susceptibility to EMI by incorporating an internal low-pass filter. Additional EMI filters may be required next to the signal inputs of the system, as well as known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing, depending on the end system requirements.

Feature Description (continued)

8.3.1.6 Output Stage

The output stage power is connected to the low-voltage supply (normally 3 V or 5 V) that is used by the subsequent signal path of the system. This design prevents overloading of the low-voltage signal path.

The output signal is fully differential around a common-mode voltage (VOCM). The VOCM input pin is typically connected to midsupply voltage to offer the widest signal amplitude range. VOCM is a high-impedance input that requires an external connection to a voltage within the supply boundaries. The usable voltage range for the VOCM input is specified in the Electrical Characteristics and must be observed.

The output stage can be set to a gain of 1 V/V and 1⅜ V/V. THe output stage is set to 1 V/V after a device reset or power-on, and is controlled by the gain multiplication factor.

Both signal outputs, VOP and VON, swing symmetrically around VOCM. The signal is represented as the voltage between the two outputs and does not require an accurate VOCM. Therefore, the signal output does not include ground noise or grounding errors. Noise or drift on VOCM is normally rejected by the common-mode rejection capability of the subsequent signal stage.

The signal that passes through the output stage is internally monitored for two error conditions: clipping of the signal to the supply rail and overcurrent. In fault conditions, an error flag bit is set (OUTerr).

8.3.1.7 Output Filter

The PGA280 uses chopper technology for excellent dc stability over temperature and life of operation. The device is designed to avoid 1/f frequency (flicker) noise, and therefore enables both high resolution and high repeatability for dc measurements. While the chopper noise components are internally filtered, a minimal residual amount of high-frequency switching noise appears at the signal outputs. An external, passive, low-pass filter after the output stage is recommended to remove this switching noise; Figure 48 shows two examples. This filter can also be used to isolate or decouple the charge switching pulses of an A/D converter input.

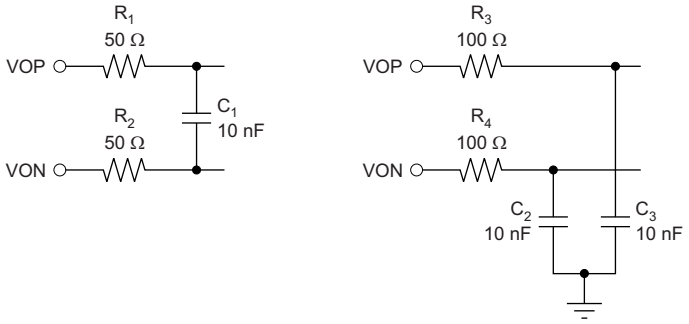


Figure 48. Typical Examples of Recommended Output Filters

8.3.1.8 Single-Ended Output

The output stage of PGA280 is designed for highest precision. The fully-differential output avoids grounding errors and noise, and delivers twice the signal amplitude compared to single-ended signals. However, if desired, the output can be taken single-ended from one of the output pins referred to the voltage at the VOCM pin. The output stage errors now relate to half the signal amplitude and half the signal gain. The unused output is unconnected, but not disconnected from error detection. The usable voltage range for the VOCM input is specified in the *Electrical Characteristics* and must be observed: the output swing (of both outputs) should not saturate to the supply. Separate specifications for offset voltage and drift indicate higher offset voltage at lower gains, because some error sources are not cancelled in the output stage connected in single-ended mode. Note that the gain is one-half of the gain set in reference to the gain table (see Table 2).

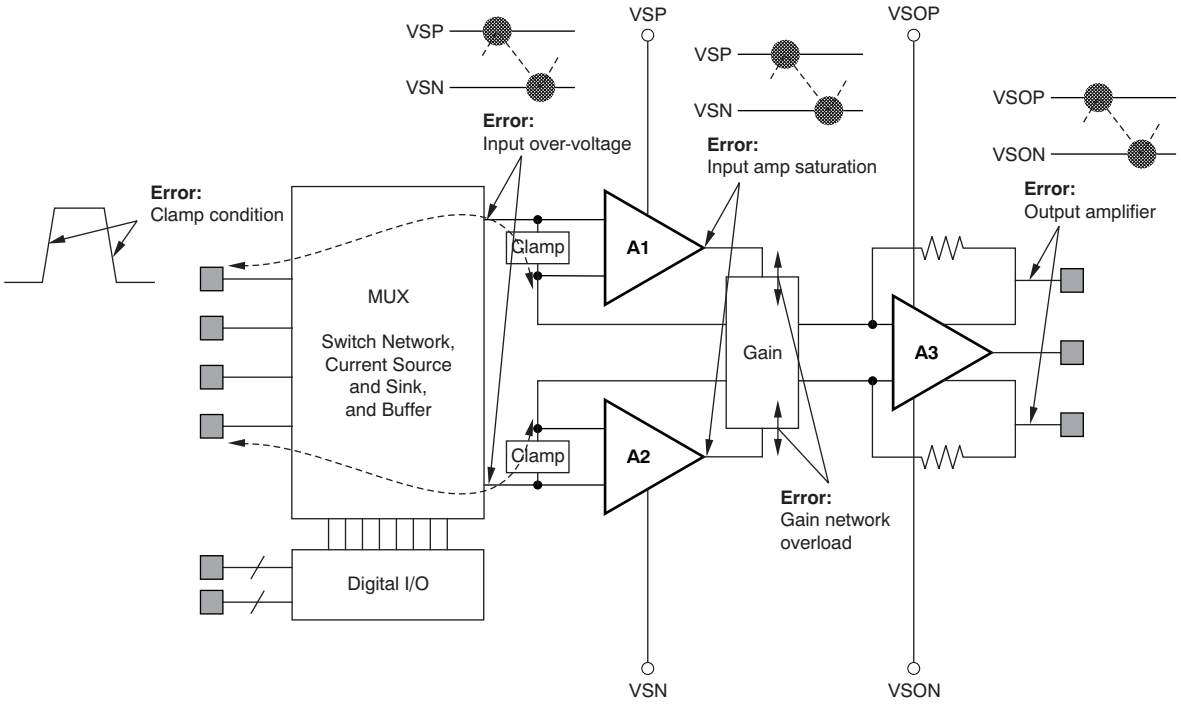
Feature Description (continued)

8.3.1.9 Error Detection

The PGA280 is designed for high dc precision and universal use, but the device also allows monitoring of signal integrity. The device contains an input switch network for signal tests and sense points that can indicate critical conditions. These added features support fully automated system setup and diagnostic capability. Out-of linear range conditions are detected and stored in the Error Status Register (Register 4) until reset. The input switches shown in Figure 44 can be used to short the input to GND, disconnect the signal, insert a 100µA test current, discharge external capacitance, and switch to a ground (VSON)-referenced signal measurement to observe the signal at the pin (versus the differential measurement). Figure 49 illustrates the diagnostic points available for error detection in the device architecture.

All switches are controlled through the SPI. The error signals can be combined using a logic *OR* function to an output pin and eventually be used as an error interrupt signal. Errors are normally latched, unless the LTD bit (latch disable) is set.

The error sensors are filtered with a suppression delay (Register 11). These error signals are normally suppressed during the buffer (BUFA) active time.



NOTE: The signal path is observed for possible limitations; flags are stored and indicated in Register 4.

Figure 49. Diagnostic Points for Error Detection

Feature Description (continued)

8.3.2 Error Indicators

8.3.2.1 Input Clamp Conduction (ICAerr)

The input clamp protects the precision input amplifier from large voltages between the inputs that occur from a fast signal slew rate in the input. This clamp circuit pulls current from the input pins while active. Current flowing through the clamp can influence the signal source and cause long settling delays on passive signal filters. The current is limited by internal resistors of approximately 2.4 kΩ. Dynamic overload can result from the difference signal as well as the common-mode signal.

The input clamp turns on when the input signal slew rate is faster than the amplifier slew rate (see the Electrical Characteristics specification) and larger than ±1V. Appropriate input filtering avoids the activation. However, transients from MUX switching, internal switches, and gain switching action cannot be filtered; therefore, to avoid these transients, activate the current buffer (BUF). The buffer isolates the signal input from the clamp, and therefore avoids the current pulse (see Figure 44).

8.3.2.2 Input Overvoltage (IOVerr)

The input amplifier can only operate at high performance within a certain input voltage range to the supply rail. The IOVerr flag indicates a loss of performance because of the input voltage or the amplifier output approaching the rail.

8.3.2.3 Gain Network Overload (GAINerr)

The gain setting network is protected against overcurrent conditions that arise because of an improper gain setting. The current into the resistors is proportional to the voltage between both inputs and the internal resistor; a low resistor value results in high gains. This error flag indicates such an overload condition that is the result of an improper gain setting.

8.3.2.4 Output Amplifier (OUTerr)

The output stage is monitored for signal clipping to the supply rail and for overcurrent conditions.

8.3.2.5 CheckSum Error (CRCerr)

SPI communication can include a checksum byte for increased data integrity, when enabled. A feature that is especially useful for an isolated SPI. This error detection is only active with the checksum activated. See the *Checksum* section for details.

8.4 Device Functional Modes

8.4.1 GPIO Operation Mode

The six GPIO port pins can be configured individually in several modes: as inputs or outputs; a special $\overline{CS}$ mode; and a connection to the PGA280 internal special function register that contains control signals or indications. See Table 1 for details. The GPIO can be accessed through SPI as soon as supply voltage is connected to DVDD and DGND.

Input: Standard CMOS high-impedance input, no internal termination. Terminate externally if not used or set to output. **Note:** The GPIOs are all set as inputs after a device reset.

Output: Push-pull output. Output current is derived from DVDD and from DGND. Avoid I/O activity and high current during high-precision measurements to avoid coupled noise.

Special Function I/O: The configuration allows connecting a designated pin to the special function register (Register 12): OSCout, SYNCin, BUFAout, BUFTin, EFout, MUX2, MUX1, and MUX0. The pin must be configured as an input or output according to the pin function.

Example (CHKsum not enabled):

0x480B GPIO0, GPIO1. and GPIO3 set to output

0x4C0B GPIO0 and GPIO1 connected to MUX0 and MUX1, EFout connected to GPIO3. MUX0 and MUX1 are controlled from Register 0.

8.4.1.1 $\overline{CS}$ Mode

A special $\overline{CS}$ mode for the GPIO extends the device communications to other external SPI devices, such as data converters or shift registers. This $\overline{CS}$ function is intended for SPI communication using four isolation couplers. To use this mode, follow this procedure:

Configure the desired GPIO pins as outputs in Register 8, then configure the respective $\overline{ECS}$ (extended $\overline{CS}$) bits in Register 9.

Register 2 allows control of the clock mode by CPn (*n* for the individual $\overline{ECS}$ pins). CP = 1 asserts $\overline{ECS}$ after the last negative SCLK edge of the command; CP = 0 asserts $\overline{ECS}$ after the positive SCLK, as Figure 50 shows.

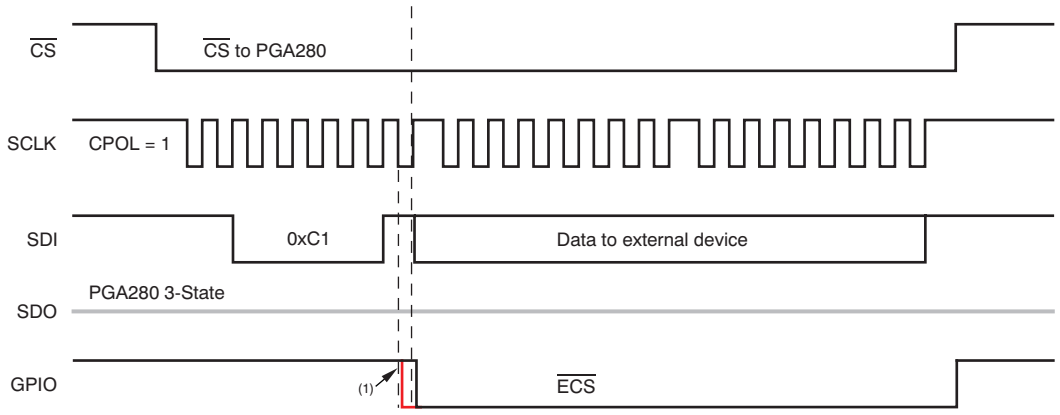
Use the $\overline{CS}$ command 1100 0cccb [ccc = $\overline{CS}$ coded for 0 to 7] to activate $\overline{ECS}$ on a single GPIO pin.

Example for $\overline{ECS}$ on pin GPIO1 (CHKsum disabled):

0x4802 GPIO1 configured output (**Note:** GPIO may output a previously stored state; default is all zeroes)

0x4902 Assign $\overline{CS}$ ($\overline{ECS}$) mode to GPIO1

0xC1 Single byte command to activate $\overline{CS}$ on GPIO1



(1) CPn = 0; the red edge applies if CPn = 1.

Figure 50. Timing for GPIO Pin Acting as $\overline{CS}$ ($\overline{ECS}$) to External Device

Device Functional Modes (continued)

This $\overline{CS}$ pin ($\overline{ECS}$) stays low as long as $\overline{CS}$ to the PGA280 is held low. The PGA280 SDO is turned to a high-impedance output (and requires external termination). The PGA280 ignores both clock and data signals during this time. Therefore, data can be read and written to another device selected by the $\overline{ECS}$ port. Communication is terminated by setting $\overline{CS}$ (to the PGA280) to high; this toggle also sets the port $\overline{ECS}$ to high and terminates the I/O transfer with the other device.

Figure 50 shows the timing for the GPIO-generated $\overline{ECS}$ pulse in clock mode SPOL = 1 (SCLK is high after $\overline{CS}$ asserts low). Register 2 allows activating SPOL = 0 by writing a 1 to the CP bit, according to SPI mode1. The initial setting is SPOL = 1.

Mode1; set bit to 1: a positive edge of SCLK follows after $\overline{ECS}$ asserts low (CP = 0). See the red edge of the GPIO trace in Figure 50.

Mode2; set bit to 0: a negative edge of SCLK follows after $\overline{ECS}$ asserts high (CP = 1). See the black edge of the GPIO trace in Figure 50.

The negative edge of SCLK senses data. The positive edge of SCLK sets data on the data out line (if applicable).

For SPI modes 0 or 3, SCLK must be inverted to indirectly sense data with the positive edge of SCLK. Figure 51 shows an example of connecting additional SPI devices, addressed by the $\overline{ECS}$. The OR connection for SDO can be a wired-OR if all devices provide a 3-state output option with the respective device $\overline{CS}$ ($\overline{ECS}$) set high.

The SPI interface allows clock rates higher than 10 MHz. Clock rates less than 10 MHz are recommended when using the $\overline{ECS}$ mode for less critical printed circuit board (PCB) layout and timing. Observe delays and distortion generated from isolation couplers. External drivers may be required to drive long and terminated cables.

With only four isolation couplers (digital galvanic isolation) connected in the SPI wires, the SPI can provide galvanic isolation for input and output channels. Figure 51 shows a block diagram of how to connect SPI devices selected by the $\overline{ECS}$ (extended $\overline{CS}$) signal.

Isolation couples or long SPI cables in harsh industrial environment are sensitive to impairments. For improved communication integrity, the communication can be extended with a checksum byte.

Figure 51 shows an example of the GPIO pins used for both the extended chip select and special functions.

The chip select ($\overline{CS}$) is connected to the PGA280 alone. The serial data input (SDI) and the serial clock (SCLK) are shared connections, and are connected to all devices [PGA280, A/D converter, and the shift register or digital-to-analog converter (DAC)]. The serial data output comes from each of the devices and are *OR*-connected or sent to an OR gate, to be received by the master. An OR gate is only required if the connected devices do not support 3-state operation. The PGA280 provides a 3-state output if not active. Pullup resistors may be required.

As mentioned previously, the GPIO pins are used to control an external multiplexer. In Figure 51, the three pins from GPIO0, GPIO1, and GPIO2 are used as a MUX address. Two other GPIO pins are used as $\overline{ECS}$ to enable communications with other slave devices.

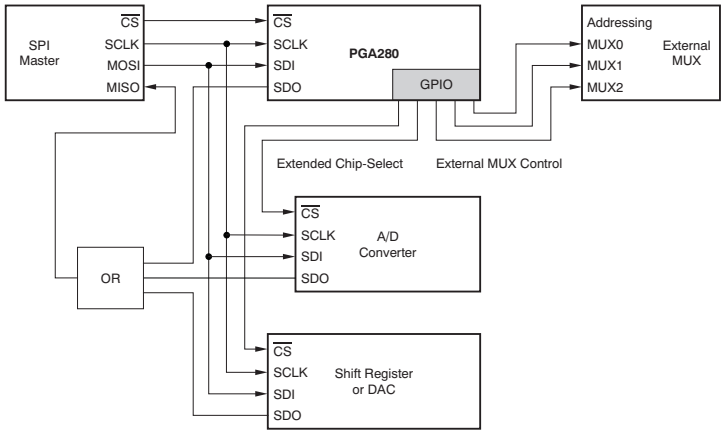


Figure 51. Example for Connecting Two Additional SPI Devices Selected by $\overline{ECS}$

8.5 Programming

8.5.1 SPI and Register Description

The serial peripheral interface uses four wires: $\overline{CS}$ (input), clock (SCLK, input), data in (SDI, or slave data input), and data out (SDO, or slave data output) and operates as a slave.

$\overline{CS}$ is active low; data are sampled with the negative clock edge. $\overline{CS}$ is insensitive to the starting condition of SCLK polarity (SPOL = 1 or 0). See Figure 52 and Figure 53.

The SPI communicates to the internal registers, starting with a byte for command and address, and followed by a single data byte (exception: *11tx 0ccc* requires no data byte). The communication can include a checksum byte. When enabled, this byte follows the last valid byte. Either power on reset or software reset (SftwrRst) disables the checksum mode. Writing to Register 11 enables or disables checksum mode.

On a read command, the device responds with the data byte and the checksum byte. If the checksum is not desired, setting $\overline{CS}$ to high terminates the transmission.

Multiple commands can be chained by holding $\overline{CS}$ low and sending the additional commands after the checksum byte (if checksum is disabled, send a dummy byte). In this mode, read and write instructions can be mixed.

This interface allows clock rates up to 16 MHz. Such high clock rates require careful board layout, short wire lengths, and low parasitic capacitance and inductance. Observe delays and distortion generated from isolation couplers. External drivers may be required to drive long and terminated cables.

8.5.2 Command Structure and Register Overview

Bit 7 is the most significant bit (MSB); bit 0 is the least significant bit (LSB). Binary numbers are denoted with *b'*. *aaaa'* is used to denote the encoded register pointer, 0000b to 1111b. *T* denotes the buffer trigger bit. Writing to unassigned bits is ignored; however, best practice is to write a 0 for all unassigned bits. PGA280 registers, addresses, and functional information are summarized in the register map shown in (Table 1.

8.5.2.1 Command Byte

01T0 aaaa dddd dddd: Write

Write 'dddd dddd' to internal PGA280 register at address *aaaa*

1000 aaaa 0000 0000: Read

Read from specified internal PGA280 register at address *aaaa* [no BUFT on read]. The number of trailing zeros provides the clock for reading data. 16 SCLK pulses are required when reading the data byte plus checksum.

00T0 aaaa:

Factory-reserved commands.

11T0 0ccc: Direct $\overline{CS}$ Command

Controls $\overline{CS}$ to pin (all pins are $\overline{CS}$-capable, but not simultaneously; only one at a time) for ccc = 0 to 6, corresponding to GPIO0 to GPIO6, if $\overline{CS}$ mode is activated.

Within the command byte, T = 1 triggers the current buffer (BUF). Each command is terminated with setting $\overline{CS}$ to high; commands can be chained within a period of $\overline{CS}$ active low, but require a checksum byte, or a dummy byte when checksum mode is disabled.

NOTE

BUF cannot be triggered during a read command.

Here are several examples (discrete commands):

Read Register 3:

Send 0x8300; response: 0xzz19 (this value is the initial setting of BUFTIM).

The first byte *zz* contains the line state (3-state) of SDO. The second byte is data.

Programming (continued)

NOTE

The PGA280 sends the CHKsum, if clocks are available while $\overline{CS}$: Send 0x830000. Response: 0xzz1937

Write Register 0:

Send 0x4018; set gain to 1V/V.

Write Register 4:

Send 0x44FF; reset all error flags.

Read Register 4:

Send 0x8400; response: 0xzz00 (no error flags set).

8.5.2.2 Extended $\overline{CS}$

The PGA280 can generate an extended chip select ($\overline{ECS}$) for other devices that are connected to the same SPI wires: SDO, SDI, and SCLK. This $\overline{ECS}$ signal redirects the SPI communication to the connected device, while the PGA280 ignores data and SCLK. The $\overline{CS}$ signal to the PGA280 must stay low during such communication; as soon as $\overline{CS}$ returns high, SPI communication is terminated. See the *GPIO Operation Mode* section for details.

8.5.2.2.1 SPI Timing Diagrams (Read and Write)

(SCLK—Data—$\overline{CS}$)

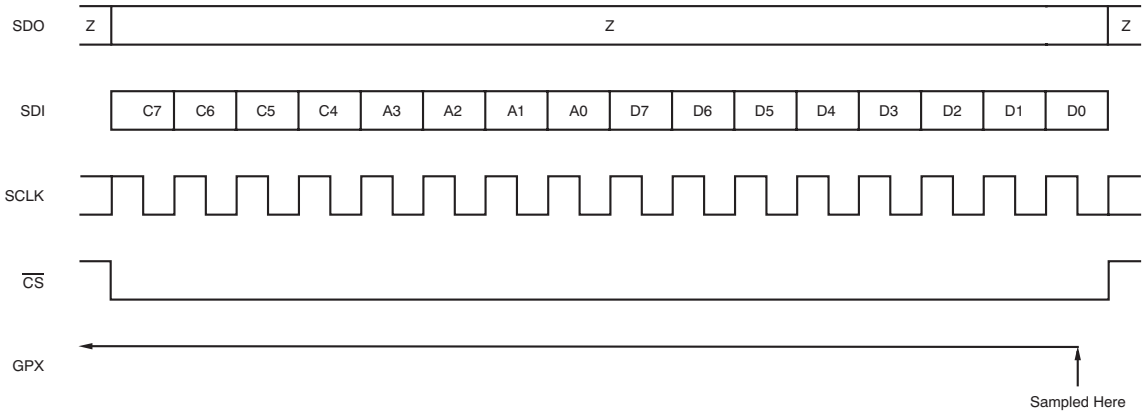


Figure 52. Write (to Device) Timing (GPX: Command Decoding); No Checksum Enabled. With Checksum, Command Decoding Occurs After 24th Falling Edge of SCLK

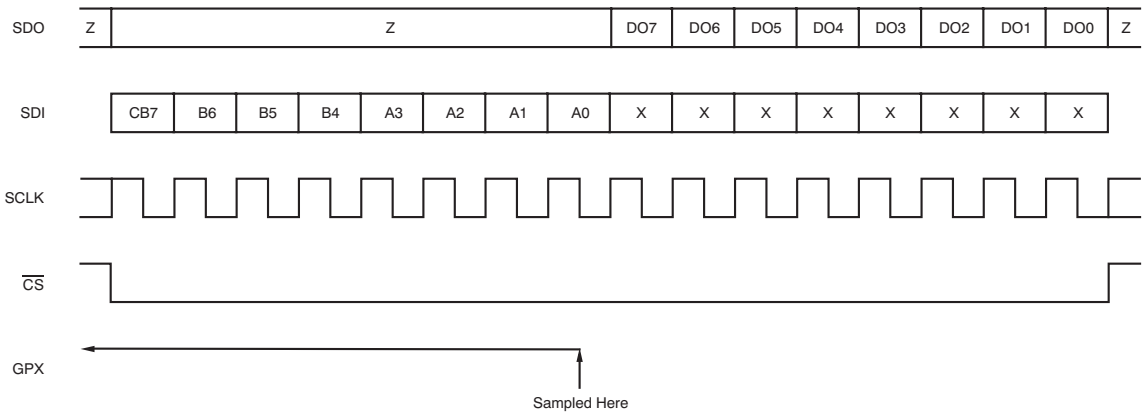


Figure 53. Read (From Register) Timing (GPX: Command Decoding); No Checksum Enabled. Falling Edge of SCLK Controls Logic

Programming (continued)

8.5.2.2.2 GPIO Pin Reference

As shown in Figure 54, the PGA280 has seven multi-function pins labeled GPIO0 through GPIO6. These pins can function as general purpose input-output (GPIO) pins either to read a digital input or to output a digital signal as an interrupt or control. GPIO functions are controlled through Register 5 and Register 8.

These pins can also be programmed to have additional special functions for the PGA280. Each of these seven pins can be used as an output for the extended chip select function ($\overline{ECS}$), using the PGA280 to redirect the SPI communications to other connected devices. $\overline{CS}$ Configuration Mode is enabled through Register 9. Additionally, Register 2 controls the clock polarity (CP) of each $\overline{ECS}$. For each bit set to 1, a positive edge of SCLK follows $\overline{CS}$ (CP = 0); for each bit set to 0, a negative edge of SCLK follows $\overline{CS}$ (CP = 1).

Together with the GPIO and $\overline{ECS}$ functions, the seven pins can perform more specialized input and output tasks as controlled by Register 12, the Special Functions Register.

GPIO0, GPIO1, and GPIO2 can be used to control an external multiplexer. If the MUX function is enabled in the first three bits of Register 12, the output value on the MUX pins is controlled through Register 0. This configuration allows for simultaneous control of the PGA280 gain and external multiplexer settings by writing to a single register.

GPIO3 can be used to output an error flag. As with bit 3 of Register 4, this option would be the logical OR of the error bits in Register 10 (IARerr, ICAerr, OUTerr, GAINerr, and IOVerr).

GPIO4 can be used as an input to trigger the current buffer. The low-to-high edge of a pulse starts the buffer with a delay of three to four clock cycles. If held high, the buffer [BUFA] remains active. The active time is extended by a minimum of three to four clock cycles in addition to the time set with FLAGTIM.

GPIO5 can be configured as an output to indicate a buffer active condition. The polarity is controlled by BUFApol of bit 5 in Register 10.

GPIO6 can be configured as either an output or an input with the Special Functions Register. With Bit 7, OSCOUT connects the internal oscillator to GPIO6. With Bit 6, SYNCIN allows an external oscillator to provide the master clock to the PGA280.

To use any of these functions, Register 8 must first be set to 0 for input or to 1 for an output (for GPIO, $\overline{ECS}$, or special function).

Once set, any 1s in Register 9 supersede the GPIO function for the related pin, allowing for $\overline{CS}$ configuration.

Likewise, any 1s in Register 12 supersede the GPIO function and $\overline{CS}$ configuration, allowing for any of the pin-specific special functions to operate.

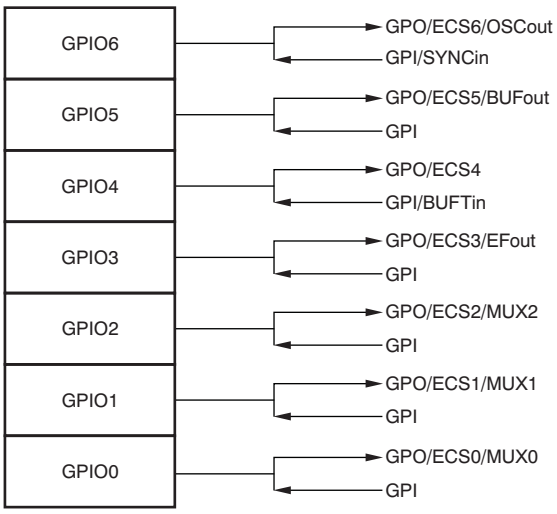


Figure 54. Special Function to Pin Assignment Reference

Programming (continued)

8.5.2.2.3 Checksum

SPI communication can be secured by adding a checksum byte to the write and read data. If this mode is activated by setting CHKsumE (bit 0 in Register 11), the PGA280 expects a valid checksum; otherwise, the device ignores the received data and sets CHKerr in Register 4. This event may require a Register 4 read after each write completes. The PGA280 always responds to a read with checksum if sufficient SCLK pulses (16) are provided after the command byte.

A straight checksum (ignore carry) with a starting value of 0x9B, an 8-bit byte, is used. Polynomial value: 1001 1010b = 0x9B (*b* denotes binary, *0x* denotes hex coding)

Write to device: Command byte + Data byte + CHKsum byte

CHKsum = Polynomial value + Command byte + Data byte*****;

Read command to device = Command byte + CHKsum byte

Response: Data byte + CHKsum byte

CHKsum = Polynomial value + Command byte + Data byte

*****The command for activating the $\overline{CS}$ on a GPIO pin (after configuration) is only a command byte: 11Tx 0ccc.

Example: 0xC15C. This instruction activates $\overline{CS}$ on GPIO1. The 5C is the checksum [(0x9B + 0xC1) mod 0x100 = 0x5C]

The checksum is calculated only for the communication to or from the PGA280. In extended SPI mode, if connecting the $\overline{CS}$ ($\overline{ECS}$) for other SPI devices to the PGA280 port, the external device has to provide its own checksum character, if available.

Examples:

0x4101DD Send Reset [CHKsum calculation: (0x9B + 0x41 + 0x01) mod 0x100 = 0xDD]

0x4B11F7 Activate CHKsum bit 0 of Register 11. Note that activation of the CHK bit requires proper Checksum.

0x8B260000 Read Configuration Register 11 (contains 0x11) [0x9B + 0x8B = 0x26]

0x1137 Response includes the CHKsum [0x9B + 0x8B + 0x11 = 0x37]

0x44FFDF Reset all error flags in Register 4 [0x9B + 0x44 + 0xFF = 0xDF]

0x841F0000 Read Register 4 [0x9B + 0x84 = 0x1F]

0x001F No errors indicated if 00 [0x9B + 0x84 + 0x00 = 0x1F]

Commands can be chained while $\overline{CS}$ is active low; all bytes are added for checksum:

Examples:

0x4C 07 EE; Activate MUX0, MUX1, and MUX2 to GPIO0, GPIO1, and GPIO2, respectively

0x64 FF FE 40 1B 59 80 D9 00 00; Write to Register 4 with BUF trigger and reset all error flags

: Write to Register 0 and set gain 1 V/V; MUX0 and MUX1 set high

: Read Register 0, provide 16 SCLKs

Programming (continued)

8.5.3 GPIO Configuration

Register priority: If GPIO pins are used, follow this procedure:

First, configure individual I/O bits as either inputs or outputs (Register 8); 0 = input, 1 = output. Bits B0 to B6 are connected to GPIO0 to GPIO6, respectively.

Then, configure individual bits to the desired function. When configuring for output, set the Data Register (Register 5) first to avoid glitches.

To configure the GPIO pins for the $\overline{CS}$ function (see Register 9):

- Configure $\overline{ECS}$ (0 = disable, 1 = enable). If set to 1 and the I/O configuration is set to output as well, this pin becomes $\overline{ECS}$. Details of this configuration are described in GPIO Operation Mode, *$\overline{CS}$ Mode*.
- Configure for clock polarity (CP), relative to $\overline{ECS}$ in Register 2; see Register 9. Set this bit to 0: a negative edge of SCLK follows $\overline{ECS}$ (CP = 1). Set this bit to 1: a positive edge of SCLK follows $\overline{ECS}$ (CP = 0).
- Configure for special function (Register 12): Special function signals can be assigned to the GPIO pins in this manner: 0 = disable, 1 = enable. Pins *xxout* must be configured as outputs, and *xxin* must be configured as inputs in Register 8.
- GPIO data to force (Register 5) GPIO data (1 = low, 0 = high). Forcing a bit, which is assigned to a special function, may be stored until GPIO is enabled.

NOTE

Data may be stored in internal registers and therefore may show on a given GPIO pin after the configuration is changed.

8.5.4 Buffer Timing

The buffer is used to isolate fast transients from the overload protection of the high-precision amplifier. The buffer avoids current into the overload clamp. Fast transients result from the switching transient of a signal multiplexer or a gain change; these transients cannot be filtered in the signal path.

The buffer can be turned on by software using the T bit in the SPI command or by activating a GPIO pin. The on-time of the buffer is set in Register 3 (BUFTIM).

If controlled by software command, the buffer turns active (indicated by BUFA shown in Figure 55) with the last falling edge of SCLK.

Controlling an external MUX through Register 0 activates the GPIO pins after the rising edge of $\overline{CS}$, providing an extra delay.

Alternatively, the buffer can be controlled by GPIO4, after configuration (Register 8, bit 4 = 0, and 0x4C10). A rising edge triggers the buffer with a delay of three to four clock cycles. If held high, the buffer [BUFA] remains active. The active time is extended by a minimum of three to four clock cycles plus FLAGTIM.

The buffer active condition can be observed at GPIO5, after configuration for output and special function (0x4820, 0x4C20). The time reference is the end of $\overline{CS}$. The buffer is turned on with the 16th falling edge of the SCLK and writing to Register 0 (0x6018). BUFA stays high for 6 μs (BUFTIM0) after $\overline{CS}$.

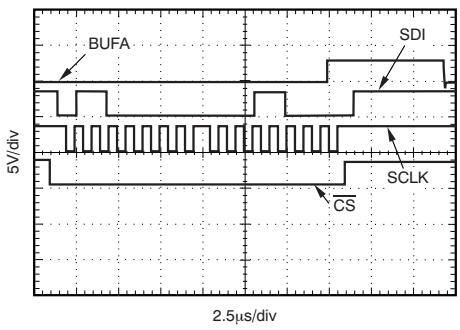


Figure 55. BUFA Timing

8.6 Register Map

Table 1. Register Map(1)

REGISTER (Decimal, [Hex])(2)	aaaa (Binary)	R/W	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION	RESET VALUES(3)
0	0000	W/R	G4	G3	G2	G1	G0	MUX2	MUX1	MUX0	Gain and optional MUX register	0000 0000b
1	0001	W								SftwrRstNote2x	Write-only register, soft reset, write 1	0000 0000b
2	0010	W/R		CP6	CP5	CP4	CP3	CP2	CP1	CP0	SPI-MODE selection to GPIO-pin	0000 0000b
3	0011	W/R			BUFTIM5	BUFTIM4	BUFTIM3	BUFTIM2	BUFTIM1	BUFTIM0	Set BUF time-out	0001 1001b
4	0100	W/R	CHKerr	IARerr	BUFA	ICAerr	EF	OUTerr	GAINerr	IOVerr	Error Register; reset error bit: write 1	0000 0000b
5	0101	W/R		GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	GPIO Register Data force out or sense	0000 0000b
6	0110	W/R		SW-A1	SW-A2	SW-B1	SW-B2	SW-C1	SW-C2	SW-D12	Input switch control 1	0110 0000b
7	0111	W/R					SW-F1	SW-F2	SW-G1	SW-G2	Input switch control 2	0000 0000b
8	1000	W/R		DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0	Configure pin to out = 1 or in = 0	0000 0000b
9	1001	W/R		ECS6	ECS5	ECS4	ECS3	ECS2	ECS1	ECS0	Extended $\overline{CS}$ mode (1 = enable)	0000 0000b
10 [A]	1010	W/R	MUX-D dis	IARerr dis	BUFAPol at pin	ICAerr dis	ED BUFA suppress	OUTerr dis	GAINerr dis	IOVerr dis	Various configuration settings	0000 0000b
11 [B]	1011	W/R	LTD		FLGTIM3	FLGTIM2	FLGTIM1	FLGTIM0	Reserved	CHKsumE	Various configuration settings	0001 0000b
12 [C]	1100	W/R	OSCout	SYNCin	BUFAout	BUFTin	EFout	MUX2	MUX1	MUX0	Special function register	0000 0000b
	PIN			GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	Register bit reference to GPIO pin(4)	

(1) Blank register bits are ignored and undefined.
(2) Registers 13 to 15 are for test purposes; read-only.
(3) Power-on reset values are SftwrRst values.
(4) Details for GPIO pin assignments are shown in Figure 54.

8.6.1 Register 0: Gain and External MUX Address (address = 00h) [reset = 0000 0000b]

Figure 56. Register 0: Gain and External MUX Address (Read = 0x8000; Write with BUF Off = 0x40, Write with BUF On = 0x60)

7	6	5	4	3	2	1	0
G4	G3	G2	G1	G0	MUX2	MUX1	MUX0
0	0	0	0	0	0	0	0

Bit Descriptions:

G4: Output stage gain setting. This setting is independent of the gain selected in the input stage and acts as a multiplication factor to the input gain.

0 = 1 V/V output gain (power-on default)

1 = 1.375 V/V output gain (= 1⅜ V/V)

G[3:0]: Input stage gain setting. Refer to Table 2.

MUX[2:0]: These ports can be used to control an external multiplexer.

Table 2. Input Stage Gain Settings

G3	G2	G1	G0	Gain
0	0	0	0	1/8
0	0	0	1	1/4
0	0	1	0	½
0	0	1	1	1
0	1	0	0	2
0	1	0	1	4
0	1	1	0	8
0	1	1	1	16
1	0	0	0	32
1	0	0	1	64
1	0	1	0	128
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

8.6.2 Register 1: Software Reset Register (address = 01h) [reset = 0000 0000b]

Figure 57. Register 1: Software Reset Register (Write = 0x4101; Write with Checksum = 0x4101DD)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	SftwrRst
0	0	0	0	0	0	0	0

Bit Descriptions:

SftwrRst: Software Reset.

Setting this bit to 1 generates a system reset that has the same effect as a power-on reset. All registers are reset to the respective default values; this bit self-clears.

8.6.3 Register 2: SPI: MODE Selection to GPIO-Pin (address = 02h) [reset = 0000 0000b]

Figure 58. Register 2: SPI: MODE Selection to GPIO-Pin (Read = 0x8200, Write = 0x012)

7	6	5	4	3	2	1	0
—	CP6	CP5	CP4	CP3	CP2	CP1	CP0
0	0	0	0	0	0	0	0

Bit Descriptions:

CP[6:0]: SPI mode1 or mode2 can be configured for each individual $\overline{\text{ECS}}$ (extended CS) output if activated in Register 9. See *$\overline{CS}$ Mode* in GPIO Operation Mode for details. CP6 controls ECS6, for example. For SPI mode1, set the respective bit to 1: a positive edge of SCLK follows $\overline{\text{CS}}$ (Clock Polarity, CP = 0). For SPI mode2, set the respective bit to 0: a negative edge of SCLK follows $\overline{\text{CS}}$ (CP = 1). See also Figure 50.

8.6.4 Register 3: BUF Timeout Register (address = 03h) [reset = 0001 1001b]

Figure 59. Register 3: BUF Timeout Register (Read = 0x8300, Write = 0x43)

7	6	5	4	3	2	1	0
—	—	BUFTIM5	BUFTIM4	BUFTIM3	BUFTIM2	BUFTIM1	BUFTIM0
0	0	0	1	1	0	0	1

Bit Descriptions:

BUFTIM[5:0]: Defines BUF timeout length. The LSB equivalent is 4 * t CLK (nominal value is 4 µs with a 1-MHz clock). Setting this register to 0x00 disables the BUF. The minimum timeout length that can be set is approximately 6 µs. The default/POR setting sets BUFA time on to 100 µs. The BUFA bit of the Error Register [D5] indicates the buffer active status. See Figure 55.

8.6.5 Register 4: Error Register (address = 04h) [reset = 0000 0000b]

The Error Register flags activate whenever an error condition is detected. These flags are cleared when a 1 is written to the error bit.

Figure 60. Register 4: Error Register (Read = 0x8400, Write = 0x44)

7	6	5	4	3	2	1	0
CHKerr	IARerr	BUFA	ICAerr	EF	OUTerr	GAINerr	IOVerr
0	0	0	0	0	0	0	0

Bit Descriptions:

CHKerr: Checksum error in SPI. This bit is only active if checksum is enabled. This bit is set to 1 when the checksum byte is incorrect.

IARerr: Input Amplifier Saturation

BUFA: Buffer Active

ICAerr: Input Clamp Active

EF: Error Flag. Logic OR combination of error bits of Register 10. This bit can be connected to GPIO3 pin if the bit is configured for output (Register 8) and as a special function (Register 12).

OUTerr: Output Stage Error (allow approximately 6µs activation delay).

GAINerr: Gain Network Overload

IOerr: Input Overvoltage

8.6.6 Register 5: GPIO Register (address = 05h) [reset = 0000 0000b]

Figure 61. Register 5: GPIO Register (Read = 0x8500, Write = 0x45)

7	6	5	4	3	2	1	0
—	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0	0	0	0	0	0	0	0

Bit Descriptions:

GPIO[6:0]: The GPIO bits correspond to GPIO6 through GPIO0, respectively. The function of each bit depends on whether the GPIO pin is configured as an input pin or an output pin, which is determined by the setting in Register 8. When the GPIO pin is configured as an input, reading this register samples the GPIO pin. When the GPIO pin is configured as an output, reading from this register reads back the forced data.

8.6.7 Register 6: Input Switch Control Register 1 (address = 06h) [reset = 0110 0000b]

Figure 62. Register 6: Input Switch Control Register 1 (Read = 0x8600, Write = 0x46)

7	6	5	4	3	2	1	0
—	SW-A1	SW-A2	SW-B1	SW-B2	SW-C1	SW-C2	SW-D12
0	1	1	0	0	0	0	0

Bit Descriptions:

Switch control; see Figure 44 for switch designation (switch closed = 1).

Example: Select INP2 and INN2: 0x18 // opens A1 and A2, and closes B1 and B2.

8.6.8 Register 7: Input Switch Control Register 2 (address =07h) [reset = 0000 0000b]

Figure 63. Register 7: Input Switch Control Register 2 (Read = 0x8700, Write = 0x47)

7	6	5	4	3	2	1	0
—	—	—	—	SW-F1	SW-F2	SW-G1	SW-G2
0	0	0	0	0	0	0	0

Bit Descriptions:

Switch control; see Figure 44 for switch designation.

8.6.9 Register 8: GPIO Configuration Register (address = 08h) [reset = 0000 0000b]

Figure 64. Register 8: GPIO Configuration Register (Read = 0x8800, Write = 0x48)

7	6	5	4	3	2	1	0
—	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
0	0	0	0	0	0	0	0

Bit Descriptions:

DIR[6:0]: GPIO configuration for input or output; 0 for input; 1 for output. Power-on default is all *inputs* (requires external termination or set to output).

8.6.10 Register 9: $\overline{CS}$ Configuration Mode Register (address = 09h) [reset = 0000 0000b]

Figure 65. Register 9: $\overline{CS}$ Configuration Mode Register (Read = 0x8900, Write = 0x49)

7	6	5	4	3	2	1	0
—	ECS6	ECS5	ECS4	ECS3	ECS2	ECS1	ECS0
0	0	0	0	0	0	0	0

Bit Descriptions:

ECS[6:0]: Configure $\overline{CS}$ function to respective pins. See $\overline{CS}$ Mode, in the *GPIO Operation Mode* section (a single byte command applies).

8.6.11 Register 10: Configuration Register 1 (address = 0Ah) [reset = 0000 0000b]

Figure 66. Register 10: Configuration Register 1 (Read = 0x8A00, Write = 0x4A)

7	6	5	4	3	2	1	0
MUX-D	IARerr	BUFA Pol	ICAerr	ED BUFA	OUTerr	GAINerr	IOVerr
0	0	0	0	0	0	0	0

Bit Descriptions:

MUX-D: Set this bit to 1 to disable MUX control from Register 0; set to 0 after reset.

BUFA Pol: Controls BUF active indication polarity. Set to 0 for high = active; set to 1 for low = active.

ED BUFA Suppress: Error detection is normally disabled during BUFA active. Errors are not suppressed if ED BUFA = 1.

Error flags are logic OR-combined and connected to the EFout in Register 12 as well as connected to the GPIO3 output pin if configured. The EFout signal is active high. Assigned errors can be disabled individually using this OR function, with the exception of CHKerr, by writing a 1 to the error bit position. [IARerr; ICAerr; OUTerr; GAINerr; IOVerr]

8.6.12 Register 11: Configuration Register 2 (address = 0Bh) [reset = 0001 0000b]

Figure 67. Register 11: Configuration Register 2 (Read = 0x8B00, Write = 0x4B)

7	6	5	4	3	2	1	0
LTD	—	FLGTIM3	FLGTIM2	FLGTIM1	FLGTIM0	Reserved	CHKsumE
0	0	0	1	0	0	0	0

Bit Descriptions:

LTD: Individual error signals are not latched if this bit is set to 1. With EFout activated on GPIO3, the error condition can be observed in real time, but error suppression time is applied. Clear errors in Register 4 after writing 1 to this bit.

FLAGTIM0 to 3: Choose the number of clock cycles (nominally 1 MHz) according to Table 3 for suppression of the error flags in Register 4. The timeout starts after the end of BUFA. Alternatively, the timeout can start with the event if the buffer is not active or Register 10, bit 3 is set high. Allow delayed activation for the individual error sources in the microsecond range.

CHKsumE: Checksum is enabled by writing a 1 to bit 0. A correct checksum is always required for enabling. After this bit is set, all communication to the device requires a valid checksum, until 0 is written to this bit. Alternatively, a software reset [0x4101DD] or power-on reset can be performed to reset this function.

Table 3. Error Flag Suppression Time

FLGTIM [3:0]	CLOCK CYCLES(1)
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	12
1010	16
1011	24
1100	32
1101	48
1110	64
1111	127

(1) Clock cycles refer to internal clock or SYNCin; nominally 1 MHz.

8.6.13 Register 12: Special Functions Register (address = 0Ch) [reset = 0000 0000b]

Figure 68. Register 12: Special Functions Register (Read = 0x8C00, Write = 0x4C)

7	6	5	4	3	2	1	0
OSCout	SYNCin	BUFAout	BUFTin	EFout	MUX2	MUX1	MUX0
0	0	0	0	0	0	0	0

Bit Descriptions:

Special function pin designation: Set to 1 for activation.

OSCout: Internal oscillator connected to pin GPIO6 for output (GPIO6 configured as an output).

SYNCin: External connection for external oscillator input to pin GPIO6 (GPIO6 configured as an input).

BUFAout: Pin GPIO5 indicates a buffer active condition (if configured as an output). The BUFA output signal is active high by default, but can be inverted to active low by BUFA Pol.

BUFTin: The current buffer can be triggered externally by pin GPIO4, if configured as an input. The low-to-high edge of a pulse starts the buffer with a delay of three to four clock cycles. If held high, the buffer [BUFA] remains active. The active time is extended by a minimum of three to four clock cycles plus the time set with FLAGTIM.

EFout: A logic OR combination of error bits; see Register 10. This flag can control GPIO3 if this pin is configured as an output and EFout = 1.

MUX2 to MUX0: If the GPIO pins are configured as outputs and these bits are set to 1, the GPIO pins are controlled from Register 0 (if MUX-D = 0).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 External Clock Synchronization

The PGA280 uses a 1-MHz internal oscillator, nominally. This clock can be brought out to pin GPIO6 if configured by the internal register setting to allow synchronization of external systems to this clock. If the PGA280 must be controlled by an external clock, GPIO06 can be configured as an oscillator input, thus overriding the internal oscillator. In order to maintain stable device performance, the frequency must be within the specified range shown in the *Electrical Characteristics*. The clock pulse duration is not critical, because this duration is internally divided down; however, less than 30% deviation is recommended. The GPIO6 input assumes a standard logic signal. Prevent overshoot at this pin, and provide approximately equal rise and fall times for the lowest influence on offset voltage as a result of coupled noise.

Expect a small amount of additional noise during the transition from the internal to external clock, or vice versa, for approximately eight clock periods because of phase mismatch.

9.1.2 Quiescent Current

The PGA280 uses internal resistor networks and switches to set the signal gain. Consequently, the current through the resistor network may vary with the gain and signal amplitude. Under normal operation, the gain-related current is low (< 400 μA). However, in signal overload conditions while a high gain is selected, this amount of current can increase.

9.1.3 Settling Time

The PGA280 provides very low drift and low noise, and therefore allows repeatable settling to a precise value with a negligible tail. Signal-related load and power dissipation variables have minimal effect on device accuracy.

9.1.4 Overload Recovery

Overload conditions can vary widely. There are multiple points in an instrumentation amplifier that can be overloaded. During input overload, the PGA280 folds the output signal partially back as a result of the differential signal structure and summing, but the error flags indicate such fault conditions. The amplifier recovers safely after removing the overload condition, if the amplifier is within the specified operating range shown in Figure 69.

Avoid dynamic overload by using adequate signal filtering that reduces the input slew rate to that of the amplifier. Fast signal jumps produced from multiplexed signal sources or gain changes cannot normally be filtered, but in such situations, the current buffer (BUF) stage can be activated to prevent current flowing through the input into the protection clamp.

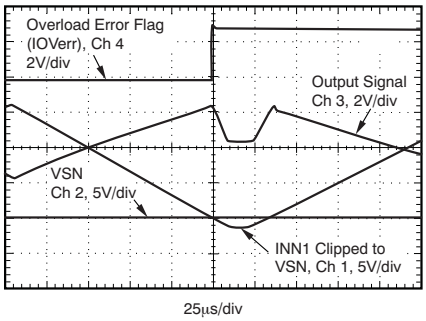


Figure 69. Input Clipping: Negative Side

10 Power Supply Recommendations

The PGA280 can connect to three supply voltages: the high-voltage analog supply, the low-voltage output amplifier supply, and the digital I/O supply. This architecture allows an optimal interface (level-shift) to the different supply domains.

The high-voltage analog supply, VSP and VSN, powers the high-voltage input section. The substrate of the IC is connected to VSN; therefore, VCN must be connected to the most negative potential.

The low-voltage analog output supply, VSOP and VSON, can operate within the high-voltage supply boundaries with two minimal limitations:

1. The usable range for VSON is from a minimum 5 V below VSP to as low as VSN. This 5 V provides the headroom for the output supply voltage of 2.7 V to 5 V. Even with less than 5V supply, this voltage difference is required for proper operation.
2. The common-mode control input, VOCM, requires a voltage at least 2 V from VSP, in order to support internal rail-to-rail performance.

These limits may only come into consideration when using a minimum supply or an extremely asymmetrical high-voltage supply. In most practical cases, VSON is connected to the ground of the system 3-V or 5-V supply.

VSOP can be turned on first or can be higher than VSP without harm, but operation fails if VSP and VSN are not present.

Observe the maximum voltage applied between VSOP and VSON, because there is no internal protection. This consideration is the same as with other standard operational amplifier devices.

The digital supply, DGND and DVDD, can also be set within the boundaries of VSP and VSN. Only the positive supply, DVDD, cannot be closer than 1 V less than VSP. DVDD can be turned on without the analog supply being present and is operational, but limited to digital functions in this case. The maximum supply voltage must be observed because there is no internal protection. VSOP and VSON can be connected with DVDD and DGND, if desired.

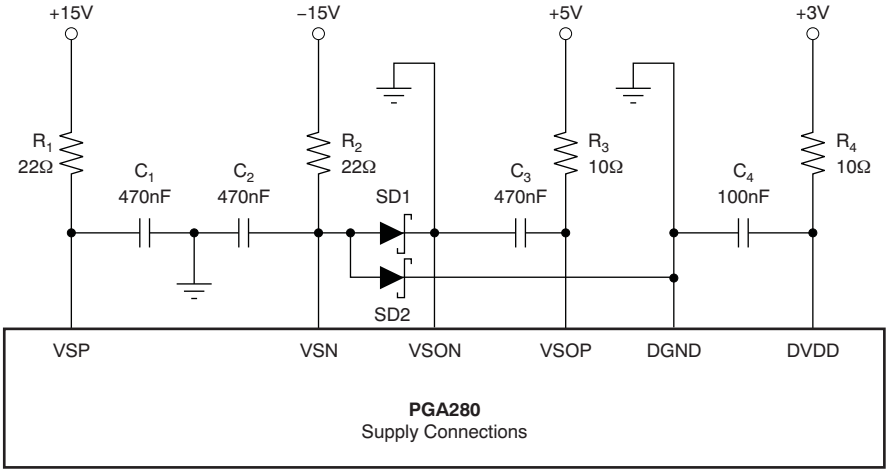
Current consumption of the digital supply is very low under static conditions, but increases with communications activity. Assuming no external load except the 20 pF load to SDO, with an SCLK = 10 MHz and a 3-V supply, the current momentarily increases by approximately 0.6 mA when reading a register. With a 5-V digital supply, the increase is in the range of 0.8 mA. This additional current is only required during communication; a larger bypass capacitor can supply this current. Driving current into SDO would further increase the current demand.

VSN is connected to the substrate; therefore, the voltage at VSON or DGND must not turn on the substrate diode to VSN. Use external Schottky diodes from VSON to VSN and from DGND to VSN (see Figure 70) to prevent such a condition.

The PGA280 uses an internal chopper technology, and therefore works best with good supply decoupling. Series resistors in the supply are recommended to build an RC low-pass filter. With the small supply current, these series resistors can be in the range of 15 Ω to 22 Ω. The RC filter also prevents a very fast rise time of the supply voltage, thus avoiding parasitic currents in the device. Connecting supply wires into an already-turned on supply (very fast rise time) without such a filter can damage the device as a result of voltage overshoot and parasitic charge currents. Figure 70 shows an example of a supply connection using RC bypass filters. DVDD may not need decoupling, but if the digital supply is noisy, a filter is recommended at C_4 and R_4.

NOTE

Rise and fall times for the high-voltage supplies must be slower than 1 V/μs.



NOTE: In this example, the Schottky diodes prevent substrate reversing. The supply voltages shown are only example values.

Figure 70. Supply Connection Example Using RC Bypass Filters for Good Decoupling

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 商標

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA280AIPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA280A	Samples
PGA280AIPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA280A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

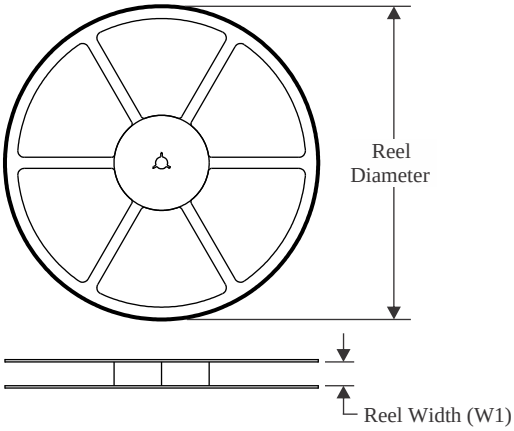
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

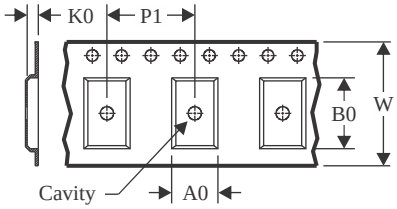
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

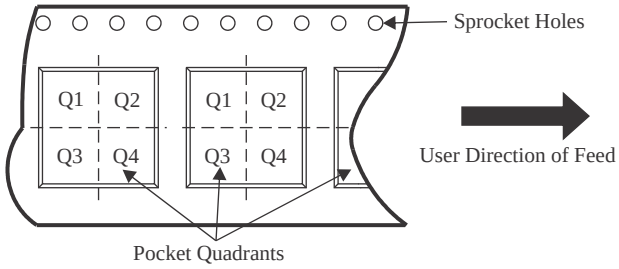


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

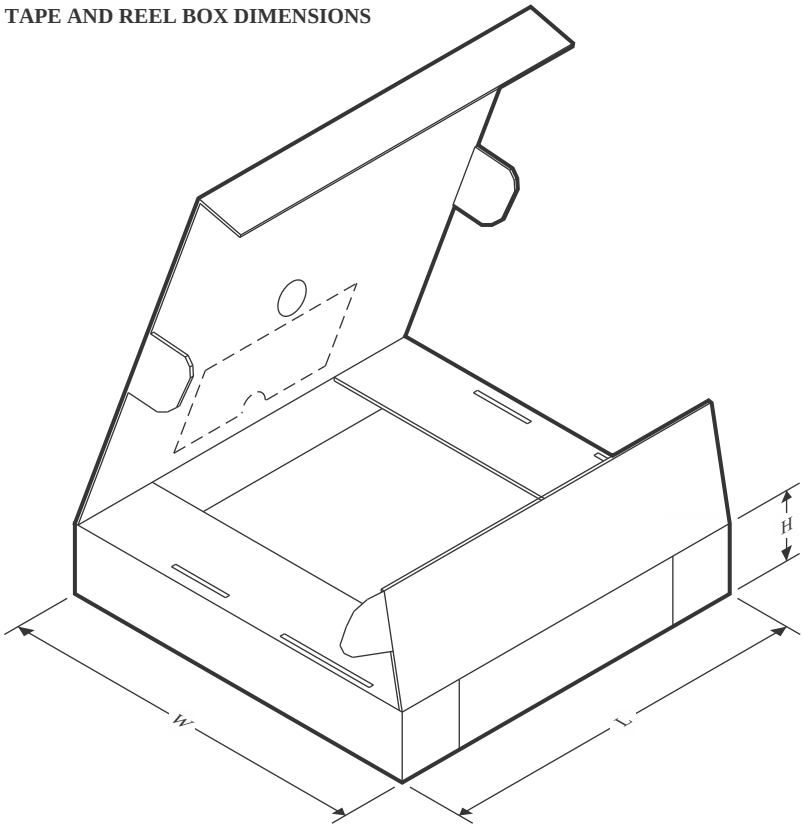
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA280AIPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

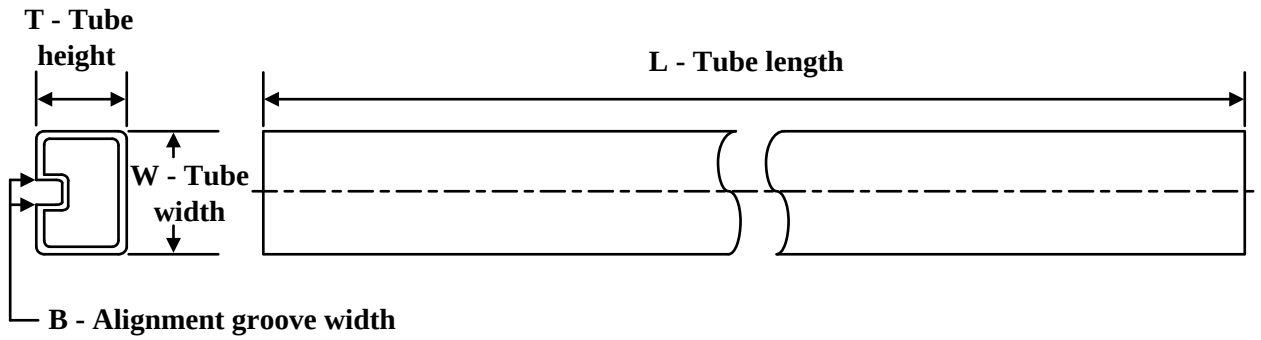
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA280AIPWR	TSSOP	PW	24	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

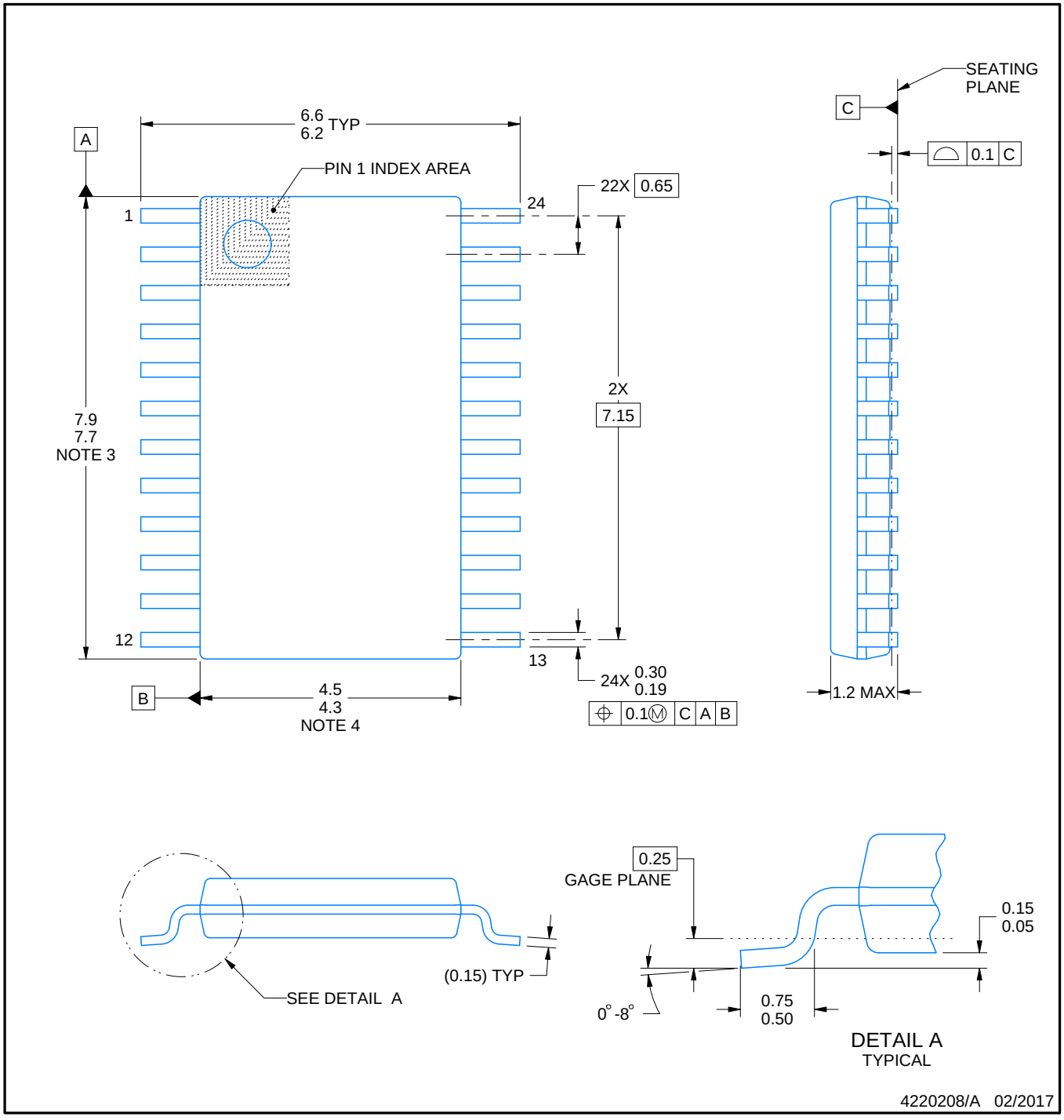
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PGA280AIPW	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

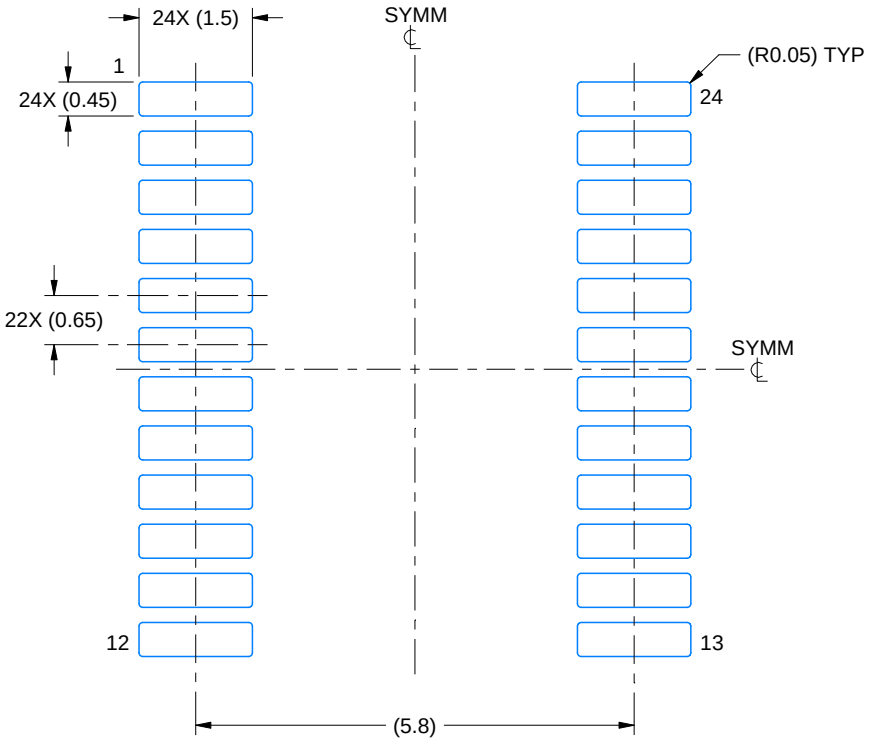
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

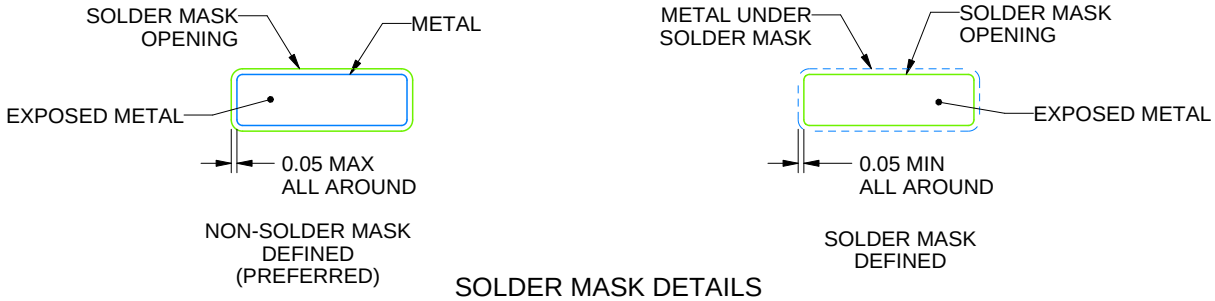


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

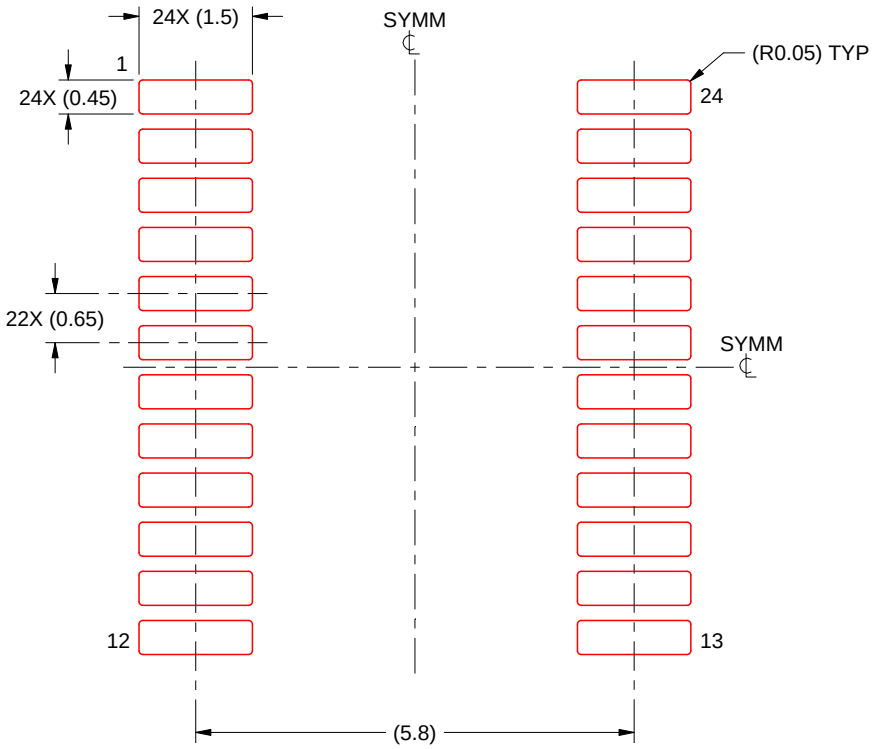


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265