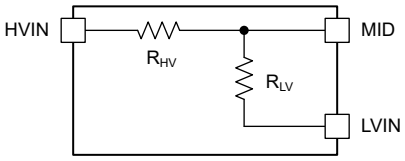
RES60A-Q1 車載対応、1400V_{DC}、高精度抵抗分割器

1 特長

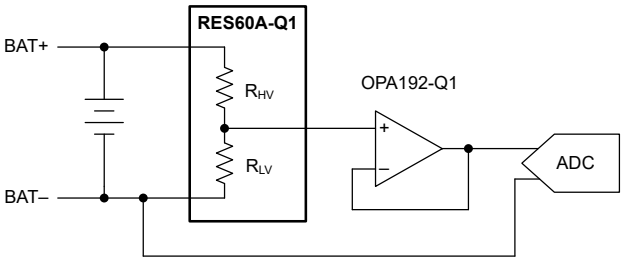
- 車載アプリケーション用に AEC-Q200 認定済み:
  - 温度グレード 1:-40℃～+125℃
- 高い電圧定格:
  - 4000V_{DC} (60 秒) で 3 回以上の HiPOT 試験に合格
  - HVIN と LVIN の間で 1700V_{DC} の沿面距離および空間距離をサポート (IEC-61010 PD 2)
- 低いシフトおよびドリフトで高い DC 精度を実現:
  - 初期比率マッチング精度:±0.1% (最大値)
  - 低いドリフト:±1ppm/°C (標準値)
  - 長い時間が経過しても全温度範囲にわたって ±0.2% の精度
- 低熱ノイズ (1kHz) 薄膜抵抗:
  - 30nV/√Hz (210:1 の比率)
  - 25nV/√Hz (310:1 の比率)
  - 22nV/√Hz (410:1 の比率)
  - 20nV/√Hz (500:1 の比率)
  - 18nV/√Hz (610:1 の比率)
  - 14nV/√Hz (1000:1 の比率)

2 アプリケーション

- 高電圧バスおよびバッテリ電圧監視
  - HEV/EV のバッテリ管理システム (BMS)
  - HEV/EV の DC/DC コンバータ
  - HEV/EV のオンボード チャージャ (OBC)
  - HEV/EV のインバータおよびモータ制御
- 非絶縁型、同一のグランド、常時オンの分割器
- 広同相範囲アンプ



機能ブロック図



代表的な回路図

3 概要

RES60A-Q1 は、マッチングされた抵抗分割器で、テキサス・インスツルメンツの最新の高性能アナログ ウエハ プロセスで薄膜 SiCr に実装されています。高品質の SiO_2 絶縁層は抵抗器をカプセル化し、継続的動作で最大 1400V_{DC}、HiPOT テスト (60 秒) で最大 4000V_{DC} という非常に高い電圧で使用できるようにします。このデバイスは、公称入力抵抗 R_{HV} = 12.5MΩ であり、幅広いシステムの要求を満たすため、いくつかの公称比率で供給されます。

RES60A-Q1 シリーズは高い比率マッチング精度を特長としており、各分割器の測定比率は公称値の ±0.1% (最大) 以内です。この精度は、仕様温度範囲全体で維持され時間が経過しても、累積ドリフトはわずか ±0.2% (最大) です。したがって、キャリブレーションなしの RES60A-Q1 の生涯耐性は、±0.3%の (max) 内に収まります。

RES60A-Q1 は、AEC-Q200 温度グレード 1 で車載認定済みで、–40°C～125°C の仕様温度範囲を満たしています。このデバイスは、8 ピン SOIC パッケージで供給され、公称本体サイズが 7.5mm × 5.85mm で、高電圧ピンと低電圧ピンの間の沿面距離と空間距離が 8.5mm 以上あります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
RES60A-Q1	DWV (SOIC、8)	5.85mm × 11.5 mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

製品情報

部品番号	公称比 (R_{HV}:R_{LV})
RES60A210-Q1 (1)	210:1
RES60A310-Q1	310:1
RES60A410-Q1	410:1
RES60A500-Q1	500:1
RES60A610-Q1 (1)	610:1
RES60A100-Q1	1000:1

(1) プレビュー情報 (事前情報ではありません)。

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Pin Configuration and Functions

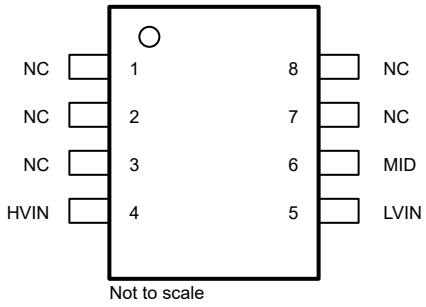


図 4-1. DWV Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
HVIN	4	Input	High-voltage input of divider
LVIN	5	Input	Low-voltage input of divider
MID	6	Output	Center tap of divider
NC	1, 2, 3	—	Noninternally-connected pins on high-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.
NC	7, 8	—	Noninternally-connected pins on low-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Maximum short-term overload voltage per divider, $\Delta V = V_{HVIN} - V_{LVIN}$ (100ms, T_A = 25°C)(2) (3)	RES60A210		2700	V
		RES60A310		2700	
		RES60A410		2700	
		RES60A500		2700	
		RES60A610		2700	
		RES60A100		2700	
	Transient high-potential voltage, ac (50Hz, T_A = 25°C)(4) (5) (6)	RES60A210		3000	V_{RMS}
		RES60A310		2500	
		RES60A410		2500	
		RES60A500		3000	
		RES60A610		3000	
		RES60A100		3000	
	Transient high-potential voltage, dc (T_A = 25°C)(4) (5) (6)	RES60A210		4000	V_{DC}
		RES60A310		3500	
		RES60A410		3500	
		RES60A500		4000	
		RES60A610		4000	
		RES60A100		4000	
T_A	Ambient temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	175	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum short-term voltage permitted under transient conditions without performance degradation. Avoid sustained operation at or beyond these voltage levels, especially if the resulting self-heating causes T_J to exceed 150°C.
(3) Tested in production.
(4) Differential voltage from high-voltage domain (pins 1-4) to low-voltage domain (pins 5-8) of the package.
(5) Total stress duration of 180s, accumulated over lifetime in increments of no longer than 60s periods, duty cycle < 10%. Repeated transient high-potential voltage testing can lead to performance degradation or device damage.
(6) Rating for Advanced-Information and preview devices only. Final value for Production-Data devices is pending.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1), all pins except 5 and 6		±4000	V
		Human body model (HBM), per AEC Q100-002(1), pins 5 and 6	RES60A210, RES60A500, RES60A610, RES60A100	±2000	
			RES60A310, RES60A410	±1500	
		Charged device model (CDM), per AEC Q100-011		±1500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ADVANCE INFORMATION

ADVANCE INFORMATION

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Maximum sustained dc voltage per divider (HVIN pin to LVIN pin, 10 years at T_A = 25°C)(1)	RES60A210			1400	V_{DC}
		RES60A310			1400	
		RES60A410			1400	
		RES60A500			1400	
		RES60A610			1400	
		RES60A100			1400	
	Maximum sustained 50Hz ac voltage per divider (HVIN pin to LVIN pin, 10 years at T_A = 25°C)(1)	RES60A210			760	V_{RMS}
		RES60A310			760	
		RES60A410			760	
		RES60A500			760	
		RES60A610			760	
		RES60A100			760	
T_A	Ambient temperature		–40		125	°C

(1) Assumes $R_{\theta JA}$ = 111.2°C/W.

5.4 Thermal Information

THERMAL METRIC(1)		RES60A-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at ΔV = 1000V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RESISTANCE							
R_{HV}	Input resistance				12.5		MΩ
R_{LV}	Ratio-dependent resistance	RES60A210			59.5		kΩ
		RES60A310			40.3		
		RES60A410			30.5		
		RES60A500			25		
		RES60A610			20.5		
		RES60A100			12.5		
G_{nom}	Nominal ratio	R_{HV} / R_{LV}	RES60A210		210		
			RES60A310		310		
			RES60A410		410		
			RES60A500(1)		499.1		
			RES60A610		610		
			RES60A100(2)		997.6		
t_D	Initial ratio tolerance(3)	(R_{HV} / R_{LV}) / G_{nom} – 1(4)	RES60A210			±0.1	%
			RES60A310		±0.03	±0.1	
			RES60A410		±0.02	±0.1	
			RES60A500		±0.02	±0.1	
			RES60A610			±0.1	
			RES60A100		±0.02	±0.1	
	Ratio tolerance drift across operating lifetime(5)	10 years, T_A = –40°C to +85°C, ΔV = 1000V, ($G_{INITIAL}$ – G_{FINAL}) / $G_{INITIAL}$ (4)				±0.2	%
t_{abs}	Absolute tolerance (per resistor)(6)					±15	%
TCR_{ratio}	Temperature coefficient of resistance ratio(3) (5)	T_A = –40°C to +85°C			±1	±5	ppm/°C
		T_A = –40°C to +125°C			±1		
TCR_{abs}	Absolute temperature coefficient of resistance (per resistor)(6) (5)	T_A = –40°C to +125°C			±20		ppm/°C
VCR_{ratio}	Voltage coefficient of resistance ratio				±2		ppm/V

ADVANCE INFORMATION

5.5 Electrical Characteristics (続き)

at ΔV = 1000V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IMPEDANCE							
C_{IN}	Pin capacitance(7)	HVIN to LVIN			TBD		pF
		MID to LVIN			TBD		
	–3dB bandwidth	$C_{MID\ to\ LVIN}$ = 10pF	RES60A210		268		kHz
			RES60A310		395		
			RES60A410		521		
			RES60A500		637		
			RES60A610		776		
			RES60A100		1270		
t_s	Settling time(5)	To 0.1%, 10V step	RES60A210		TBD		µs
			RES60A310		TBD		
			RES60A410		TBD		
			RES60A500		TBD		
			RES60A610		TBD		
			RES60A100		TBD		
		To 0.01%, 10V step	RES60A210		TBD		µs
			RES60A310		TBD		
			RES60A410		TBD		
			RES60A500		TBD		
			RES60A610		TBD		
			RES60A100		TBD		
e_N	Thermal noise density(7)	f = 1kHz	RES60A210		30		nV/√Hz
			RES60A310		25		
			RES60A410		22		
			RES60A500		20		
			RES60A610		18		
			RES60A100		14		

(1) For Advanced-Information devices, the typical value is 499.1. For Production-Data devices, this value will be 500.
(2) For Advanced-Information devices, the typical value is 997.6. For Production-Data devices, this value will be 1000.
(3) R_{HV} / R_{LV} vs nominal ratio.
(4) The specification is the result of this expression, given as a percentage (multiplied by 100%)
(5) Specified by characterization.
(6) R_{HV} and R_{LV} vs nominal values.
(7) Specified by design.

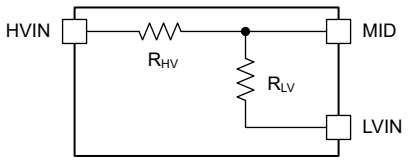
ADVANCE INFORMATION

6 Detailed Description

6.1 Overview

The RES60A-Q1 consists of two, precision, thin-film SiCr resistors, arranged to form a matched divider and encapsulated by an insulative SiO_2 layer. The device contains an *input* resistor, R_{HV}, that is nominally 12.5MΩ. The device also incorporates a *gain* resistor, R_{LV}, with a value that depends on the nominal ratio (R_{HV} / R_{LV}) of the RES60A-Q1.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Ratiometric Matching

The resistors of the RES60A-Q1 are described by the following two equations:

$$R_{HV} = R_{HVnom} \times (1 \pm t_{abs}) = R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr}) \quad (1)$$

$$R_{LV} = R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr}) \quad (2)$$

where

- R_{HVnom} and R_{LVnom} are the nominal values of each resistor.
- t_{abs} is an error term that describes the absolute tolerance of the resistors of the RES60A-Q1, such that $|t_{abs}| \leq 15\%$.
- t_{SiCr} is the variation in the SiCr resistivity for a wafer, and dominates the absolute tolerance for a given resistor. The two resistors of a given RES60A-Q1 are interdigitated and come from the same area of the wafer; therefore, t_{SiCr} is effectively the same for both of the two resistors, although t_{SiCr} varies on a part-to-part basis. When the divider is considered in ratiometric terms, these error terms drop out; see the following equations.
- t_{RHV} and t_{RLV} are localized per-resistor variation or offset error terms. These terms describe the remaining effective tolerances of the respective resistors for a given RES60A-Q1 device, after accounting for the universal t_{SiCr}.

$$\frac{R_{HV}}{R_{LV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr})} = \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV})} = G_{nom} \times \frac{(1 \pm t_{RHV})}{(1 \pm t_{RLV})} = G \quad (3)$$

$$\frac{R_{HV}}{R_{LV} + R_{HV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr}) + R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})} = \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV}) + R_{HVnom} \times (1 \pm t_{RHV})} \quad (4)$$

The RES60A-Q1 is specified with a maximum initial divider ratio tolerance of 0.1%, meaning that the relationship between the actual divider ratio, G, and the nominal ratio, G_{nom}, of a given divider is described by the following:

$$G = G_{nom} \times (1 \pm t_D) \quad (5)$$

such that $t_D \leq 0.1\%$. Because any devices that do not meet these criteria are screened out at final test, these equations can be used with the previous equations to prove the effective bounds of t_{RHV} and t_{RLV}. Therefore, despite the device absolute end-to-end tolerance bounds of ±15%, the effective error tolerances of each resistor (for ratiometric applications) are within approximately ±0.05%, for the worst-case t_{RHV} and t_{RlV}.

ADVANCE INFORMATION

6.3.2 Ultra-Low Noise

Noise in resistors can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less that 100Hz. The flicker noise for thin-film resistors, including the RES60A-Q1, is lower than that of thick-film resistor processes. Thermal noise typically dominates in the region greater than 1kHz, and increases as resistor magnitude increases. Noise is modeled as a voltage source in series with the resistor.

For a resistive divider such as the RES60A-Q1, the thermal noise as measured at the center tap of two resistors R_{HV} and R_{LV} is equivalent to the thermal noise of a resistor with value $R_{HV} \parallel R_{LV}$:

$$e_N = \sqrt{(4k_B TR)} \tag{6}$$

where:

- e_N is the thermal noise density in nV/√Hz
- T is the absolute temperature in kelvins (K)
- k_B is the Boltzmann constant, 1.381 × 10-23 J/K
- $R = R_{HV} \parallel R_{LV}$

$R_{HV} >> R_{LV}$; therefore, $R \approx R_{LV}$. As an example, for the RES60A610-Q1:

$$e_N = \sqrt{(4k_B TR)} = \sqrt{4 \times 1.38E^{-23} \frac{J}{K} \times 278K \times (12.5M\Omega \parallel 20.49k\Omega)} = 18nV/\sqrt{Hz} \tag{7}$$

6.4 Device Functional Modes

The RES60A-Q1 features a single pad for the HVIN pin and two pads for the MID and LVIN pins, with all other pads and pins electrically floating. Connect both the MID and LVIN pins to the *low-voltage domain* of the system, such as a microcontroller ADC input and chassis ground, respectively. Bias the HVIN pin to the high potential of the measured system, such as the high side of the battery stack.

HVIN and LVIN can be used to measure directly between the high side and low side of the battery. However, to avoid an overvoltage condition, verify that the downstream circuitry driven by MID is properly referenced to the low side (LVIN).

ADVANCE INFORMATION

7 Application and Implementation

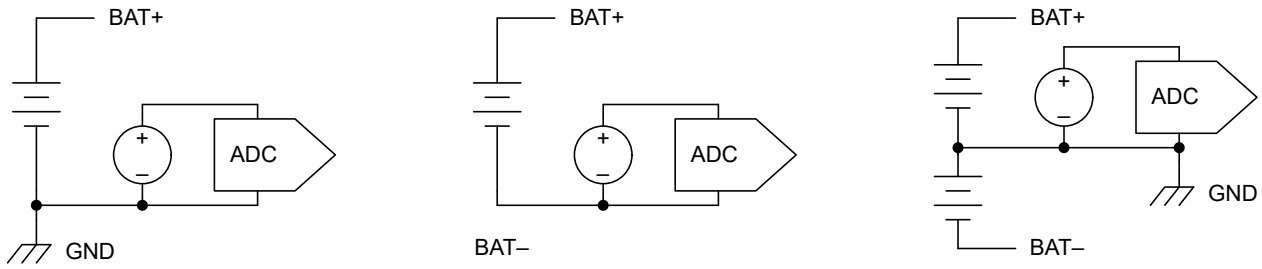
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Battery Stack Measurement

The RES60A-Q1 can be used in conjunction with an automotive precision amplifier, such as the OPA192-Q1, for single-ended measurement of the high side (BAT+) of an EV battery relative to a fixed potential. For those systems where BAT– and GND are equivalent, as in 図 7-1 (a), the configuration shown in 図 7-2 applies. An alternative approach is to measure directly across the battery from BAT+ to BAT–, as shown in 図 7-3. This approach is useful for systems referenced to the low side of the battery, BAT–, as in 図 7-1 (b).



(a) Referenced to GND, GND = BAT–

(b) Referenced to BAT–, BAT+ > GND > BAT–

(c) Referenced to GND, BAT+ > GND > BAT–

図 7-1. Common Battery and System Configurations

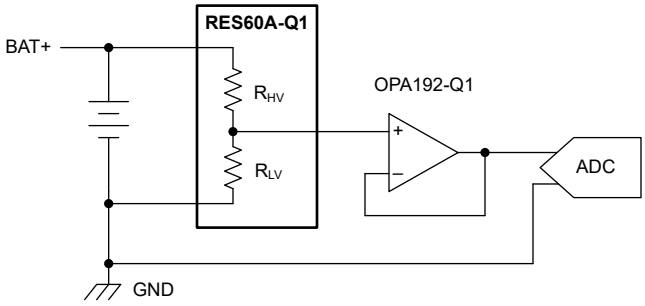


図 7-2. Single-Ended Measurement, BAT+ to GND

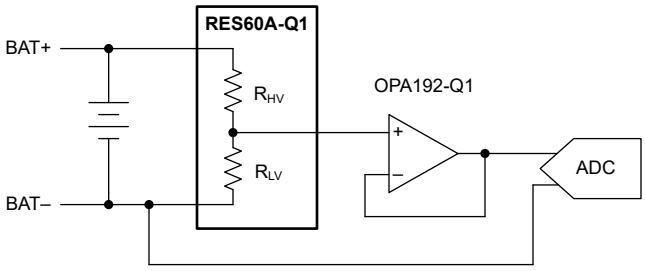


図 7-3. Single-Ended Measurement, BAT+ to BAT–

ADVANCE INFORMATION

For some system architectures, BAT– floats relative to the chassis GND; see also 図 7-1 (c). If for example a microcontroller referenced to chassis ground needs to measure the voltage across the entire battery stack, a difference amplifier can be constructed using two RES60A-Q1 devices and an OPA192-Q1. 図 7-4 shows this approach. If two ADC channels are available, two single-ended measurements can be done using two RES60A-Q1 devices and an OPA2192-Q1.

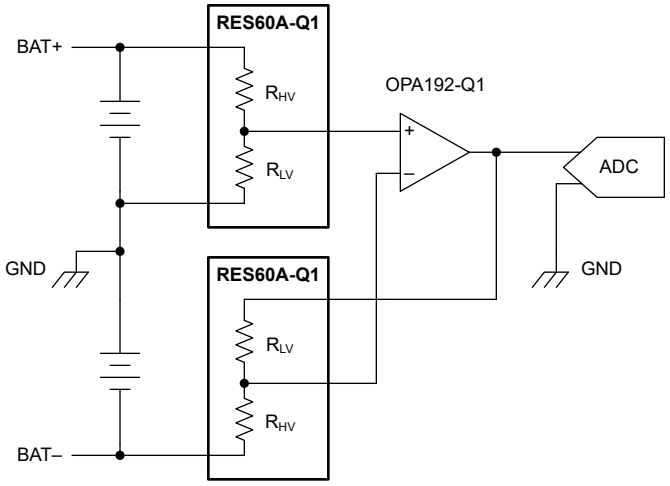


図 7-4. Differential Measurement, BAT+ to BAT–

Leakage in the system and quiescent current from the amplifier input reduce the precision of the measurement. In some cases, a guard buffer can be used to reduce leakage currents. Follow best practices to reduce board contamination and leakage.

For an 800V single-ended battery measurement (see also 図 7-2), the static current through the divider is:

$$I_{STATIC} = \frac{V_{BATT}}{(R_{HV} + R_{LV})} = \frac{800V}{(12.5M\Omega + 20.49k\Omega)} = 63.9\mu A \quad (8)$$

Therefore, the buffer amplifier used must have a low bias current, such that $I_B << I_{STATIC}$. The low bias current of the OPA192-Q1 (5pA typical at 25°C, 5nA maximum from –40°C to +125°C) makes the device an excellent choice for this role.

ADVANCE INFORMATION

7.2 Typical Application

The RES60A-Q1 can be configured with an isolated amplifier such as the AMC1311B-Q1 for measurements requiring reinforced isolation. 図 7-5 shows an example circuit configuration for such an application, where the RES60A-Q1 attenuates the input voltage and the AMC1311B-Q1 crosses the isolation barrier. A discrete difference amplifier with RES11A-Q1 and OPA388-Q1 is used to adapt the differential output voltage of the AMC1311B-Q1 for use with a single-ended 5V ADC.

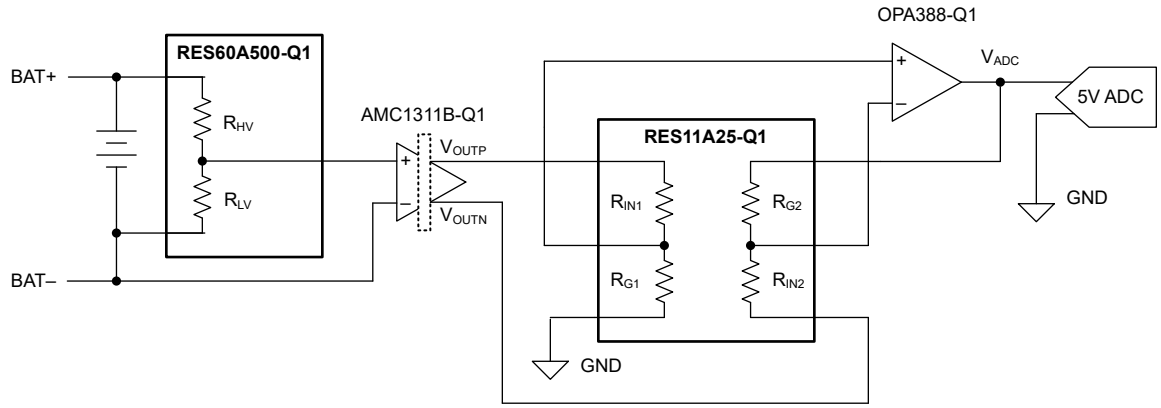


図 7-5. DC Bus Measurement With the RES60A-Q1 and AMC1311B-Q1

7.2.1 Design Requirements

PARAMETER	DESIGN GOAL
DC bus voltage range	0V to 1000V
Output (V_{ADC}) full-scale range	0V to 5V
Attenuation (nominal ratio)	500:1
Uncalibrated initial measurement error	±0.5% FSR

7.2.2 Detailed Design Procedure

This design attenuates the high common-mode voltage of the bus to a level that falls within the linear input range of the AMC1311B-Q1. Some key possible circuit error sources can be considered as follows:

- The AMC1311B-Q1 has a typical input bias current of 3.5nA. With R_{LV} = 25kΩ, this input bias current manifests appears as an 88µV offset error at MID. When this offset is calculated in a root-sum-of-squares with the 400µV typical input offset voltage of the AMC1311B-Q1, a 410µV offset results. This offset represents 0.0205% of the 2V full-scale range, and is typically not the dominating error factor.
- The gain error and integrated nonlinearity error of the AMC1311B-Q1 can be approximated using the Isolated Amplifier Voltage Sensing Excel Calculator. For this example, the typical FSR error is calculated as 0.06%.
- The typical initial ratiometric gain tolerance of the RES60A500-Q1 is 0.02%, which sums with the previously mentioned errors of the AMC1311B-Q1 in a root-sum-of-squares manner to give a total typical FSR error of 0.066%.
- The level-shifting circuit introduces additional errors, and applies a gain factor to the previously discussed errors. However, due to the low offset of the OPA388-Q1 and high precision of the RES11A-Q1, these errors (0.012% FSR) are low enough to not significantly impact the final typical error.

The final calculated result of 0.068% typical FSR error represents a 1σ value, so a ±6σ estimate gives ±0.41% FSR error. The results suggest the circuit meets the ±0.5% FSR application requirement, with margin.

ADVANCE INFORMATION

7.2.3 Application Curves

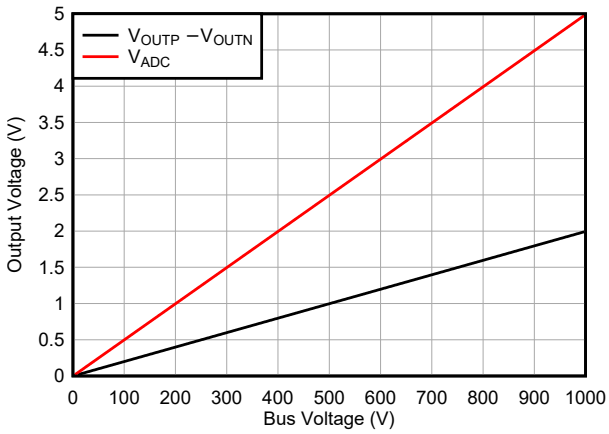


図 7-6. Transfer Function

7.3 Power Supply Recommendations

The RES60A-Q1 is a high-voltage resistor divider, with no active circuitry or protective diodes. There are no specific power-supply connection requirements other than respecting the limits expressed in *Absolute Maximum Ratings* and *Recommended Operating Conditions*. To provide additional protection against high-edge-rate transient events, use a high-voltage capacitor at the device input. Be aware that additional input capacitance extends step-response settling times. A TVS diode at the MID pin provides additional protection against fast transients for downstream low-voltage circuitry, if necessary.

ADVANCE INFORMATION

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running sensitive traces, such as the MID connection, as far away from supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Make sure supply voltages are adequately filtered.
- Power dissipated in the RES60A-Q1 causes the junction temperature to rise. For reliable operation, junction temperature must be limited to 150°C, maximum. Maintaining a lower junction temperature results in higher reliability.
  - Package thermal resistance, $R_{\theta JA}$, is affected by mounting techniques and environments. Poor air circulation can significantly increase thermal resistance to the ambient environment. Best thermal performance is achieved by soldering the RES60A-Q1 onto a circuit board with wide printed circuit traces, especially for the LVIN connection, to allow greater conduction through the device leads.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process.
  - A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- Use conformal coating or potting, the deposition of an insulating polymer or other material layer over an assembled PCB, to reduce the pollution degree around the RES60A-Q1. This process reduces the requirements for creepage and clearance distances by eliminating or reducing the influence of pollutants.
- Use groove cutting to attain a lower PCB creepage distance. For grooves wider than 1mm, the effective creepage distance is the existing creepage distance plus the width of the groove and twice the depth of the groove. This sum must equal or exceed the required creepage distance. The groove must not weaken the substrate to the point of failure to meet mechanical test requirements. All layers under the groove must be free from traces, vias, and pads to maintain the maximum creepage distance.

7.4.2 Layout Example

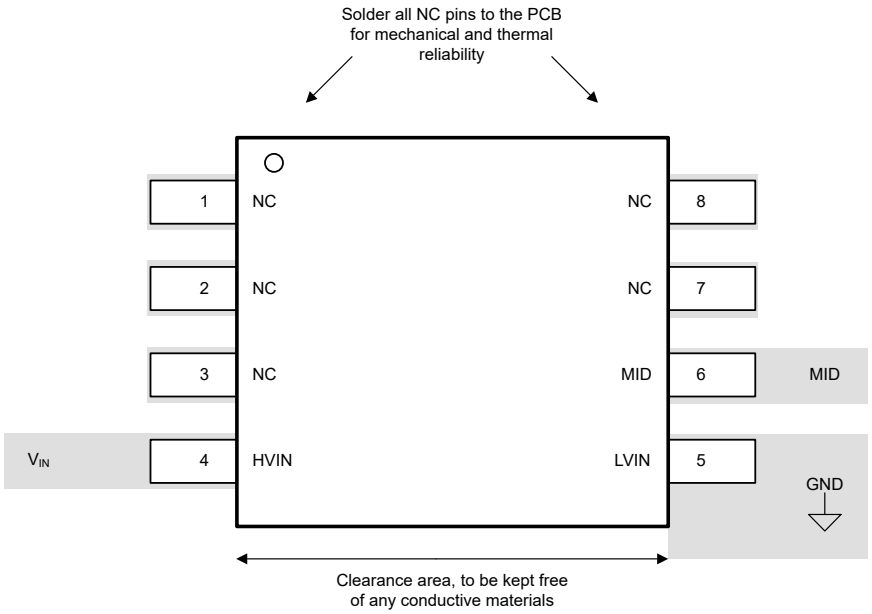


図 7-7. Layout Example

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

8.1.1.2 TINA-TI™シミュレーション ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション プログラムです。TINA-TI シミュレーション ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ モデルとアクティブ モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション ソフトウェアは設計およびシミュレーション ツール Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな形式で処理できる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック スタート ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア フォルダから、無償の TINA-TI シミュレーション ソフトウェアをダウンロードしてください。

8.1.1.3 TI のリファレンス・デザイン

TI のリファレンス・デザインは、TI の高精度アナログ・アプリケーション専門家により作成されたアナログ・ソリューションです。TI のリファレンス・デザインは、動作原理、部品の選択、シミュレーション、完全な PCB 回路図およびレイアウト、部品表、測定済みの性能を提供します。TI のリファレンス・デザインは、http://www.ti.com/ww/en/analog/precision-designs/ からオンラインで入手できます。

8.1.1.4 Analog Filter Designer

Analog Filter Designer は、設計およびシミュレーション ツール Web ページから Web ベースのツールとして利用でき、包括的な複数段アクティブ フィルタ ソリューションの設計、最適化、シミュレーションをわずか数分で行います。

ADVANCE INFORMATION

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *What Are Creepage And Clearance?* TI Precision Labs video
- Texas Instruments, *RES11A-Q1 Automotive, Low-Noise, Precision, Matched, Thin-Film Resistor Pairs* data sheet
- Texas Instruments, *RES60EVM* evaluation module

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.5 Trademarks

TINA-TI™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
すべての商標は、それぞれの所有者に帰属します。

8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2024	*	Initial Draft

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XRES60A100QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XRES60A310QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XRES60A410QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XRES60A500QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

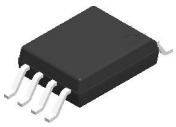
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

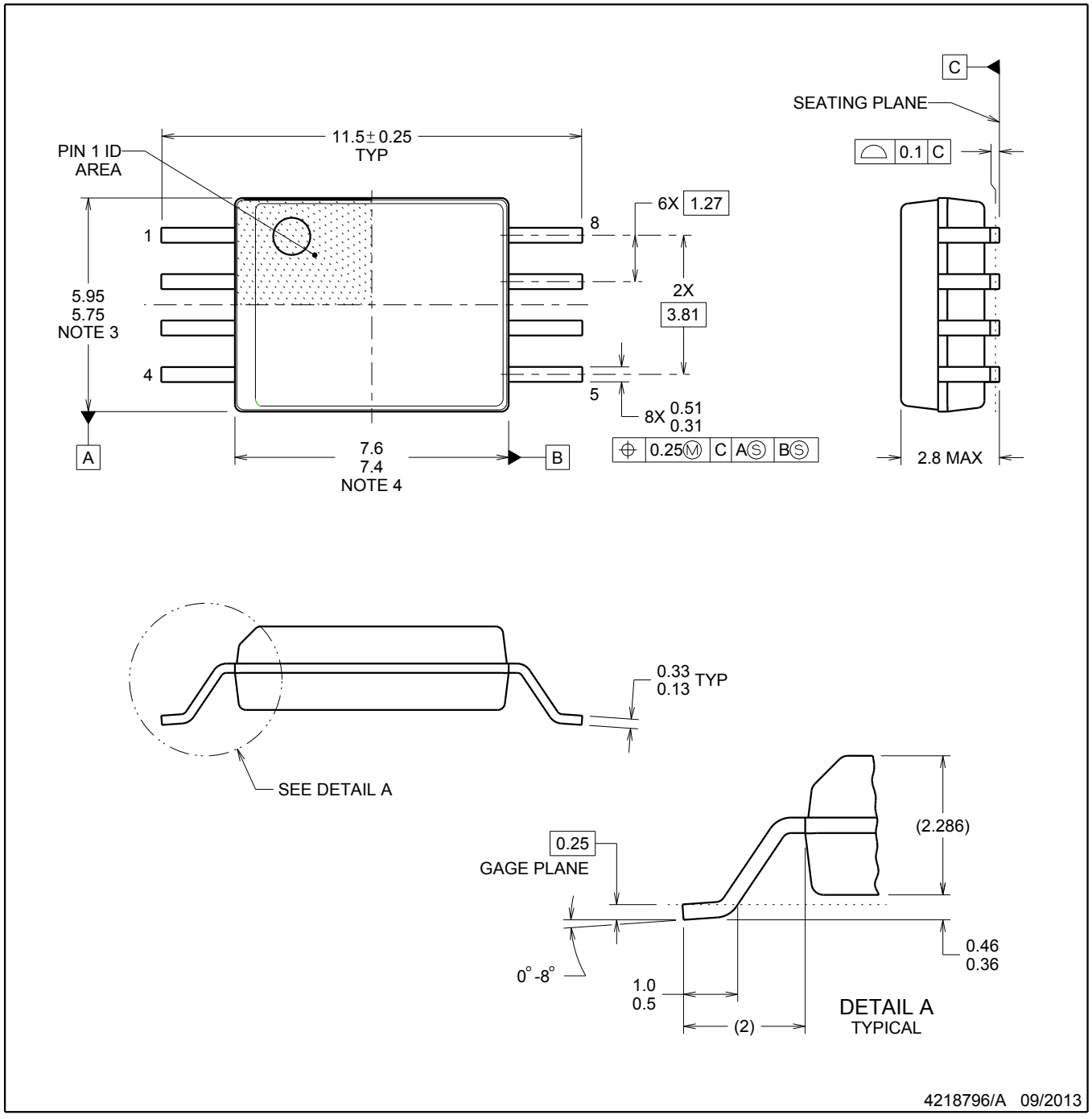
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



DWV0008A

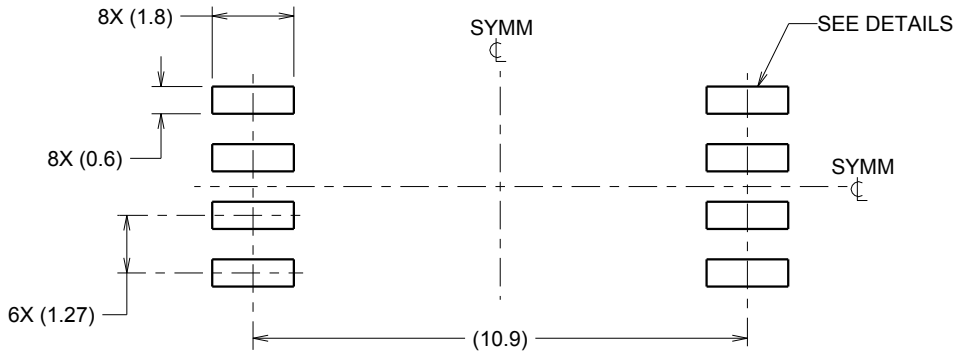
SOIC - 2.8 mm max height

SOIC

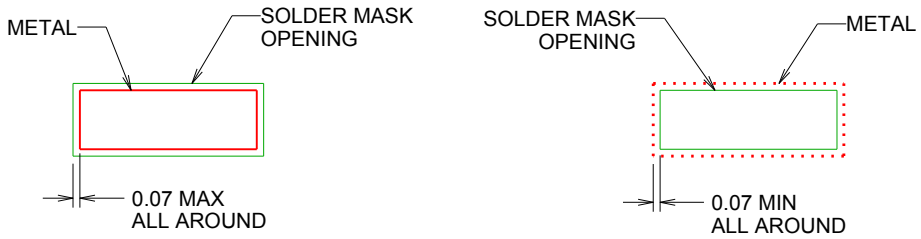


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

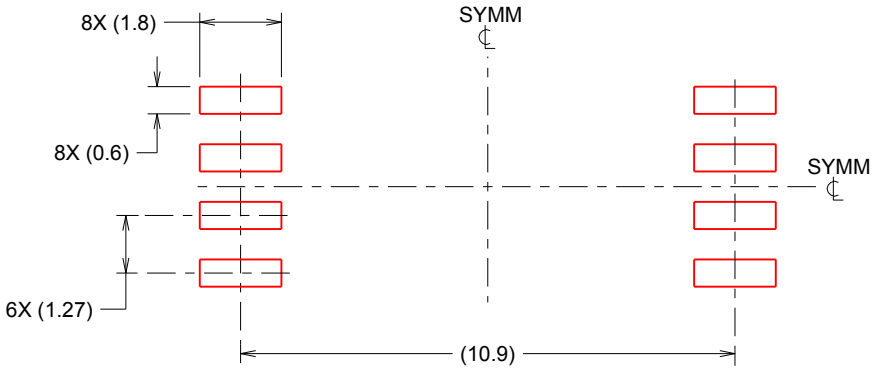
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265