

## SNx4AHCT32 クワッド、2 入力正論理 OR ゲート

### 1 特長

- 入力は TTL 電圧互換
- JESD 17 準拠で 250mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 人体モデルで 2000V
  - マシン・モデルで 200V
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません

### 2 アプリケーション

- レジ用電子機器
- 通信インフラ
- ネットワーク・スイッチ
- 試験および測定機器

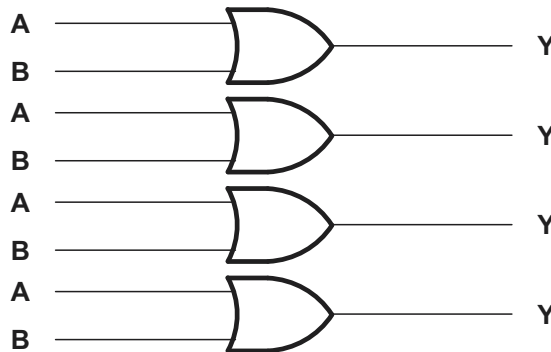
### 3 概要

SNx4AHCT32 デバイスは、クワッド 2 入力正論理 OR ゲートです。これらのデバイスは、ブール関数  $Y = \bar{A} \times \bar{B}$  または  $Y = A + B$  を正論理で実行します。

#### パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN54AHCT32	J (CDIP, 14)	19.56mm × 6.67mm
	W (CFP, 14)	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm
SN74AHCT32	N (PDIP, 14)	19.3mm × 6.35mm
	D (SOIC, 14)	8.65mm × 3.91mm
	NS (SOP, 14)	10.30mm × 5.30mm
	DB (SSOP, 14)	6.20mm × 5.30mm
	PW (TSSOP, 14)	5.00mm × 4.40mm
	DGV (TVSOP, 14)	3.60mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm
BQA (WQFN, 14)	3.00mm × 2.50mm	

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図



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## 4 Revision History

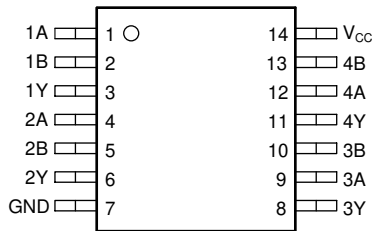
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision N (May 2023) to Revision O (July 2023)	Page
<ul style="list-style-type: none"> <li>Updated thermal values for R<math>\theta</math>JA: PW = 125.1 to 147.7, R<math>\theta</math>JC(top) = 53.7 to 77.4, R<math>\theta</math>JB = 66.9 to 90.9, <math>\Psi</math>JT = 7.6 to 27.2, <math>\Psi</math>JB = 66.3 to 90.2, all values in °C/W.”</li> </ul>	6

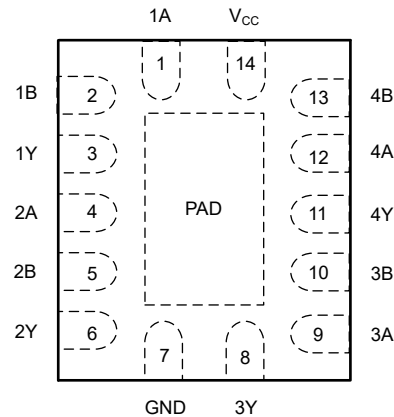
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Changes from Revision M (October 2014) to Revision N (May 2023)	Page
<ul style="list-style-type: none"> <li>ドキュメント全体にわたって表、図、相互参照の採番方法を更新</li> <li>「パッケージ情報」表を更新</li> <li>データシートに BQA パッケージを追加</li> </ul>	1

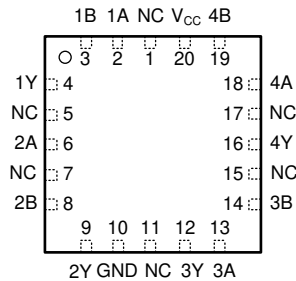
## 5 Pin Configuration and Functions



**图 5-1. SN54AHCT32 J or W Package, 14-Pin (Top View)**  
**SN74AHCT32 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)**



**图 5-2. SN74AHCT32 RGY or BQA Package, 14-Pin (Top View)**



**图 5-3. SN54AHCT32 FK Package, 20-Pin (Top View)**

**表 5-1. Pin Functions**

NAME	PIN				TYPE <sup>(1)</sup>	DESCRIPTION
	SN74AHCT32		SN54AHCT32			
	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK		
1A	1	1	1	2	I	1A Input
1B	2	2	2	3	I	1B Input
1Y	3	3	3	4	O	1Y Output
2A	4	4	4	6	I	2A Input
2B	5	5	5	8	I	2B Input
2Y	6	6	6	9	O	2Y Output
3Y	8	8	8	12	O	3Y Output
3A	9	9	9	13	I	3A Input
3B	10	10	10	14	I	3B Input
4Y	11	11	11	16	O	4Y Output
4A	12	12	12	18	I	4A Input
4B	13	13	13	19	I	4B Input
GND	7	7	7	10	—	Ground Pin
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No Connection
V <sub>CC</sub>	14	14	14	20	I	Power Pin

表 5-1. Pin Functions (continued)

NAME	PIN				TYPE <sup>(1)</sup>	DESCRIPTION
	SN74AHCT32		SN54AHCT32			
	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK		
Thermal Pad	—	PAD	—	—	—	Thermal Pad

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
Continuous current through V <sub>CC</sub> or GND				±50 mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM)	±1000
		Charged device model (CDM)	±750

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		SN54AHCT32		SN74AHCT32		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8		-8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT32								UNIT
		D	DB	DGV	N	NS	PW	RGY	BQA	
		14 PINS								
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	97.5	109.5	133.3	59.7	92.2	147.7	59.0	88.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	58.7	62.1	55.6	47.3	49.8	77.4	72.5	90.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	51.8	56.9	66.3	39.5	51.0	90.9	35.0	56.8	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	22.6	22.6	7.8	32.4	15.7	27.2	3.9	9.9	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	51.6	56.3	56.6	39.4	50.6	90.2	35.1	56.7	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	15.4	33.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT32		SN74AHCT32		–40°C to 125°C SN74AHCT32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4	4.5		4.4		4.4		4.4	V	
	I <sub>OH</sub> = –8 mA		3.94			3.8		3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44		0.44		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(1)</sup>		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20		20		20	μA
ΔI <sub>CC</sub> <sup>(2)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10		10		10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		SN54AHCT32		SN74AHCT32		–40°C to 125°C SN74AHCT32		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5 <sup>(1)</sup>	6.9 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	1	8	1	9	ns
t <sub>PHL</sub>				5 <sup>(1)</sup>	6.9 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	1	8	1	9	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.5	7.9	1	9	1	9	1	10	ns
t <sub>PHL</sub>				5.5	7.9	1	9	1	9	1	10	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 6.7 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER		SN74AHCT32			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

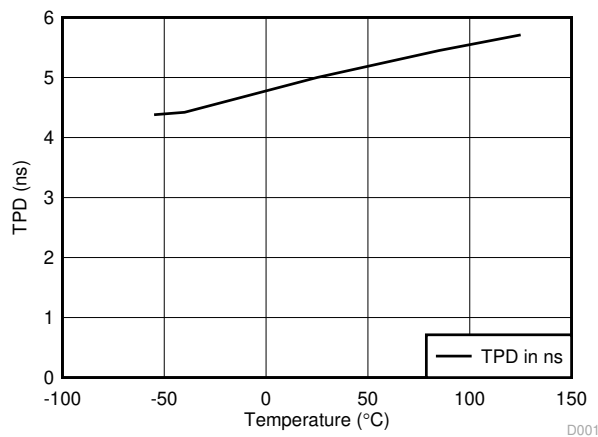
(1) Characteristics are for surface-mount packages only.

### 6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

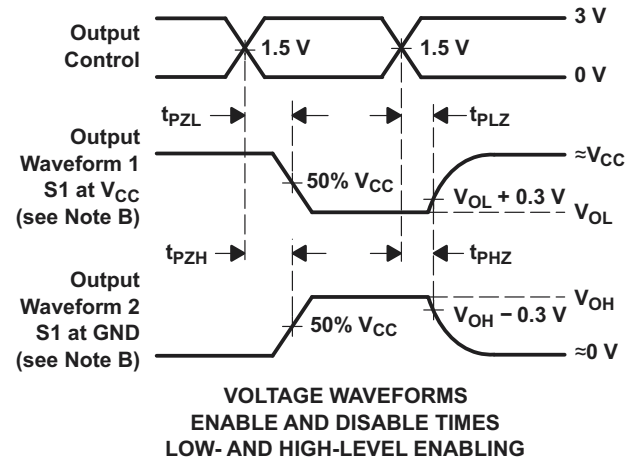
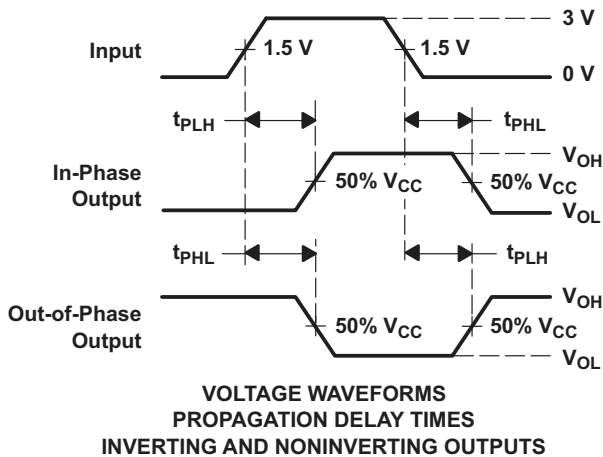
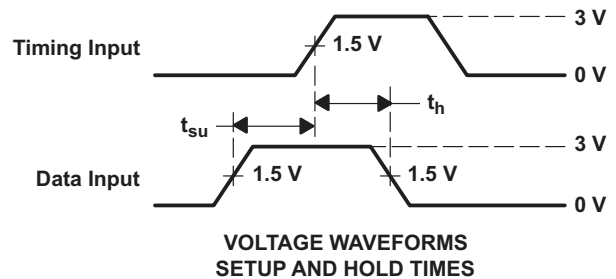
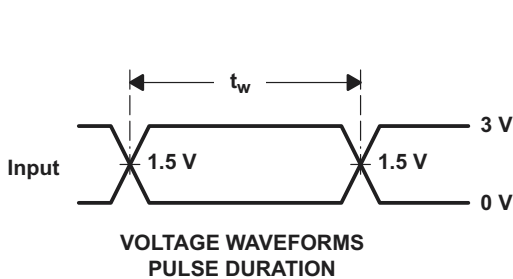
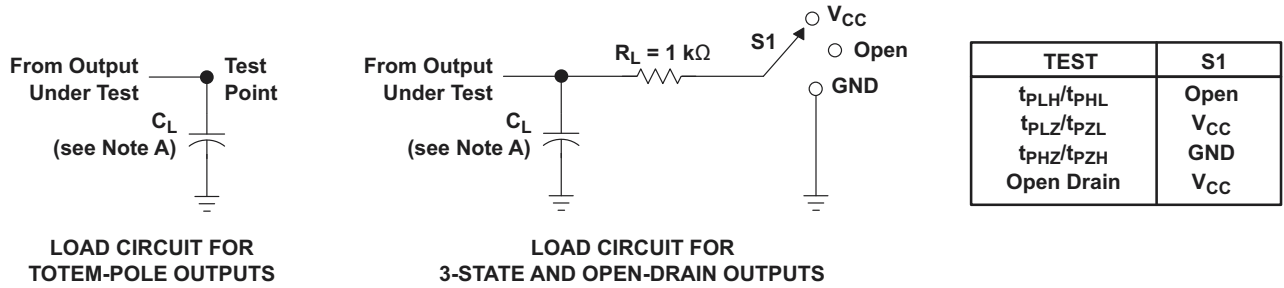
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	No load, $f = 1\text{ MHz}$	11.5	pF

### 6.9 Typical Characteristics



**6-1. TPD vs Temperature**

## 7 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**7-1. Load Circuit and Voltage Waveforms**

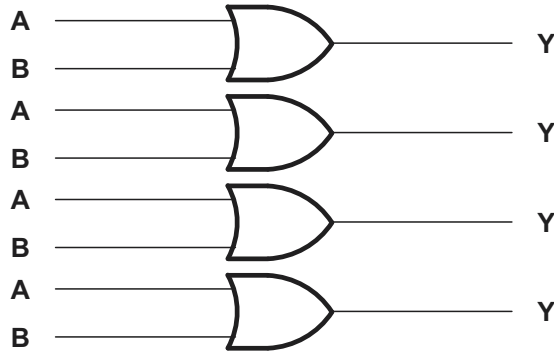


## 8 Detailed Description

### 8.1 Overview

The SNx4AHCT32 is a quadruple 2-input positive-OR gate with low drive that will produce slow rise and fall times. This slow transition reduces ringing on the output signal. The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when  $V_{CC} = 0$  V.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- Slow rise and fall time on outputs allows for low-noise outputs
- TTL inputs allow up translation from 3.3 V to 5 V

### 8.4 Device Functional Modes

**表 8-1. Function Table  
(Each Gate)**

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The SNx4AHCT32 is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and can translate up to 5 V.

### 9.2 Typical Application

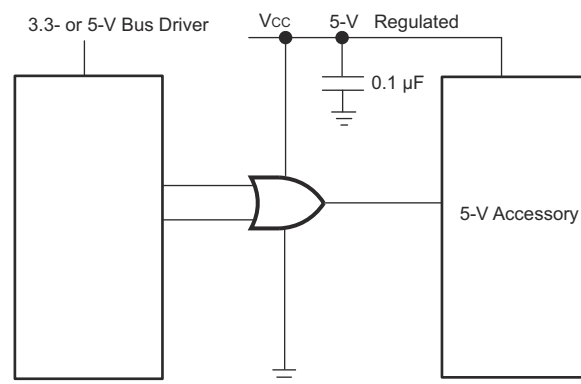


図 9-1. Typical Application Diagram for a Single Gate

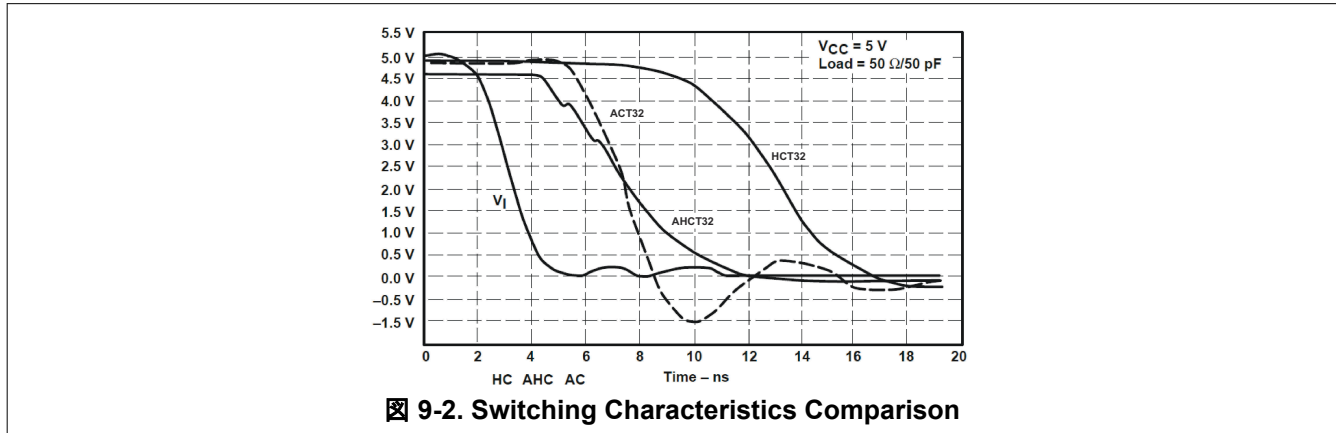
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Recommended Operating Conditions](#) table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommend output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curves



### 9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply-voltage rating located in [Recommended Operating Conditions](#).

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins then a 0.01  $\mu\text{F}$  or a 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

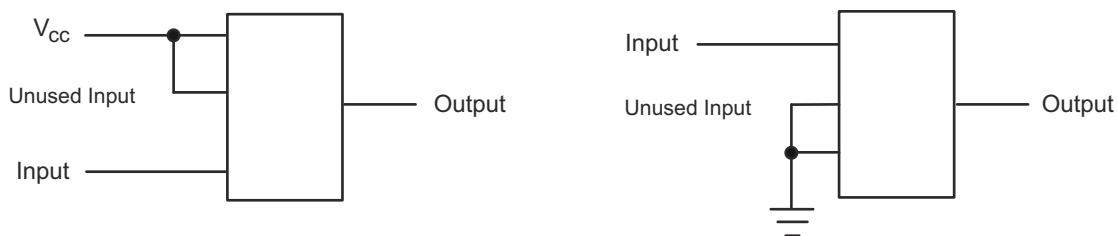
### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 9-3](#) shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

#### 9.4.2 Layout Example



## 10 Device and Documentation Support

### 10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
すべての商標は、それぞれの所有者に帰属します。

### 10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9682601Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682601Q2A SNJ54AHCT32FK	<a href="#">Samples</a>
5962-9682601QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682601QCA SNJ54AHCT32J	<a href="#">Samples</a>
5962-9682601QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682601QDA SNJ54AHCT32W	<a href="#">Samples</a>
SN74AHCT32BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT32	<a href="#">Samples</a>
SN74AHCT32D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	AHCT32	
SN74AHCT32DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB32	<a href="#">Samples</a>
SN74AHCT32DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB32	<a href="#">Samples</a>
SN74AHCT32DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT32	<a href="#">Samples</a>
SN74AHCT32N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT32N	<a href="#">Samples</a>
SN74AHCT32NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT32	<a href="#">Samples</a>
SN74AHCT32PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	HB32	
SN74AHCT32PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HB32	<a href="#">Samples</a>
SN74AHCT32RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB32	<a href="#">Samples</a>
SNJ54AHCT32FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682601Q2A SNJ54AHCT32FK	<a href="#">Samples</a>
SNJ54AHCT32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682601QCA SNJ54AHCT32J	<a href="#">Samples</a>
SNJ54AHCT32W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682601QDA SNJ54AHCT32W	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54AHCT32W	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AHCT32, SN74AHCT32 :**

- Catalog : [SN74AHCT32](#)

- Automotive : [SN74AHCT32-Q1](#), [SN74AHCT32-Q1](#)
- Enhanced Product : [SN74AHCT32-EP](#), [SN74AHCT32-EP](#)
- Military : [SN54AHCT32](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT32BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT32DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT32DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT32NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT32PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74AHCT32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT32RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT32BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT32DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHCT32DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHCT32DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHCT32NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHCT32PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74AHCT32PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHCT32PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT32RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

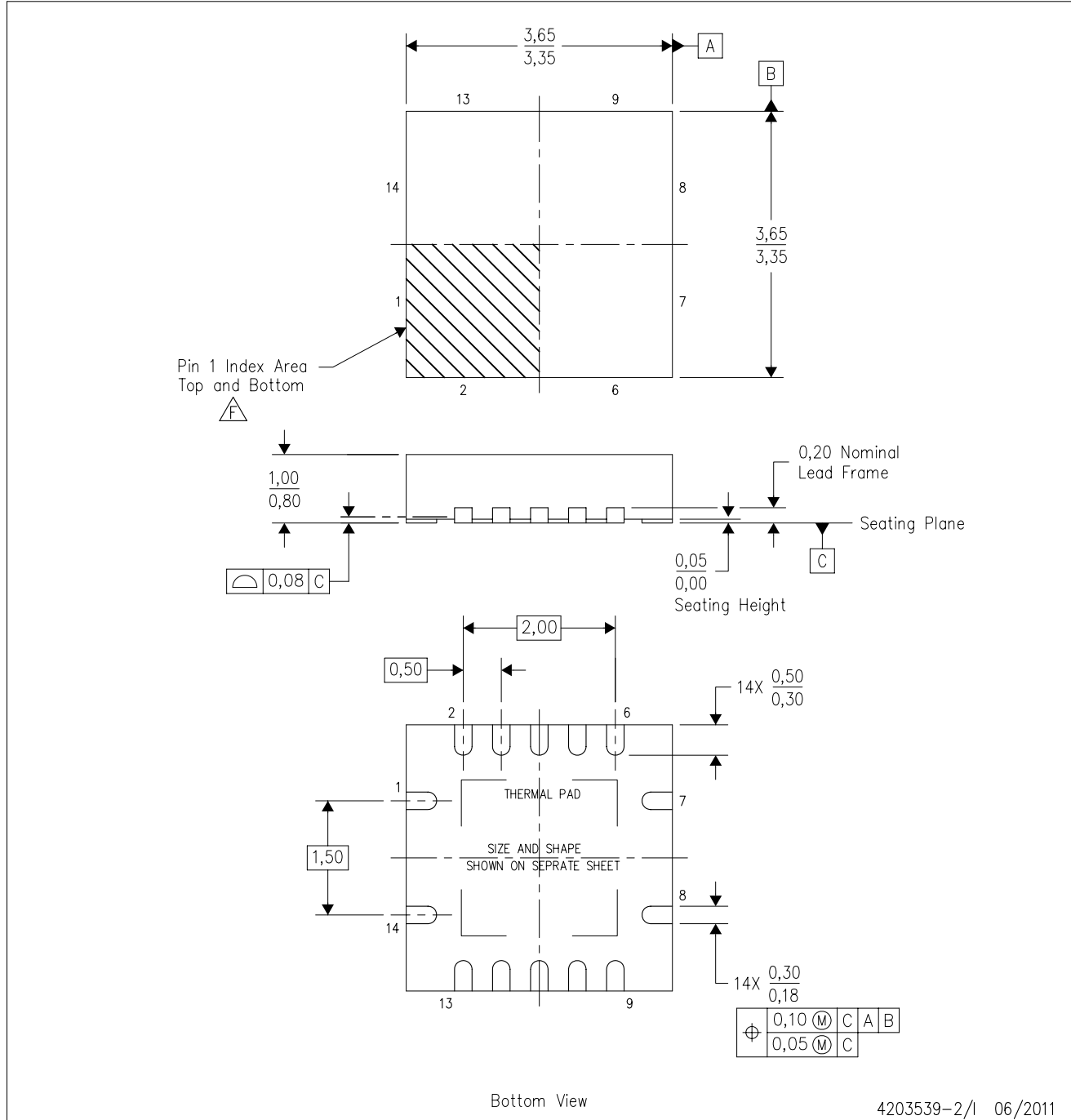
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9682601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9682601QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHCT32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT32N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCT32FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT32W	W	CFP	14	25	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

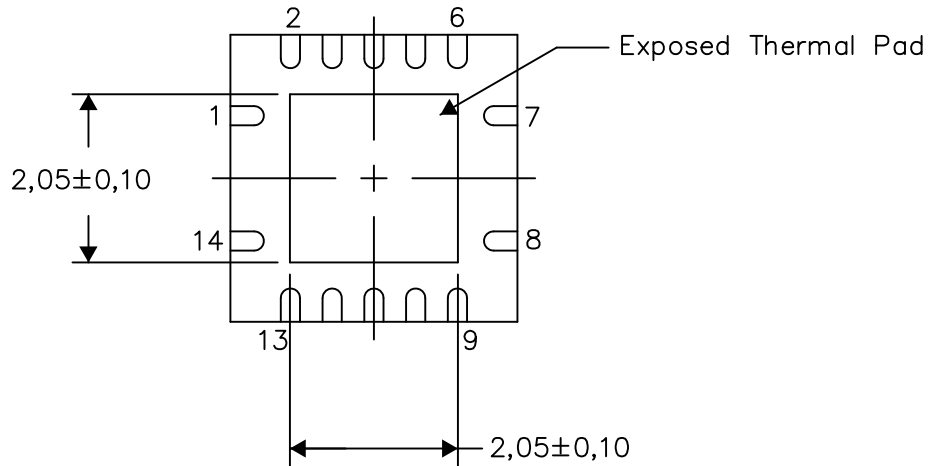
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## GENERIC PACKAGE VIEW

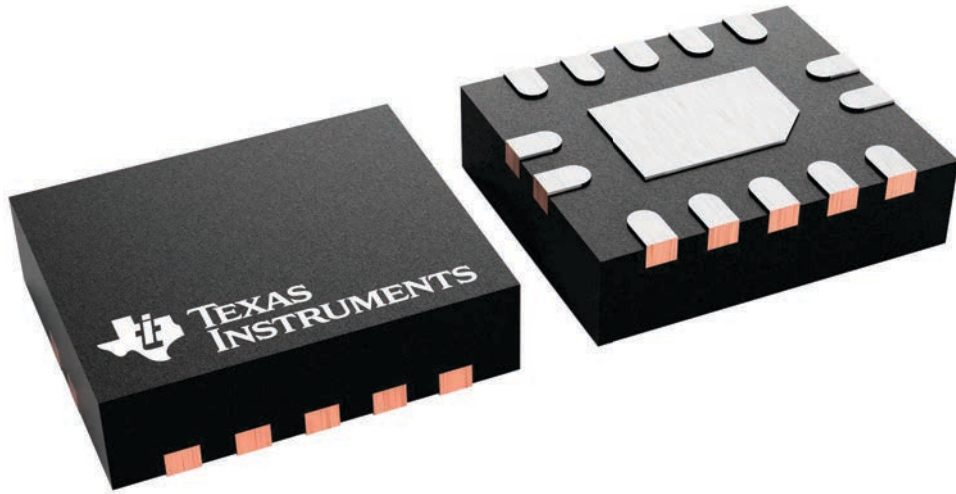
**BQA 14**

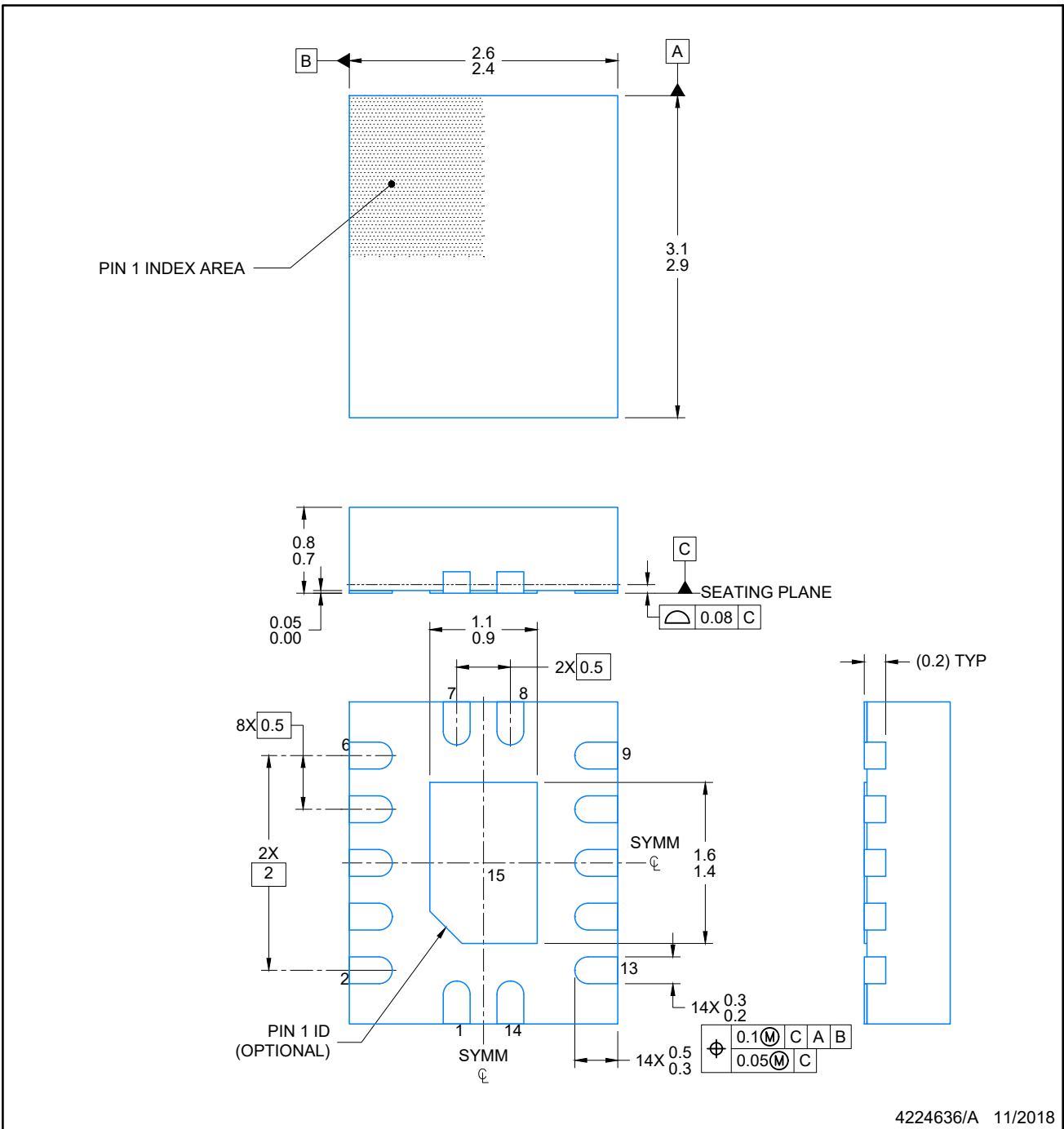
**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

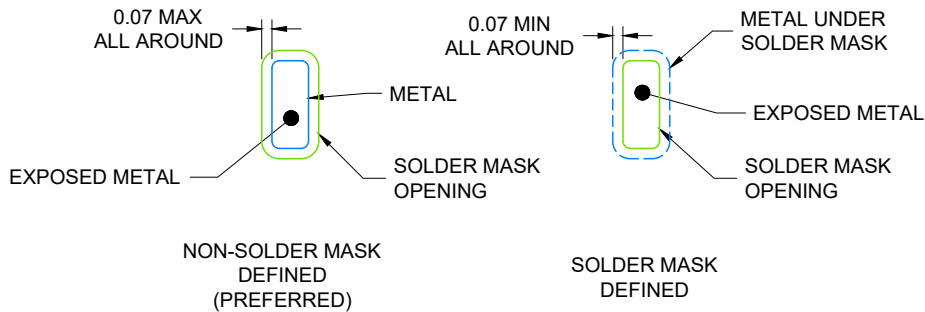
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
88% PRINTED COVERAGE BY AREA  
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

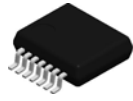
W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

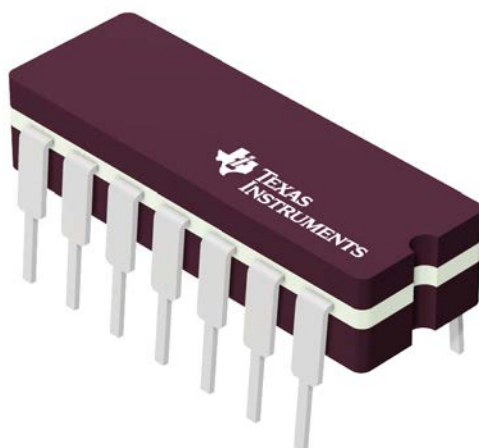
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G



J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



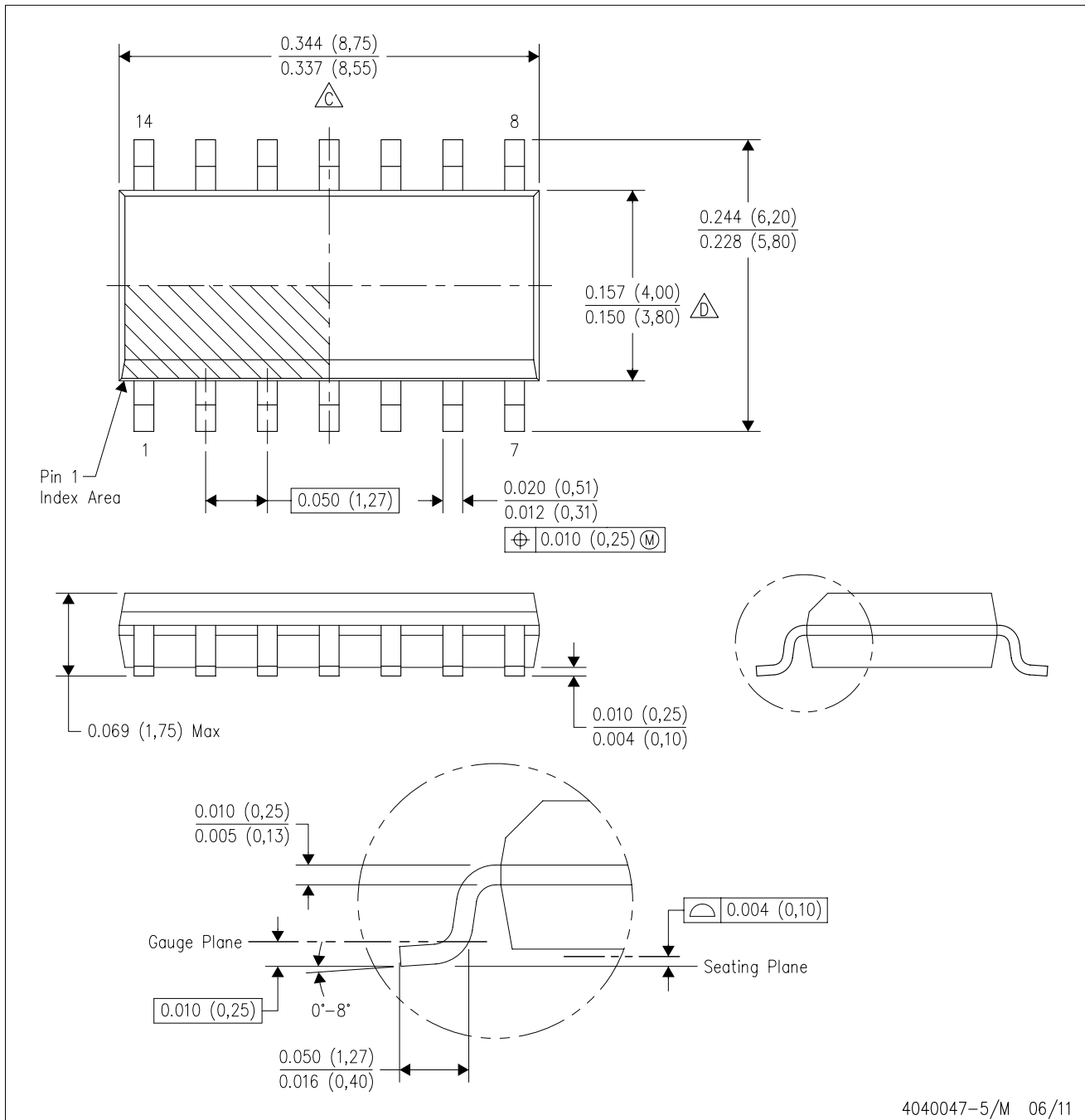
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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