参考資料

TEXAS INSTRUMENTS

SNx4AHCT573 3 ステート出力、オクタル トランスペアレント D タイプ ラッチ

1 特長

- 入力は TTL 電圧互換
- JESD 17 準拠で 250mA 超のラッチアップ性能
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。
  その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- サーバー
- PC およびノートパソコン
- ネットワーク スイッチ
- ウェアラブルなヘルスケア / フィットネス機器
- テレコム インフラストラクチャ
- レジ用電子機器

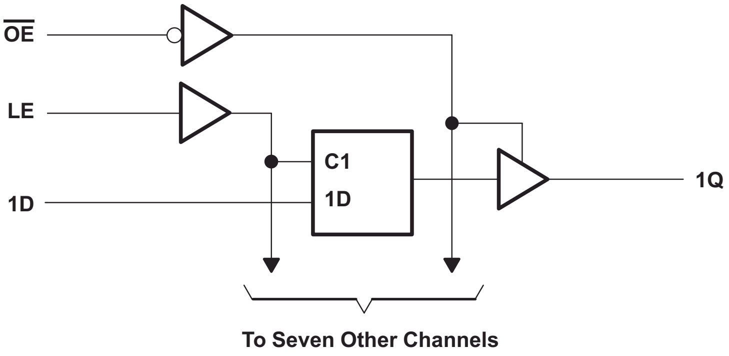
3 概要

SNx4AHCT573 デバイスはオクタル トランスペアレント D タイプ ラッチです。ラッチ イネーブル (LE) 入力が HIGH の場合、Q 出力はデータ (D) 入力に従います。LE を LOW にすると、D 入力のロジック レベルで Q 出力がラッチされます。

製品情報

部品番号	定格[1]	パッケージ [1]
SN74AHCT573	カタログ	DB (SSOP、20)
		DGV (TVSOP、20)
		DW (SOIC、20)
		N (PDIP、20)
		PW (TSSOP、20)
SN54AHCT573	軍用	J (CDIP、20)
		W (CFP、20)

(1) 詳細については、セクション 11 を参照してください。



概略回路図

English Data Sheet: SCLS243

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4 Pin Configuration and Functions

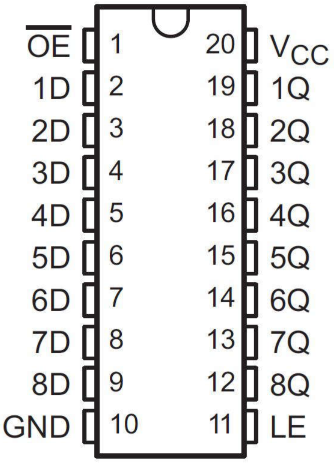


図 4-1. SN54AHCT573 J or W Package SN74AHCT573 DB, DGV, DW, N, NS, or PW Package (Top View)

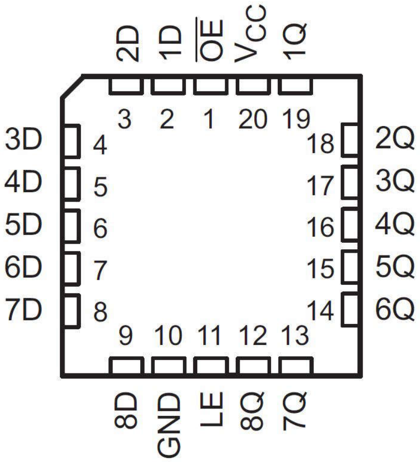


図 4-2. SN54AHCT573 FK Package (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	$\overline{\text{OE}}$	I	Output Enable
2	1D	I	1D Input
3	2D	I	2D Input
4	3D	I	3D Input
5	4D	I	4D Input
6	5D	I	5D Input
7	6D	I	6D Input
8	7D	I	7D Input
9	8D	I	8D Input
10	GND	—	Ground
11	LE	I	Latch Enable
12	8Q	O	8Q Output
13	7Q	O	7Q Output
14	6Q	O	6Q Output
15	5Q	O	5Q Output
16	4Q	O	4Q Output
17	3Q	O	3Q Output
18	2Q	O	2Q Output
19	1Q	O	1Q Output
20	V_{CC}	—	Power Pin

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AHCT573		SN74AHCT573		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT573 DW 20 PINS	SN74AHCT573 DB 20 PINS	SN74AHCT573 DGV 20 PINS	SN74AHCT573 N 20 PINS	SN74AHCT573 NS 20 PINS	SN74AHCT573 PW 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.4	97.9	117.2	53.3	79.2	116.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	59.6	32.7	40.0	45.7	58.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	53.1	58.7	34.2	46.8	78.7	
Ψ_{JT}	Junction-to-top characterization parameter	18.7	21.3	1.15	26.4	19.3	12.6	
Ψ_{JB}	Junction-to-board characterization parameter	46.5	52.7	58.0	34.1	46.4	77.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	–55°C to 125°C SN54AHCT573 MIN	–55°C to 125°C SN54AHCT573 MAX	–40°C to 85°C SN74AHCT573 MIN	–40°C to 85°C SN74AHCT573 MAX	–40°C to 125°C SN74AHCT573 MIN	–40°C to 125°C SN74AHCT573 MAX	UNIT
V_{OH}	I_{OH} = −50 µA	4.5V	4.4	4.5		4.4		4.4		4.4		V
	I_{OH} = −8mA		3.94			3.8		3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5V			0.1		0.1		0.1		0.1	V
	I_{OL} = 8mA				0.36		0.44		0.44		0.44	
I_I	V_I = 5.5V or GND	0V to 5.5V			±0.1		±1(1)		±1		±2	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5V			±0.25		±2.5		±2.5		±2.5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5V			4		40		40		40	µA
ΔI_{CC} (2)	One input at 3.4V, Other inputs at V_{CC} or GND	5.5V			1.35		1.5		1.5		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5V		2.5	10				10		10	pF
C_o	$V_O = V_{CC}$ or GND	5V		3								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0V or V_{CC}.

5.6 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see セクション 6)

PARAMETER		T_A = 25°C MIN	T_A = 25°C MAX	–55°C to 125°C SN54AHCT573 MIN	–55°C to 125°C SN54AHCT573 MAX	–40°C to 85°C SN74AHCT573 MIN	–40°C to 85°C SN74AHCT573 MAX	–40°C to 125°C SN74AHCT573 MIN	–40°C to 125°C SN74AHCT573 MAX	UNIT
t_w	Pulse duration, LE high	5		5		5		5		ns
t_{su}	Setup time, data before LE↓	3.5		3.5		3.5		3.5		ns
t_h	Hold time, data after LE↓	1.5		1.5		1.5		1.5		ns

5.7 Switching Characteristics, SNx4AHCT573

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see セクション 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = –40°C to 85°C		T_A = –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_L = 15pF										
t_{pd}	D	Q		5.1	7	1	9	1	9.5	ns
t_{pd}	LE	Q		5.6	7.5	1	9	1	9.5	ns
t_{en}	$\overline{OE}$	Q		5.5	7.5	1	10	1	11	ns
t_{dis}	$\overline{OE}$	Q		5.5	8	1	11	1	12	ns
C_L = 50pF										
t_{pd}	D	Q		6.1	8	1	10	1	10.5	ns
t_{pd}	LE	Q		6.6	8.5	1	10	1	10.5	ns
t_{en}	$\overline{OE}$	Q		6.5	8.5	1	11	1	11.5	ns
t_{dis}	$\overline{OE}$	Q		6.7	9	1	12	1	12.5	ns
$t_{sk(o)}$					1.5		1.5			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Switching Characteristics, SN54AHCT573

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see セクション 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = –55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
C_L = 15pF								
t_{pd}	D	Q		5.1(1)	7(1)	1(1)	9(1)	ns
t_{pd}	LE	Q		5.6(1)	7.5(1)	1(1)	9(1)	ns
t_{en}	$\overline{OE}$	Q		5.5(1)	7.5(1)	1(1)	9(1)	ns
t_{dis}	$\overline{OE}$	Q		5.5(1)	8(1)	1(1)	11(1)	ns
C_L = 50pF								
t_{pd}	D	Q		6.1	8	1	10	ns
t_{pd}	LE	Q		6.6	8.5	1	10	ns
t_{en}	$\overline{OE}$	Q		6.5	8.5	1	11	ns
t_{dis}	$\overline{OE}$	Q		6.7	9	1	12	ns
$t_{sk(o)}$					1.5(2)			ns

5.9 Operating Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1MHz	16	pF

5.10 Typical Characteristics

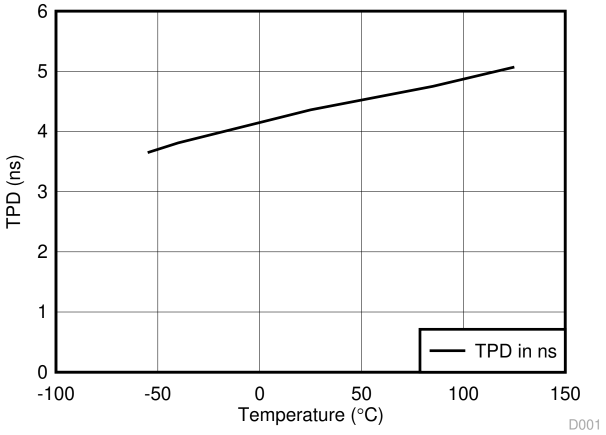


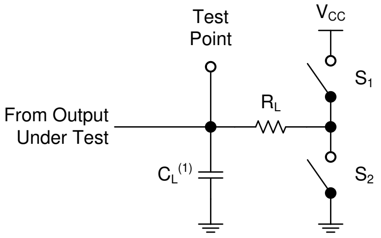
図 5-1. TPD vs Temperature at 5V

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O = 50\Omega$, $R_L = 1k\Omega$, $t_t < 3ns$, $V_t = 1.5V$.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

図 6-1. Load Circuit for 3-State Outputs

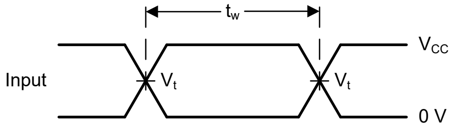


図 6-2. Voltage Waveforms, Pulse Duration

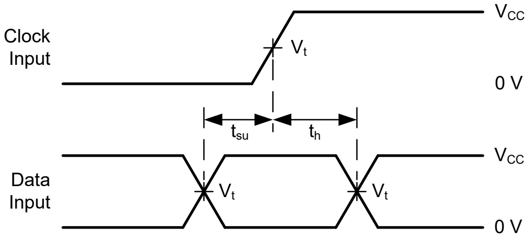
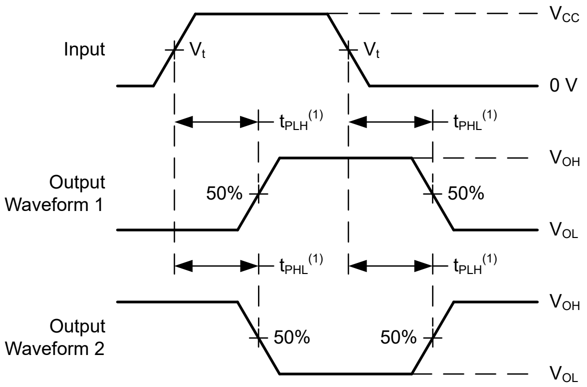
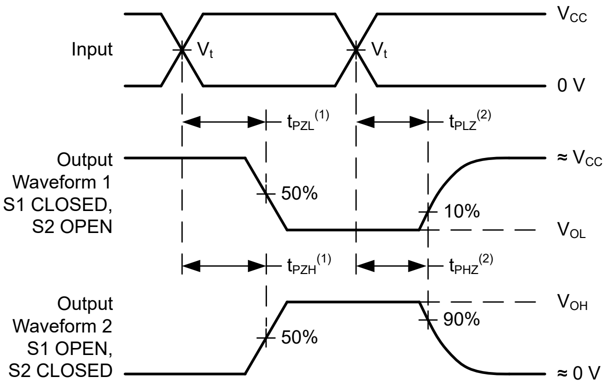


図 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

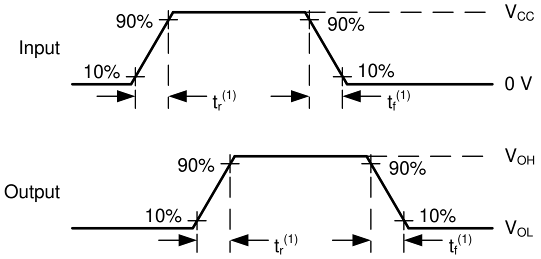
図 6-4. Voltage Waveforms, Propagation Delays



(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

図 6-5. Voltage Waveforms, Propagation Delays for 3-State Outputs



(1) The greater between t_r and t_f is the same as t_t.

図 6-6. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

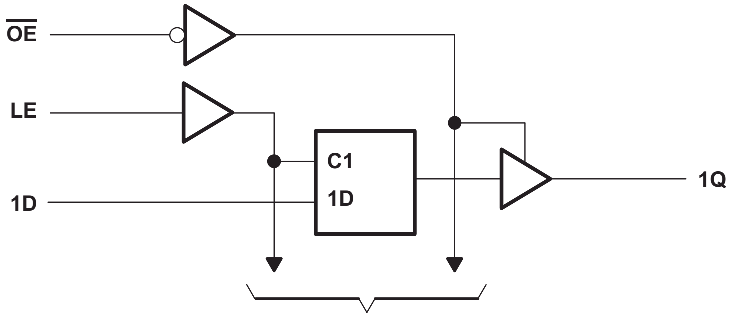
The SNx4AHCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

To put the device in the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pull-up resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

7.2 Functional Block Diagram



To Seven Other Channels

7.3 Feature Description

- TTL inputs
  - Lowered switching threshold allows up translation 3.3V to 5V
- Slow edges reduce output ringing

7.4 Device Functional Modes

表 7-1. Function Table
(Each Latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The SN74AHCT573 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8V V_{IL} and 2V V_{IH}. This feature makes the device an excellent choice for translating up from 3.3V to 5V. 図 8-2 shows this type of translation.

8.2 Typical Application

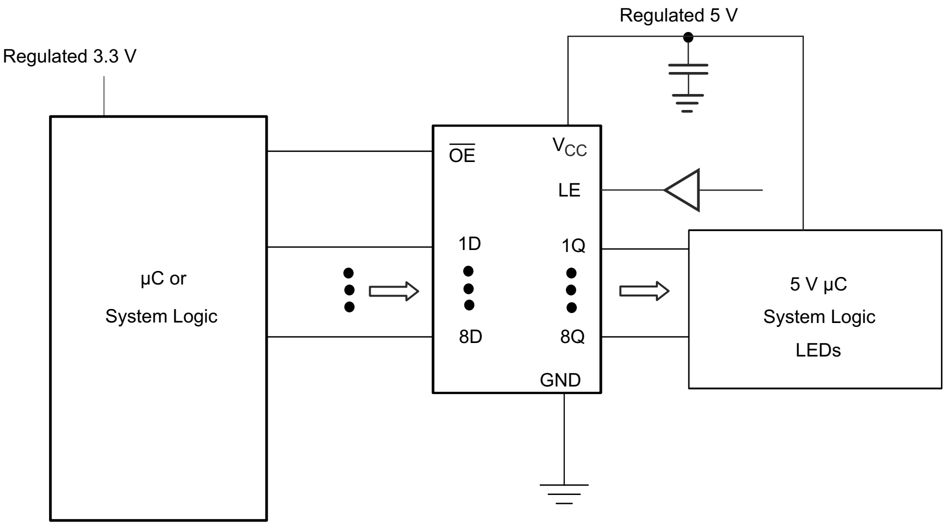


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified High and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommend output conditions
   - Load currents should not exceed 25mA per output and 75mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

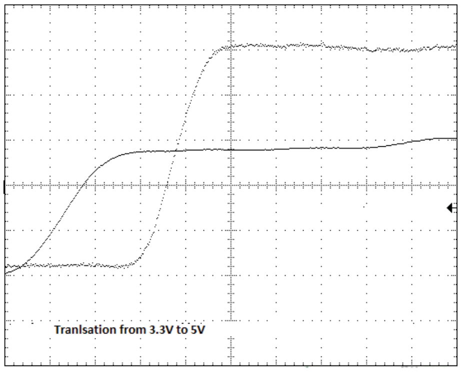


図 8-2. Up Translation

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µF bypass capacitor is recommended. If there are multiple V_{CC} pins, 0.01µF or 0.022µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1µF and 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 図 8-3 specifies the rules that must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they cannot float when disabled.

8.4.2 Layout Example

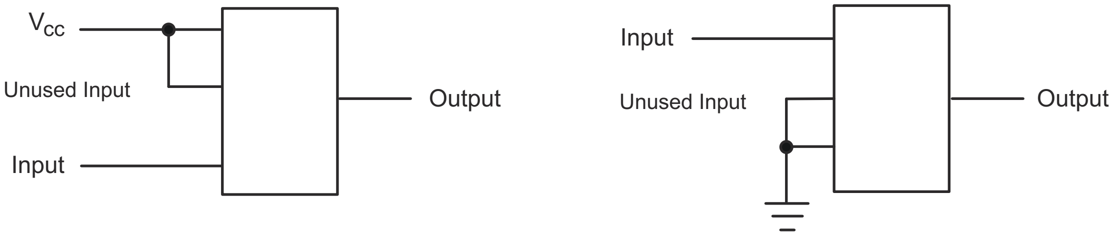


図 8-3. Layout Diagram

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.3 Trademarks

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9.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision P (April 2024) to Revision Q (July 2024) **Page**

- Updated thermal values for PW package from RθJA = 103.3 to 116.8, RθJC(top) = 37.8 to 58.5, RθJB = 54.3 to 78.7, ΨJT = 2.9 to 12.6, ΨJB = 53.8 to 77.9, RθJC(bot) = N/A, all values in °C/W 5

Changes from Revision O (July 2014) to Revision P (April 2024) **Page**

- Moved storage temperature from *Handling Ratings* table to *Absolute Maximum Ratings* table........................ 4
- Changed Handling Ratings table to ESD Ratings table... 4
- Added temperature range column labels in Electrical Characteristics table...5
- Added temperature range column labels in Timing Requirements table...5
- Changed t_{PLH} and t_{PHL} to be t_{pd}, t_{PZH} and t_{PZL} to be t_{en}, and t_{PLZ} and t_{PHZ} to be t_{dis}... 6
- Changed *Switching Characteristics* table to be two tables separating military and catalog device characteristics.. 6
- Changed parameter measurement information section images and tables to improve clarity and update formatting..7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685501QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QR A SNJ54AHCT573J	Samples
5962-9685501QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QS A SNJ54AHCT573W	Samples
SN74AHCT573DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	Samples
SN74AHCT573DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	Samples
SN74AHCT573DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	AHCT573	
SN74AHCT573DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT573	Samples
SN74AHCT573N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT573N	Samples
SN74AHCT573PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125	HB573	
SN74AHCT573PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HB573	Samples
SN74AHCT573PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	Samples
SN74AHCT573PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	Samples
SNJ54AHCT573J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QR A SNJ54AHCT573J	Samples
SNJ54AHCT573W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QS A SNJ54AHCT573W	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHCT573, SN74AHCT573 :

- Catalog : SN74AHCT573

- Military : SN54AHCT573

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

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