

## SNx4HCT244 3 ステート出力、オクタール・バッファ/ライン・ドライバ

### 1 特長

- 4.5V~5.5V の動作電源電圧範囲
- 大電流出力は最大 15 個の LSTTL 負荷を駆動可能
- 低消費電力:  $I_{CC} = 80\mu A$  (最大値)
- $t_{pd} = 13ns$  (標準値)
- 5V で  $\pm 6mA$  の出力駆動能力
- 低い入力電流: 最大値  $1\mu A$
- 入力は TTL 電圧互換
- バス・ラインおよびバッファ・メモリ・アドレス・レジスタを駆動できる 3 ステート出力

### 2 アプリケーション

- サーバー
- LED ディスプレイ
- ネットワーク・スイッチ
- 通信インフラ
- モーター・ドライバ
- I/O エクスパンダ

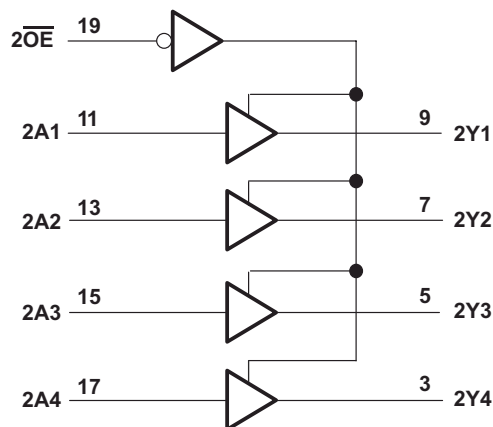
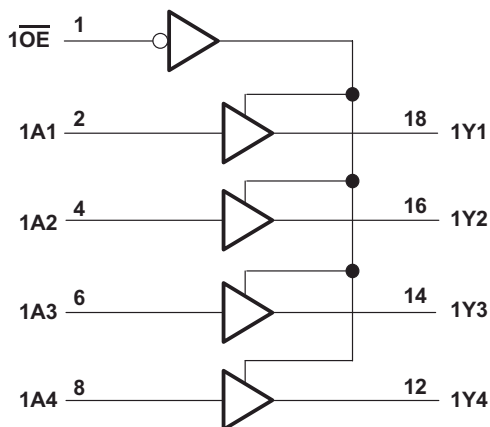
### 3 概要

これらのオクタール・バッファ/ライン・ドライバは、3 ステート・メモリ・アドレス・ドライバ、クロック・ドライバ、バス用レシーバ/トランスミッタの性能と密度の両方を向上することに特化して設計されています。SNx4HCT244 デバイスは、独立した出力イネーブル ( $\overline{OE}$ ) 入力を備えた 2 つの 4 ビット・バッファ/ドライバで構成されています。 $\overline{OE}$  (出力イネーブル) が Low の場合、A 入力からのデータを非反転のまま Y 出力に渡します。 $\overline{OE}$  が High の場合、出力は高インピーダンス状態になります。

#### 製品情報

部品番号	定格	パッケージ (1)
SN74HCT244	カタログ	DB (SSOP, 20)
		DW (SOIC, 20)
		N (PDIP, 20)
		NS (SO, 20)
		PW (TSSOP, 20)
		DGS (VSSOP, 20)
SN54HCT244	軍用	J (CDIP, 20)
		FK (LCCC, 20)

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



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#### 論理図 (正論理)



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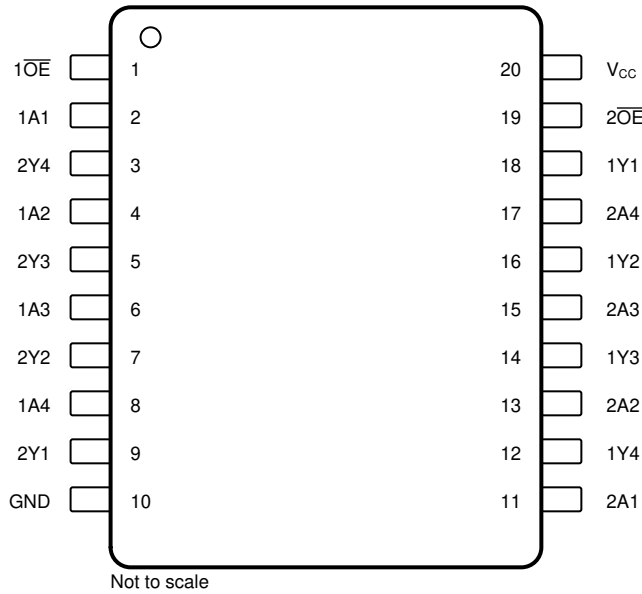
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## 4 Revision History

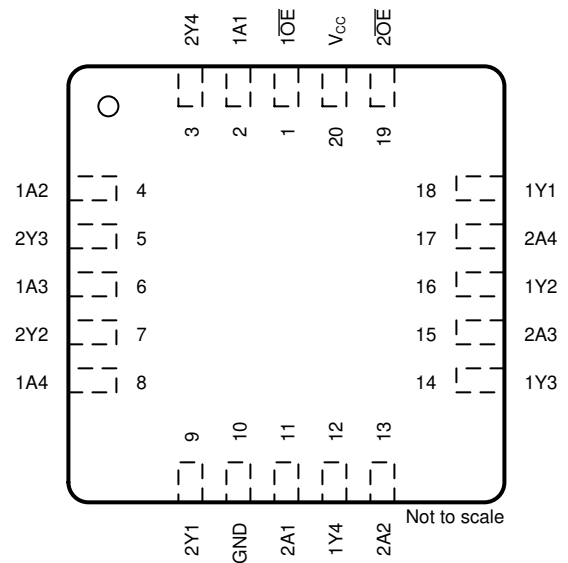
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (December 2022) to Revision H (August 2023)	Page
• DGS (SOT) パッケージのサポート情報を追加.....	1
• 定格を含めるよう「製品情報」表を更新.....	1
• データシートから「W (CFP、20)」パッケージを削除.....	1
Changes from Revision F (May 2022) to Revision G (December 2022)	Page
• DGS (SOT) のパッケージ情報を追加.....	1
• Added DGS (SOT) package information.....	3
• Added DGS (SOT) package thermal information.....	5
Changes from Revision E (August 2016) to Revision F (May 2022)	Page
• Junction-to-ambient thermal resistance values increased. DW was 76.6 is now 109.1, DB was 89.4 is now 122.7, N was 44.8 is now 84.6, NS was 71.8 is now 113.4, PW was 97.4 is now 131.8.....	5
Changes from Revision D (August 2013) to Revision E (August 2016)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• 「注文情報」表を削除 (データシートの末尾にある POA を参照).....	1
• Changed <i>Thermal Information</i> table.....	5
• Added ESD warning.....	9

## 5 Pin Configuration and Functions



**J, DB, DW, N, NS, PW or DGS Packages, 20-Pin  
CDIP, CFP, SSOP, SOIC, PDIP, SO, TSSOP, or  
VSSOP (Top View)**



**FK Package, 20-Pin LCCC (Top View)**

**表 5-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1 OE	1	I	Output enable
1A1	2	I	Input
2Y4	3	O	Output
1A2	4	I	Input
2Y3	5	O	Output
1A3	6	I	Input
2Y2	7	O	Output
1A4	8	I	Input
2Y1	9	O	Output
GND	10	—	Ground
2A1	11	I	Input
1Y4	12	O	Output
2A2	13	I	Input
1Y3	14	O	Output
2A3	15	I	Input
1Y2	16	O	Output
2A4	17	I	Input
1Y1	18	O	Output
2 OE	19	I	Output enable
V <sub>CC</sub>	20	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±35	mA
	Continuous channel current through V <sub>CC</sub> or GND			±70	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
<b>SN74HCT244 in DB, DW, N, NS, or PW package</b>				
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
<b>SN54HCT244 in J or FK package</b>				
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM)	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8	V
V <sub>I</sub>	Input voltage		0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise and fall time				500	ns
T <sub>A</sub>	Operating free-air temperature	SN54HCT244	-55		125	°C
		SN74HCT244 <sup>(2)</sup>	-40		85	
			-40		125	

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the [Implications of Slow or Floating CMOS Inputs](#) application report.
- (2) For correct operating free-air temperature, see the orderable addendum at the end of the data sheet.

## 6.4 Thermal Information

THERMAL METRIC		SN74HCT244						UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	DGS (VSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	109.1	122.7	84.6	113.4	131.8	130.6	°C/W
R <sub>θJC (top)</sub>	Junction-to-case (top) thermal resistance	76	81.6	72.5	78.6	72.2	68.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	77.6	77.5	65.3	78.4	82.8	85.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	51.5	46.1	55.3	47.1	21.5	10.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	85.0	°C/W
R <sub>θJC (bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics - SN54HCT244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4			V
		I <sub>OH</sub> = -6 mA		3.98	4.3		3.7			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1			0.1	V
		I <sub>OL</sub> = 6 mA			0.17	0.26		0.4		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		5.5 V		±0.1	±100			±1000	nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		5.5 V		±0.01	±0.5			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V			8			160	μA
ΔI <sub>CC</sub> <sup>(1)</sup>	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>		5.5 V		1.4	2.4			3	mA
C <sub>i</sub>			4.5 V to 5.5 V		3	10			10	pF

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 6.6 Electrical Characteristics - SN74HCT244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4		V		
		I <sub>OH</sub> = -6 mA		3.98	4.3		3.84		3.7				
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V	0.001		0.1	0.1		0.1		V		
		I <sub>OL</sub> = 6 mA		0.17		0.26	0.33		0.4				
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		5.5 V	±0.1	±100		±1000		±1000		nA		
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		5.5 V	±0.01	±0.5		±5		±10		μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V			8	80		160		μA		
ΔI <sub>CC</sub> <sup>(1)</sup>	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>		5.5 V	1.4	2.4		2.9		3		mA		
C <sub>i</sub>			4.5 V to 5.5 V	3	10		10		10		pF		

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 6.7 Switching Characteristics: SN54HCT244

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			-55°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	4.5 V	C <sub>L</sub> = 50 pF		15	28	42		ns
				C <sub>L</sub> = 150 pF		21	45	68		
			5.5 V	C <sub>L</sub> = 50 pF		13	25	38		
				C <sub>L</sub> = 150 pF		18	40	61		
t <sub>en</sub>	OE	Y	4.5 V	C <sub>L</sub> = 50 pF		21	35	53		ns
				C <sub>L</sub> = 150 pF		25	52	79		
			5.5 V	C <sub>L</sub> = 50 pF		19	32	48		
				C <sub>L</sub> = 150 pF		22	47	71		
t <sub>dis</sub>	OE	Y	4.5 V	C <sub>L</sub> = 50 pF		19	35	53		ns
			5.5 V	C <sub>L</sub> = 50 pF		18	32	48		
t <sub>t</sub>		Y	4.5 V	C <sub>L</sub> = 50 pF		8	12	18		ns
				C <sub>L</sub> = 150 pF		17	42	63		
			5.5 V	C <sub>L</sub> = 50 pF		7	11	16		
				C <sub>L</sub> = 150 pF		14	38	57		

## 6.8 Switching Characteristics: SN74HCT244

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

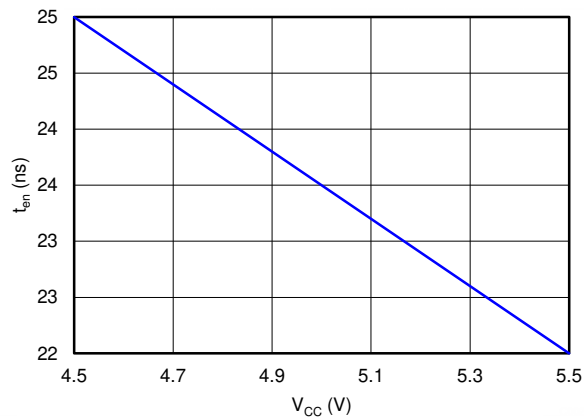
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			-40°C to 85°C		-40°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	4.5 V	C <sub>L</sub> = 50 pF	15	28		35		42	ns	
				C <sub>L</sub> = 150 pF	21	45		56		68		
			5.5 V	C <sub>L</sub> = 50 pF	13	25		32		38		
				C <sub>L</sub> = 150 pF	18	40		51		61		
t <sub>en</sub>	OE	Y	4.5 V	C <sub>L</sub> = 50 pF	21	35		44		53	ns	
				C <sub>L</sub> = 150 pF	25	52		65		79		
			5.5 V	C <sub>L</sub> = 50 pF	19	32		40		48		
				C <sub>L</sub> = 150 pF	22	47		59		71		
t <sub>dis</sub>	OE	Y	4.5 V	C <sub>L</sub> = 50 pF	19	35		44		53	ns	
			5.5 V		18	32		40		48		
t <sub>t</sub>		Y	4.5 V	C <sub>L</sub> = 50 pF	8	12		15		18	ns	
				C <sub>L</sub> = 150 pF	17	42		53		63		
			5.5 V	C <sub>L</sub> = 50 pF	7	11		14		16		
				C <sub>L</sub> = 150 pF	14	38		48		57		

## 6.9 Operating Characteristics

T<sub>A</sub> = 25°C

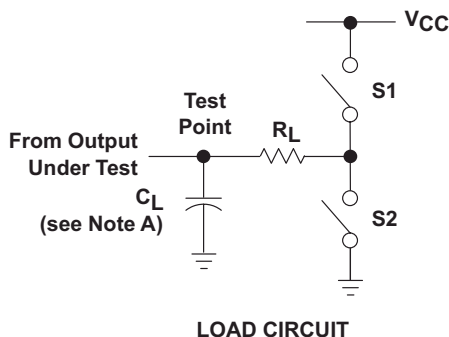
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per buffer or driver No load	40	pF

## 6.10 Typical Characteristics

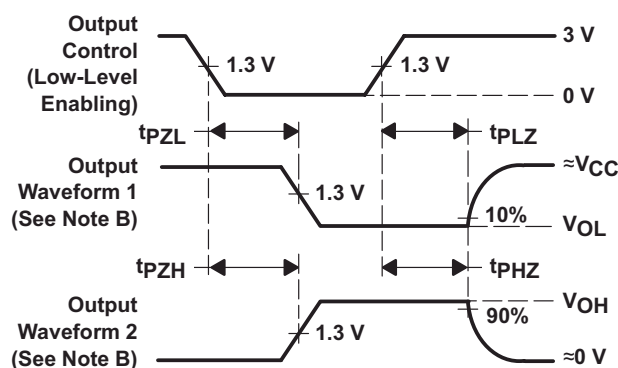
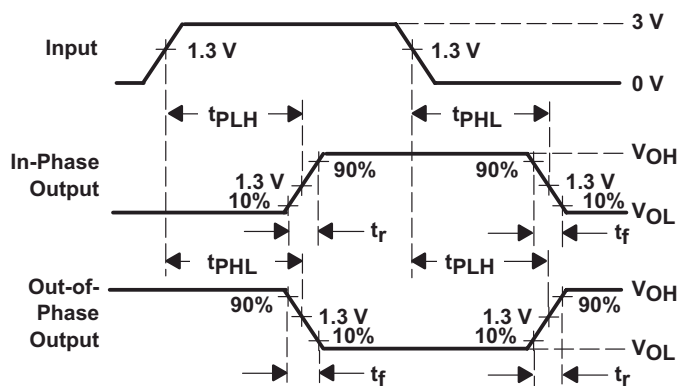
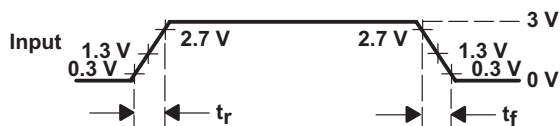


**Figure 6-1. Enable Time vs V<sub>CC</sub>**

## 7 Parameter Measurement Information



PARAMETER		$R_L$	$C_L$	S1	S2
$t_{en}$	$t_{pZH}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
	$t_{pZL}$			Closed	Open
$t_{dis}$	$t_{pHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{pLZ}$			Closed	Open
$t_{pd}$ or $t_t$		—	50 pF or 150 pF	Open	Open



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
  - G.  $t_{pLH}$  and  $t_{pHL}$  are the same as  $t_{pd}$ .

**7-1. Load Circuit and Voltage Waveforms**

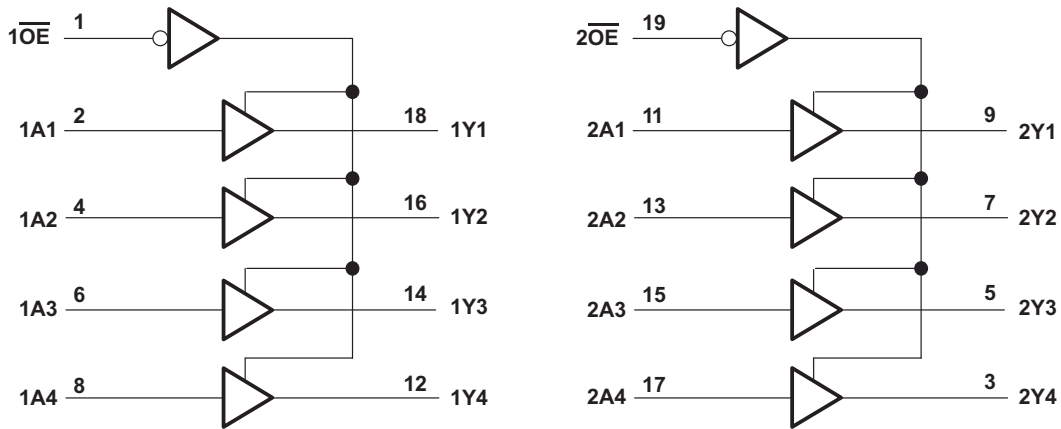


## 8 Detailed Description

### 8.1 Overview

The SNx4HCT244 device is organized as two 4-bit buffers and line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. For the high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



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图 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

The SN74HCT244 device can drive up to 15 LSTTL loads. This device has low power consumption of 80- $\mu$ A  $I_{CC}$ . The SN74HCT244 also has 3 state outputs that allow the outputs to go to high impedance, low or high.

### 8.4 Device Functional Modes

表 8-1 lists the functions of the SNx4HC244.

表 8-1. Function Table

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

## 9 Application and Implementation

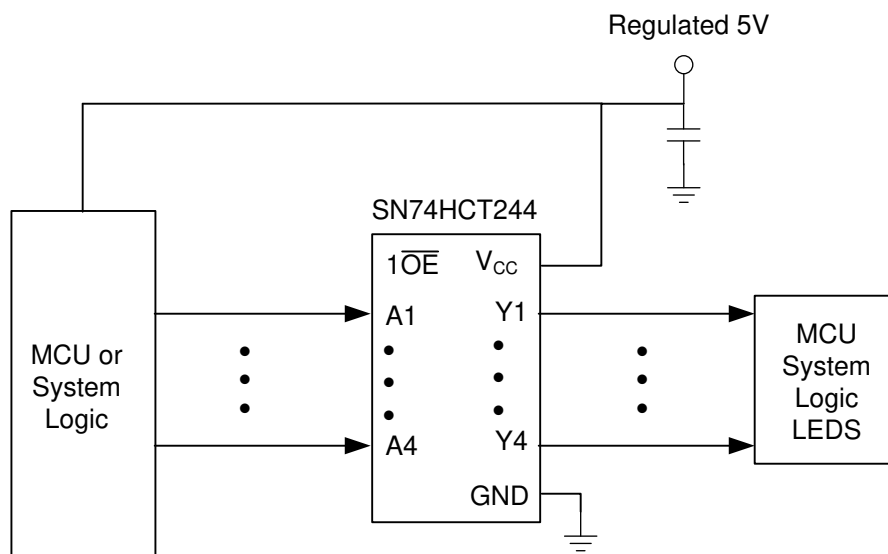
### 注

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### 9.1 Application Information

The SN74HC244 is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

### 9.2 Typical Application



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图 9-1. Application Schematic

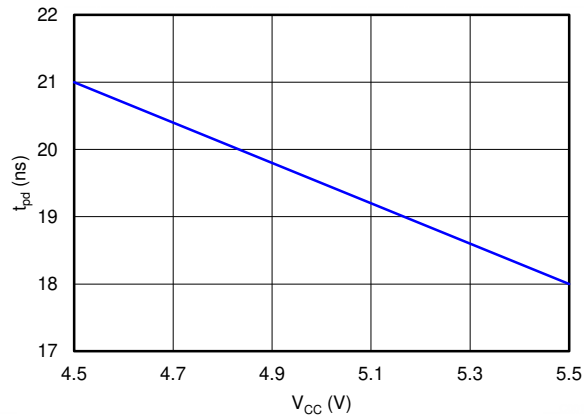
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in [Recommended Operating Conditions](#).
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#).
- Recommend output conditions:
  - Load currents must not exceed the  $I_O$  maximum per output and must not exceed the continuous current through  $V_{CC}$  or GND total current for the part. These limits are located in [Absolute Maximum Ratings](#).
  - Outputs must not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curve



**Figure 9-2. Propagation Delay vs V<sub>CC</sub>**

### 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V<sub>CC</sub> terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor. If there are multiple V<sub>CC</sub> terminals, then TI recommends 0.01-μF or 0.022-μF capacitors for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

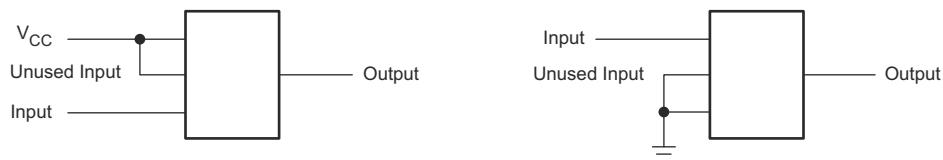
### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input and gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 9-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V<sub>CC</sub>, whichever makes more sense or is more convenient.

#### 9.4.2 Layout Example



**Figure 9-3. Layout Diagram**

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

### 10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8513001VRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8513001VR A SNV54HCT244J	Samples
5962-8513001VSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8513001VS A SNV54HCT244W	Samples
85130012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85130012A SNJ54HCT 244FK	Samples
8513001RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8513001RA SNJ54HCT244J	Samples
JM38510/65755B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755B2A	Samples
JM38510/65755BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755BRA	Samples
M38510/65755B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755B2A	Samples
M38510/65755BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755BRA	Samples
SN54HCT244J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HCT244J	Samples
SN74HCT244DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SN74HCT244DGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HT244	Samples
SN74HCT244DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	HCT244	
SN74HCT244DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT244N	Samples
SN74HCT244NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT244N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT244NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	<a href="#">Samples</a>
SN74HCT244PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	HT244	
SN74HCT244PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HT244	<a href="#">Samples</a>
SN74HCT244PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HT244	<a href="#">Samples</a>
SN74HCT244PWT	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	HT244	
SNJ54HCT244FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85130012A SNJ54HCT 244FK	<a href="#">Samples</a>
SNJ54HCT244J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8513001RA SNJ54HCT244J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HCT244, SN54HCT244-SP, SN74HCT244 :**

- Catalog : [SN74HCT244](#), [SN54HCT244](#)
  
- Automotive : [SN74HCT244-Q1](#), [SN74HCT244-Q1](#)
  
- Enhanced Product : [SN74HCT244-EP](#), [SN74HCT244-EP](#)
  
- Military : [SN54HCT244](#)
  
- Space : [SN54HCT244-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
  
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
  
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
  
- Military - QML certified for Military and Defense Applications
  
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT244DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74HCT244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HCT244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HCT244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HCT244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HCT244DGSR	VSSOP	DGS	20	5000	356.0	356.0	35.0
SN74HCT244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HCT244DWR	SOIC	DW	20	2000	356.0	356.0	41.0
SN74HCT244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT244PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT244PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8513001VSA	W	CFP	20	25	506.98	26.16	6220	NA
85130012A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65755B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/65755B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HCT244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HCT244FK	FK	LCCC	20	55	506.98	12.06	2030	NA

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## 重要なお知らせと免責事項

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郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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