

SNx4LVC02A クワッド、2 入力、正論理 NOR ゲート

1 特長

- 1.65V～3.6V で動作
- 40°C～85°C、
-40°C～125°C、-55°C～125°C で動作を規定
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 4.4ns (3.3V 時)
- V_{OLP} 標準値 (出力グランド バウンス)
<0.8V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- V_{OHV} 標準値 (出力 V_{OH} アンダーシュート)
>2V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 概要

入力は 3.3V または 5V のデバイスから駆動できます。この機能により、3.3V と 5V が混在するシステム環境での変換装置としてこのデバイスを使用できます。

デバイスは、ブール関数 $Y = \overline{A + B}$ すなわち $Y = \bar{A} \cdot \bar{B}$ を正論理で実行します。

入力は 3.3V または 5V のデバイスから駆動できます。この機能により、3.3V と 5V が混在するシステム環境での変換装置としてこのデバイスを使用できます。

製品情報

部品番号	パッケージサイズ ⁽¹⁾	パッケージサイズ ⁽²⁾	本体サイズ ⁽³⁾
SNx4LVC02A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	RGY (VQFN, 14)	3.5mm × 3.5mm	3.5mm × 3.5mm
	FK (LCCC, 20)	8.9mm × 8.9mm	8.89mm × 8.89mm
	J (CDIP, 14)	19.55mm × 7.9mm	19.55mm × 6.7mm
	W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



各ゲートの論理図 (正論理)

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3 Pin Configuration and Functions

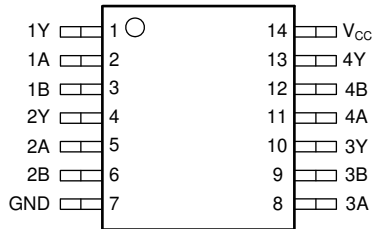


図 3-1. SN54LVC02A J or W Package, 14-Pin (Top View)

SN74LVC02A D, DB, NS, or PW Package, 14-Pin SOIC, SSOP, SOP or TSSOP (Top View)

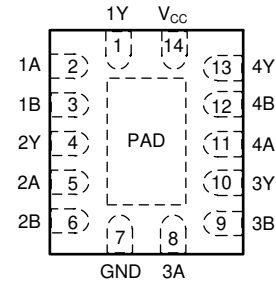


図 3-2. SN74LVC02A RGY or BQA Package, 14-Pin VQFN or WQFN (Top View)

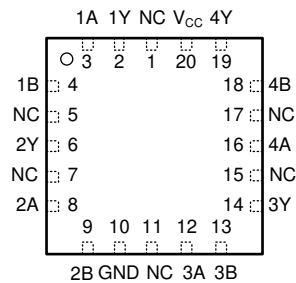


図 3-3. SN54LVC02A FK Package, 20-Pin (Top View)

表 3-1. Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	SN74LVC02A D, DB, NS, PW, RGY, BQA	SN54LVC02A J, W FK		
1Y	1	1 2	O	1Y Output
1A	2	2 3	I	1A Input
1B	3	3 4	I	1B Input
2Y	4	4 6	O	2Y Output
2A	5	5 8	I	2A Input
2B	6	6 9	I	2B Input
GND	7	7 10	—	Ground Pin
3A	8	8 12	I	3A Input
3B	9	9 13	I	3B Input
3Y	10	20 14	O	3Y Output
4A	11	11 16	I	4A Input
4B	12	12 18	I	4B Input
4Y	13	13 19	O	4Y Output
V _{CC}	14	14 20	—	Power Pin
NC	—	— 1, 5, 7, 11, 15, 17	—	No Connection

(1) I = input, O = output

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽¹⁾	-0.5	6.5	V
V _O	Output voltage range ^{(1) (2)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current			±50 mA
	Continuous current through V _{CC} or GND			±100 mA
T _{stg}	Storage temperature range	-65	150	°C
P _{tot}	Power dissipation	T _A = -40°C to 125°C ^{(3) (4)}		500 mW

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of V_{CC} is provided in the recommended operating conditions table.

(3) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.

(4) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

4.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions, SN54LVC02A

		SN54LVC02A		UNIT
		-55°C to 125°C		
		MIN	MAX	
V _{CC}	Supply voltage	Operating	2 3.6	V
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 2.7V to 3.6V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7V to 3.6V		V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7V	-12	mA
		V _{CC} = 3V	-24	
I _{OL}	Low-level output current	V _{CC} = 2.7V	12	mA
		V _{CC} = 3V	24	

4.4 Recommended Operating Conditions, SN74LVC02A

		SN74LVC02A						UNIT	
		T _A = 25°C		-40°C to 85°C		-40°C to 125°C			
		MIN	MAX	MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		

			SN74LVC02A						UNIT
			T _A = 25°C		–40°C to 85°C		–40°C to 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH}	High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7		1.7		1.7		
		V _{CC} = 2.7V to 3.6V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65V to 1.95V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3V to 2.7 V	0.7		0.7		0.7		
		V _{CC} = 2.7V to 3.6 V	0.8		0.8		0.8		
V _I	Input voltage	0	5.5	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65V	–4		–4		–4		mA
		V _{CC} = 2.3V	–8		–8		–8		
		V _{CC} = 2.7V	–12		–12		–12		
		V _{CC} = 3V	–24		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65V	4		4		4		mA
		V _{CC} = 2.3V	8		8		8		
		V _{CC} = 2.7V	12		12		12		
		V _{CC} = 3V	24		24		24		

4.5 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC02A						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	102.3	86	140.4	123.8	150.8	92.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

4.6 Electrical Characteristics, SN54LVC02A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC02A			UNIT
			–55°C to 125°C			
			MIN	TYP	MAX	
V _{OH}	I _{OH} = –100μA	2.7V to 3.6V	V _{CC} – 0.2			V
	I _{OH} = –12mA	2.7V	2.2			
	I _{OH} = –24mA	3V	2.4			
V _{OL}	I _{OL} = 100μA	2.7V to 3.6V	0.2			V
	I _{OL} = 12mA	2.7V	0.4			
	I _{OL} = 24mA	3V	0.55			
I _I	V _I = 5.5V or GND	3.6V	±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V	10			μA
ΔI _{CC}	One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND	2.7V to 3.6V	500			μA

SN54LVC02A, SN74LVC02A

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over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC02A			UNIT
			–55°C to 125°C			
			MIN	TYP	MAX	
C _i	V _I = V _{CC} or GND	3.3V	5 ⁽¹⁾			pF

 (1) T_A = 25°C

4.7 Electrical Characteristics, SN74LVC02A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC02A						UNIT	
			T _A = 25°C			–40°C to 85°C		–40°C to 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{OH}	I _{OH} = –100μA	1.65V to 3.6V	V _{CC} – 0.2			V _{CC} – 0.2		V _{CC} – 0.3		V
	I _{OH} = –4mA	1.65V	1.29			1.2		1.05		
	I _{OH} = –8mA	2.3V	1.9			1.7		1.55		
	I _{OH} = –12mA	2.7V	2.2			2.2		2.05		
	I _{OH} = –24mA	3V	2.4			2.4		2.25		
V _{OL}	I _{OL} = 100μA	1.65V to 3.6V				0.1		0.2		V
	I _{OL} = 4mA	1.65V				0.24		0.45		
	I _{OL} = 8mA	2.3V				0.3		0.7		
	I _{OL} = 12mA	2.7V				0.4		0.4		
	I _{OL} = 24mA	3V				0.55		0.55		
I _I	V _I = 5.5V or GND	3.6V				±1		±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V				1		10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7V to 3.6V				500		500		μA
C _i	V _I = V _{CC} or GND	3.3 V				5				pF

4.8 Switching Characteristics, SN54LVC02A

 over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC02A		UNIT
				–55°C to 125°C		
				MIN	MAX	
t _{pd}	A or B	Y	2.7V	5.4		ns
			3.3V ± 0.3V	1	4.4	

4.9 Switching Characteristics, SN74LVC02A

 over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC02A						UNIT	
				T _A = 25°C			–40°C to 85°C		–40°C to 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{pd}	A or B	Y	1.8V ± 0.15V	1	3.8	8.4	1	8.9	1	10.4	ns
			2.5V ± 0.2V	1	2.9	6.9	1	7.4	1	9.5	
			2.7V	1	3	5.2	1	5.4	1	7	
			3.3V ± 0.3V	1	3.6	4.2	1	4.4	1	5.5	

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

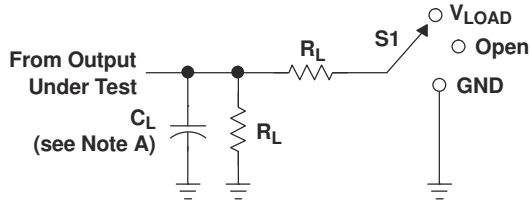
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC02A				UNIT			
				T _A = 25°C			–40°C to 85°C		–40°C to 125°C		
				MIN	TYP	MAX	MIN		MAX	MIN	MAX
t _{sk(o)}			3.3V ± 0.3V				1	1.5	ns		

4.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10MHz	1.8V	7.5	pF
			2.5V	8.5	
			3.3V	9.5	

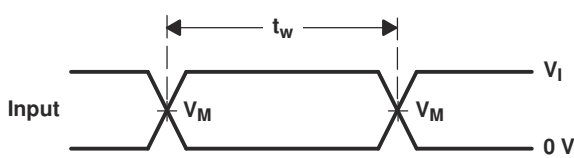
5 Parameter Measurement Information



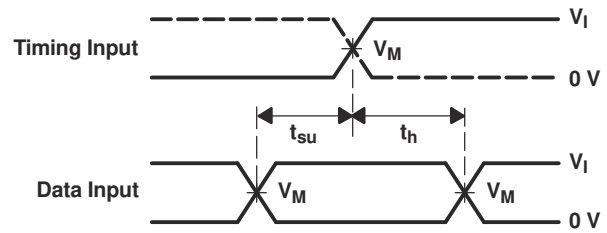
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

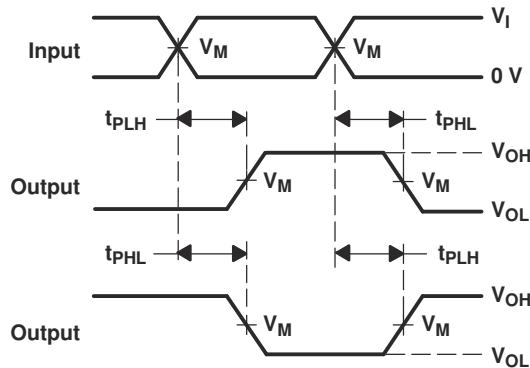
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



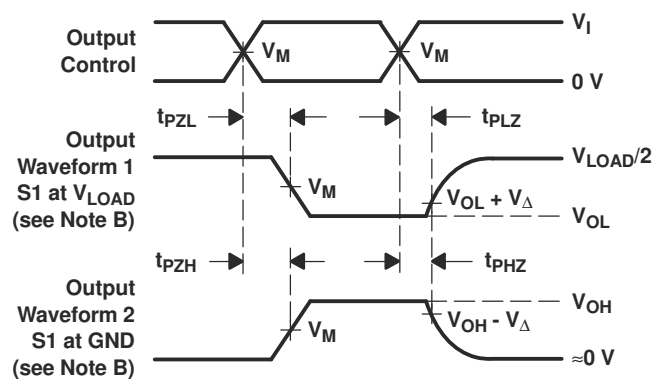
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Functional Block Diagram



☒ 6-1. Logic Diagram, Each Gate (Positive Logic)

6.2 Device Functional Modes

**Function Table
(Each Gate)**

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.2.2 Layout Example

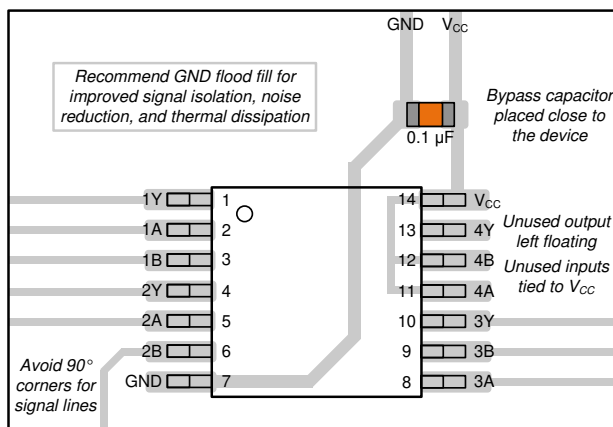


図 7-1. Example Layout for the SNx4LVC02A

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC02A	Click here	Click here	Click here	Click here	Click here
SN74LVC02A	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision R (March 2024) to Revision S (May 2024)	Page
• Updated RθJA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.....	5

Changes from Revision Q (July 2005) to Revision R (March 2024) **Page**

- 「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加..... **1**
- 「パッケージ情報」表、「ピン構成および機能」セクション、および「熱に関する情報」表に **BQA** パッケージを追加..... **1**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9760401Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9760401Q2A SNJ54LVC 02AFK	Samples
5962-9760401QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760401QC A SNJ54LVC02AJ	Samples
5962-9760401QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760401QD A SNJ54LVC02AW	Samples
SN74LVC02ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	Samples
SN74LVC02AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	Samples
SN74LVC02ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	Samples
SN74LVC02ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	Samples
SN74LVC02ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	Samples
SN74LVC02ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02A	Samples
SN74LVC02APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	Samples
SN74LVC02APWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	Samples
SN74LVC02APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	Samples
SN74LVC02APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02A	Samples
SN74LVC02ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC02A	Samples
SNJ54LVC02AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9760401Q2A SNJ54LVC 02AFK	Samples
SNJ54LVC02AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760401QC A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LVC02AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LVC02AJ 5962-9760401QD A SNJ54LVC02AW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LVC02A, SN74LVC02A :

- Catalog : [SN74LVC02A](#)
- Automotive : [SN74LVC02A-Q1](#), [SN74LVC02A-Q1](#)
- Enhanced Product : [SN74LVC02A-EP](#), [SN74LVC02A-EP](#)
- Military : [SN54LVC02A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC02ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC02ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC02ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC02ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC02APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC02APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC02ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC02ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC02ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC02ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC02ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC02APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC02APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC02ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

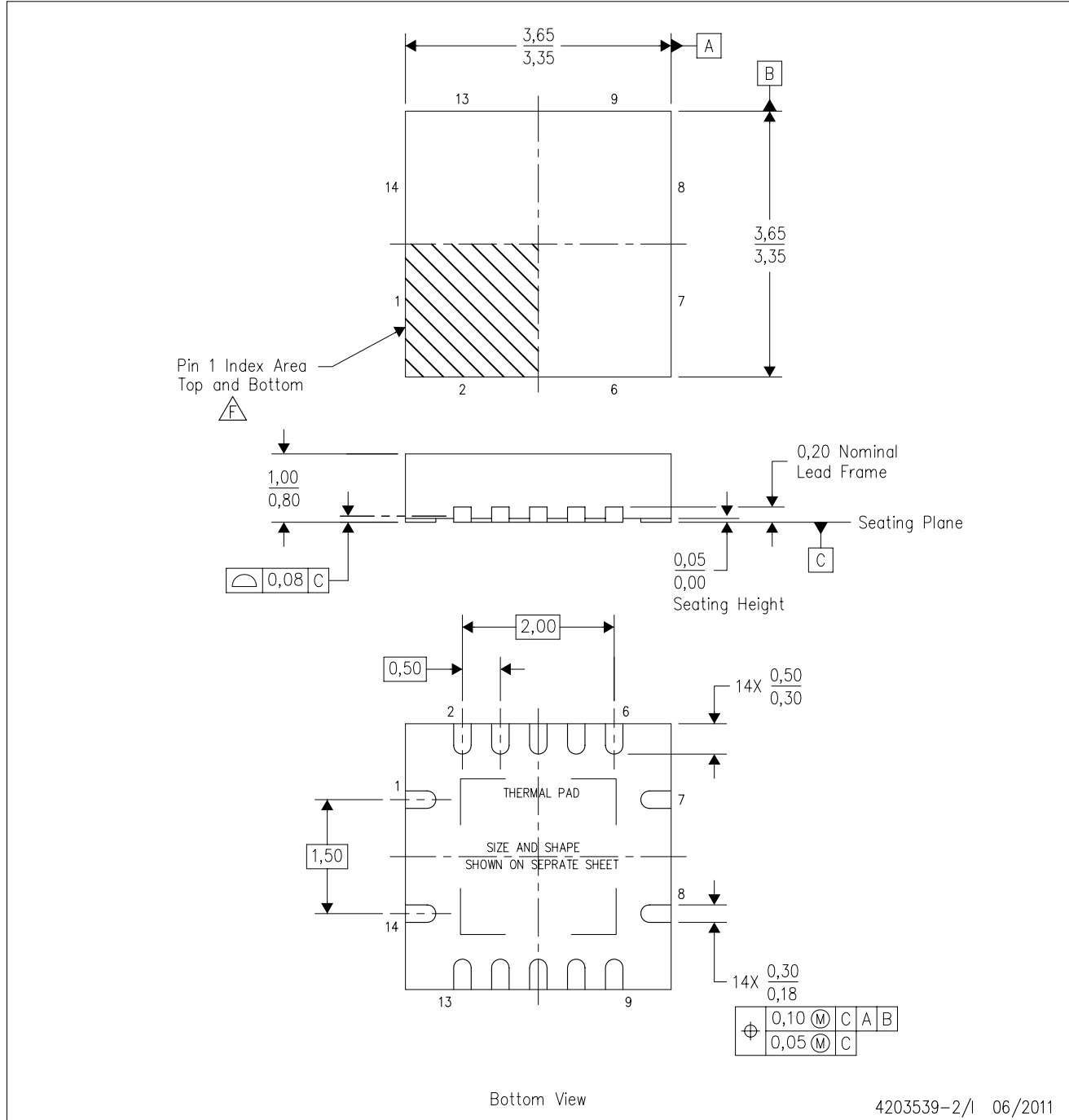
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9760401Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9760401QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC02AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC02APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC02APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC02AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC02AW	W	CFP	14	25	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - $\triangle F$ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

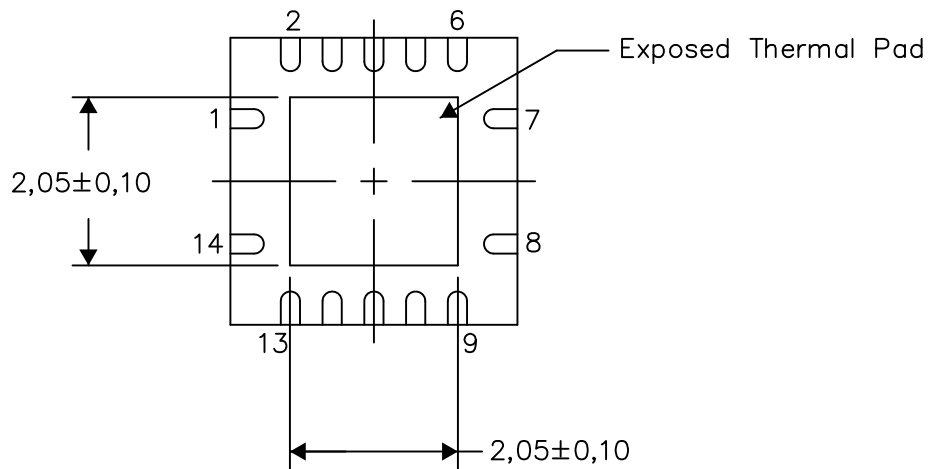
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

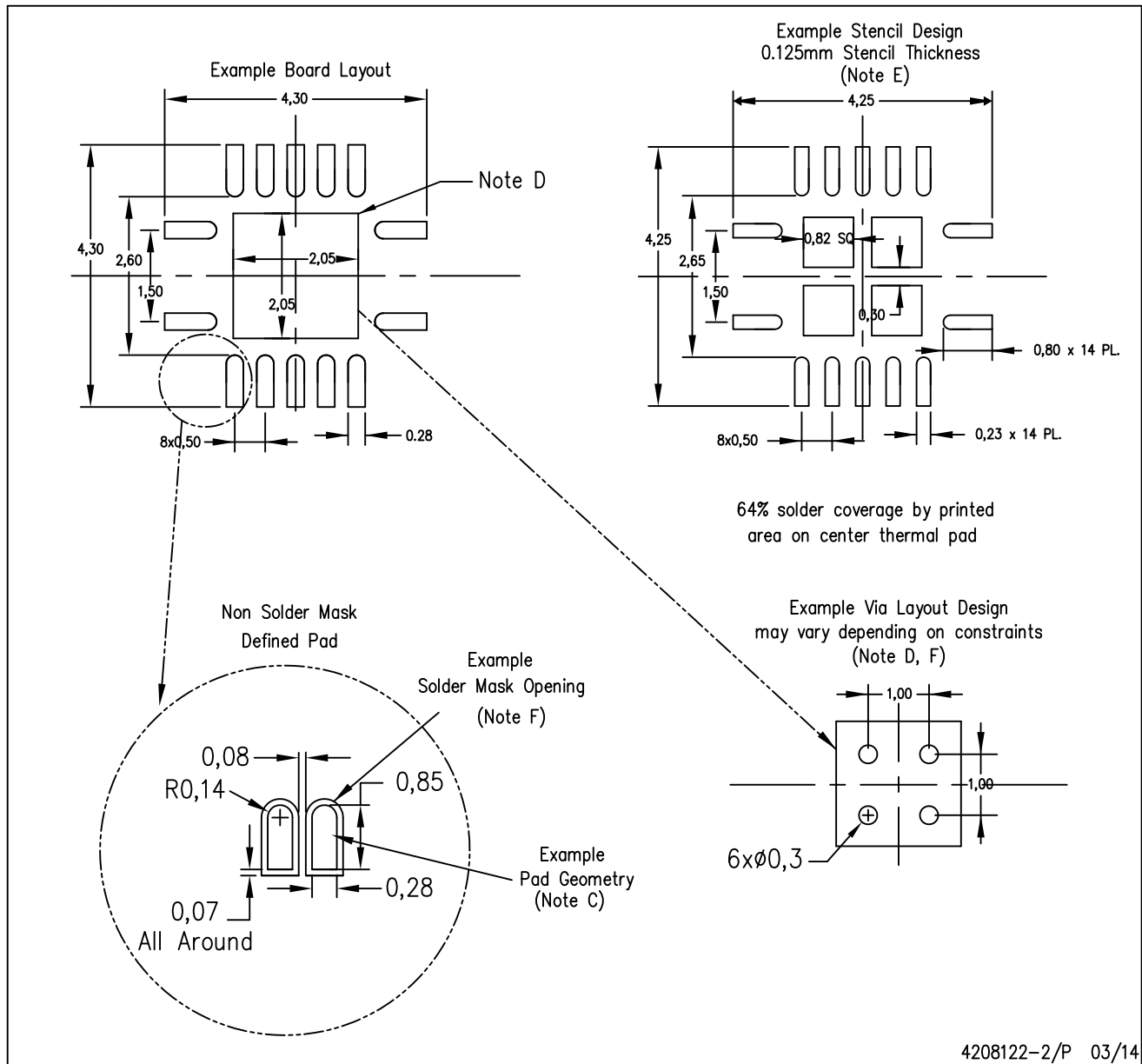
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

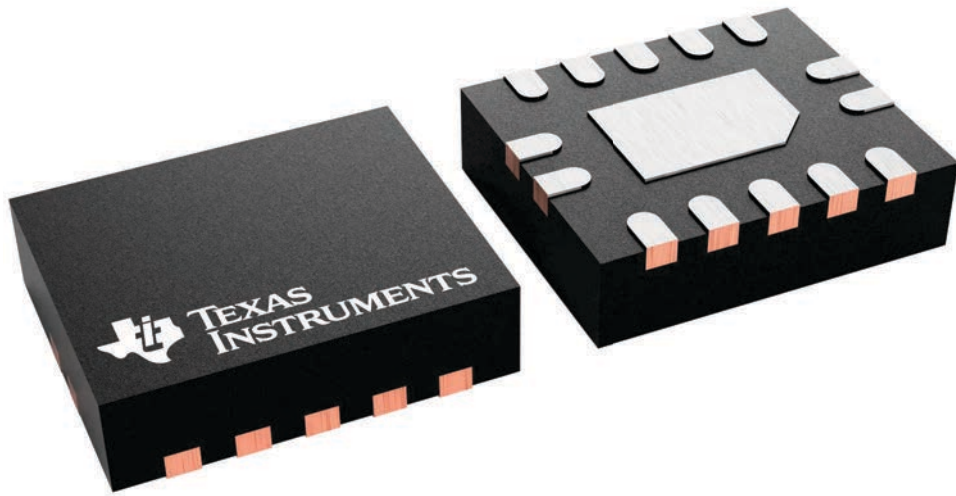
BQA 14

WQFN - 0.8 mm max height

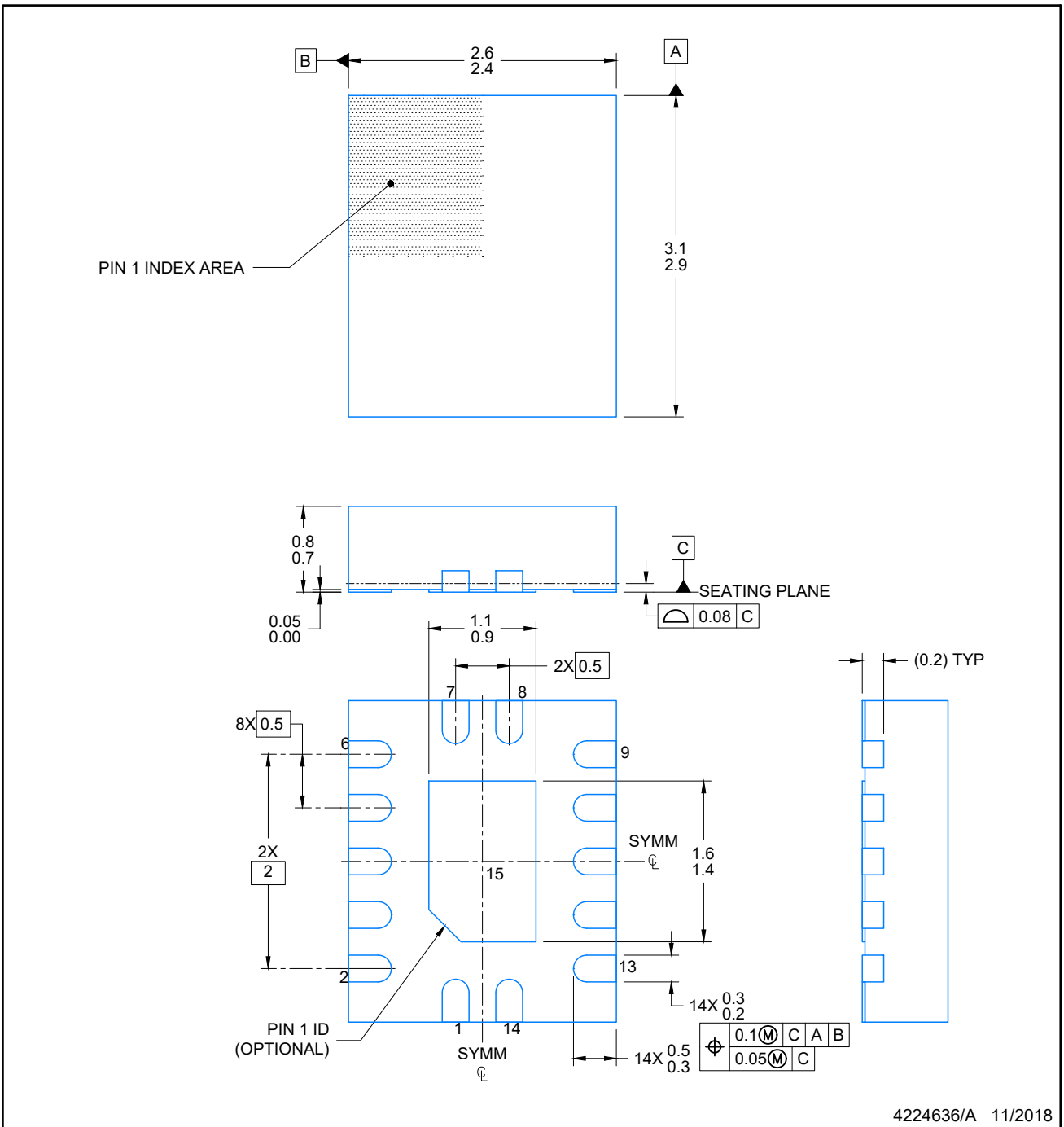
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



NOTES:

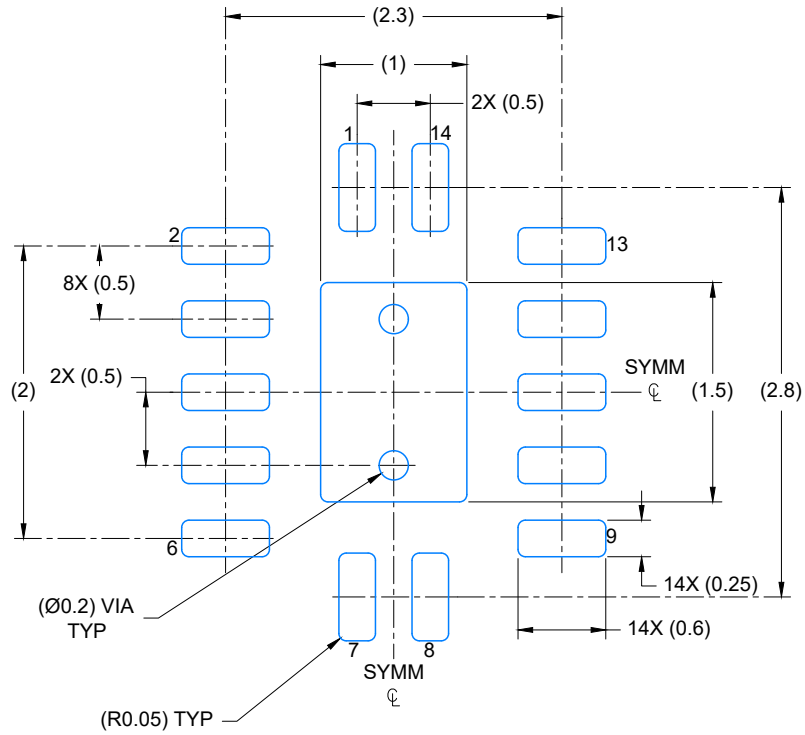
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

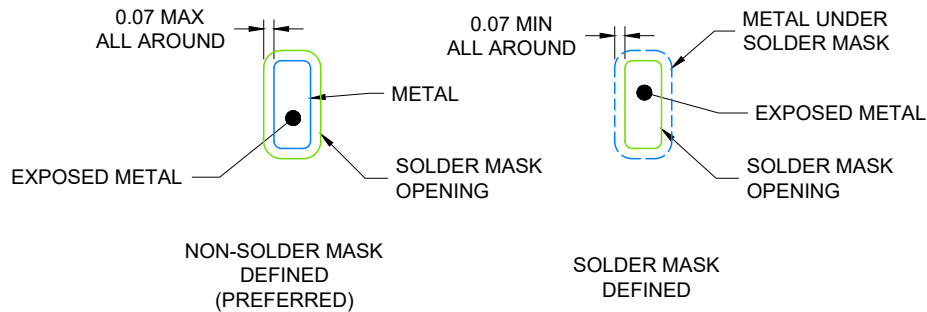
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

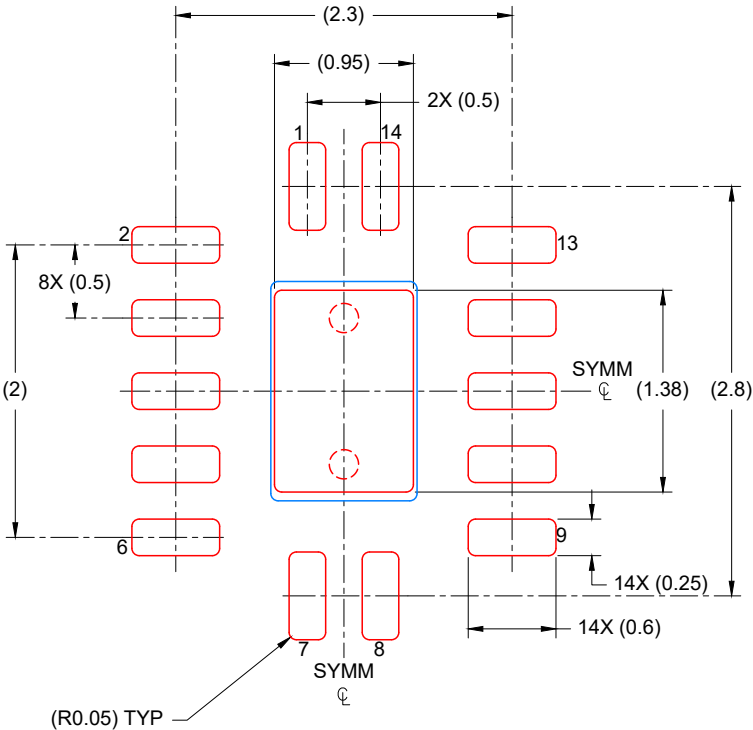
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

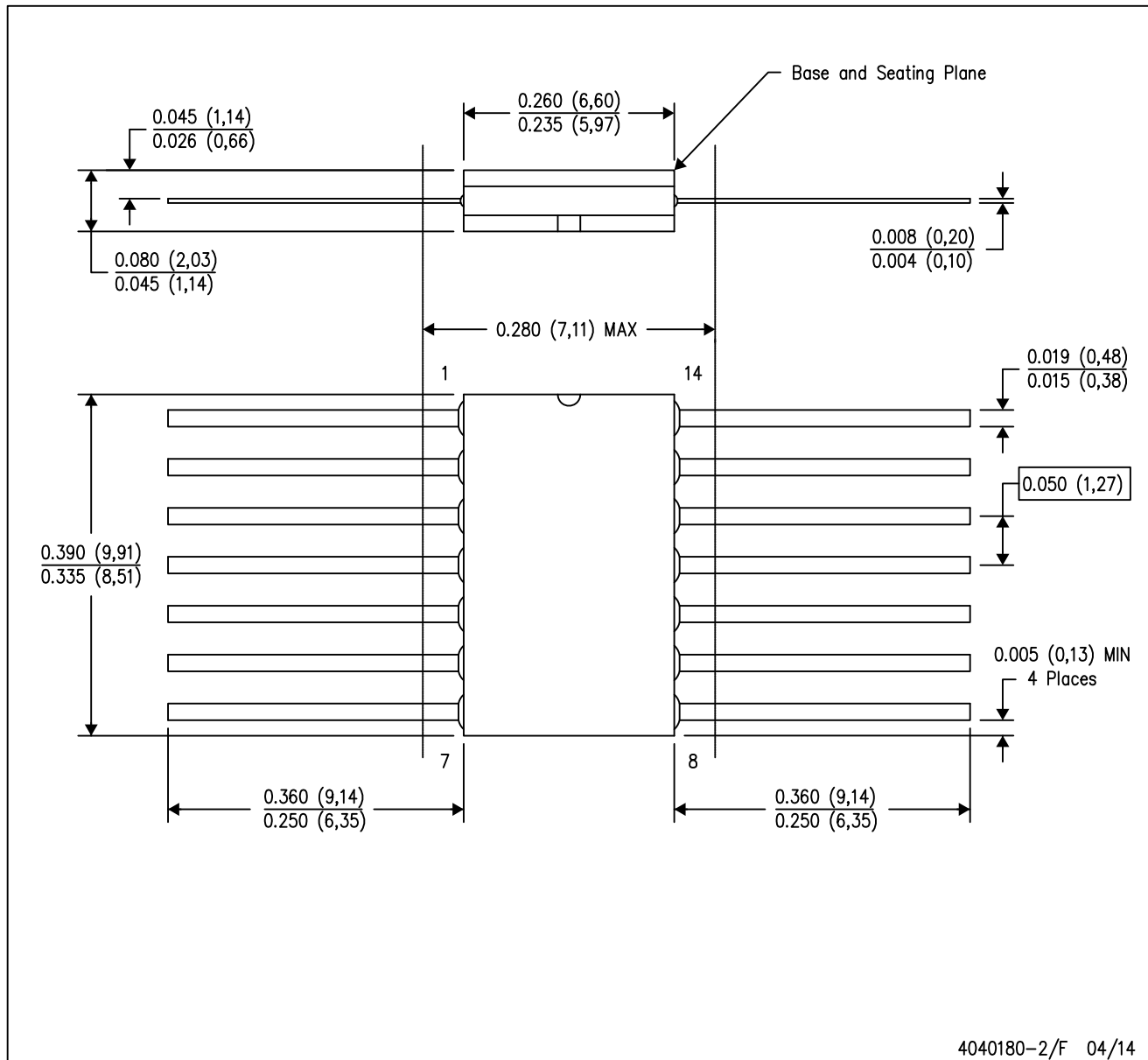
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

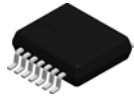
CERAMIC DUAL FLATPACK



4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

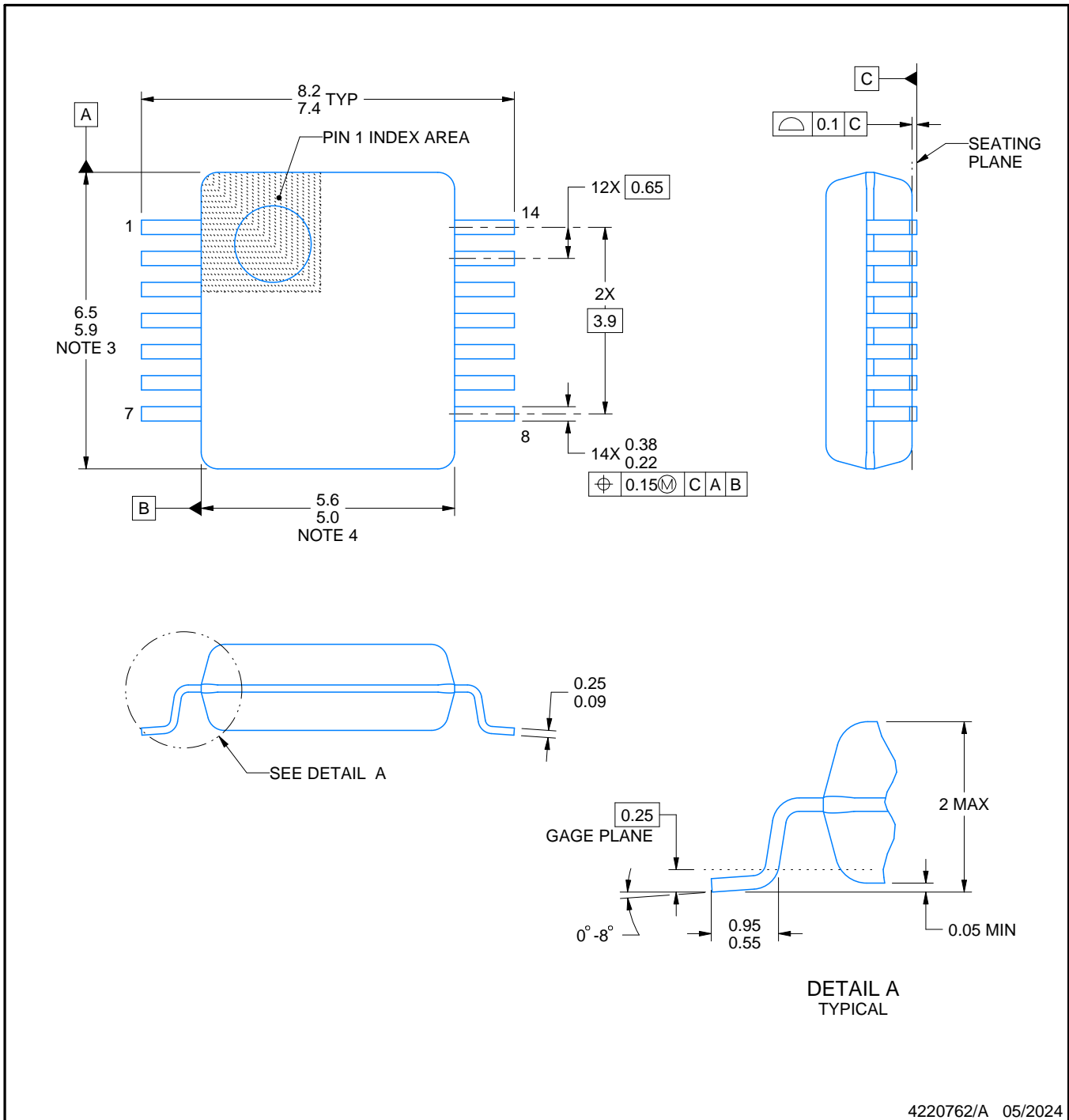
DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

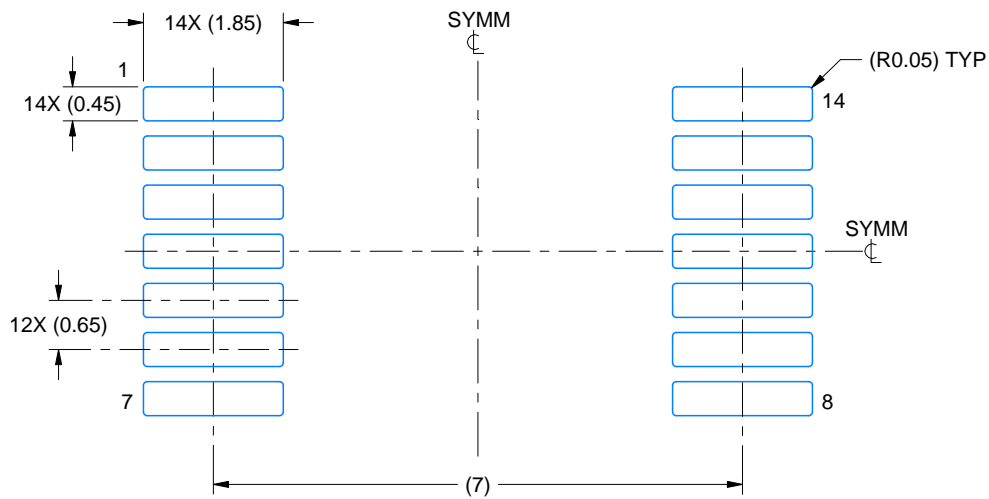
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

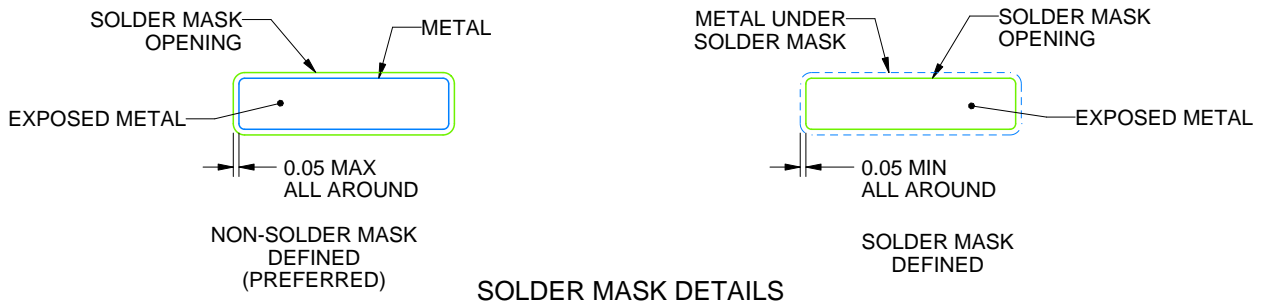
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

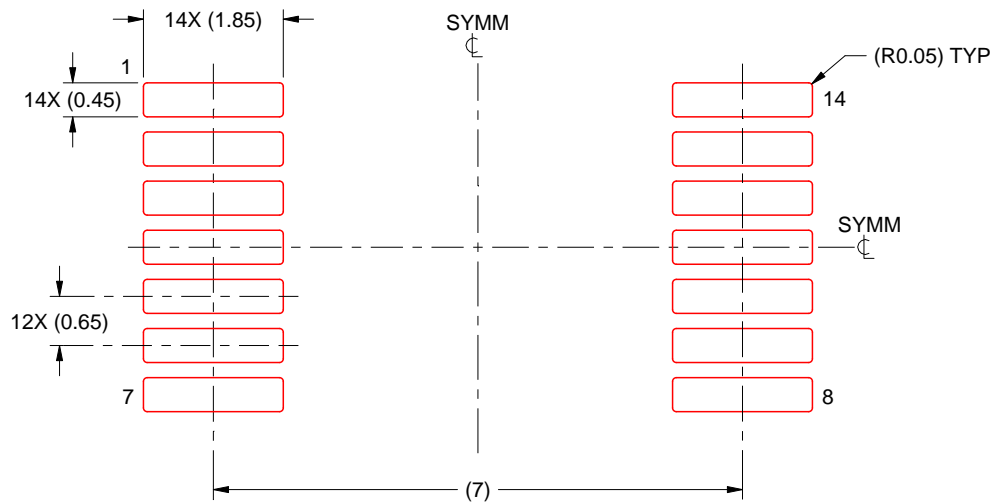
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

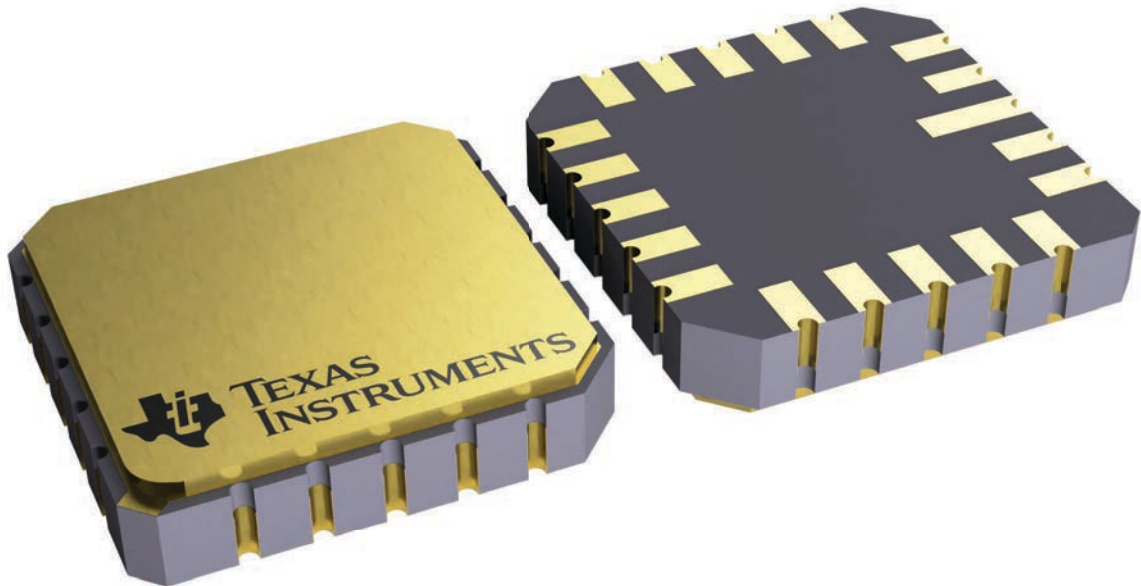
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

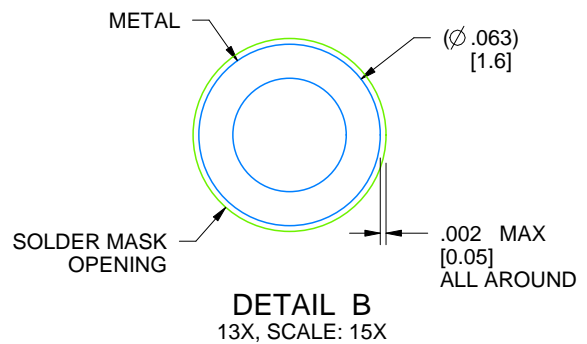
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



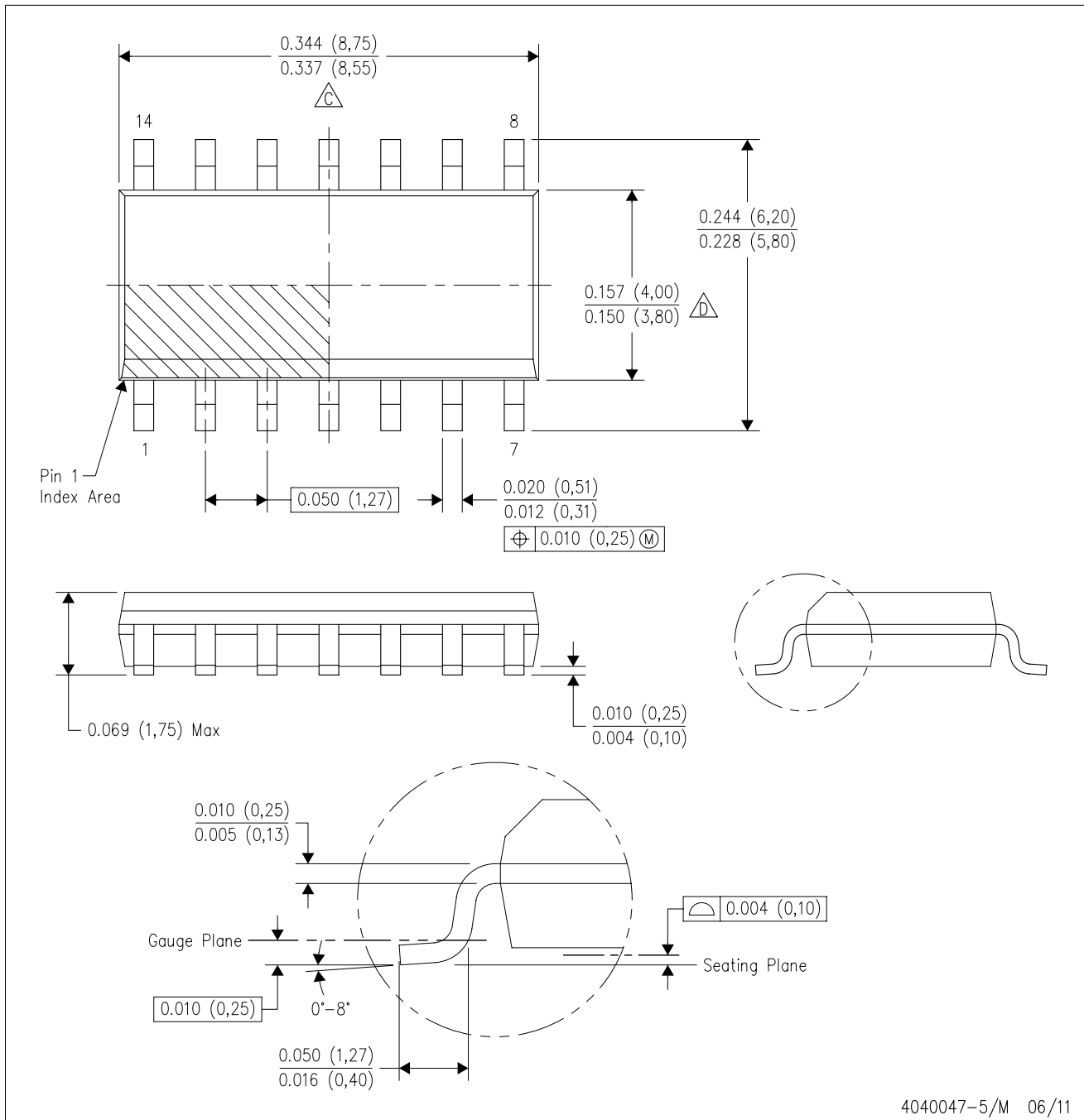
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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