

SNx4LVC74A デュアル ポジティブ エッジトリガ D タイプ フリップフロップ、クリア/プリセット搭載

1 特長

- 1.65V～3.6V で動作
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 5.2ns (3.3V 時)
- V_{OLP} 標準値 (出力グランド バウンス)
$0.8V (V_{CC} = 3.3V, T_A = 25^\circ C)$
- V_{OHV} 標準値 (出力 V_{OH} アンダーシュート)
>2V ($V_{CC} = 3.3V, T_A = 25^\circ C$)
- JESD 17 準拠で 250mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
 - 2000V、人体モデル (A114-A)
 - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- サーバー
- 医療、ヘルスケア、フィットネス
- テレコム インフラストラクチャ
- テレビ、セットトップ ボックス、オーディオ
- 試験 / 測定機器
- 産業用輸送
- ワイヤレス インフラ
- エンタープライズ スイッチング
- モータードライブ
- ファクトリ オートメーション / 制御

3 概要

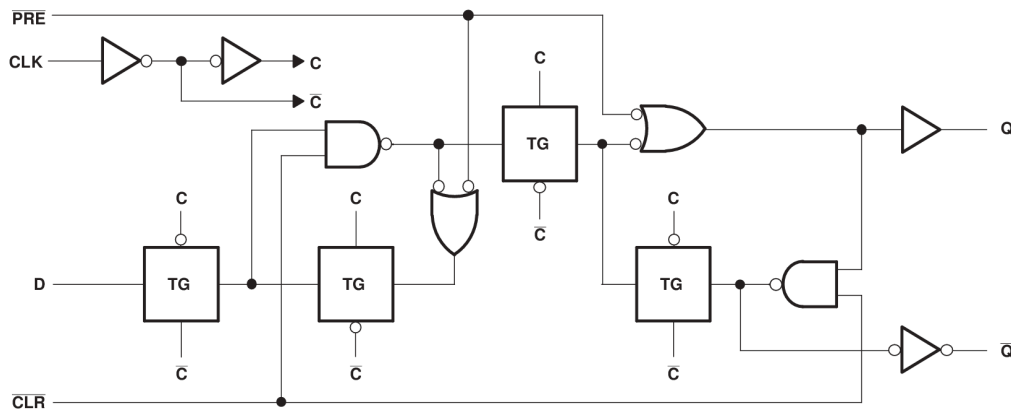
SNx4LVC74A デバイスは、2 つのポジティブ エッジトリガ D タイプ フリップ フロップを 1 つに統合した便利なデバイスです。

SN54LVC74A は 2.7V～3.6V の V_{CC} で動作するように設計されており、SN74LVC74A は 1.65V～3.6V の V_{CC} で動作するように設計されています。

製品情報

| 部品番号 | パッケージ ⁽¹⁾ | パッケージサイズ ⁽²⁾ | 本体サイズ ⁽³⁾ |
|---------------|----------------------|-------------------------|----------------------|
| SNx4LVC74A | BQA (WQFN, 14) | 3mm × 2.5mm | 3mm × 2.5mm |
| | D (SOIC, 14) | 8.65mm × 6mm | 8.65mm × 3.91mm |
| | DB (SSOP, 14) | 6.2mm × 7.8mm | 6.20mm × 5.30mm |
| | NS (SOP, 14) | 10.2mm × 7.8mm | 10.20mm × 5.30mm |
| | PW (TSSOP, 14) | 5mm × 6.4mm | 5.00mm × 4.40mm |
| | RGY (VQFN, 14) | 3.50mm × 3.50mm | 3.50mm × 3.50mm |
| | J (CDIP, 14) | 19.55mm × 7.9mm | 19.56 mm × 6.67 mm |
| | W (CFP, 14) | 9.21mm × 9 mm | 9.21 mm × 5.97 mm |
| FK (LCCC, 20) | 8.9mm × 8.9mm | 8.89 mm × 8.89 mm | |

- (1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



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論理図、各フリップフロップ (正論理)



Table of Contents

| | | | |
|---|----------|--|-----------|
| 1 特長 | 1 | 7 Detailed Description | 10 |
| 2 アプリケーション | 1 | 7.1 Overview..... | 10 |
| 3 概要 | 1 | 7.2 Functional Block Diagram..... | 10 |
| 4 Pin Configuration and Functions | 3 | 7.3 Feature Description..... | 10 |
| 5 Specifications | 4 | 7.4 Device Functional Modes..... | 10 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8 Application and Implementation | 11 |
| 5.2 ESD Ratings..... | 4 | 8.1 Application Information..... | 11 |
| 5.3 Recommended Operating Conditions..... | 4 | 8.2 Typical Application..... | 11 |
| 5.4 Thermal Information: SN74LVC74A..... | 5 | 8.3 Power Supply Recommendations..... | 12 |
| 5.5 Electrical Characteristics..... | 5 | 8.4 Layout..... | 12 |
| 5.6 Timing Requirements: SN54LVC74A..... | 6 | 9 Device and Documentation Support | 14 |
| 5.7 Timing Requirements: SN74LVC74A..... | 6 | 9.1 Documentation Support..... | 14 |
| 5.8 Timing Requirements: SN74LVC74A, –40°C to 125°C and –40°C to 85°C..... | 7 | 9.2 ドキュメントの更新通知を受け取る方法..... | 14 |
| 5.9 Switching Characteristics: SN54LVC74A..... | 7 | 9.3 サポート・リソース..... | 14 |
| 5.10 Switching Characteristics: SN74LVC74A..... | 7 | 9.4 Trademarks..... | 14 |
| 5.11 Switching Characteristics: SN74LVC74A, – 40°C to 125°C and –40°C to 85°C..... | 8 | 9.5 静電気放電に関する注意事項..... | 14 |
| 5.12 Operating Characteristics..... | 8 | 9.6 用語集..... | 14 |
| 5.13 Typical Characteristics..... | 8 | 10 Revision History | 14 |
| 6 Parameter Measurement Information | 9 | 11 Mechanical, Packaging, and Orderable Information | 15 |

4 Pin Configuration and Functions

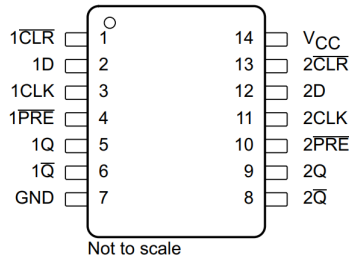


図 4-1. D, DB, J, PW, NS, or W Package 14-Pin SOIC, SSOP, CDIP, TSSOP, SO, or CFP (Top View)

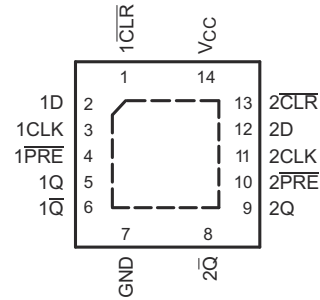


図 4-2. BQA or RGY Package 14-Pin WQFN or VQFN With Exposed Thermal Pad (Top View)

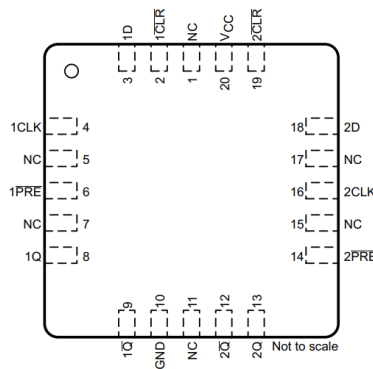


図 4-3. FK Package 20-Pin LCCC (Top View)

表 4-1. Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|-----------------|--|---------------------|-----|--|
| | CDIP, CFP, PDIP, SO, SOIC, SSOP, TSSOP, VQFN | LCCC | | |
| 1CLK | 3 | 4 | I | Channel 1 clock input |
| 1 CLR | 1 | 2 | I | Channel 1 clear input. Pull low to set Q output low. |
| 1D | 2 | 3 | I | Channel 1 data input |
| 1 PRE | 4 | 6 | I | Channel 1 preset input. Pull low to set Q output high. |
| 1Q | 5 | 8 | O | Channel 1 output |
| 1 Q̄ | 6 | 9 | O | Channel 1 inverted output |
| 2CLK | 11 | 16 | I | Channel 2 clock input |
| 2 CLR | 13 | 19 | I | Channel 2 clear input. Pull low to set Q output low. |
| 2D | 12 | 18 | I | Channel 2 data input |
| 2 PRE | 10 | 14 | I | Channel 2 preset input. Pull low to set Q output high. |
| 2Q | 9 | 13 | O | Channel 2 output |
| 2 Q̄ | 8 | 12 | O | Channel 2 Inverted output |
| GND | 7 | 10 | — | Ground |
| NC | — | 1, 5, 7, 11, 15, 17 | — | No connect |
| V _{CC} | 14 | 20 | — | Supply |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|--|-----------|----------------|------|
| Supply voltage, V_{CC} | -0.5 | 6.5 | V |
| Input voltage, V_I ⁽²⁾ | -0.5 | 6.5 | V |
| Output voltage, V_O ^{(2) (3)} | -0.5 | $V_{CC} + 0.5$ | V |
| Input clamp current, I_{IK} | $V_I < 0$ | -50 | mA |
| Output clamp current, I_{OK} | $V_O < 0$ | -50 | mA |
| Continuous output current, I_O | | ±50 | mA |
| Continuous current through V_{CC} or GND | | ±100 | mA |
| Storage temperature, T_{stg} | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

5.2 ESD Ratings

| | VALUE | UNIT |
|-------------------------------------|--|-------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

see⁽¹⁾

| | | | MIN | MAX | UNIT |
|--|---|------------|----------------------|----------|------|
| V_{CC} Supply voltage | Operating | SN54LVC74A | 2 | 3.6 | V |
| | | SN74LVC74A | 1.65 | 3.6 | |
| | Data retention only | | 1.5 | | |
| V_{IH} High-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | SN74LVC74A | $0.65 \times V_{CC}$ | | V |
| | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | SN74LVC74A | 1.7 | | |
| | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 2 | | |
| V_{IL} Low-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | SN74LVC74A | $0.35 \times V_{CC}$ | | V |
| | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | SN74LVC74A | 0.7 | | |
| | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 0.8 | | |
| V_I Input voltage | | | 0 | 5.5 | V |
| V_O Output voltage | | | 0 | V_{CC} | V |
| I_{OH} High-level output current | $V_{CC} = 1.65\text{ V}$ | SN74LVC74A | -4 | | mA |
| | $V_{CC} = 2.3\text{ V}$ | SN74LVC74A | -8 | | |
| | $V_{CC} = 2.7\text{ V}$ | | -12 | | |
| | $V_{CC} = 3\text{ V}$ | | -24 | | |
| I_{OL} Low-level output current | $V_{CC} = 1.65\text{ V}$ | SN74LVC74A | 4 | | mA |
| | $V_{CC} = 2.3\text{ V}$ | SN74LVC74A | 8 | | |
| | $V_{CC} = 2.7\text{ V}$ | | 12 | | |
| | $V_{CC} = 3\text{ V}$ | | 24 | | |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | | | 10 | ns/V |

5.3 Recommended Operating Conditions (続き)

see⁽¹⁾

| | | | MIN | MAX | UNIT |
|----------------|--------------------------------|------------|-----|-----|------|
| T _A | Operating free-air temperature | SN54LVC74A | -55 | 125 | °C |
| | | SN74LVC74A | -40 | 125 | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

5.4 Thermal Information: SN74LVC74A

| THERMAL METRIC ⁽¹⁾ | | SN74LVC74A | | | | | | UNIT |
|-------------------------------|--|------------|----------|-----------|---------|------------|------------|------|
| | | BQA (WQFN) | D (SOIC) | DB (SSOP) | NS (SO) | PW (TSSOP) | RGY (VQFN) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 102.3 | 93.7 | 107.3 | 90.3 | 121.7 | 54.9 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 96.8 | 54.8 | 59.2 | 48.1 | 50.3 | 52.2 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 70.9 | 48 | 54.6 | 49.1 | 63.4 | 30.8 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 16.6 | 20.3 | 24.1 | 17.9 | 6.2 | 2.4 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 70.9 | 47.7 | 54.1 | 48.8 | 62.8 | 30.9 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 50.1 | — | — | — | — | 12.5 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|--|--|-----------------------|-----|------|------|
| V _{OH} High-level output voltage | I _{OH} = -100 μA | V _{CC} = 1.65 V to 3.6 V and T _A = -55°C to 125°C (SN54LVC74A only) | V _{CC} - 0.2 | | | V |
| | | V _{CC} = 2.7 V to 3.6 V and T _A = -40°C to 125°C (SN74LVC74A only) | V _{CC} - 0.2 | | | |
| | I _{OH} = -4 mA, V _{CC} = 1.65 V, and T _A = -40°C to 125°C (SN74LVC74A only) | | 1.2 | | | |
| | I _{OH} = -8 mA, V _{CC} = 2.3 V, and T _A = -40°C to 125°C (SN74LVC74A only) | | 1.7 | | | |
| | I _{OH} = -12 mA | V _{CC} = 2.7 V | 2.2 | | | |
| | | V _{CC} = 3 V | 2.4 | | | |
| I _{OH} = -24 mA, V _{CC} = 3 V | | 2.2 | | | | |
| V _{OL} Low-level output voltage | I _{OL} = 100 μA | V _{CC} = 1.65 V to 3.6 V, and T _A = -40°C to 125°C (SN74LVC74A only) | | | 0.2 | V |
| | | V _{CC} = 2.7 V to 3.6 V and T _A = -55°C to 125°C (SN54LVC74A only) | | | 0.2 | |
| | I _{OL} = 4 mA, V _{CC} = 1.65 V, and T _A = -40°C to 125°C (SN74LVC74A only) | | | | 0.45 | |
| | I _{OL} = 8 mA, V _{CC} = 2.3 V, and T _A = -40°C to 125°C (SN74LVC74A only) | | | | 0.7 | |
| | I _{OL} = 12 mA, V _{CC} = 2.7 V | | | | 0.4 | |
| | I _{OL} = 24 mA, V _{CC} = 3 V | | | | 0.55 | |
| I _I Input current | V _I = 5.5 V or GND, V _{CC} = 3.6 V | | | | ±5 | μA |
| I _{CC} Supply current | V _I = V _{CC} or GND, I _O = 0, V _{CC} = 3.6 V | | | | 10 | μA |

5.5 Electrical Characteristics (続き)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|---|-----|-----|-----|---------|
| ΔI_{CC} | Change in supply current | One input at $V_{CC} - 0.6$ V, other inputs at V_{CC} or GND, and $V_{CC} = 2.7$ V to 3.6 V | | | 500 | μ A |
| C_i | Input capacitance | $V_i = V_{CC}$ or GND, $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C | | 5 | | pF |

5.6 Timing Requirements: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

| | | | MIN | MAX | UNIT |
|-------------|--------------------------------------|------------------------------|------------------------------|-----|------|
| f_{clock} | Clock frequency | $V_{CC} = 2.7$ V | | 83 | MHz |
| | | $V_{CC} = 3.3$ V \pm 0.3 V | | 100 | |
| t_w | Pulse duration | PRE or CLR low | 3.3 | | ns |
| | | CLK high or low | 3.3 | | |
| t_{su} | Setup time before CLK \uparrow | Data | $V_{CC} = 2.7$ V | 3.4 | ns |
| | | | $V_{CC} = 3.3$ V \pm 0.3 V | 3 | |
| | | PRE or CLR inactive | $V_{CC} = 2.7$ V | 2.2 | |
| | | | $V_{CC} = 3.3$ V \pm 0.3 V | 2 | |
| t_h | Hold time, data after CLK \uparrow | | 1 | | ns |

5.7 Timing Requirements: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

| | | | MIN | MAX | UNIT |
|-------------|--------------------------------------|---------------------------|-------------------------------|-----|------|
| f_{clock} | Clock frequency | $V_{CC} = 1.8$ V or 2.5 V | | 83 | MHz |
| t_w | Pulse duration | PRE or CLR low | $V_{CC} = 1.8$ V \pm 0.15 V | 4.1 | ns |
| | | | $V_{CC} = 2.5$ V \pm 0.2 V | 3.3 | |
| | | CLK high or low | $V_{CC} = 1.8$ V \pm 0.15 V | 4.1 | |
| | | | $V_{CC} = 2.5$ V \pm 0.2 V | 3.3 | |
| t_{su} | Setup time before CLK \uparrow | Data | $V_{CC} = 1.8$ V \pm 0.15 V | 3.6 | ns |
| | | | $V_{CC} = 2.5$ V \pm 0.2 V | 2.3 | |
| | | PRE or CLR inactive | $V_{CC} = 1.8$ V \pm 0.15 V | 2.7 | |
| | | | $V_{CC} = 2.5$ V \pm 0.2 V | 1.9 | |
| t_h | Hold time, data after CLK \uparrow | $V_{CC} = 1.8$ V or 2.5 V | 1 | | ns |

5.8 Timing Requirements: SN74LVC74A, –40°C to 125°C and –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

| | | | | MIN | MAX | UNIT |
|--|-----------------------------|--|--|---------------------------------|-----|------|
| f _{clock} | Clock frequency | T _A = –40°C to 125°C | V _{CC} = 2.7 V | | 83 | MHz |
| | | | V _{CC} = 3.3 V ± 0.3 V | | 100 | |
| | | T _A = –40°C to 85°C and V _{CC} = 3.3 V ± 0.3 V | | | | |
| t _w | Pulse duration | PRE or CLR low | V _{CC} = 2.7 V or 3.3 V | | 3.3 | ns |
| | | CLK high or low | V _{CC} = 2.7 V or 3.3 V | | 3.3 | |
| t _{su} | Setup time before CLK ↑ | Data | T _A = –40°C to 125°C | V _{CC} = 2.7 V | 3.4 | ns |
| | | | | V _{CC} = 3.3 V ± 0.3 V | 3 | |
| | | | T _A = –40°C to 85°C and V _{CC} = 3.3 V ± 0.3 V | | 3 | |
| | | PRE or CLR inactive | T _A = –40°C to 125°C | V _{CC} = 2.7 V | 2.2 | |
| | | | | V _{CC} = 3.3 V ± 0.3 V | 2 | |
| T _A = –40°C to 85°C and V _{CC} = 3.3 V ± 0.3 V | | 2 | | | | |
| t _h | Hold time, data after CLK ↑ | V _{CC} = 2.7 V or 3.3 V | | 1 | ns | |

5.9 Switching Characteristics: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--------------------|----------------|---------------------------------|-----|-----|------|
| f _{max} | — | — | V _{CC} = 2.7 V | 83 | | MHz |
| | | | V _{CC} = 3.3 V ± 0.3 V | 100 | | |
| t _{pd} | CLK | Q or \bar{Q} | V _{CC} = 2.7 V | | 6 | ns |
| | | | V _{CC} = 2.7 V | 1 | 5.2 | |
| | PRE or \bar{CLR} | | V _{CC} = 3.3 V ± 0.3 V | | 6.4 | |
| | | | V _{CC} = 3.3 V ± 0.3 V | 1 | 5.4 | |

5.10 Switching Characteristics: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|----------------|----------------|----------------------------------|-----|-----|------|
| f _{max} | — | — | | 83 | | MHz |
| t _{pd} | CLK PRE | Q or \bar{Q} | V _{CC} = 1.8 V ± 0.15 V | 1 | 7.1 | ns |
| | | | V _{CC} = 2.5 V ± 0.2 V | 1 | 4.4 | |
| | or \bar{CLR} | | V _{CC} = 1.8 V ± 0.15 V | 1 | 6.9 | |
| | | | V _{CC} = 2.5 V ± 0.2 V | 1 | 4.6 | |

5.11 Switching Characteristics: SN74LVC74A, –40°C to 125°C and –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

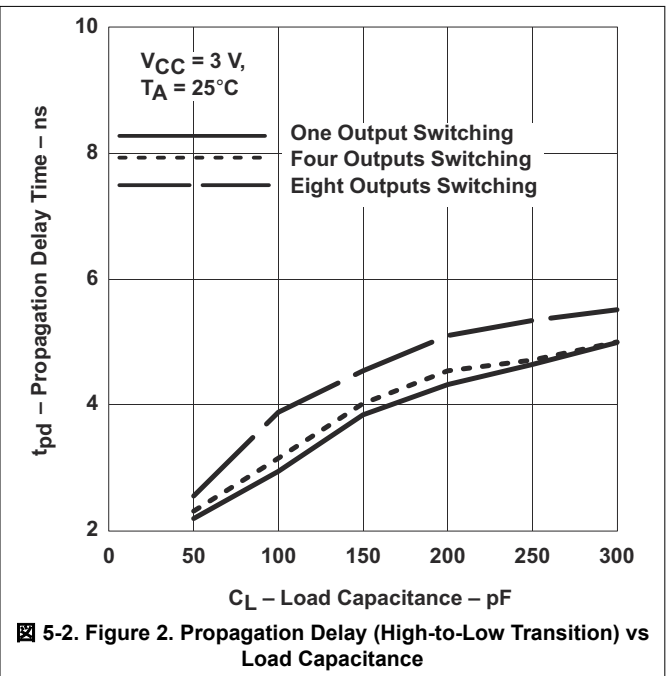
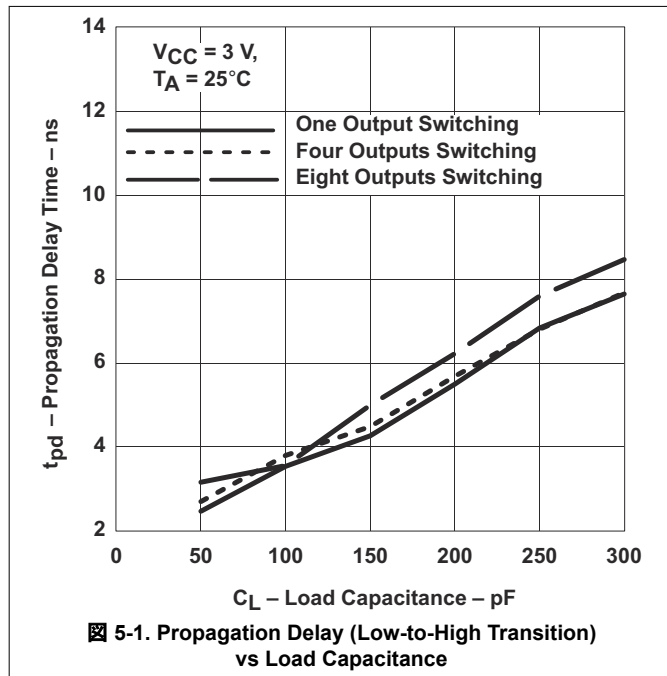
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | MAX | UNIT |
|-----------------------------------|--------------|----------------|--|--|-----|-----|------|
| | | | T_A | V_{CC} | | | |
| f_{max} Maximum clock frequency | — | — | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ | $V_{CC} = 2.7\text{ V}$ | 83 | MHz | |
| | | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | |
| | | | $T_A = -40^\circ\text{C to } 85^\circ\text{C and } V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 150 | | | |
| t_{pd} Propagation (delay) time | CLK | Q or \bar{Q} | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ | $V_{CC} = 2.7\text{ V}$ | 1 | 6 | ns |
| | | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1 | 5.2 | |
| | | | $T_A = -40^\circ\text{C to } 85^\circ\text{C and } V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1 | 5.2 | | |
| | PRE or CLR | | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ | $V_{CC} = 2.7\text{ V}$ | 1 | 6.4 | |
| | | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1 | 5.4 | |
| | | | $T_A = -40^\circ\text{C to } 85^\circ\text{C and } V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1 | 5.4 | | |
| $t_{sk(o)}$ Skew (time), output | — | — | $T_A = -40^\circ\text{C to } 85^\circ\text{C and } V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 1 | ns | |

5.12 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT | |
|--|---------------------|-------------------------|------|----|
| C_{pd} Power dissipation capacitance per flip-flop | $f = 10\text{ MHz}$ | $V_{CC} = 1.8\text{ V}$ | 24 | pF |
| | | $V_{CC} = 2.5\text{ V}$ | 24 | |
| | | $V_{CC} = 3.3\text{ V}$ | 26 | |

5.13 Typical Characteristics

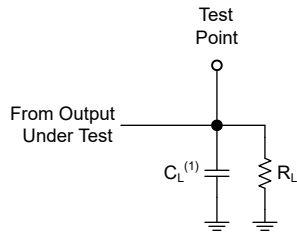


6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_f ≤ 2.5ns.

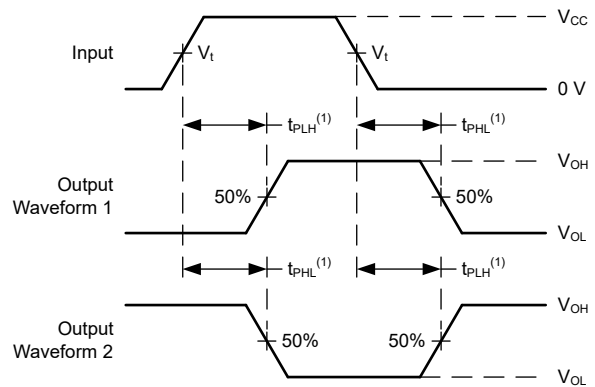
The outputs are measured individually with one input transition per measurement.

| V _{CC} | V _t | R _L | C _L | ΔV |
|-----------------|--------------------|----------------|----------------|-------|
| 1.8V ± 0.15V | V _{CC} /2 | 1kΩ | 30pF | 0.15V |
| 2.5V ± 0.2V | V _{CC} /2 | 500Ω | 30pF | 0.15V |
| 2.7V | 1.5V | 500Ω | 50pF | 0.3V |
| 3.3V ± 0.3V | 1.5V | 500Ω | 50pF | 0.3V |



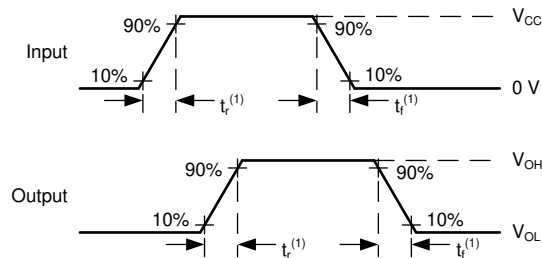
(1) C_L includes probe and test-fixture capacitance.

6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

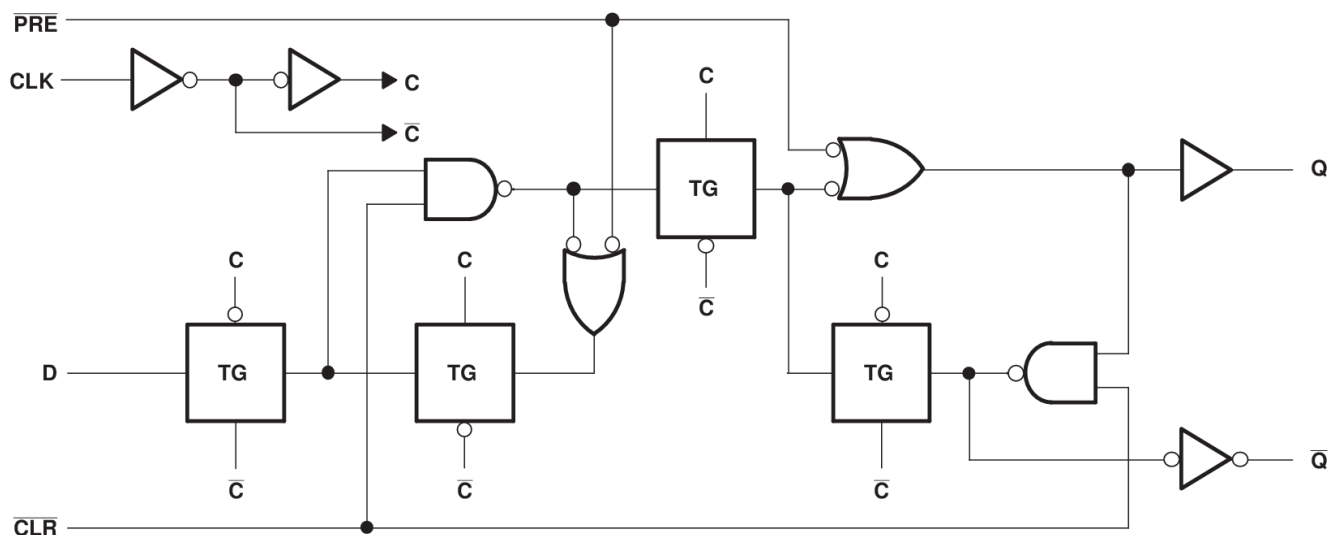
The SNx4LVC74A devices feature two independent positive-edge triggered D flip-flops. Integrated preset ($\overline{\text{PRE}}$) and clear ($\overline{\text{CLR}}$) functions allow for easy setup and control during operation.

The SN54LVC74A device is specified from -55°C to 125°C , and the SN74LVC74A device is specified from -40°C to 125°C .

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of these devices for down-translation in a mixed-voltage environment.

7.2 Functional Block Diagram



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7.3 Feature Description

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

7.4 Device Functional Modes

表 7-1 describes the SNx4LVC74A functionality and interactions between the $\overline{\text{PRE}}$, $\overline{\text{CLR}}$, CLK, and D inputs.

表 7-1. Function Table

| INPUTS | | | | OUTPUTS | |
|--------|-----|-----|---|------------------|-----------------------|
| PRE | CLR | CLK | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H ⁽¹⁾ | H ⁽¹⁾ |
| H | H | ↑ | H | H | L |

表 7-1. Function Table (続き)

| INPUTS | | | | OUTPUTS | |
|--------|-----|------------|---|---------|-------------|
| PRE | CLR | CLK | D | Q | \bar{Q} |
| H | H | \uparrow | L | L | H |
| H | H | L | X | Q_0 | \bar{Q}_0 |

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A common application for the SN74LVC74A is a frequency divider. By connecting the \bar{Q} output to the D input, the Q output toggles states on each positive edge of the incoming clock signal. Because it takes two positive edges, or two clock pulses, to complete one complete pulse on the output (one pulse to toggle from low to high, another to toggle from high to low), the incoming clock frequency is effectively divided by two.

8.2 Typical Application

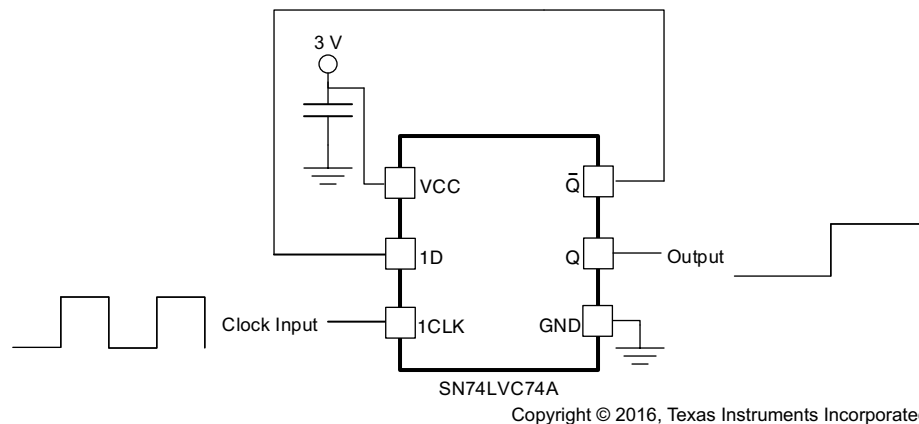


図 8-1. Frequency Divider

8.2.1 Design Requirements

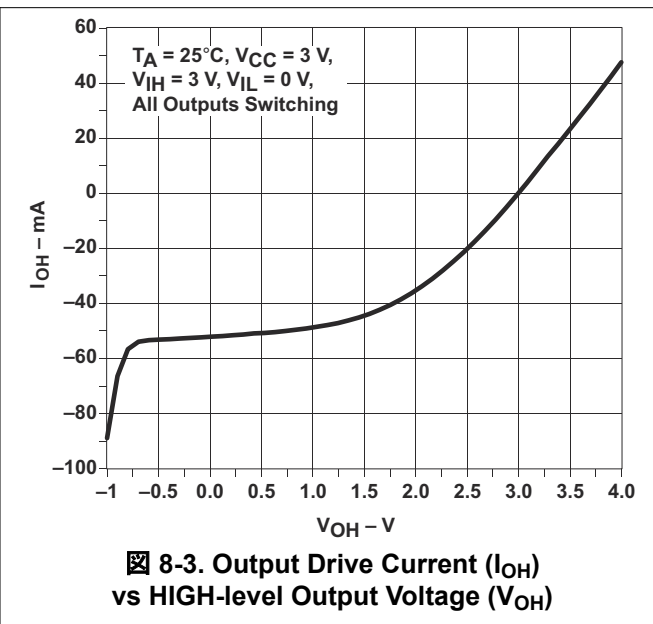
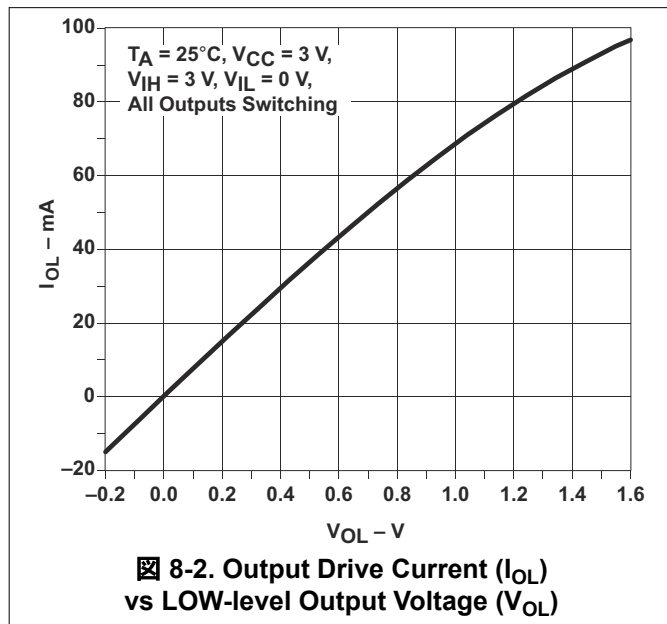
This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended input conditions:
 - For rise time and fall time specification, see $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#).
 - For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#).
 - Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in [Recommended Operating Conditions](#) at any valid V_{CC} .
- Recommended maximum output conditions:

- Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in [Absolute Maximum Ratings](#).
- Outputs must not be pulled above V_{CC} .

8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply may be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01- μF or 0.022- μF capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

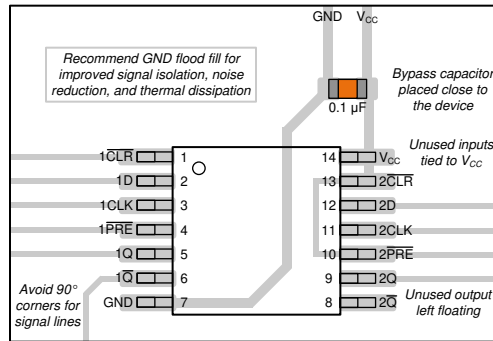
8.4 Layout

8.4.1 Layout Guidelines

Inputs must not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [图 8-4](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} , whichever makes more sense or is more convenient.

8.4.2 Layout Example



☒ 8-4. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision U (January 2017) to Revision V (May 2024) Page

| | |
|--|---|
| ドキュメント全体にわたって表、図、相互参照の採番方法を更新..... | 1 |
| 「製品情報」表、「ピン構成および機能」セクション、および「熱に関する情報」表に BQA パッケージを追加 | 1 |
| 「製品情報」表にパッケージ サイズを追加..... | 1 |

Changes from Revision T (July 2013) to Revision U (January 2017) Page

| | |
|--|---|
| 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加..... | 1 |
| Changed Package thermal impedance, $R_{\theta JA}$, values in <i>Thermal Information: SN74LVC74A</i> From: 86 To: 93.7 (D), From: 96 To: 107.3 (DB), From: 76 To: 90.3 (NS), From: 113 To: 121.7 (PW), and From: 47 To: 54.9 (RGY)..... | 5 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-9761601Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9761601Q2A SNJ54LVC74AFK | Samples |
| 5962-9761601QCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9761601QC A SNJ54LVC74AJ | Samples |
| 5962-9761601QDA | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9761601QD A SNJ54LVC74AW | Samples |
| 5962-9761601VDA | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9761601VD A SNV54LVC74AW | Samples |
| SN74LVC74ABQAR | ACTIVE | WQFN | BQA | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC74A | Samples |
| SN74LVC74AD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC74A | Samples |
| SN74LVC74ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74ADBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC74A | Samples |
| SN74LVC74ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC74A | Samples |
| SN74LVC74ADT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC74A | Samples |
| SN74LVC74ANSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC74A | Samples |
| SN74LVC74APW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| SN74LVC74APWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74APWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC74A | Samples |
| SN74LVC74ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC74A | Samples |
| SNJ54LVC74AFK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9761601Q2A SNJ54LVC74AFK | Samples |
| SNJ54LVC74AJ | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9761601QC A SNJ54LVC74AJ | Samples |
| SNJ54LVC74AW | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9761601QD A SNJ54LVC74AW | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LVC74A, SN54LVC74A-SP, SN74LVC74A :

- Catalog : [SN74LVC74A](#), [SN54LVC74A](#)

- Automotive : [SN74LVC74A-Q1](#), [SN74LVC74A-Q1](#)

- Enhanced Product : [SN74LVC74A-EP](#), [SN74LVC74A-EP](#)

- Military : [SN54LVC74A](#)

- Space : [SN54LVC74A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC74ABQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74LVC74ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LVC74ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC74ADT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC74ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC74APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC74APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC74APWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC74APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC74ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC74ABQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC74ADBR | SSOP | DB | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC74ADR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74LVC74ADT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC74ANSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC74APWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC74APWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC74APWRG4 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC74APWT | TSSOP | PW | 14 | 250 | 356.0 | 356.0 | 35.0 |
| SN74LVC74ARGYR | VQFN | RGY | 14 | 3000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9761601Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9761601VDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LVC74AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LVC74APW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC74APWG4 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54LVC74AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - △ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

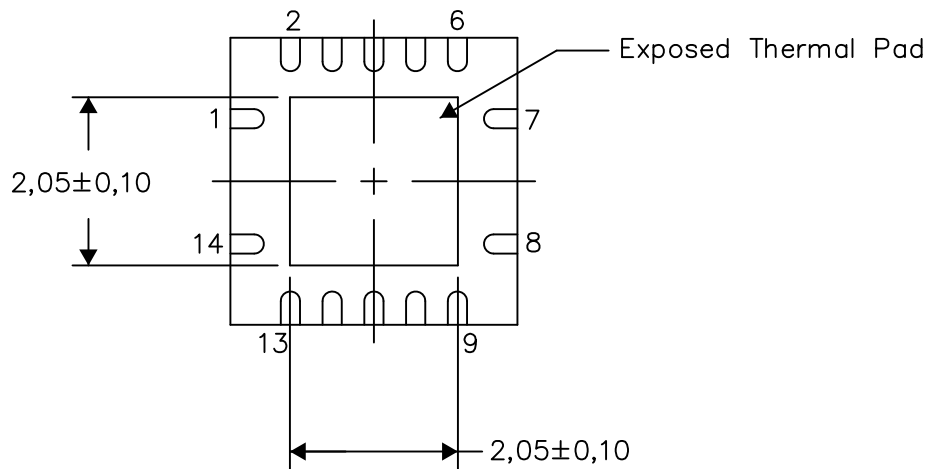
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

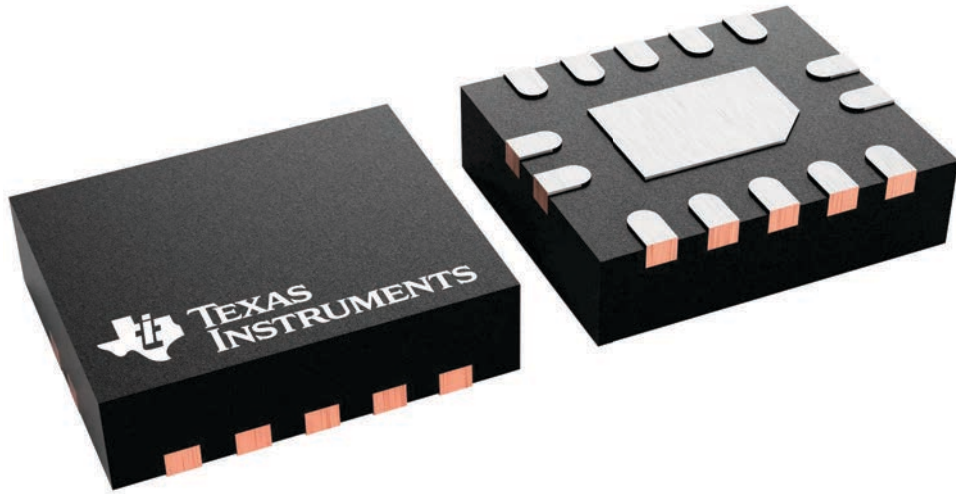
BQA 14

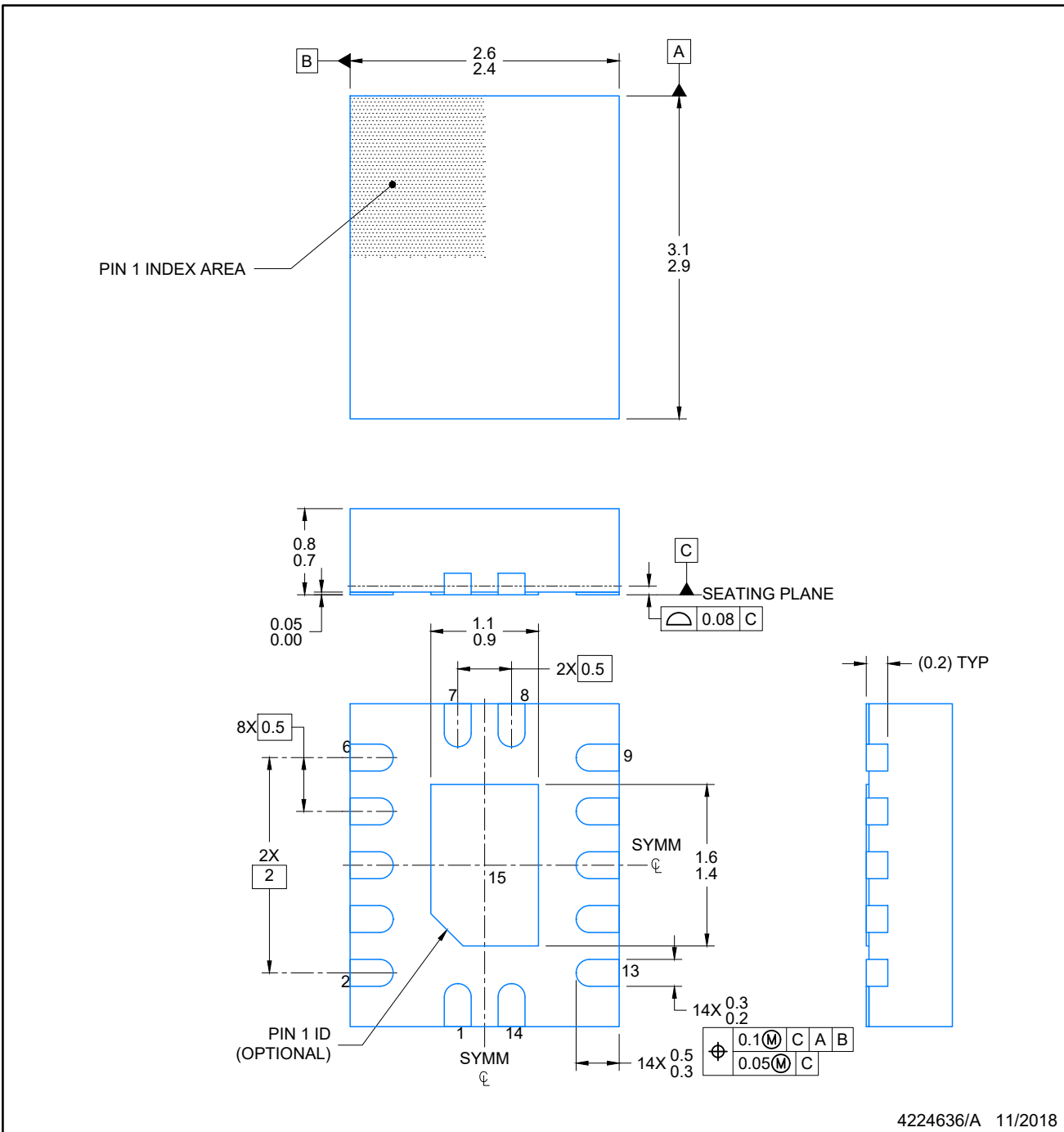
WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4224636/A 11/2018

NOTES:

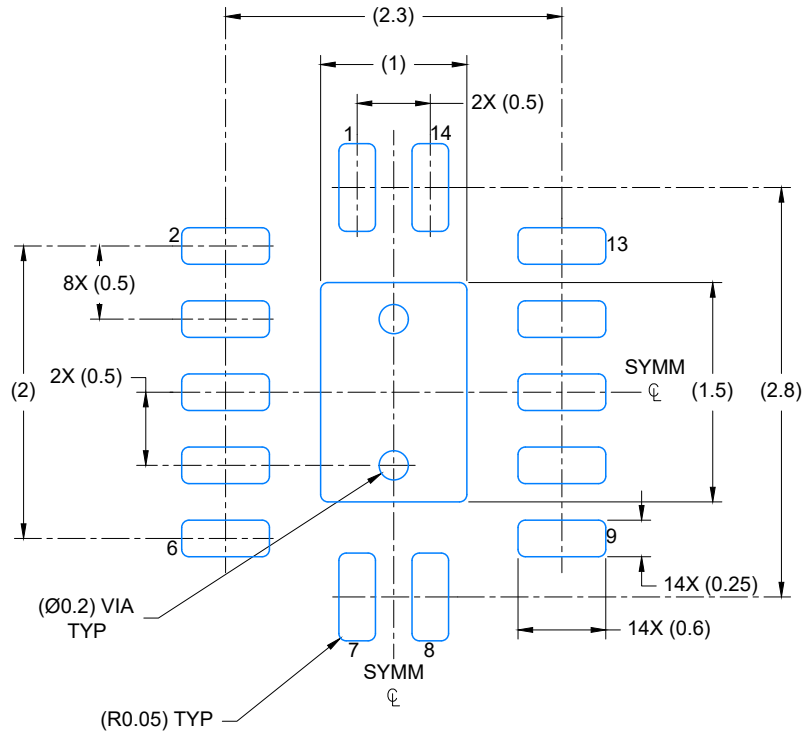
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

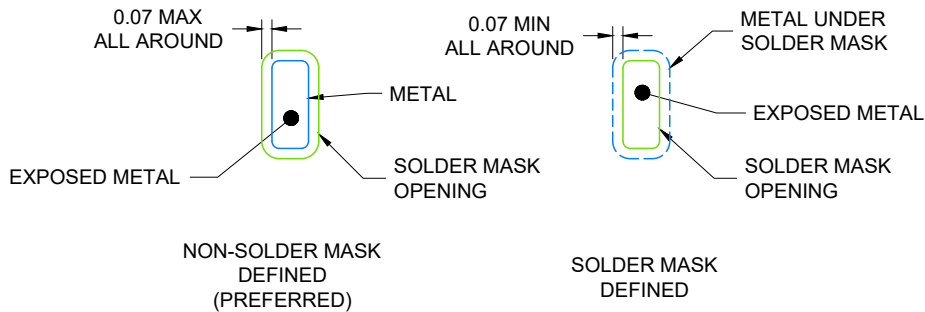
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

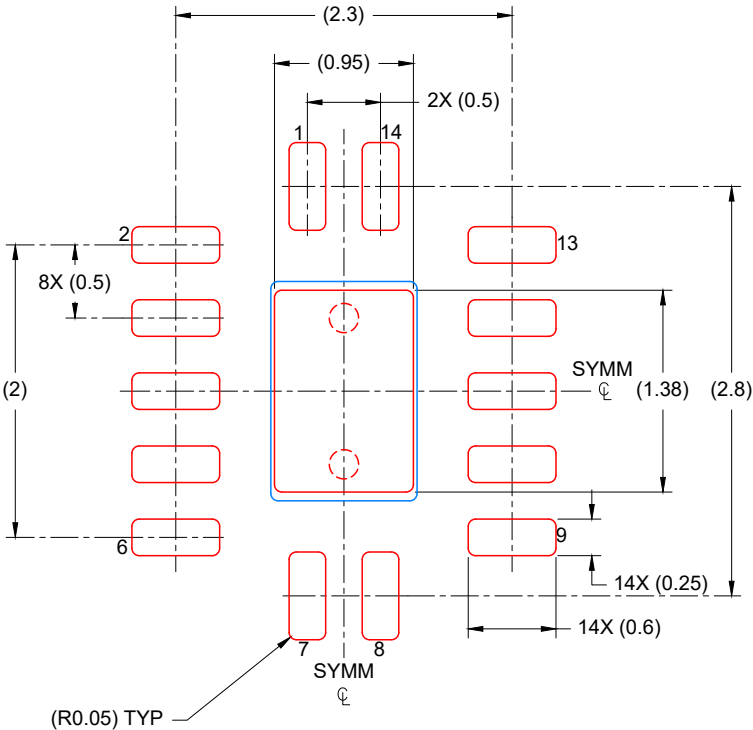
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

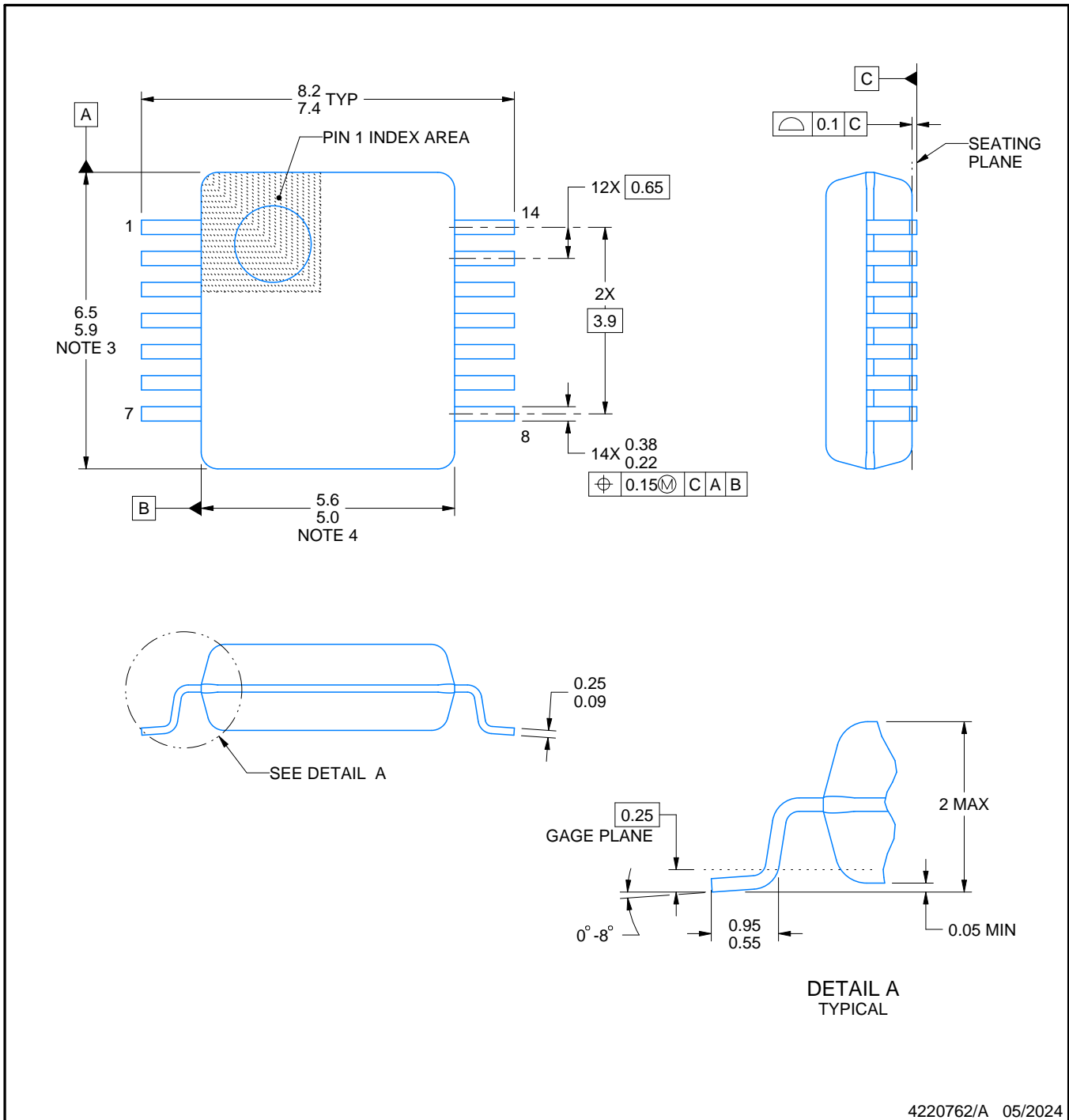
DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

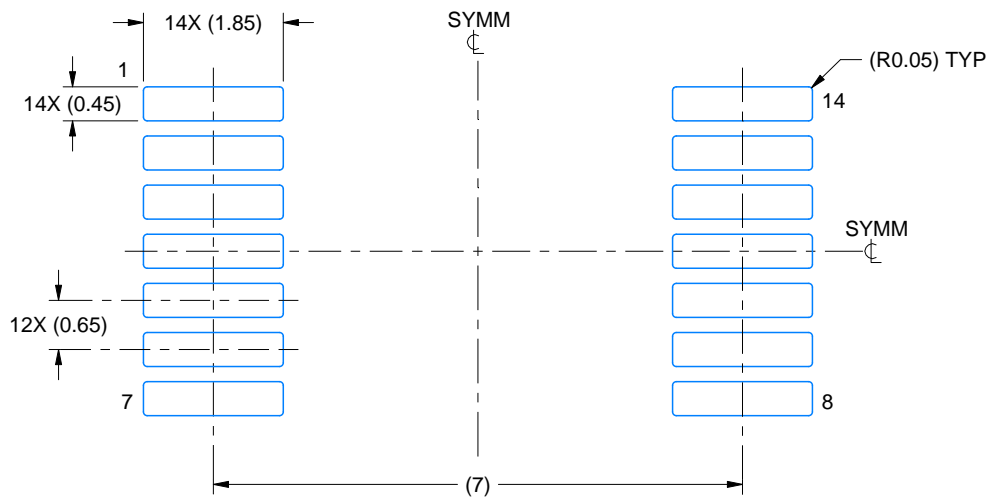
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

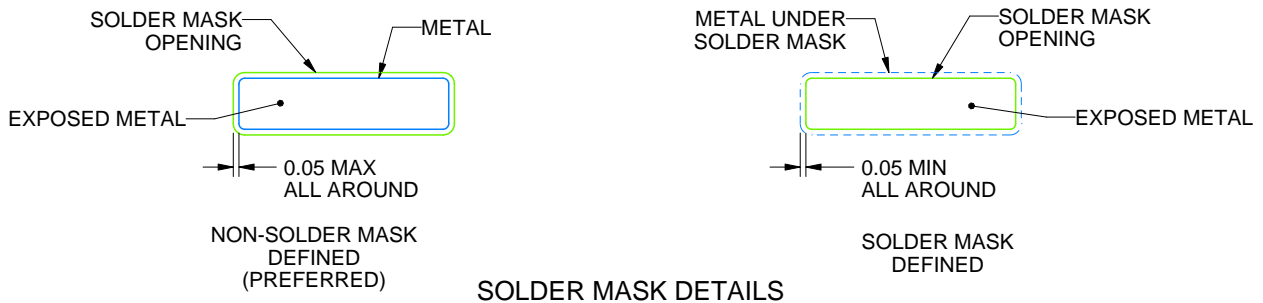
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

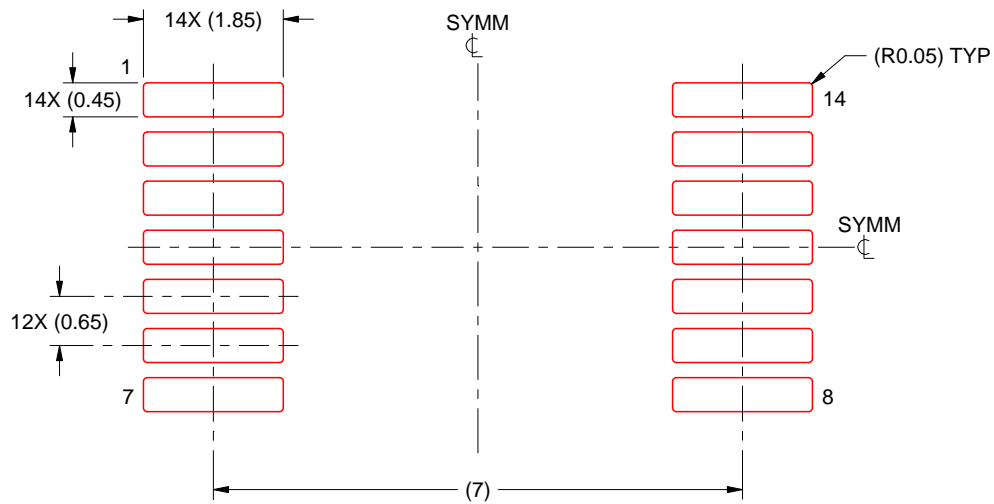
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

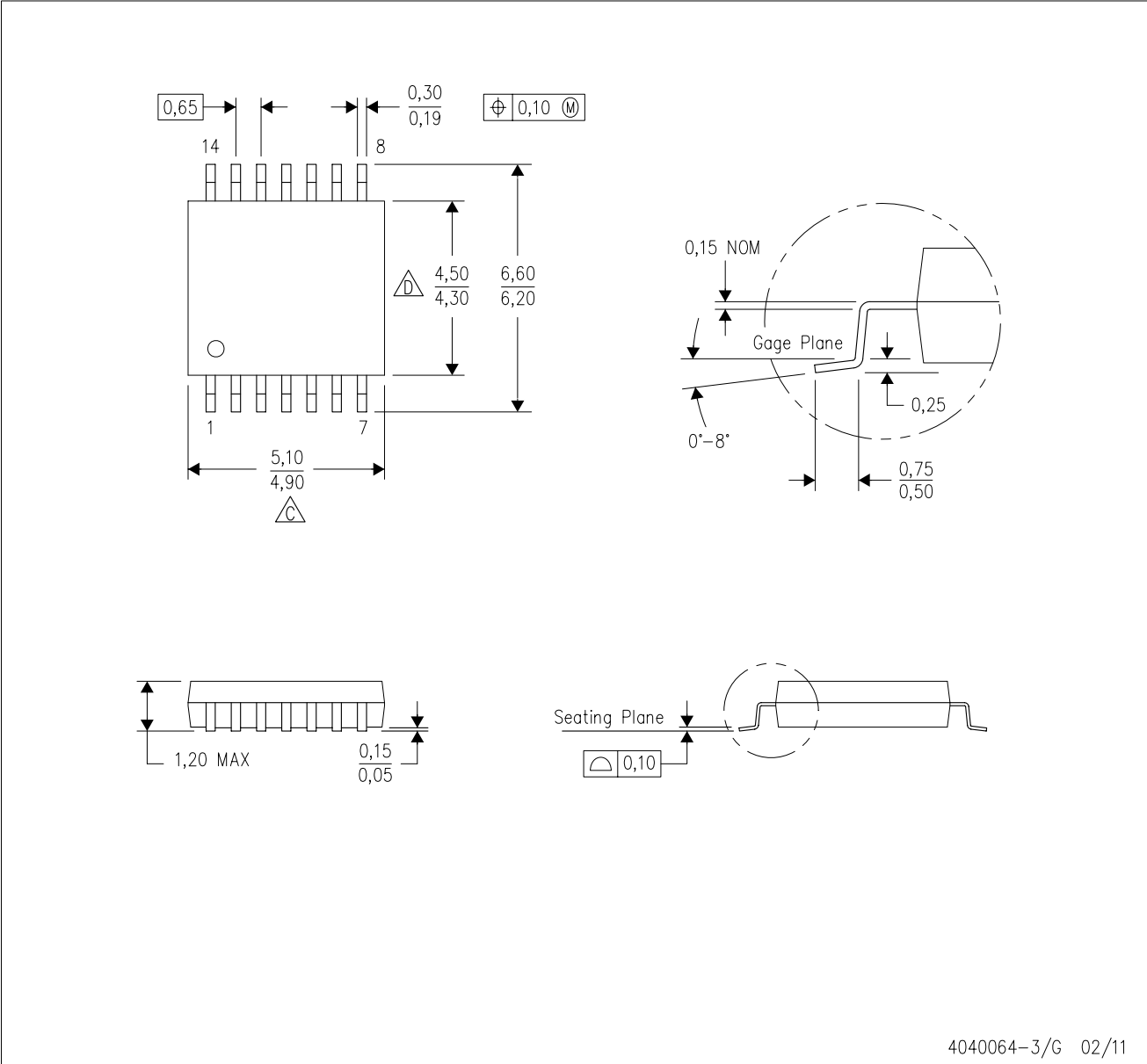


4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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