

3V~5.5V、1チャンネルRS-232 1Mbit/s ライン・ドライバ/レシーバ、 ±15kV IEC ESD 保護機能搭載

1 特長

- RS-232 ピンの ESD 保護
 - ±15kV 人体モデル (HBM)
 - ±8kV IEC 61000-4-2 接触放電
 - ±15kV IEC 61000-4-2 エアギャップ放電
- 3V~5.5V の V_{CC} 電源で動作
- 最大 1Mbit/s で動作
- 低スタンバイ電流 ...標準値 1μA
- 外付けコンデンサ ...4 × 0.1μF
- 3.3V 電源で 5V ロジック入力を受容
- ±15kV (人体モデル (HBM)) を超える RS-232 バス・ピン ESD 保護
- 自動パワー・ダウン機能により、ドライバを自動的にディスエーブルすることで電力を節約

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリー駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

3 概要

SN65C3221E と SN75C3221E は 1 つのライン・ドライバ、1 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、±15kV のピン間 (シリアル・ポート接続ピン、GND を含む) IEC ESD 保護機能を備えています。これらのデバイスは、非同期通信コントローラとシリアルポート・コネクタの間の電氣的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。

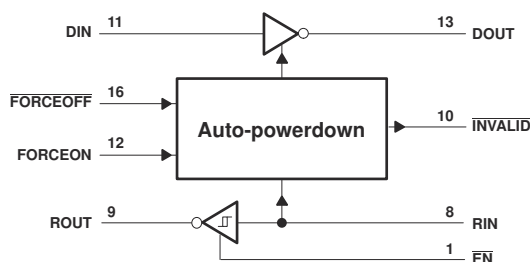
これらのデバイスは最大 1Mbit/s のデータ信号速度、24V/μs~150V/μs のドライバ出力スlewレートで動作します。

シリアル・ポートが使われていない際のパワー・マネージメントを柔軟に制御できます。FORCEON が LOW かつ FORCEOFF が HIGH の場合、自動パワー・ダウン機能が動作します。この動作モード中、デバイスがレシーバ入力で有効な RS-232 信号を検出しない場合、ドライバ出力はディスエーブルになります。FORCEOFF を LOW に設定しかつ EN を HIGH に設定すると、ドライバとレシーバはどちらもシャットダウンされ、消費電流は 1μA に減少します。シリアル・ポートを切り離れた場合、またはペリフェラル・ドライバをオフにした場合、自動パワー・ダウン状態になります。FORCEON と FORCEOFF を HIGH にすると、自動パワー・ダウンを無効にできます。自動パワー・ダウンが有効な場合、レシーバの入力に有効な信号が印加されると、デバイスは自動的にアクティブになります。INVALID 出力は、レシーバの入力に RS-232 信号が存在するかどうかをユーザーに通知します。INVALID は、レシーバの入力電圧が 2.7V を上回っている場合、-2.7V を下回っている場合、-0.3V と 0.3V の間にあった期間が 30μs 未満である場合のいずれかの場合、HIGH (有効データ) になります。INVALID は、レシーバの入力電圧が 30μs を超える期間 -0.3V と 0.3V の間にある場合、LOW (無効データ) になります。レシーバの入力レベルについては、図 8-5 を参照してください。

製品情報

| 部品番号 | パッケージ ⁽¹⁾ | 本体サイズ (公称) |
|------------|----------------------|-----------------|
| SNx5C3221E | SSOP (DB) 16 | 6.20mm × 5.30mm |
| | TSSOP (DW) 16 | 10.3mm × 7.50mm |

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision B (April 2009) to Revision C (July 2021) | Page |
|---|------|
| • 「アプリケーション」の一覧を変更..... | 1 |
| • 「注文情報」表を削除..... | 1 |
| • 製品情報の表を追加..... | 1 |
| • Added the <i>Pin Configuration and Functions</i> | 4 |
| • Removed the thermal information from <i>Absolute Maximum Rating</i> stable and moved the thermal information to its own table..... | 5 |
| • Added a table note for PW package of SN65C3221E regarding the minimum capacitance in <i>ESD Ratings - IEC Specifications</i> table..... | 5 |
| • Changed thermal information for PW package of SN65C3221E. Added additional thermal information for other packages..... | 6 |
| • Added the <i>Detailed Description</i> section..... | 13 |

5 Device Comparison Table

表 5-1. 1-Mbit/s RS-232 Parts

| PART NO. | TEMPERATURE RANGE | DRIVER NO. | RECEIVER NO. | ESD | SUPPLY V _{CC} (V) | FEATURE | PIN/PACKAGE |
|------------|-------------------|------------|--------------|---|----------------------------|--------------------------------------|-----------------------------|
| SN65C3221E | -40°C to 85°C | 1 | 1 | ±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM | 3.3 or 5 | Auto powerdown | 16-pin SOIC, SSOP, TSSOP |
| SN65C3232E | | 2 | 2 | ±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM | 3.3 or 5 | Low pin count | 16-pin SOIC, SSOP, TSSOP |
| MAX3227I | | 1 | 1 | ±8-kV Air-Gap, ±8-kV Contact, ±15-kV HBM | 3.3 or 5 | Auto powerdown plus, ready signal | 16-pin SSOP |
| SN65C3221 | | 1 | 1 | ±15-kV HBM | 3.3 or 5 | Auto powerdown | 16-pin SOIC, SSOP, TSSOP |
| SN65C3223 | | 2 | 2 | ±15-kV HBM | 3.3 or 5 | Auto powerdown, enable signal | 20-pin SOIC, SSOP, TSSOP |
| SN65C3222 | | 2 | 2 | ±15-kV HBM | 3.3 or 5 | Enable, powerdown signal | 20-pin SOIC, SSOP, TSSOP |
| SN65C3232 | | 2 | 2 | ±15-kV HBM | 3.3 or 5 | Low pin count | 16-pin SOIC, SSOP, TSSOP |
| SN65C3238 | | 5 | 3 | ±15-kV HBM | 3.3 or 5 | Auto powerdown plus | 28-pin SOIC, SSOP, TSSOP |
| SN65C3243 | | 3 | 5 | ±15-kV HBM | 3.3 or 5 | Auto powerdown | 28-pin SOIC, SSOP, TSSOP |
| SN75C3221E | 0°C to 70°C | 1 | 1 | ±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM | 3.3 or 5 | Auto powerdown | 16-pin SOIC, SSOP, TSSOP |
| SN75C3232E | | 2 | 2 | ±15-kV Air-Gap, ±8-kV Contact, ±15-kV HBM | 3.3 or 5 | Low pin count | 16-pin SOIC, SSOP, TSSOP |
| MAX3227C | | 1 | 1 | ±8-kV Air-Gap, ±8-kV Contact, ±15-kV HBM | 3.3 or 5 | Auto powerdown plus, ready signal | 16-pin SSOP |
| SN75C3221 | | 1 | 1 | ±15-kV HBM | 3.3 or 5 | Auto powerdown | 16-pin SOIC, SSOP, TSSOP |
| SN75C3223 | | 2 | 2 | ±15-kV HBM | 3.5 or 5 | Auto powerdown, enable signal | 20-pin SOIC, SSOP, TSSOP |
| SN75C3222 | | 2 | 2 | ±15-kV HBM | 3.3 or 5 | Enable, powerdown signal | 20-pin SOIC, SSOP, TSSOP |
| SN75C3232 | | 2 | 2 | ±15-kV HBM | 3.3 or 5 | Low pin count | 16-pin SOIC, SSOP, TSSOP |
| SN75C3238 | | 5 | 3 | ±15-kV HBM | 3.3 or 5 | Auto powerdown plus | 28-pin SOIC, SSOP, TSSOP |
| SN75C3243 | | 3 | 5 | ±15-kV HBM | 3.3 or 5 | Auto powerdown | 28-pin SOIC, SSOP, TSSOP |

6 Pin Configuration and Functions

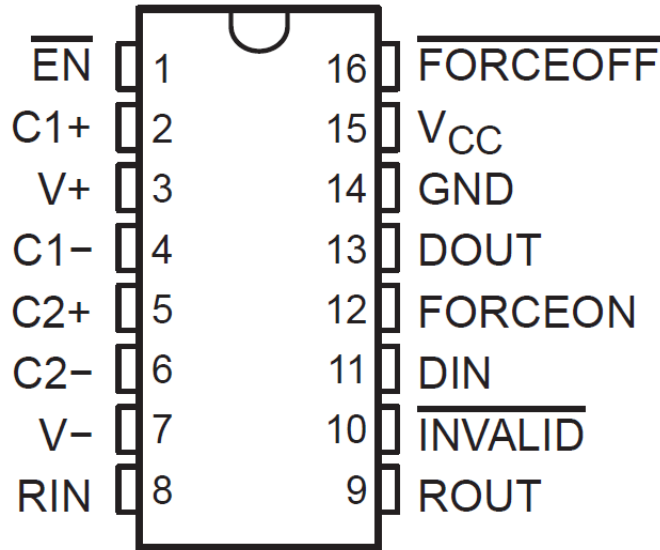


图 6-1. DB or PW Package
Top View

表 6-1. Pin Configurations

| PIN | | I/O | DESCRIPTION |
|-----------------|----|-----|---|
| NAME | NO | | |
| EN | 1 | I | Low input enables receiver ROUT output. High input sets ROUT to high impedance. |
| C1+ | 2 | — | Positive terminals of the voltage-doubler charge-pump capacitors |
| V+ | 3 | O | 5.5-V supply generated by the charge pump |
| C1- | 4 | — | Negative terminals of the voltage-doubler charge-pump capacitors |
| C2+ | 5 | — | Positive terminals of the voltage-doubler charge-pump capacitors |
| C2- | 6 | — | Negative terminals of the voltage-doubler charge-pump capacitors |
| V- | 7 | O | -5.5-V supply generated by the charge pump |
| RIN | 8 | I | RS-232 receiver input |
| ROUT | 9 | O | Receiver output |
| INVALID | 10 | O | Invalid output pin. Output low when all RIN inputs are unpowered. |
| DIN | 11 | I | Driver input |
| FORCEON | 12 | I | Automatic power-down control input |
| DOUT | 13 | O | RS-232 driver output |
| GND | 14 | — | Ground |
| V _{CC} | 15 | — | 3-V to 5.5-V supply voltage |
| FORCEOFF | 16 | I | Automatic power-down control input |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|---------------------------------|-----|------|
| V _{CC} | Supply voltage range ⁽²⁾ | -0.3 | 6 | V |
| V+ | Positive output supply voltage range ⁽²⁾ | -0.3 | 7 | V |
| V- | Negative output supply voltage range ⁽²⁾ | 0.3 | -7 | V |
| V+ - V- | Supply voltage difference ⁽²⁾ | | 13 | V |
| V _I | Input voltage range | Driver (FORCEOFF, FORCEON, EN) | | V |
| | | Receiver | | |
| V _O | Output voltage range | Driver | | V |
| | | Receiver (INVALID) | | |
| T _J | Operating virtual junction temperature | | 150 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

7.2 ESD Ratings

| | | | VALUE | UNIT | |
|--------------------|-------------------------|--|----------------|--------|---|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | DOUT, RIN | ±15000 | V |
| | | | All other pins | ±3000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | | ±1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC Specifications

| | | | VALUE | UNIT | |
|--------------------|-------------------------|--|------------------------|--------|---|
| V _(ESD) | Electrostatic discharge | IEC 61000-4-2 Contact Discharge ⁽¹⁾ | RIN and DOUT pins only | ±8000 | V |
| | | IEC 61000-4-2 Air Discharge ⁽¹⁾ | RIN and DOUT pins only | ±15000 | |

- (1) For the PW package of SN65C3221E only, a minimum of 1-μF capacitor is required between VCC and GND to meet the specified IEC-ESD level.

7.4 Recommended Operating Conditions

See [10-1](#). see ⁽¹⁾

| | | | MIN | NOM | MAX | UNIT |
|----------------|---|----------------------------|-------------------------|-----|-----|------|
| Supply voltage | | $V_{CC} = 3.3\text{ V}$ | 3 | 3.3 | 3.6 | V |
| | | $V_{CC} = 5\text{ V}$ | 4.5 | 5 | 5.5 | |
| V_{IH} | Driver and control high-level input voltage | DIN, FORCEOFF, FORCEON, EN | $V_{CC} = 3.3\text{ V}$ | 2 | | V |
| | | | $V_{CC} = 5\text{ V}$ | 2.4 | | |
| V_{IL} | Driver and control low-level input voltage | DIN, FORCEOFF, FORCEON, EN | | | 0.8 | V |
| V_I | Driver and control input voltage | DIN, FORCEOFF, FORCEON | 0 | | 5.5 | V |
| V_I | Receiver input voltage | | -25 | | 25 | V |
| T_A | Operating free-air temperature | SN65C3221E | -40 | | 85 | °C |
| | | SN75C3221E | 0 | | 70 | |

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

7.5 Thermal Information

| THERMAL METRIC ¹ | | SN65C3221E | | SN75C3221E | | UNIT |
|-----------------------------|--|------------|-----------|------------|-----------|------|
| | | PW (TSSOP) | DB (SSOP) | PW (TSSOP) | DB (SSOP) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 110.9 | 82 | 108 | 82 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 41.7 | 45.7 | 41.1 | 45.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 57.2 | 44.4 | 51.4 | 44.4 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 4.2 | 11.0 | 3.9 | 11.0 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 56.6 | 43.8 | 50.9 | 43.8 | °C/W |

7.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [10-1](#))

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-----------|--|--------------------------------|--|--------------------|-----|------|
| I_I | Input leakage current | FORCEOFF, FORCEON, EN | | ±0.01 | ±1 | μA |
| I_{CC} | Supply current ($T_A = 25^\circ\text{C}$) | Auto-powerdown disabled | No load, FORCEOFF and FORCEON at V_{CC} | 0.3 | 1 | mA |
| | | Powered off | No load, FORCEOFF at GND | 1 | 10 | μA |
| | | Auto-powerdown enabled | No load, FORCEOFF at V_{CC} , FORCEON at GND, All RIN are open or grounded | 1 | 10 | |

- (1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF, C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.
(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

7.7 Driver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [10-1](#))

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-----------|---|--|--|--------------------|-----|------|
| V_{OH} | High-level output voltage | DOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = GND | 5 | 5.4 | | V |
| V_{OL} | Low-level output voltage | DOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = V_{CC} | –5 | –5.4 | | V |
| I_{IH} | High-level input current | $V_I = V_{CC}$ | | ±0.01 | ±1 | μA |
| I_{IL} | Low-level input current | V_I at GND | | ±0.01 | ±1 | μA |
| I_{OS} | Short-circuit output current ⁽³⁾ | $V_{CC} = 3.6\text{ V}$, $V_O = 0\text{ V}$ | | ±35 | ±60 | mA |
| | | $V_{CC} = 5.5\text{ V}$, $V_O = 0\text{ V}$ | | ±35 | ±90 | |
| r_o | Output resistance | V_{CC} , $V+$, and $V- = 0\text{ V}$, $V_O = \pm 2\text{ V}$ | 300 | 10M | | Ω |
| I_{off} | Output leakage current | FORCEOFF = GND | $V_O = \pm 12\text{ V}$, $V_{CC} = 3\text{ V to } 3.6\text{ V}$ | | ±25 | μA |
| | | | $V_O = \pm 10\text{ V}$, $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ | | ±25 | |

- (1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF, C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.
(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

7.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [10-1](#))

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|---|---|---|-----|--------------------|-----|--------|
| Maximum data rate (see 8-1) | $R_L = 3\text{ k}\Omega$ | $C_L = 1000\text{ pF}$ | | 250 | | kbit/s |
| | | $C_L = 250\text{ pF}$, $V_{CC} = 3\text{ V to } 4.5\text{ V}$ | | 1000 | | |
| | | $C_L = 1000\text{ pF}$, $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ | | 1000 | | |
| $t_{sk(p)}$ | Pulse skew ⁽³⁾ | $C_L = 150\text{ pF to } 2500\text{ pF}$, $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, See 8-2 | | 100 | | ns |
| SR(tr) | Slew rate, transition region (see 8-1) | $V_{CC} = 3.3\text{ V}$, $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 150\text{ pF to } 1000\text{ pF}$ | 18 | | 150 | V/μs |

- (1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF, C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.
(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

7.9 Receiver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [10-1](#))

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|------------------|---|--------------------------------|-------------------------|-------------------------|-----|------|
| V _{OH} | High-level output voltage | I _{OH} = -1 mA | V _{CC} - 0.6 V | V _{CC} - 0.1 V | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{IT+} | Positive-going input threshold voltage | V _{CC} = 3.3 V | | 1.6 | 2.4 | V |
| | | V _{CC} = 5 V | | 1.9 | 2.4 | |
| V _{IT-} | Negative-going input threshold voltage | V _{CC} = 3.3 V | 0.6 | 1.1 | | V |
| | | V _{CC} = 5 V | 0.8 | 1.4 | | |
| V _{hys} | Input hysteresis (V _{IT+} - V _{IT-}) | | | 0.5 | | V |
| I _{off} | Output leakage current | FORCEOFF = 0 V | | ±0.05 | ±10 | µA |
| r _i | Input resistance | V _i = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

7.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [10-1](#))

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | TYP ⁽²⁾ | UNIT |
|--------------------|---|---|--------------------|------|
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 150 pF, See 8-3 | 150 | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | C _L = 150 pF, See 8-3 | 150 | ns |
| t _{en} | Output enable time | C _L = 150 pF, R _L = 3 kΩ, See 8-4 | 200 | ns |
| t _{dis} | Output disable time | C _L = 150 pF, R _L = 3 kΩ, See 8-4 | 200 | ns |
| t _{sk(p)} | Pulse skew ⁽³⁾ | See 8-3 | 50 | ns |

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

7.11 Auto-powerdown Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [8-5](#))

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--|--|----------------|-----|------|
| $V_{T+(valid)}$ | Receiver input threshold for INVALID high-level output voltage | FORCEON = GND, FORCEOFF = V_{CC} | | 2.7 | V |
| $V_{T-(valid)}$ | Receiver input threshold for INVALID high-level output voltage | FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$ | -2.7 | | V |
| $V_{T(invalid)}$ | Receiver input threshold for INVALID low-level output voltage | FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$ | -0.3 | 0.3 | V |
| V_{OH} | INVALID high-level output voltage | $I_{OH} = -1 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC} | $V_{CC} - 0.6$ | | V |
| V_{OL} | INVALID low-level output voltage | $I_{OL} = 1.6 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC} | | 0.4 | V |

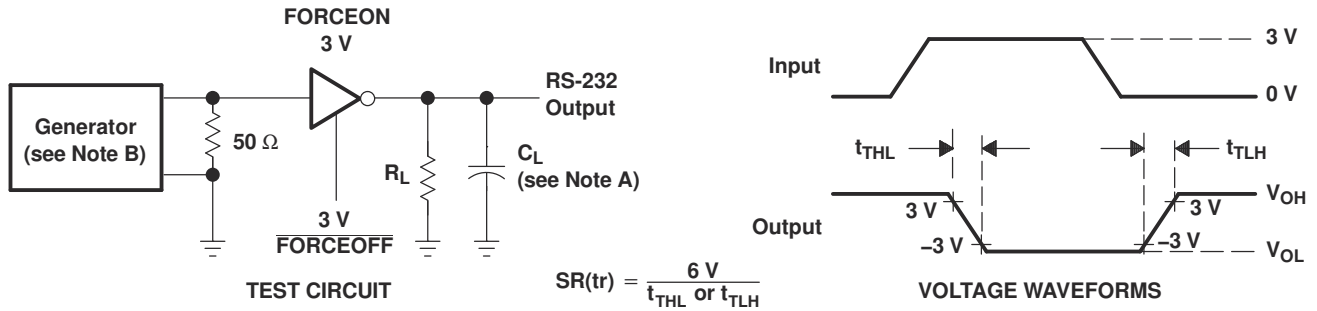
7.12 Switching Characteristics: Auto-powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [8-5](#))

| PARAMETER | | TYP ⁽¹⁾ | UNIT |
|---------------|---|--------------------|---------------|
| t_{valid} | Propagation delay time, low- to high-level output | 1 | μs |
| $t_{invalid}$ | Propagation delay time, high- to low-level output | 30 | μs |
| t_{en} | Supply enable time | 100 | μs |

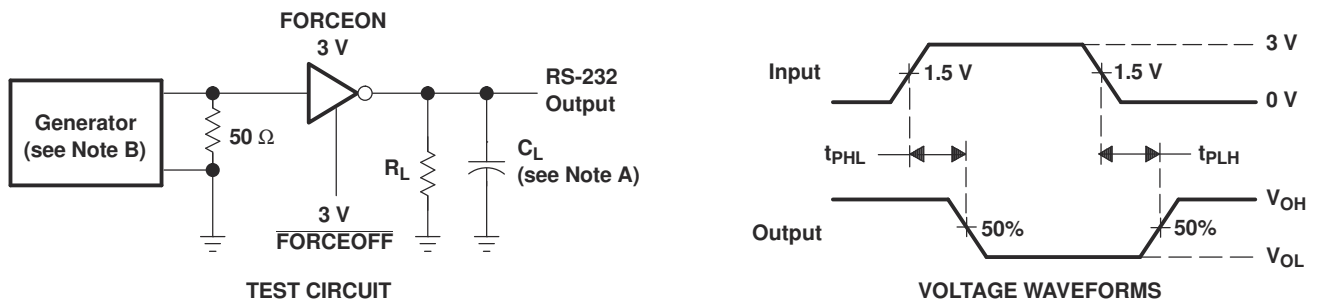
(1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

8 Parameter Measurement Information



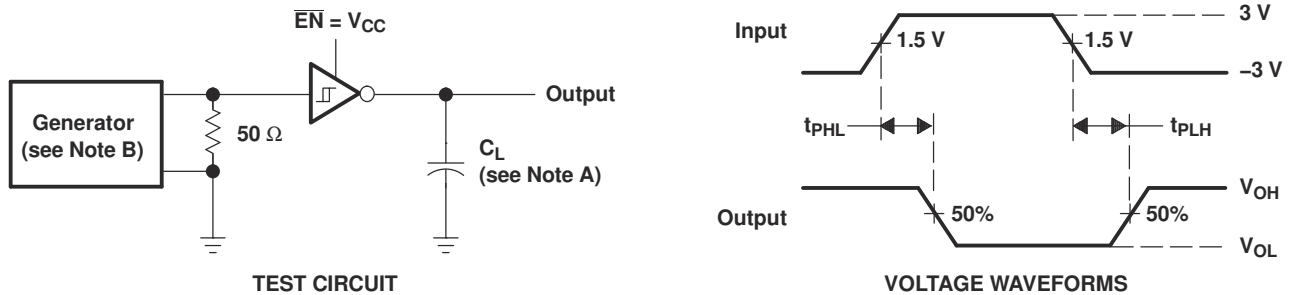
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

8-1. Driver Slew Rate



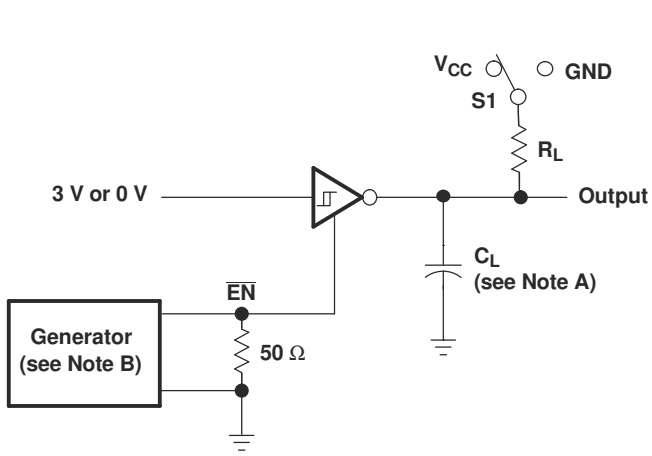
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

8-2. Driver Pulse Skew

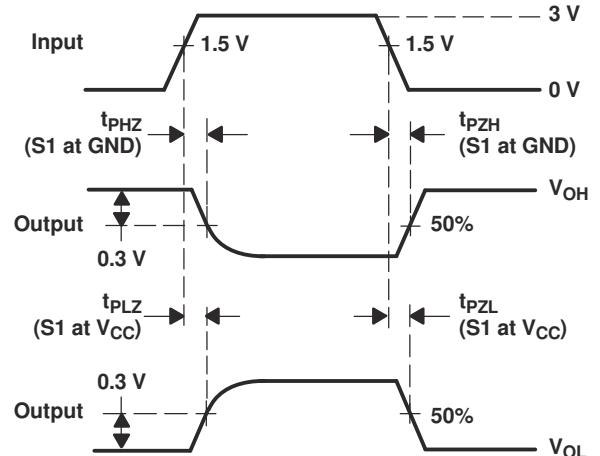


NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

8-3. Receiver Propagation Delay Times



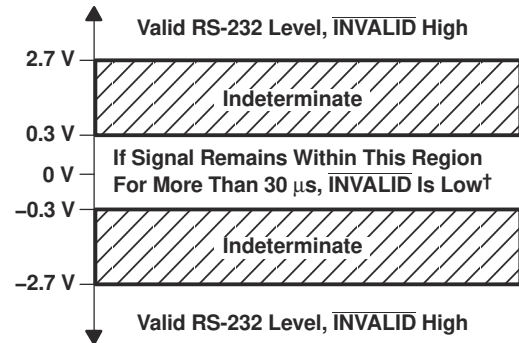
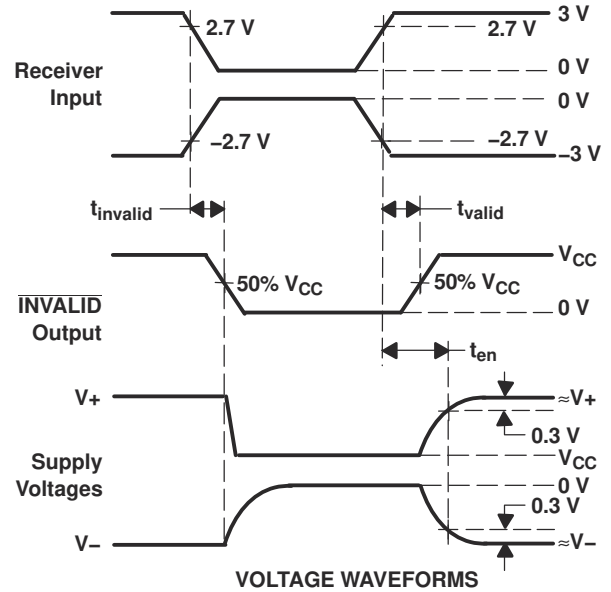
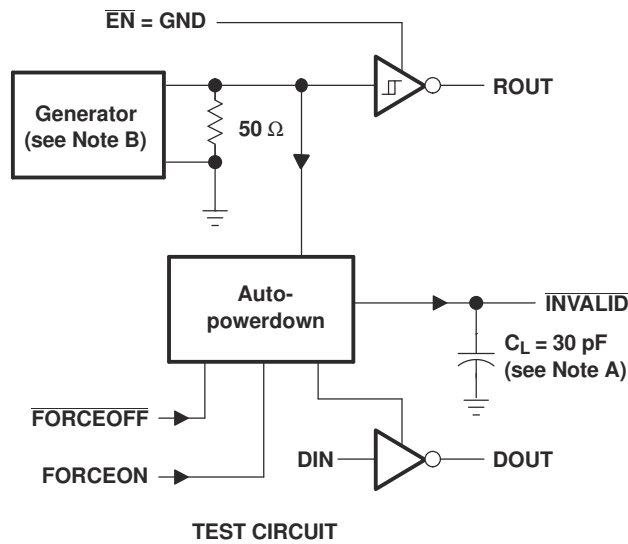
TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\ \text{ns}$, $t_f \leq 10\ \text{ns}$.
 - C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - D. t_{PZL} and t_{PZH} are the same as t_{en} .

8-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μ A.

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

8-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

9 Detailed Description

9.1 Device Functional Modes

表 9-1. Each Driver

| INPUTS ⁽¹⁾ | | | | OUTPUT DOUT | DRIVER STATUS |
|-----------------------|---------|----------|---------------------------|----------------|--|
| DIN | FORCEON | FORCEOFF | VALID RIN RS-232 LEVEL | | |
| X | X | L | X | Z | Powered off |
| L | H | H | X | H | Normal operation with auto-powerdown disabled |
| H | H | H | X | L | |
| L | L | H | Yes | H | Normal operation with auto-powerdown enabled |
| H | L | H | Yes | L | |
| L | L | H | No | Z | Powered off by auto-powerdown feature |
| H | L | H | No | Z | |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 9-2. Each Receiver

| INPUTS ⁽¹⁾ | | | OUTPUT ROUT |
|-----------------------|----|---------------------------|----------------|
| RIN | EN | VALID RIN RS-232 LEVEL | |
| L | L | X | H |
| H | L | X | L |
| X | H | X | Z |
| Open | L | No | H |

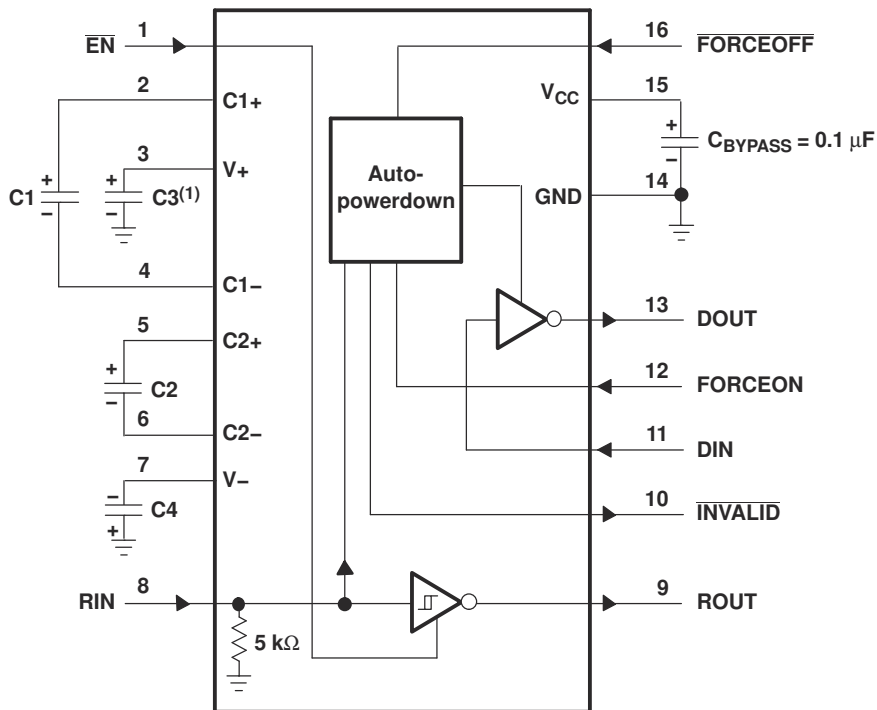
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

| V _{CC} | C1 | C2, C3, and C4 |
|-----------------|----------|----------------|
| 3.3 V ± 0.3 V | 0.1 μF | 0.1 μF |
| 5 V ± 0.5 V | 0.047 μF | 0.33 μF |
| 3 V to 5.5 V | 0.1 μF | 0.47 μF |

 10-1. Typical Operating Circuit and Capacitor Values

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65C3221EDBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU221E | Samples |
| SN65C3221EPWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU221E | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65C3221EDBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN65C3221EPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65C3221EDBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C3221EPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

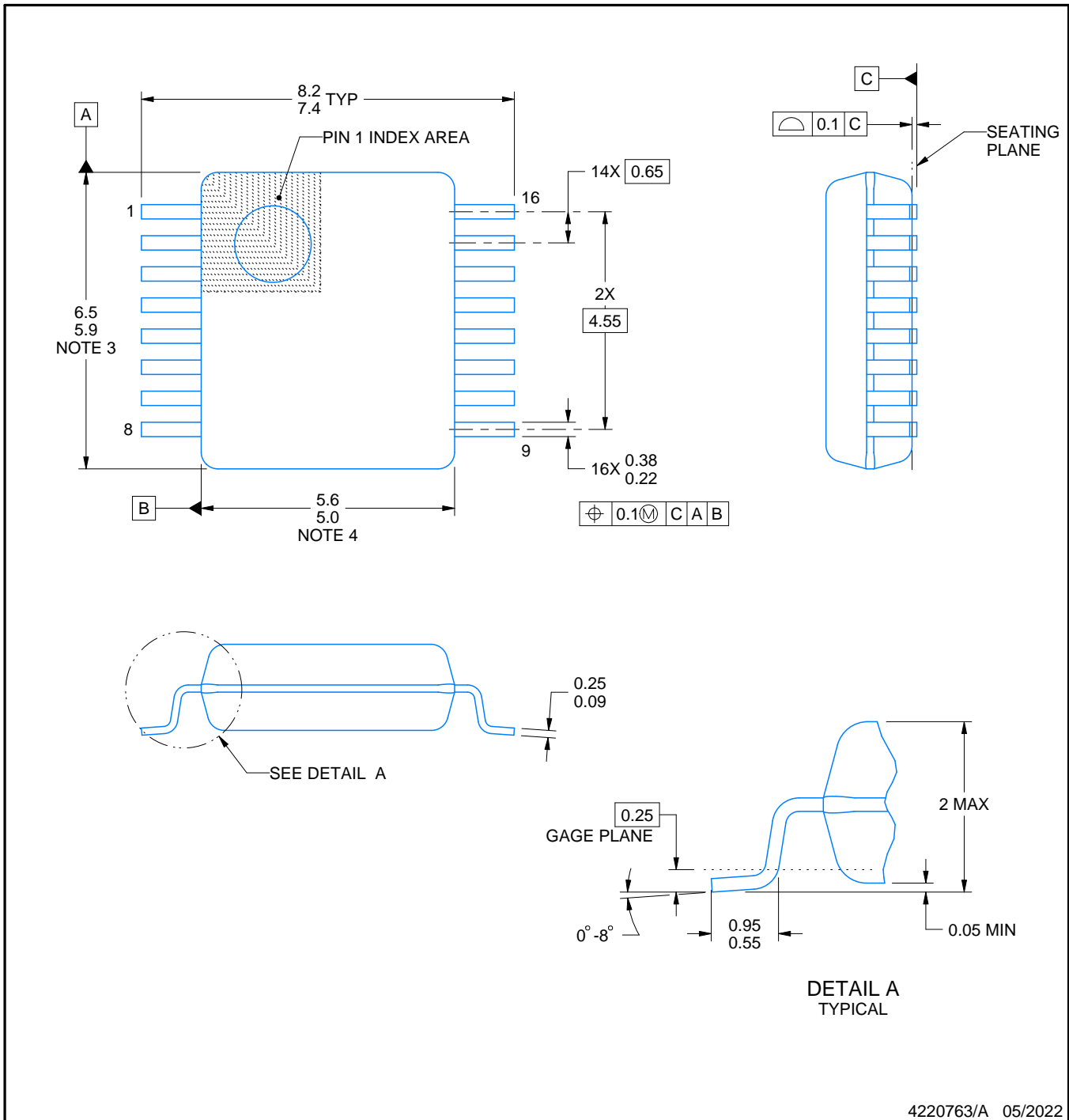
DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

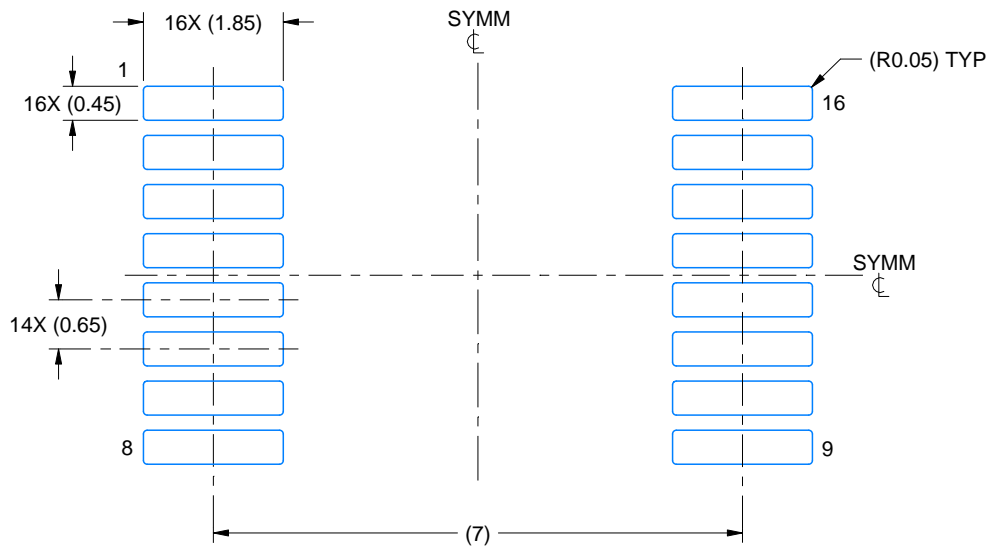
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

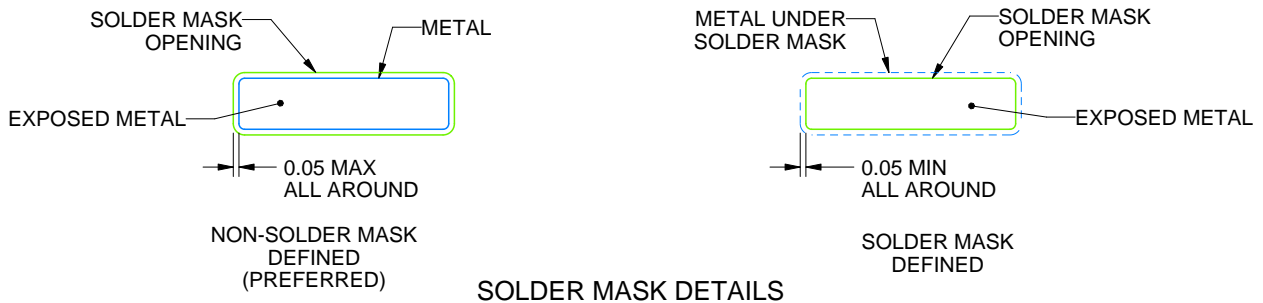
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

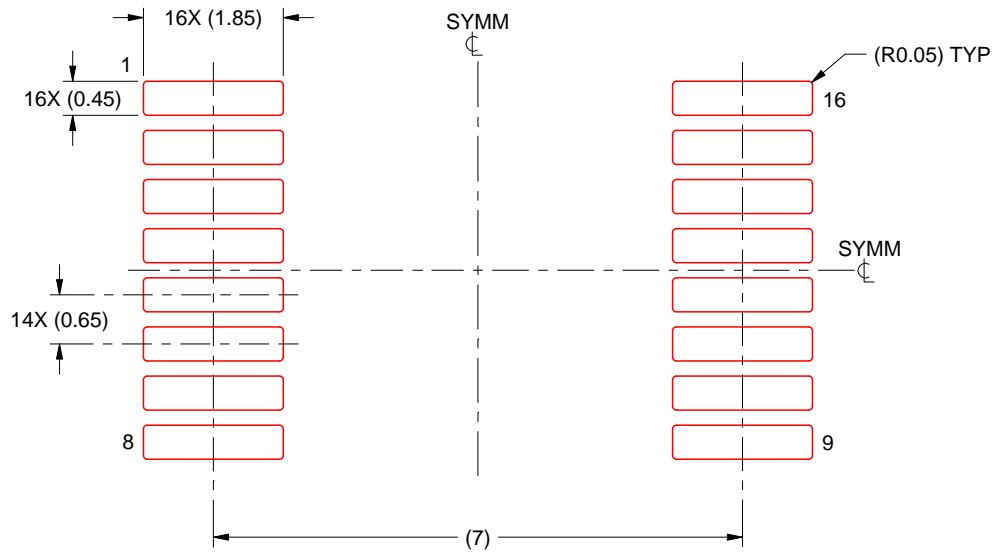
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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