

SN65HVD0x、SN75HVD0x 高出力 RS-485 トランシーバ

1 特長

- 54Ω の負荷に 2.5V の最小差動出力電圧
- 開路、短絡、アイドル・バスのフェイルセーフ・レシーバ
- 1/8 ユニット負荷オプションが使用可能 (バス上に最大 256 ノード)
- 16kV HBM を超えるバス・ピンの ESD 保護
- ドライバ出力スルーレート制御オプション
- ANSI TIA/EIA-485-A 標準と電氣的に互換
- 低電流のスタンバイ・モード: 1μA (標準値)
- ホットプラグ・アプリケーションに適したグリッチのない電源オン/オフ
- 業界標準の SN75176 とピン互換

2 アプリケーション

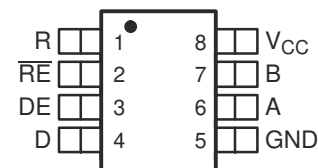
- 長距離または損失の多いライン、または電氣的にノイズの多い環境でのデータ転送
- PROFIBUS ライン・インターフェイス
- 産業用プロセス制御ネットワーク
- POS (販売時点情報管理) ネットワーク
- 電気料金のメーター
- ビル・オートメーション
- デジタル・モーター制御

3 概要

SN65HVD05、SN75HVD05、SN65HVD06、SN75HVD06、SN65HVD07、SN75HVD07 は、3 ステート差動ライン・ドライバと作動ライン・レシーバを組み合わせた製品です。これらは平衡データ転送用に設計されており、ANSI TIA/EIA-485-A および ISO 8482E 標準準拠のデバイスと相互運用が可能です。このドライバは、ノイズ・マージンを大きくするため、これらの規格で要求されている以上の差動出力電圧を供給できるよう設計されています。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。

ドライバ差動出力とレシーバ差動入力は内部で接続されており、差動入出力 (I/O) バス・ポートを形成しています。この設計により、ドライバが無効になったり、電力が供給されなくなっても、バスへの負荷が最小限になります。これらのデバイスは正負の同相電圧範囲が広いので、パーティライン・アプリケーションに適しています。

D OR P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM
(POSITIVE LOGIC)

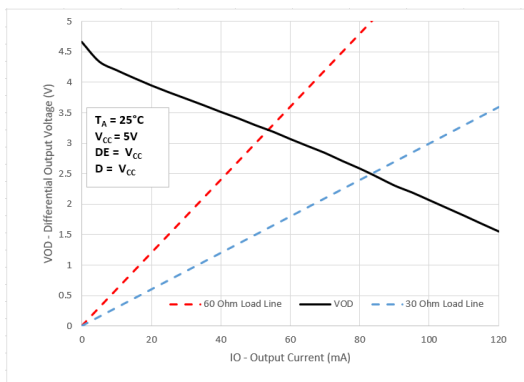
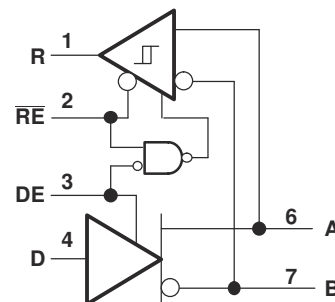


図 3-1. 差動出力電圧と差動出力電流との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision E (August 2009) to Revision F (March 2023) | Page |
|---|-------------|
| • 「注文情報」表を削除..... | 1 |
| • Added the <i>Thermal Information</i> table..... | 4 |
| • Changed the <i>Typical Characteristics</i> | 9 |

| Changes from Revision D (July 2006) to Revision E (August 2009) | Page |
|--|-------------|
| • Added IDLE Bus to the Receivers Function Table..... | 16 |
| • Added the Receiver Failsafe paragraph..... | 16 |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted^{(1) (2)}

| | | | SN65HVD05, SN65HVD06, SN65HVD07 SN75HVD05, SN75HVD06, SN75HVD07 |
|---|-------------------------------------|---------------|--|
| Supply voltage range, V_{CC} | | | -0.3 V to 6 V |
| Voltage range at A or B | | | -9 V to 14 V |
| Input voltage range at D, DE, R or RE | | | -0.5 V to $V_{CC} + 0.5$ V |
| Voltage input range, transient pulse, A and B, through 100 Ω (see 6-11) | | | -50 V to 50 V |
| Receiver output current, I_O | | | -11 mA to 11mA |
| Electrostatic discharge | Human body model ⁽³⁾ | A, B, and GND | 16 kV |
| | | All pins | 4 kV |
| | Charged-device model ⁽⁴⁾ | All pins | 1 kV |
| Continuous total power dissipation | | | See Dissipation Rating Table |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

5.2 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|-----------|--|-------------------|-----|-----|--------------|
| Supply voltage, V_{CC} | | | 4.5 | | 5.5 | V |
| Voltage at any bus terminal (separately or common mode) V_I or V_{IC} | | | -7 ⁽¹⁾ | | 12 | V |
| High-level input voltage, V_{IH} | D, DE, RE | | 2 | | | V |
| Low-level input voltage, V_{IL} | D, DE, RE | | | | 0.8 | V |
| Differential input voltage, V_{ID} (see 6-7) | | | -12 | | 12 | V |
| High-level output current, I_{OH} | Driver | | -100 | | | mA |
| | Receiver | | -8 | | | |
| Low-level output current, I_{OL} | Driver | | | | 100 | mA |
| | Receiver | | | | 8 | |
| Operating free-air temperature, T_A | SN65HVD05 | | -40 | | 85 | $^{\circ}$ C |
| | SN65HVD06 | | | | | |
| | SN65HVD07 | | | | | |
| | SN75HVD05 | | 0 | | 70 | $^{\circ}$ C |
| | SN75HVD06 | | | | | |
| | SN75HVD07 | | | | | |

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D (SOIC) SN65 Variation | D (SOIC) SN75 Variation | P (PDIP) | UNIT |
|-------------------------------|--|-------------------------------|-------------------------------|----------|------|
| | | 8 PINS | 8 PINS | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 116.7 | 175.4 | 125 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 56.3 | 53.6 | 34.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 63.4 | 45.1 | 23.7 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 8.8 | 10.1 | 12.1 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 62.6 | 44.4 | 23.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.4 Package Dissipation Ratings

(See [5-1](#) and [5-2](#))

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|------------------|---------------------------------------|---|---------------------------------------|---------------------------------------|
| D ⁽²⁾ | 710 mW | 5.7 mW/°C | 455 mW | 369 mW |
| D ⁽³⁾ | 1282 mW | 10.3 mW/°C | 821 mW | 667 mW |
| P | 1000 mW | 8.0 m W/°C | 640 mW | 520 mW |

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
- (2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3
- (3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

5.5 Driver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|--|---|---|------|--------------------|-----------------|------|
| V _{IK} | Input clamp voltage | I _I = -18 mA | | -1.5 | | | V |
| V _{OD} | Differential output voltage | No Load | | | | V _{CC} | V |
| | | R _L = 54 Ω, See 6-4 | | 2.5 | | | |
| | | V _{test} = -7 V to 12 V, See 6-2 | | 2.2 | | | |
| Δ V _{OD} | Change in magnitude of differential output voltage | See 6-4 and 6-2 | | -0.2 | | 0.2 | V |
| V _{OC(SS)} | Steady-state common-mode output voltage | See 6-3 | | 2.2 | | 3.3 | V |
| ΔV _{OC(SS)} | Change in steady-state common-mode output voltage | See 6-3 | | -0.1 | | 0.1 | V |
| V _{OC(PP)} | Peak-to-peak common-mode output voltage | HVD05 | See 6-3 | | 600 | | mV |
| | | HVD06 | | 500 | | | |
| | | HVD07 | | 900 | | | |
| I _{OZ} | High-impedance output current | See receiver input currents | | | | | |
| I _I | Input current | D | | -100 | | 0 | μA |
| | | DE | | 0 | | 100 | |
| I _{OS} | Short-circuit output current | -7 V ≤ V _O ≤ 12 V | | -250 | | 250 | mA |
| C _(diff) | Differential output capacitance | V _{ID} = 0.4 sin(4E6πt) + 0.5 V, DE at 0 V | | | 16 | | pF |
| I _{CC} | Supply current | RE at V _{CC} , D and DE at V _{CC} , No load | Receiver disabled and driver enabled | | 9 | 15 | mA |
| | | RE at V _{CC} , D at V _{CC} DE at 0 V, No load | Receiver disabled and driver disabled (standby) | | 1 | 5 | μA |
| | | RE at 0 V, D and DE at V _{CC} , No load | Receiver enabled and driver enabled | | 9 | 15 | mA |

(1) All typical values are at 25°C and with a 5-V supply.

5.6 Driver Switching Characteristics

over operating free-air temperature range unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | | |
|------------------------------------|---|---|---|---|-----|------|-----|----|
| t _{PLH} | Propagation delay time, low-to-high-level output | HVD05 | | 6.5 | 11 | ns | | |
| | | HVD06 | | 27 | 40 | | | |
| | | HVD07 | | 250 | 400 | | | |
| t _{PHL} | Propagation delay time, high-to-low-level output | HVD05 | | 6.5 | 11 | ns | | |
| | | HVD06 | | 27 | 40 | | | |
| | | HVD07 | | 250 | 400 | | | |
| t _r | Differential output signal rise time | HVD05 | R _L = 54 Ω, C _L = 50 pF, See 6-4 | 2.7 | 3.6 | 6 | ns | |
| | | HVD06 | | 18 | 28 | 55 | | |
| | | HVD07 | | 150 | 300 | 450 | | |
| t _f | Differential output signal fall time | HVD05 | | 2.7 | 3.6 | 6 | ns | |
| | | HVD06 | | 18 | 28 | 55 | | |
| | | HVD07 | | 150 | 300 | 450 | | |
| t _{sk(p)} | Pulse skew (t _{PHL} - t _{PLH}) | HVD05 | | | | 2 | ns | |
| | | HVD06 | | | | 2.5 | | |
| | | HVD07 | | | | 10 | | |
| t _{sk(pp)} ⁽²⁾ | Part-to-part skew | HVD05 | | | 3.5 | ns | | |
| | | HVD06 | | | 14 | | | |
| | | HVD07 | | | 100 | | | |
| t _{PZH1} | Propagation delay time, high-impedance-to-high-level output | HVD05 | R _Ē at 0 V, R _L = 110 Ω, See 6-5 | | | 25 | ns | |
| | | HVD06 | | | | 45 | | |
| | | HVD07 | | | | 250 | | |
| t _{PHZ} | Propagation delay time, high-level-to-high-impedance output | HVD05 | | 25 | | | ns | |
| | | HVD06 | | | | 60 | | |
| | | HVD07 | | | | 250 | | |
| t _{PZL1} | Propagation delay time, high-impedance-to-low-level output | HVD05 | | R _Ē at 0 V, R _L = 110 Ω, See 6-6 | | | 15 | ns |
| | | HVD06 | | | | | 45 | |
| | | HVD07 | | | | | 200 | |
| t _{PLZ} | Propagation delay time, low-level-to-high-impedance output | HVD05 | 14 | | | | ns | |
| | | HVD06 | | | | 90 | | |
| | | HVD07 | | | | 550 | | |
| t _{PZH2} | Propagation delay time, standby-to-high-level output | R _L = 110 Ω, R _Ē at 3 V, See 6-5 | | | | 6 | μs | |
| t _{PZL2} | Propagation delay time, standby-to-low-level output | R _L = 110 Ω, R _Ē at 3 V, See 6-6 | | | | 6 | μs | |

(1) All typical values are at 25°C and with a 5-V supply.

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.7 Receiver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|--------------|--|--|---|---------------------------------|------------------------|--------------------|-------|---------------|------|
| V_{IT+} | Positive-going input threshold voltage | $I_O = -8 \text{ mA}$ | | | | | -0.01 | V | |
| V_{IT-} | Negative-going input threshold voltage | $I_O = 8 \text{ mA}$ | | | | -0.2 | | | |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | | | 35 | | mV | |
| V_{IK} | Enable-input clamp voltage | $I_I = -18 \text{ mA}$ | | | -1.5 | | | V | |
| V_{OH} | High-level output voltage | $V_{ID} = 200 \text{ mV}$, | $I_{OH} = -8 \text{ mA}$, | See 6-7 | 4 | | | V | |
| V_{OL} | Low-level output voltage | $V_{ID} = -200 \text{ mV}$, | $I_{OL} = 8 \text{ mA}$, | See 6-7 | | | 0.4 | V | |
| I_{OZ} | High-impedance-state output current | $V_O = 0$ or V_{CC} | \overline{RE} at V_{CC} | | -1 | | 1 | μA | |
| I_I | Bus input current | HVD05 | Other input at 0 V | V_A or $V_B = 12 \text{ V}$ | | 0.23 | 0.5 | mA | |
| | | | | V_A or $V_B = 12 \text{ V}$, | $V_{CC} = 0 \text{ V}$ | | 0.3 | | 0.5 |
| | | | | V_A or $V_B = -7 \text{ V}$ | | -0.4 | 0.13 | | |
| | | | | V_A or $V_B = -7 \text{ V}$, | $V_{CC} = 0 \text{ V}$ | -0.4 | 0.15 | | |
| | | HVD06 HVD07 | Other input at 0 V | V_A or $V_B = 12 \text{ V}$ | | 0.06 | 0.1 | mA | |
| | | | | V_A or $V_B = 12 \text{ V}$, | $V_{CC} = 0 \text{ V}$ | | 0.08 | | 0.13 |
| | | | | V_A or $V_B = -7 \text{ V}$ | | -0.1 | 0.05 | | |
| | | | | V_A or $V_B = -7 \text{ V}$, | $V_{CC} = 0 \text{ V}$ | -0.05 | 0.03 | | |
| I_{IH} | High-level input current, \overline{RE} | $V_{IH} = 2 \text{ V}$ | | | -60 | 26.4 | | μA | |
| I_{IL} | Low-level input current, \overline{RE} | $V_{IL} = 0.8 \text{ V}$ | | | -60 | 27.4 | | μA | |
| $C_{(diff)}$ | Differential input capacitance | $V_I = 0.4 \sin(4E6\pi t) + 0.5 \text{ V}$, DE at 0 V | | | | 16 | | pF | |
| I_{CC} | Supply current | \overline{RE} at 0 V, D and DE at 0 V, No load | Receiver enabled and driver disabled | | | 5 | 10 | mA | |
| | | \overline{RE} at V_{CC} , DE at 0 V, D at V_{CC} , No load | Receiver disabled and driver disabled (standby) | | | 1 | 5 | μA | |
| | | \overline{RE} at 0 V, D and DE at V_{CC} , No load | Receiver enabled and driver enabled | | | 9 | 15 | mA | |

(1) All typical values are at 25°C and with a 5-V supply.

5.8 Receiver Switching Characteristics

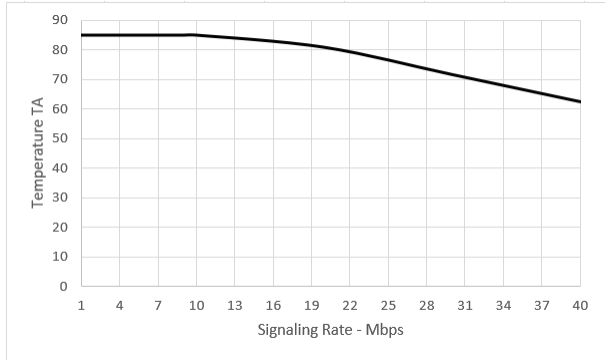
over operating free-air temperature range unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|------------------------------------|---|--|--|--------------------|-----|------|----|
| t _{PLH} | Propagation delay time, low-to-high-level output 1/2 UL | HVD05 | | 14.6 | 25 | ns | |
| t _{PHL} | Propagation delay time, high-to-low-level output 1/2 UL | HVD05 | | 14.6 | 25 | ns | |
| t _{PLH} | Propagation delay time, low-to-high-level output 1/8 UL | HVD06 | | 55 | 70 | ns | |
| | | HVD07 | | 55 | 70 | | |
| t _{PHL} | Propagation delay time, high-to-low-level output 1/8 UL | HVD06 | V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See 6-8 | 55 | 70 | ns | |
| | | HVD07 | | 55 | 70 | | |
| t _{sk(p)} | Pulse skew (t _{PHL} - t _{PLH}) | HVD05 | | | | 2 | ns |
| | | HVD06 | | | | 4.5 | |
| | | HVD07 | | | | 4.5 | |
| t _{sk(pp)} ⁽²⁾ | Part-to-part skew | HVD05 | | | | 6.5 | ns |
| | | HVD06 | | | 14 | | |
| | | HVD07 | | | 14 | | |
| t _r | Output signal rise time | C _L = 15 pF, See 6-8 | | 2 | 3 | ns | |
| t _f | Output signal fall time | | | 2 | 3 | | |
| t _{PZH1} | Output enable time to high level | C _L = 15 pF, DE at 3 V, See 6-9 | | | 10 | ns | |
| t _{PZL1} | Output enable time to low level | | | | 10 | | |
| t _{PHZ} | Output disable time from high level | | | | 15 | | |
| t _{PLZ} | Output disable time from low level | | | | 15 | | |
| t _{PZH2} | Propagation delay time, standby-to-high-level output | C _L = 15 pF, DE at 0, See 6-10 | | | 6 | μs | |
| t _{PZL2} | Propagation delay time, standby-to-low-level output | | | | 6 | | |

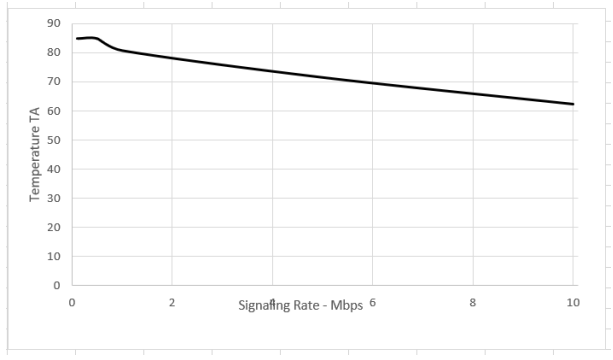
(1) All typical values are at 25°C and with a 5-V supply.

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

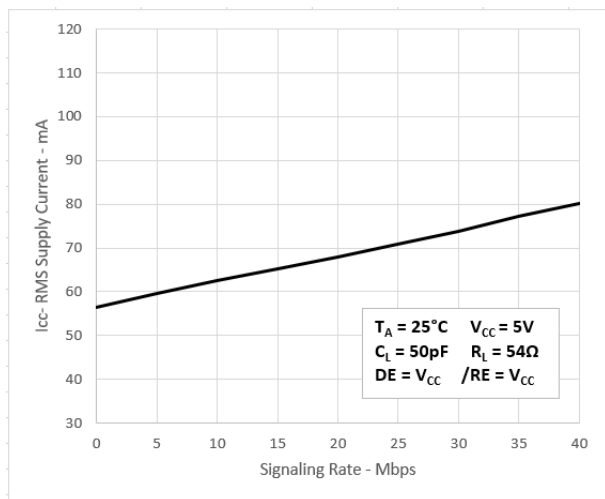
5.9 Typical Characteristics



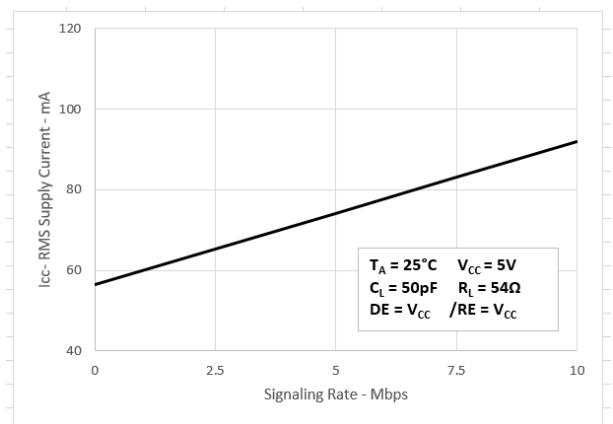
5-1. HVD05 Maximum Recommended Still-Air Operating Temperature vs Signaling Rate (D-Package)



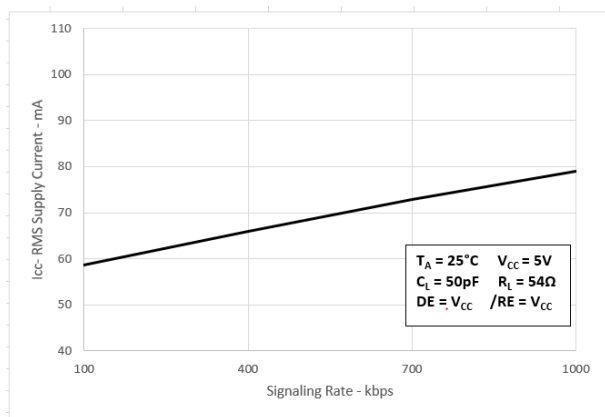
5-2. HVD06 Maximum Recommended Still-Air Operating Temperature vs Signaling Rate (D-Package)



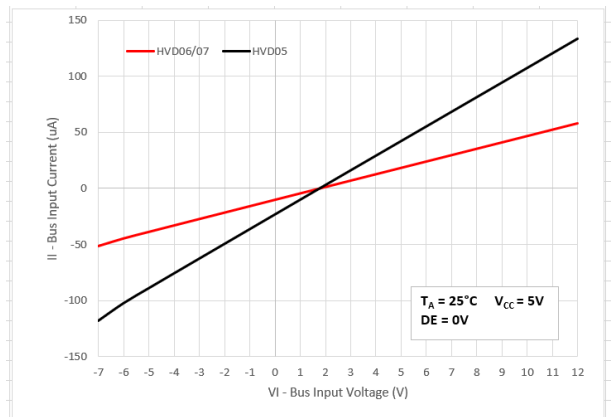
5-3. HVD05 RMS Supply Current vs Signaling Rate



5-4. HVD06 RMS Supply Current vs Signaling Rate



5-5. HVD07 RMS Supply Current vs Signaling Rate



5-6. BUS Input Current vs BUS Input Voltage

5.9 Typical Characteristics (continued)

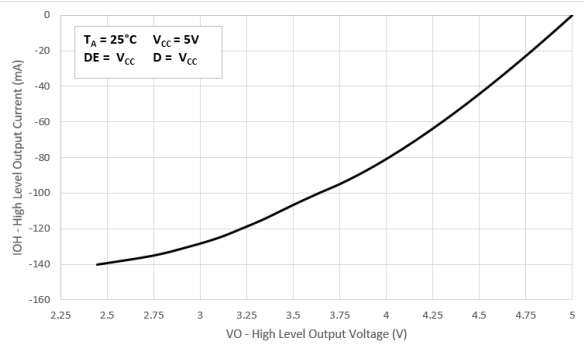


Fig 5-7. Driver High-Level Output Current vs High-Level Output Voltage

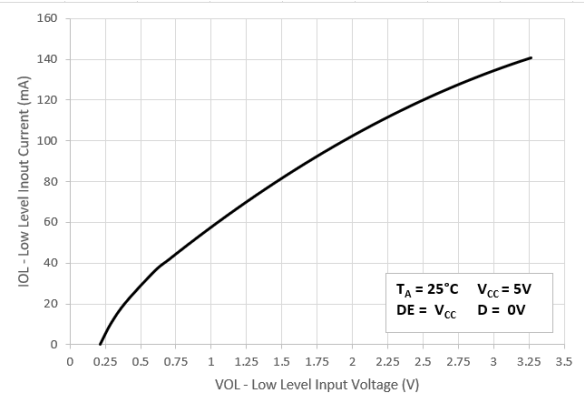


Fig 5-8. Driver Low-Level Output Current vs Low-Level Output Voltage

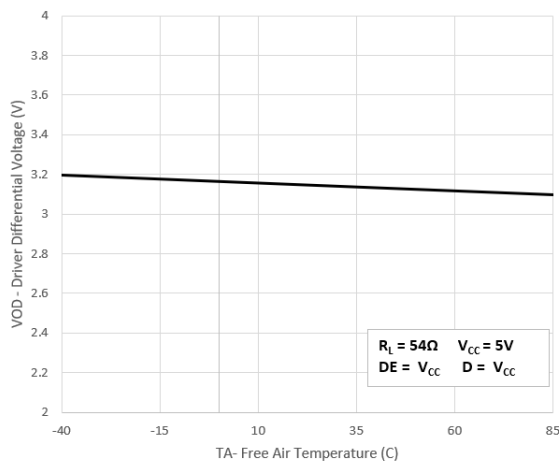


Fig 5-9. Differential Output Voltage vs Free-Air Temperature

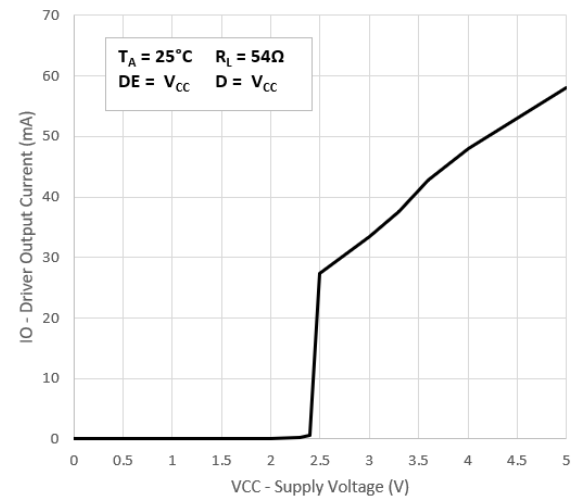


Fig 5-10. Driver Output Current vs Supply Voltage

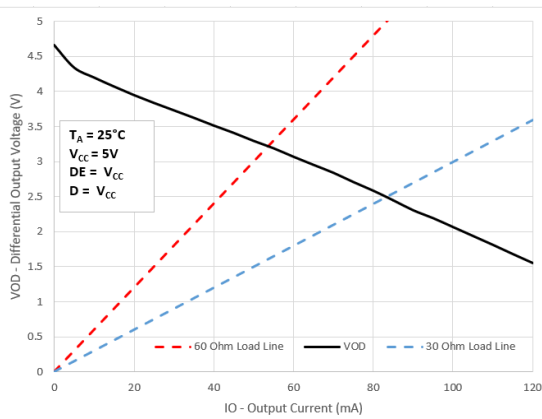


Fig 5-11. Differential Output Voltage vs Differential Output Current

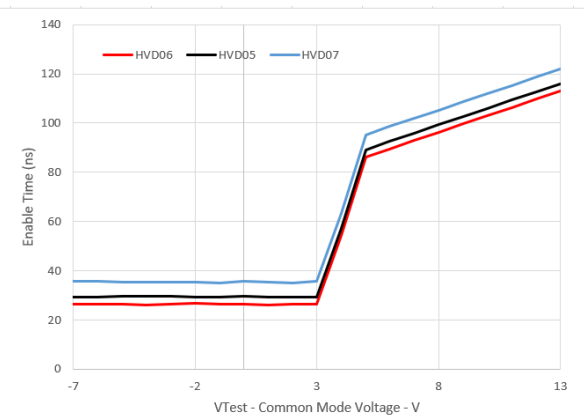
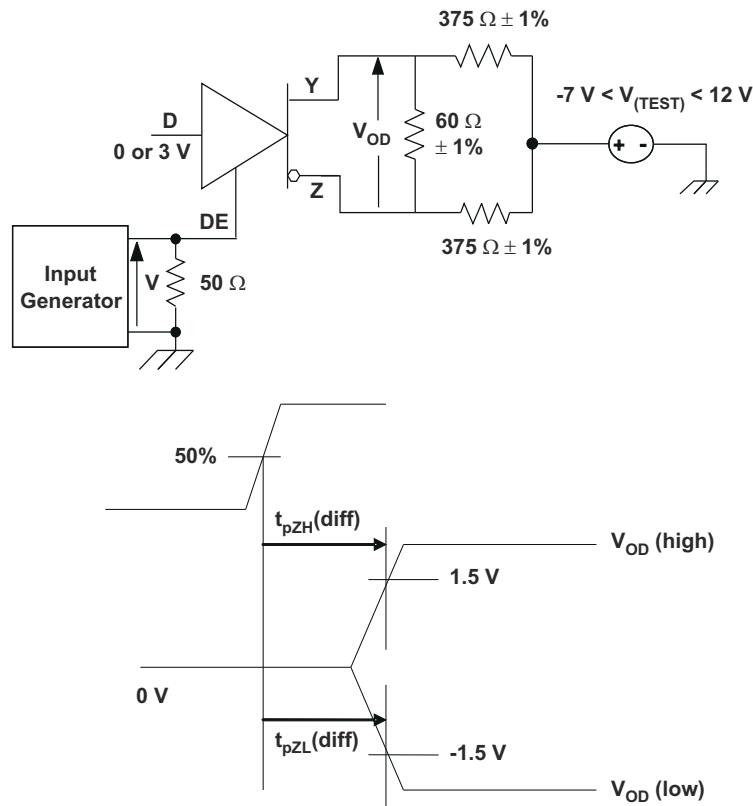


Fig 5-12. Enable Time vs Common-Mode Voltage
(See Fig 5-13)

5.9 Typical Characteristics (continued)



 5-13. Driver Enable Time From DE to V_{OD}

Parameter Measurement Information

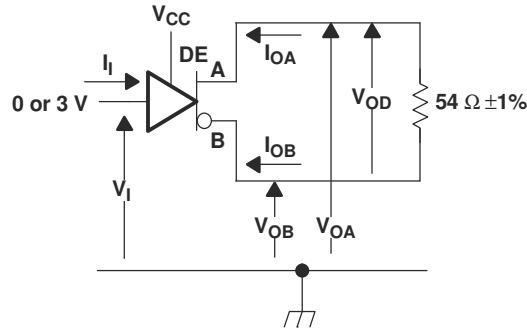


Figure 6-1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

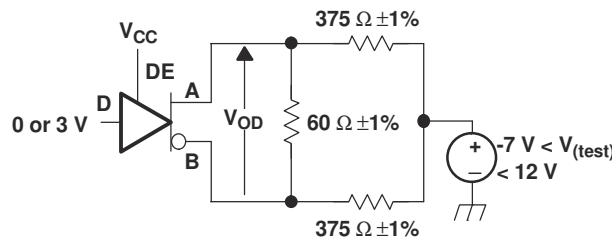
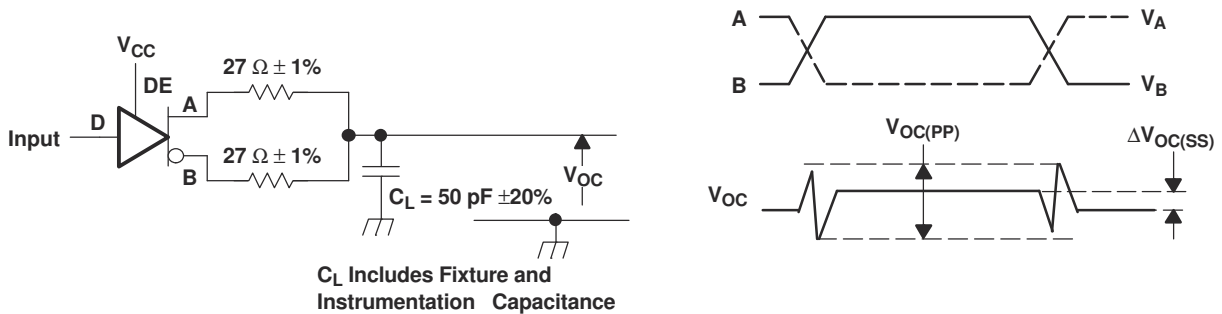
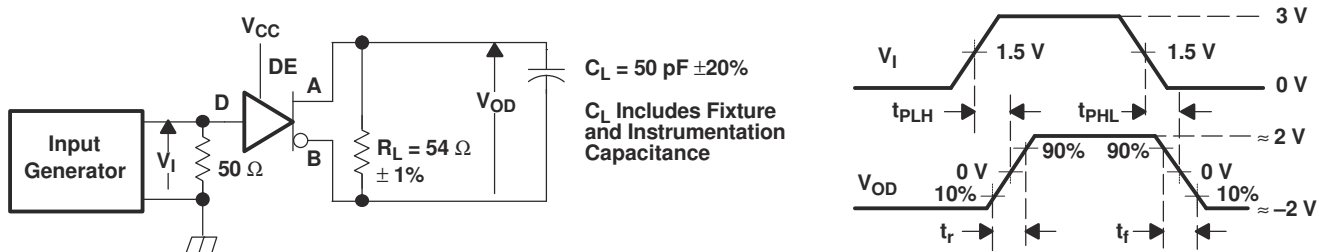


Figure 6-2. Driver V_{OD} With Common-Mode Loading Test Circuit



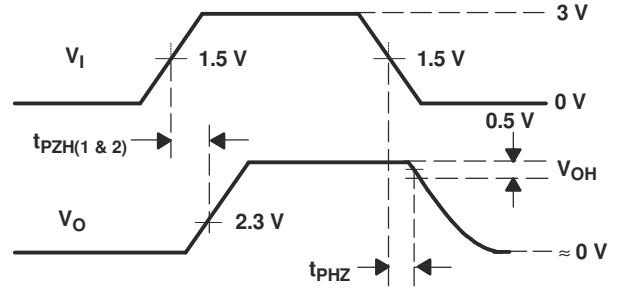
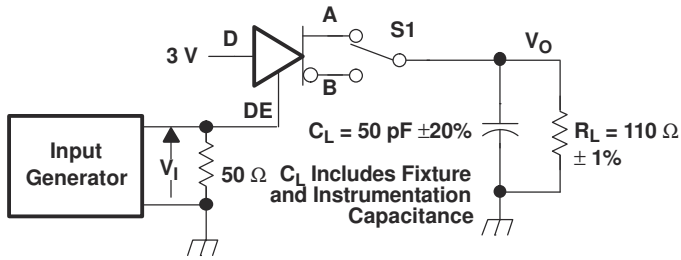
Input: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_o = 50 \Omega$

Figure 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



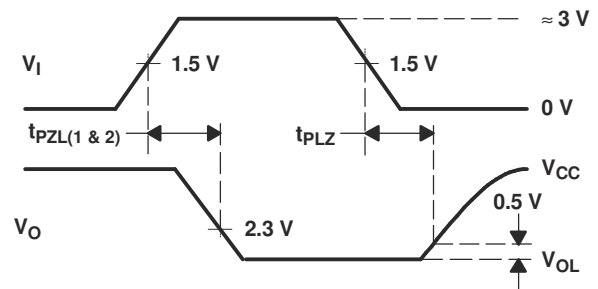
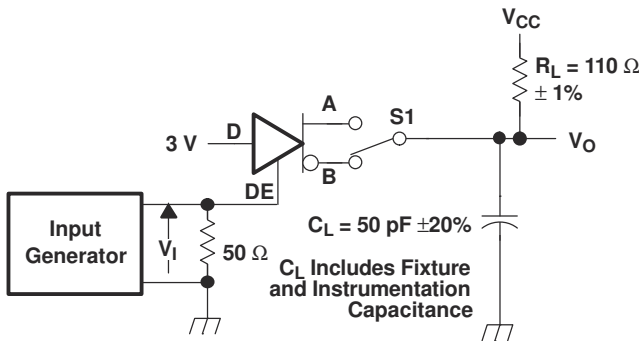
Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_o = 50 \Omega$

Figure 6-4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_o = 50 \Omega$

图 6-5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_o = 50 \Omega$

图 6-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

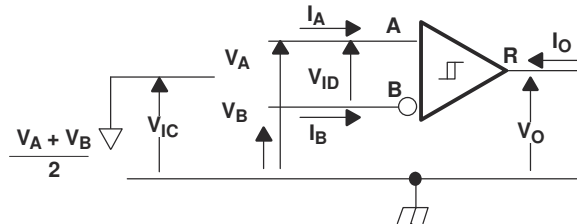
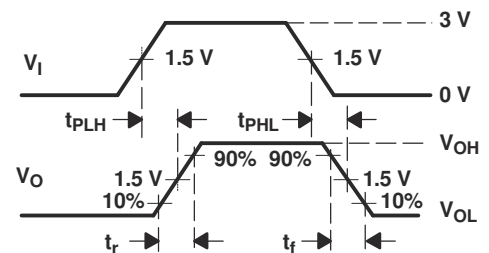
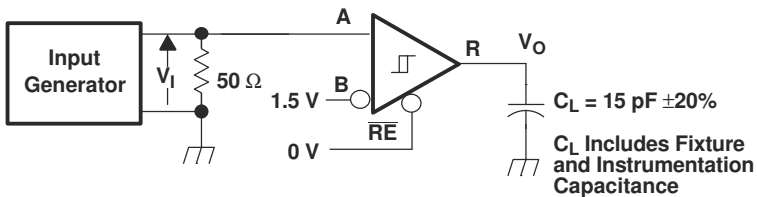
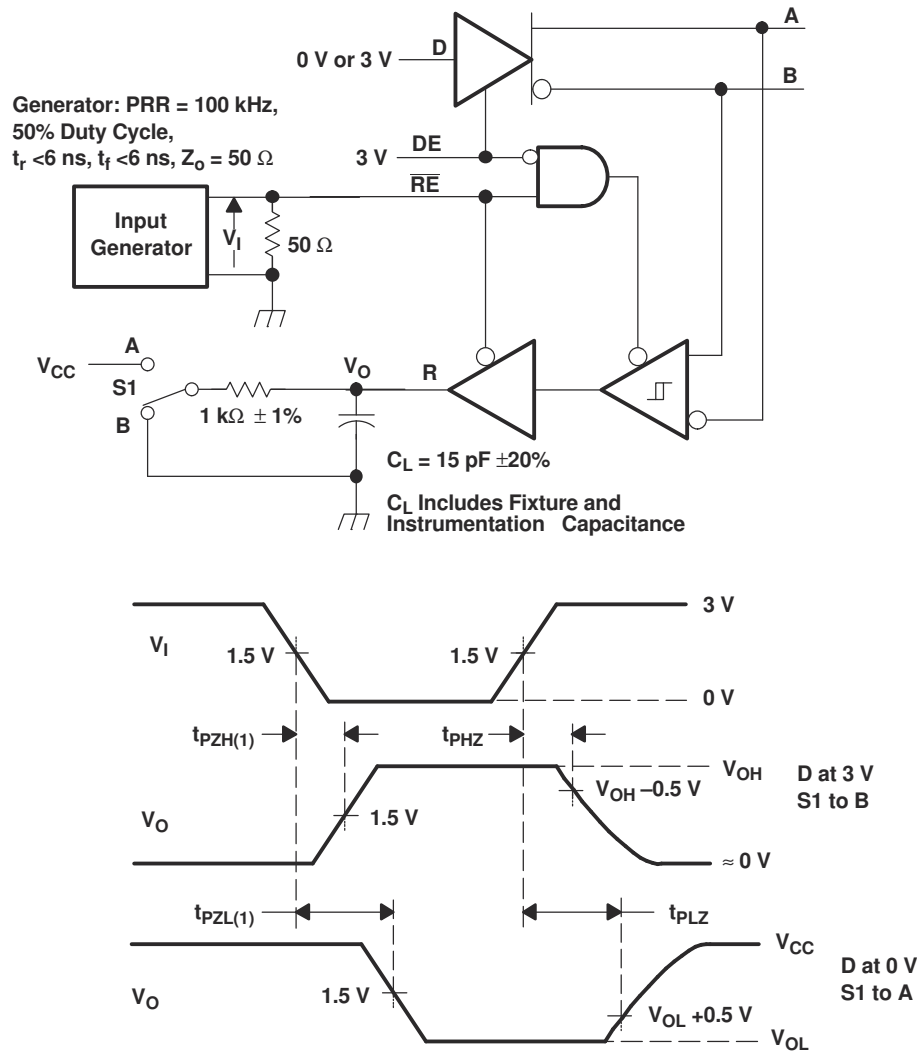


图 6-7. Receiver Voltage and Current Definitions

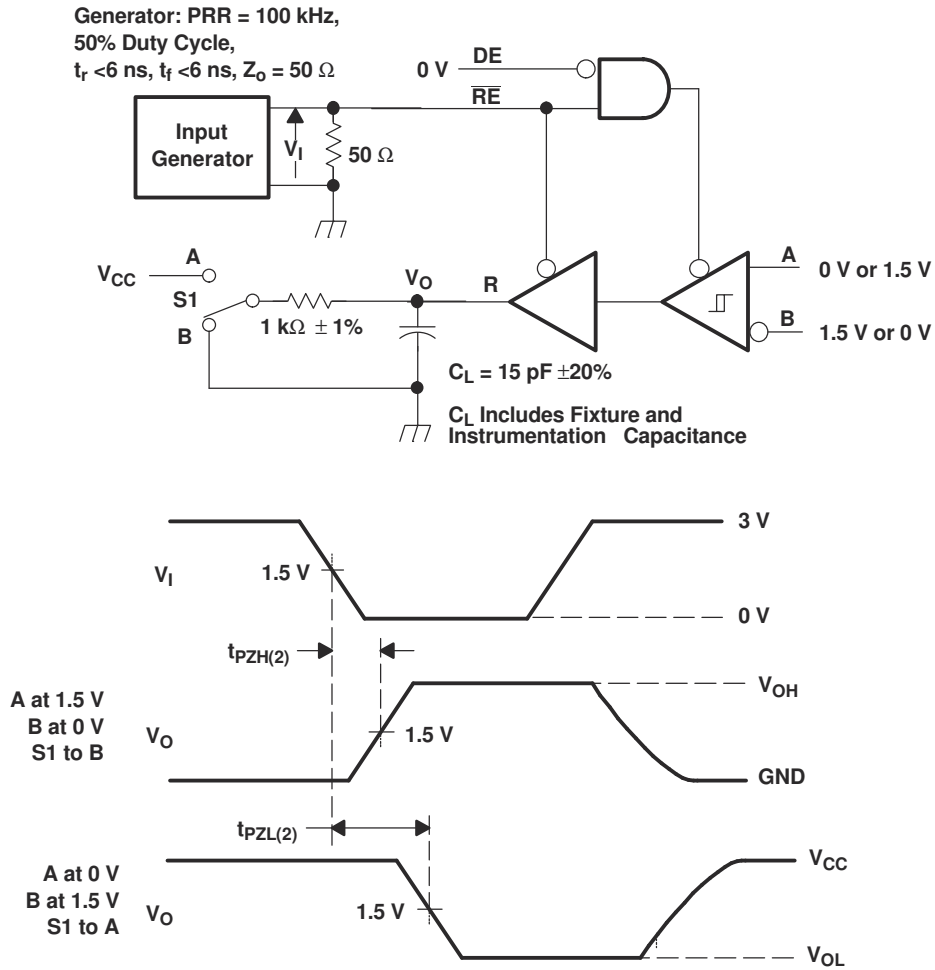


Generator: PRR = 100 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_o = 50 \Omega$

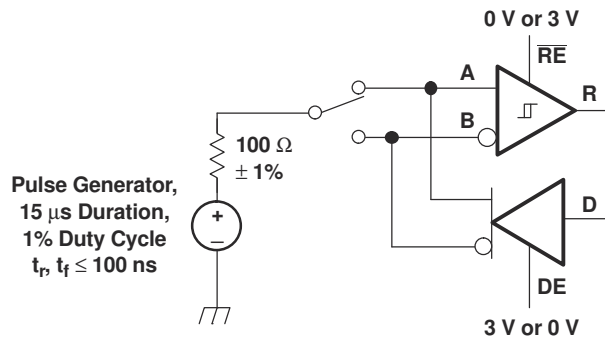
图 6-8. Receiver Switching Test Circuit and Voltage Waveforms



6-9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled



6-10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

6-11. Test Circuit, Transient Over Voltage Test

6 Function Tables

表 6-1. DRIVER

| INPUT | ENABLE | OUTPUTS | |
|-------|--------|---------|---|
| D | DE | A | B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |
| Open | H | H | L |
| X | Open | Z | Z |

表 6-2. RECEIVER

| DIFFERENTIAL INPUTS ⁽¹⁾ | ENABLE | OUTPUT |
|---|--------|--------|
| $V_{ID} = V_A - V_B$ | RE | R |
| $V_{ID} \leq -0.2\text{ V}$ | L | L |
| $-0.2\text{ V} < V_{ID} < -0.01\text{ V}$ | L | ? |
| $-0.01\text{ V} \leq V_{ID}$ | L | H |
| X | H | Z |
| Open Circuit | L | H |
| Short Circuit | L | H |
| IDLE Bus | L | H |
| X | Open | Z |

(1) H = high level; L = low level; Z = high impedance; X = irrelevant;
 ? = indeterminate

6.1 Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

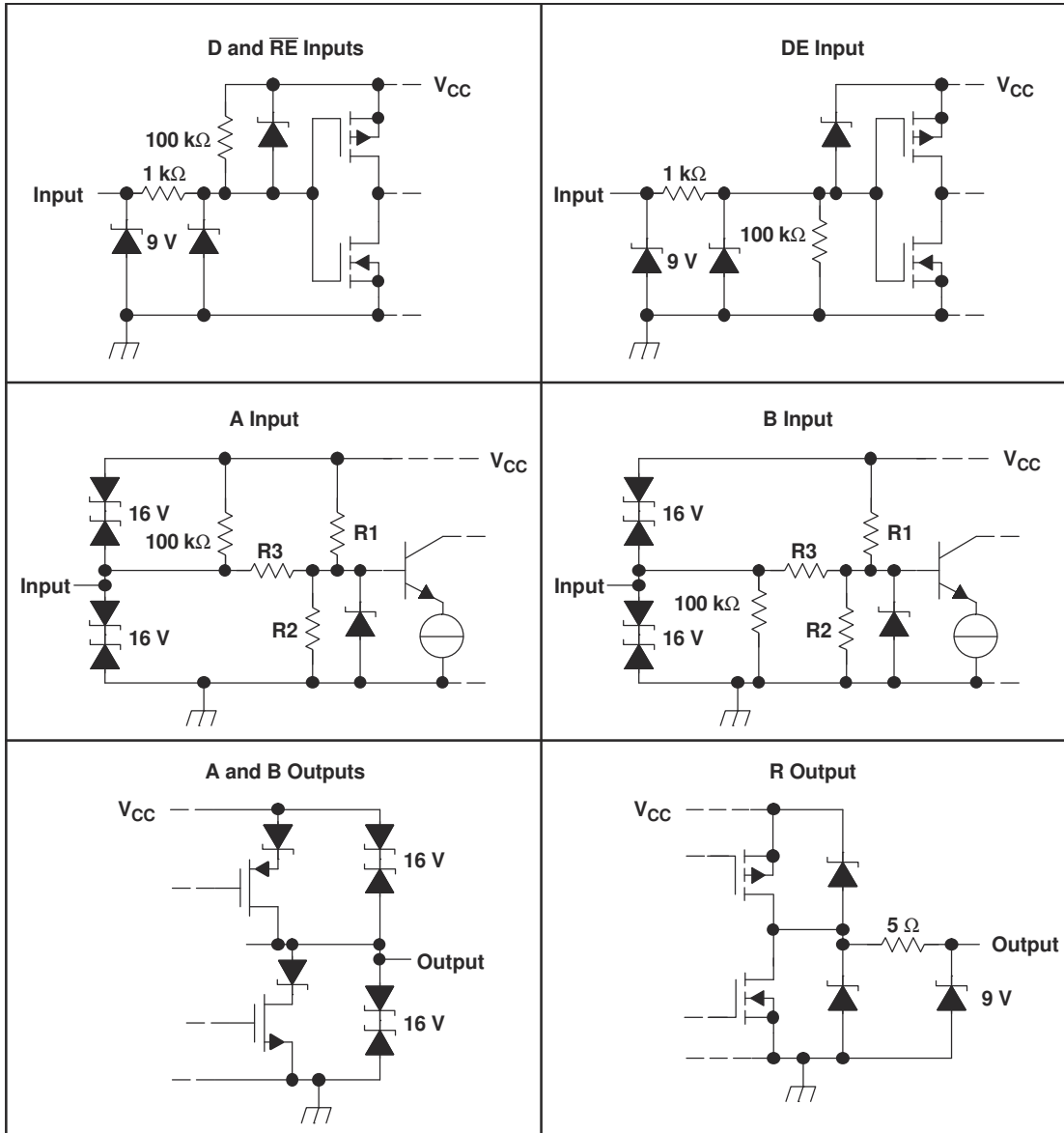
- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output *must* output a High when the differential input V_{ID} is more positive than +200 mV, and *must* output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS} . As seen in the [Receiver Electrical Characteristics](#) table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will *always* cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+} .

7 Equivalent Input and Output Schematic Diagrams



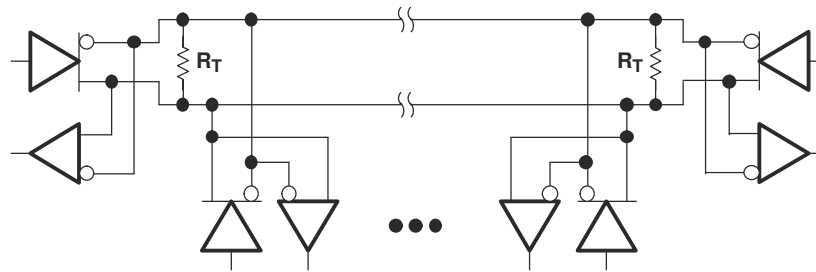
| | R1/R2 | R3 |
|-----------|-------|--------|
| SN65HVD05 | 9 kΩ | 45 kΩ |
| SN65HVD06 | 36 kΩ | 180 kΩ |
| SN65HVD07 | 36 kΩ | 180 kΩ |

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

Typical Application



| Device | Number of Devices on Bus |
|--------|--------------------------|
| HVD05 | 64 |
| HVD06 | 256 |
| HVD07 | 256 |

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_0$).
 Stub lengths off the main line should be kept as short as possible.

☒ 8-1. Typical Application Circuit

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN65HVD05D | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | VP05 | |
| SN65HVD05DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VP05 | Samples |
| SN65HVD05P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | 65HVD05 | Samples |
| SN65HVD06D | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | VP06 | |
| SN65HVD06DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VP06 | Samples |
| SN65HVD06P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | 65HVD06 | Samples |
| SN65HVD07D | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | VP07 | |
| SN65HVD07DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VP07 | Samples |
| SN65HVD07P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | 65HVD07 | Samples |
| SN75HVD05D | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | 0 to 70 | VN05 | |
| SN75HVD05P | OBSOLETE | PDIP | P | 8 | | TBD | Call TI | Call TI | 0 to 70 | 75HVD05 | |
| SN75HVD06D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VN06 | Samples |
| SN75HVD06DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VN06 | Samples |
| SN75HVD07D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VN07 | Samples |
| SN75HVD07DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VN07 | Samples |
| SN75HVD07P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | 75HVD07 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVD05DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD06DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD07DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75HVD06DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75HVD07DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVD05DR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| SN65HVD06DR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| SN65HVD07DR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| SN75HVD06DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| SN75HVD07DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65HVD05P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN65HVD06P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN65HVD07P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75HVD06D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75HVD07D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75HVD07P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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