SN65HVD50, SN65HVD51, SN65HVD52
SN65HVD53, SN65HVD54, SN65HVD55
JAJSPZ5F – SEPTEMBER 2005 – REVISED MARCH 2023

SN65HVD5x 高出力全二重 RS-485 ドライバおよびレシーバ

1 特長

- 1/8 ユニット負荷オプションが使用可能 (バス上に最大 256 ノード)
- 15kV HBM を超えるバス・ピンの ESD 保護
- 1Mbps、5Mbps、25Mbps の信号速度 (1) に対応する、
  ドライバ出力遷移時間オプション
- 1µA 未満の低電流スタンバイ・モード
- グリッチの発生しないパワーアップ / パワーダウン・バス I/O
- バス・アイドル、オープン、短絡回路のフェイルセーフ
- RS-422 および RS485 ネットワーク用に設計
- 3.3V デバイスが利用可能、SN65HVD30-35 [1]

2 アプリケーション

- ユーティリティ・メーター
- シャーシ間相互接続
- DTE/DCE インターフェイス
- 産業用、プロセス、およびビル・オートメーション
- POS 端末とネットワーク

3 概要

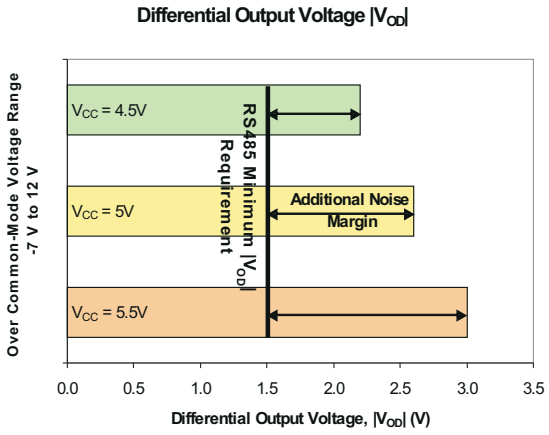
SN65HVD5X デバイスは、5V 電源で動作する 3 ステート差動ライン・ドライバおよび差動入力ライン・レシーバです。各ドライバおよびレシーバは、全二重バス通信設計用に、独立した入力および出力ピンを備えています。これらのデバイスは、平衡伝送ラインと、ANSI TIA/EIA-485A、TIA/EIA-422-B、ITU-T v.11、ISO 8482:1993 標準に準拠したデバイスとの相互運用を目的として設計されています。

SN65HVD50、SN65HVD51、SN65HVD52 デバイスは、外部イネーブル・ピンなしで完全にイネーブルになります。

SN65HVD53、SN65HVD54、SN65HVD55 デバイスは、アクティブ High のドライバ・イネーブルと、アクティブ Low のレシーバ・イネーブルを備えています。ドライバとレシーバの両方をディセーブルにすると、1µA 未満の低いスタンバイ電流が得られます。

これらのデバイスはすべて、-40℃～85℃での動作が規定されています。

SN65HVD5x の高い出力機能により、標準的な RS-485 ドライバよりもノイズ・マージンが大きくなります。ノイズ・マージンが大きくなることにより、長いケーブルや過酷なノイズ環境でもアプリケーションを利用できます。



[1] ラインの信号速度は 1 秒当たりの電圧遷移の回数であり、単位は bps (ビット / 秒) で表記されます。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (October 2009) to Revision F (March 2023) — **Page**

- Changed the *Thermal Characteristics* table ... 11
- Changed the *Typical Characteristics* ... 12

Changes from Revision D (June 2008) to Revision E (October 2009) — **Page**

- 「特長」の箇条書きのテキストを以下のように変更:「3.3V デバイスが利用可能、SN65HVD30-39」から「3.3V デバイスが利用可能、SN65HVD30-35」 ... 1
- データシート全体を通して、SN65HVD56、SN65HVD57、SN65HVD58、SN65HVD59 へのすべての参照を削除. 1
- Deleted RECEIVER EQUALIZATION CHARACTERISTICS from the data sheet ... 4
- Changed scale of 図 7-6 ... 12
- Changed scale of 図 7-7 ... 12
- Added 図 7-11 ... 12
- Changed 図 10-1 ... 22

Changes from Revision C (July 2006) to Revision D (June 2008) — **Page**

- 「特長」の箇条書きのテキストを以下のように変更:「ANSI TIA/EIA-485-A および RS-422 互換の要件を満たす、または超える」から「RS-422 および RS485 ネットワーク用に設計」 ... 1

Changes from Revision B (May 2006) to Revision C (July 2006) — **Page**

- Added 図 7-10 ... 12
- Added 図 7-12 ... 12

Changes from Revision A (February 2006) to Revision B (May 2006) — **Page**

- Added $t_{sk(p)}$ TYP Values ... 8
- Deleted $t_{sk(p)}$ MAX Values ... 8

Changes from Revision * (September 2005) to Revision A (February 2006) **Page**

- 「概要」と図を変更 ... 1
- Changed device SN65HVD50, 51, and 52 SOIC Markings From Preview To 65HVD50, 65HVD51, and 65HVD52 ... 4
- Changed $V_{OD(RING)}$ Max value From 0.05|$V_{OD(SS)}$| To: 10% with the associated note ... 7
- Changed t_r MIN value From: 25 ns To: 20 ns ... 8
- Changed t_f MIN value From: 25 ns To: 20 ns ... 8
- Changed Supply Current - HVD50 MAX value From 8 mA To: 2.7 mA ... 9
- Changed section LOW-POWER SHUTDOWN MODE To: LOW-POWER STANDBY MODE ... 19

5 Available Options

SIGNALING RATE	UNIT LOADS	ENABLES	BASE PART NUMBER	SOIC MARKING
25 Mbps	1/2	No	SN65HVD50	65HVD50
5 Mbps	1/8	No	SN65HVD51	65HVD51
1 Mbps	1/8	No	SN65HVD52	65HVD52
25 Mbps	1/2	Yes	SN65HVD53	65HVD53
5 Mbps	1/8	Yes	SN65HVD54	65HVD54
1 Mbps	1/8	Yes	SN65HVD55	65HVD55

6 Pin Configurations

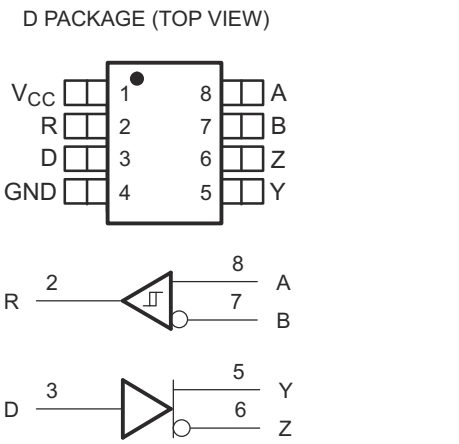


図 6-1. SN65HVD50, SN65HVD51, SN65HVD52

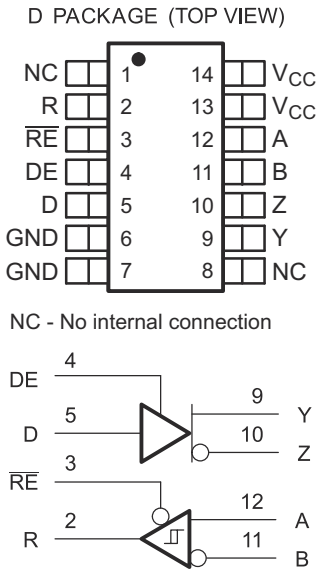


図 6-2. SN65HVD53, SN65HVD54, SN65HVD55

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		UNIT
V_{CC}	Supply voltage range	–0.3 V to 6 V
$V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω. See 図 8-12 (A, B, Y, Z)(3)	–50 to 50 V
V_I	Voltage input range (D, DE, $\overline{RE}$)	-0.5 V to 7 V
$P_{D(cont)}$	Continuous total power dissipation	Internally limited(4)
I_O	Output current (receiver output only, R)	11 mA

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) This tests survivability only and the output state of the receiver is not specified.
(4) The thermal shutdown typically occurs when the junction temperature reaches 165°C.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7(1)		12	
$1/t_{UI}$	Signaling rate	SN65HVD50, SN65HVD53			25	Mbps
		SN65HVD51, SN65HVD54			5	
		SN65HVD52, SN65HVD55			1	
R_L	Differential load resistance		54	60		Ω
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	
V_{ID}	Differential input voltage		-12		12	
I_{OH}	High-level output current	Driver	-60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_J (2)	Junction temperature		–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) See thermal characteristics table for information regarding this specification.

7.3 Electrostatic Discharge Protection

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Human body model	Bus terminals and GND		±16		kV
Human body model(2)	All pins		±4		
Charged-device-model(3)	All pins		±1		

(1) All typical values at 25°C and with a 5-V supply.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

7.4 Driver Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{I(K)}$	Input clamp voltage		I_I = –18 mA		–1.5			V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage		I_O = 0		4		V_{CC}	
			R_L = 54 Ω, See 図 8-1 (RS-485)		1.7	2.6		
			R_L = 100 Ω, See 図 8-1 (RS-422)		2.4	3.2		
			V_{test} = –7 V to 12 V, See 図 8-2		1.6			
$\Delta\|V_{OD(SS)}\|$	Change in magnitude of steady-state differential output voltage between states		R_L = 54 Ω, See 図 8-1 and 図 8-2		–0.2		0.2	
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot		R_L = 54 Ω, C_L = 50 pF, See 図 8-5 See 図 8-3 for definition				10%(2)	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD50, HVD53	See 図 8-4			0.5		
		HVD51, HVD54				0.4		
		HVD52, HVD55				0.4		
$V_{OC(SS)}$	Steady-state common-mode output voltage		See 図 8-4		2.2		3.3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.1		0.1	
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	HVD50, HVD51, HVD52	V_{CC} = 0 V, V_Z or V_Y = 12 V, Other input at 0 V				90	μA
			V_{CC} = 0 V, V_Z or V_Y = –7 V, Other input at 0 V		–10			
		HVD53, HVD54, HVD55	V_{CC} = 5 V or 0 V, DE = 0 V, V_Z or V_Y = 12 V	Other input at 0 V			90	
			V_{CC} = 5 V or 0 V, DE = 0 V, V_Z or V_Y = –7 V		–10			
$I_{Z(S)}$ or $I_{Y(S)}$	Short-circuit output current(3)		V_Z or V_Y = –7 V	Other input at 0 V	–250		250	mA
			V_Z or V_Y = 12 V		–250		250	
I_I	Input current	D, DE			0		100	μA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF

(1) All typical values are at 25°C and with a 5-V supply.
(2) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485
(3) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure may affect device reliability.

7.5 Driver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD50, HVD53	R_L = 54 Ω, C_L = 50 pF, See 図 8-5	4	8	12	ns
		HVD51, HVD54		20	29	46	
		HVD52, HVD55		90	143	230	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD50, HVD53		4	8	12	ns
		HVD51, HVD54		20	30	46	
		HVD52, HVD55		90	143	230	
t_r	Differential output signal rise time	HVD50, HVD53		3	6	12	ns
		HVD51, HVD54		20	34	60	
		HVD52, HVD55		120	197	300	
t_f	Differential output signal fall time	HVD50, HVD53		3	6	11	ns
		HVD51, HVD54		20	33	60	
		HVD52, HVD55		120	192	300	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD50, HVD53			1.4		ns
		HVD51, HVD54			1.6		
		HVD52, HVD55			7.4		
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD50, HVD53			1		ns
		HVD51, HVD54			4		
		HVD52, HVD55			22		
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD53	R_L = 110 Ω, $\overline{RE}$ at 0 V, See 図 8-6 D = 3 V and S1 = Y, D = 0 V and S1 = Z			30	ns
		HVD54				180	
		HVD55				380	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD53				16	ns
		HVD54				40	
		HVD55				110	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD53	R_L = 110 Ω, $\overline{RE}$ at 0 V, See 図 8-7 D = 3 V and S1 = Z, D = 0 V and S1 = Y			23	ns
		HVD54				200	
		HVD55				420	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD53				19	ns
		HVD54				70	
		HVD55				160	
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See 図 8-6 D = 3 V and S1 = Y, D = 0 V and S1 = Z			3300	ns
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See 図 8-7 D = 3 V and S1 = Z, D = 0 V and S1 = Y			3300	ns

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.6 Receiver Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –8 mA				–0.02	V
V_{IT-}	Negative-going differential input threshold voltage		I_O = 8 mA		–0.2			
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})					50		mV
V_{IK}	Enable-input clamp voltage		I_I = –18 mA		–1.5			V
V_O	Output voltage		V_{ID} = 200 mV, I_O = –8 mA, See 図 8-8		4			V
			V_{ID} = –200 mV, I_O = 8 mA, See 図 8-8				0.3	
$I_{O(Z)}$	High-impedance-state output current		V_O = 0 or V_{CC} $\overline{RE}$ at V_{CC}		–1		1	µA
I_A or I_B	Bus input current	HVD50, HVD53,	V_A or V_B = 12 V	Other input at 0 V		0.19	0.3	mA
			V_A or V_B = 12 V, V_{CC} = 0 V			0.24	0.4	
			V_A or V_B = -7 V		–0.35	–0.19		
			V_A or V_B = -7 V, V_{CC} = 0 V		–0.25	–0.14		
		HVD51, HVD52, HVD54, HVD55	V_A or V_B = 12 V	Other input at 0 V		0.05	0.1	mA
			V_A or V_B = 12 V, V_{CC} = 0 V			0.06	0.1	
			V_A or V_B = -7 V		–0.1	–0.05		
			V_A or V_B = -7 V, V_{CC} = 0 V		–0.1	–0.03		
I_{IH}	Input current, $\overline{RE}$		V_{IH} = 2 V		–60			µA
			V_{IL} = 0.8 V		–60			µA
C_{ID}	Differential input capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF
Supply Current								
I_{CC}	Supply current	HVD50	D at 0 V or V_{CC} and No Load				2.7	mA
		HVD51, HVD52					8	
		HVD53	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at 0 V, No load (Receiver enabled and driver disabled)				2.3	
		HVD54, HVD55					2.9	
		HVD53, HVD54, HVD55	$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load (Receiver disabled and driver disabled)			0.08	1	µA
		HVD53	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at V_{CC}, No load (Receiver enabled and driver enabled)				2.7	mA
		HVD54, HVD55					8	
		HVD53	$\overline{RE}$ at V_{CC}, D at 0 V or V_{CC}, DE at V_{CC} No load (Receiver disabled and driver enabled)				2.3	
		HVD54, HVD55					7.7	

(1) All typical values are at 25°C and with a 5-V supply.

7.7 Receiver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD50, HVD53	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See 図 8-9		24	40	ns
		HVD51, HVD52, HVD54, HVD55			43	55	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD50, HVD53			26	35	
		HVD51, HVD52, HVD54, HVD55			47	60	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD50, HVD53				5	
		HVD51, HVD54				7	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD50, HVD53			5		
		HVD51, HVD54			6		
		HVD52, HVD55			6		
t_r	Output signal rise time				2.3	4	
t_f	Output signal fall time				2.4	4	
t_{PHZ}	Output disable time from high level		DE at 3 V, C_L = 15 pF See 図 8-10			17	
t_{PZH1}	Output enable time to high level					10	
t_{PZH2}	Propagation delay time, standby-to-high-level output		DE at 0 V, C_L = 15 pF See 図 8-10			3300	
t_{PLZ}	Output disable time from low level		DE at 3 V, C_L = 15 pF See 図 8-11			13	
t_{PZL1}	Output enable time to low level					10	
t_{PZL2}	Propagation delay time, standby-to-low-level output		DE at 0 V, C_L = 15 pF See 図 8-11			3300	

(1) All typical values are at 25°C and with a 5-V supply
(2) .$t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.8 Thermal Characteristics

over operating free-air temperature range unless otherwise noted(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction−to−ambient thermal resistance	Low-K board	HVD51		230.8		°C/W
			HVD53, HVD54, HVD55, HVD52, HVD50		-		
	Junction−to−ambient thermal resistance	High-K board	HVD51		135.1		
			HVD50, HVD52		116.7		
			HVD53, HVD54, HVD55		93.2		
θ_{JB}	Junction−to−board thermal resistance	High-K board	HVD51		44.4		
			HVD50, HVD52		63.4		
			HVD53, HVD54, HVD55		49.4		
θ_{JC}	Junction−to−case thermal resistance	No board	HVD51		43.5		
			HVD50, HVD52		56.3		
			HVD53, HVD54, HVD55		47.5		
P_D	Device power dissipation	R_L= 60Ω, C_L = 50 pF, Input to D a 50% duty cycle square wave at indicated signaling rate	HVD50 (25Mbps)			420	mW
			HVD51 (10Mbps)			404	
			HVD52 (1Mbps)			383	
		R_L= 60Ω, C_L = 50 pF, DE at V_{CC} $\overline{RE}$ at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate	HVD53 (25Mbps)			420	
			HVD54 (10Mbps)			404	
			HVD55 (1Mbps)			383	
T_A	Ambient air temperature	Low-K board, No airflow	HVD50	–40		55	°C
			HVD51, HVD52	–40		84	
			HVD53, HVD54, HVD55	–40		85	
		High-K board, No airflow	HVD50, HVD51, HVD52	–40		85	
			HVD53, HVD54, HVD55	–40		85	
T_{JSD}	Thermal shutdown junction temperature				165		

(1) See *Application Information* section for an explanation of these parameters.

7.9 Typical Characteristics

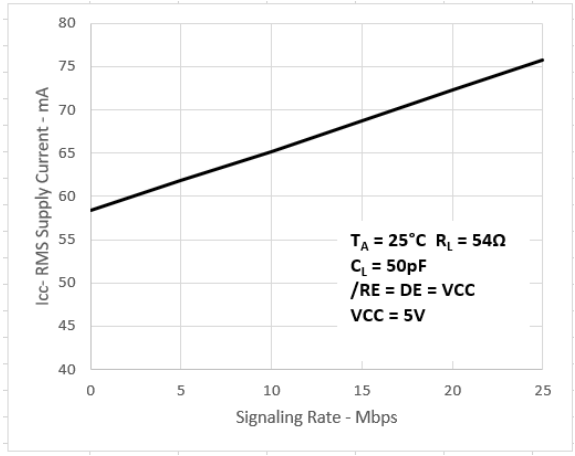


図 7-1. HVD50, HVD53 RMS Supply Current vs Signaling Rate

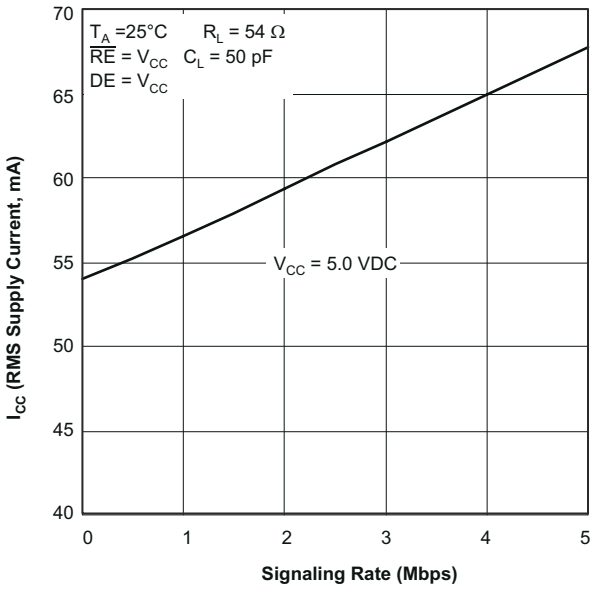


図 7-2. HVD51, HVD54 RMS Supply Current vs Signaling Rate

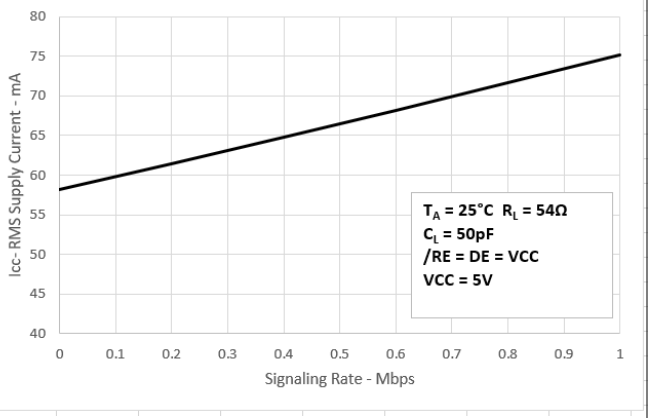


図 7-3. HVD52, HVD55 RMS Supply Current vs Signaling Rate

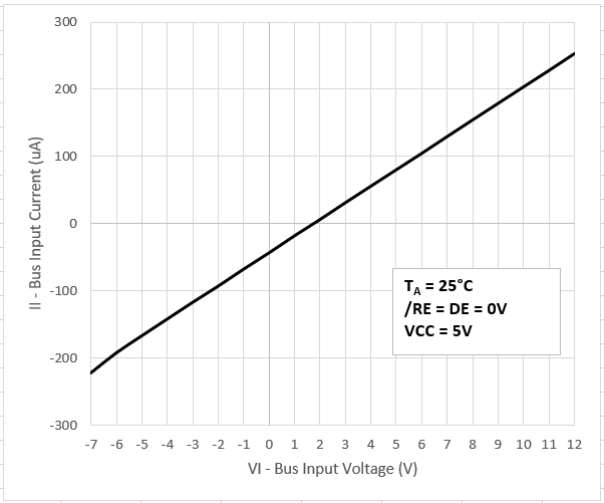


図 7-4. HVD50, HVD53 BUS Input Current vs Input Voltage

7.9 Typical Characteristics (continued)

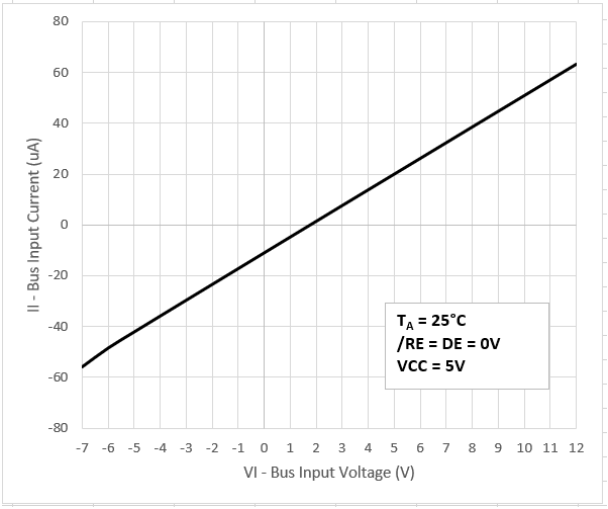


図 7-5. HVD51, HVD52, HVD54, HVD55 BUS Input Current vs Input Voltage

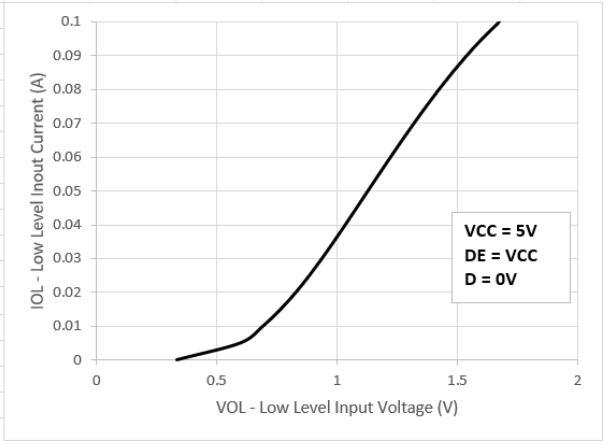


図 7-6. Driver LOW-Level Output Current vs Low-Level Output Voltage

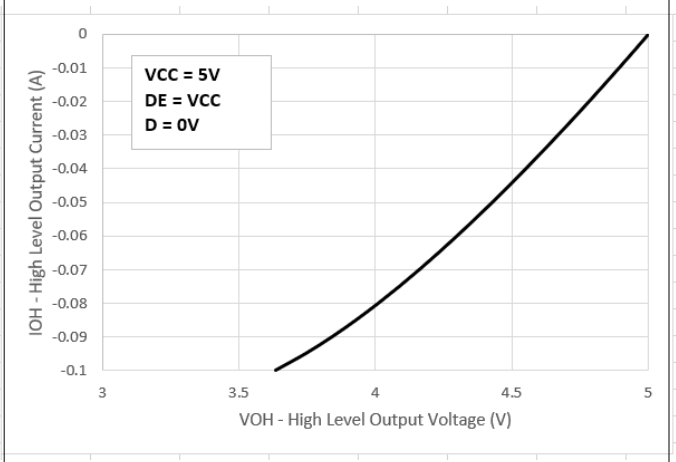


図 7-7. Driver High-Level Output Current vs High-Level Output Voltage

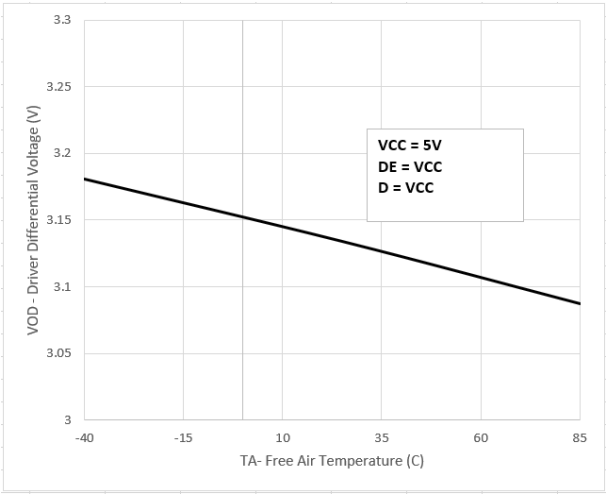


図 7-8. Driver Differential Output Voltage vs Free-Air Temperature

7.9 Typical Characteristics (continued)

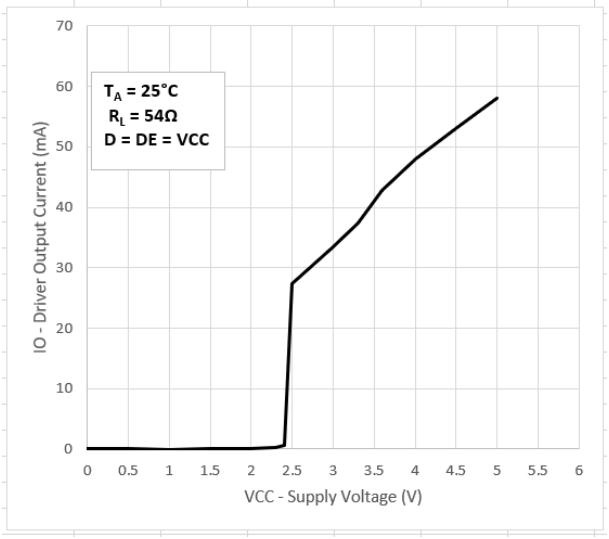


図 7-9. Driver Output Current vs Supply Voltage

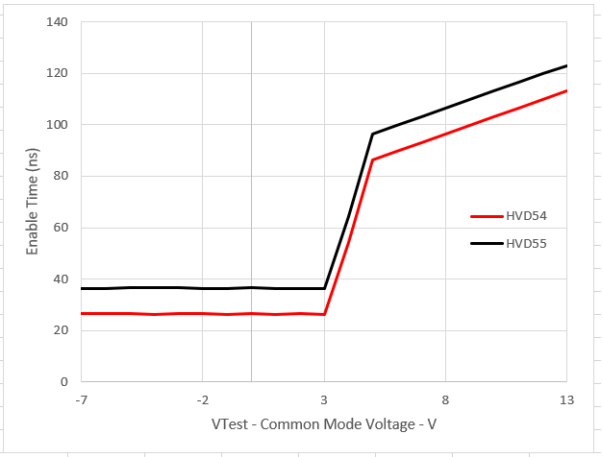


図 7-10. Enable Time vs Common-Mode Voltage (See 図 7-12)

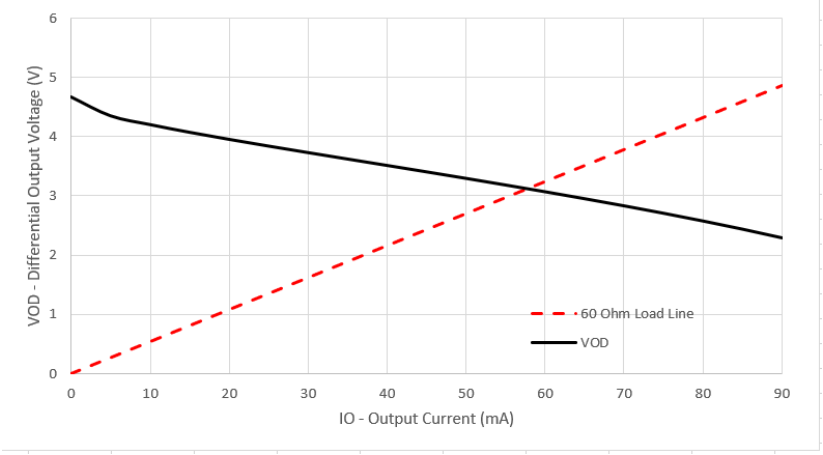
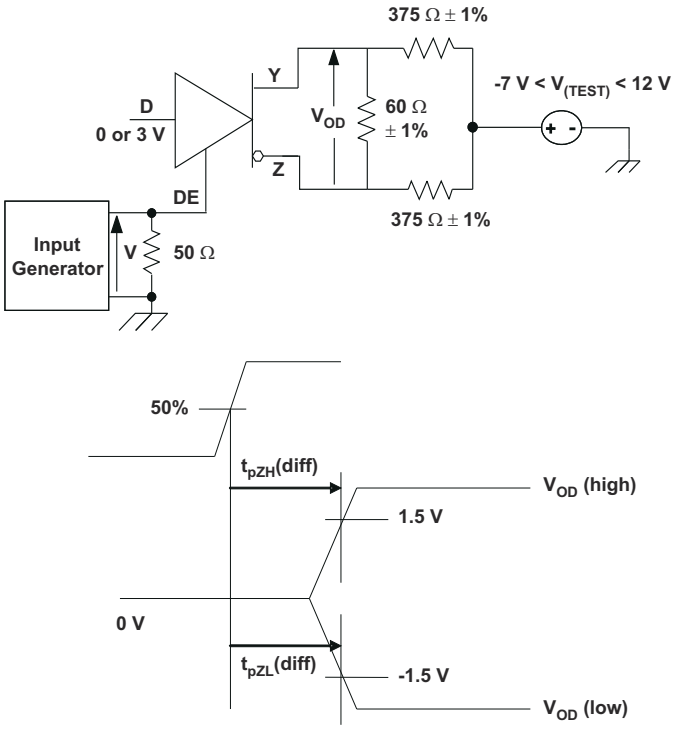


図 7-11. Diferential Output Voltage vs Output Current

7.9 Typical Characteristics (continued)



1. The time $t_{pZL}(x)$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

図 7-12. Driver Enable Time From DE to V_{OD}

8 Parameter Measurement Information

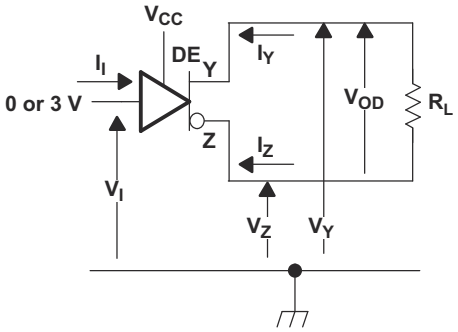


図 8-1. Driver V_{OD} Test Circuit: Voltage and Current Definitions

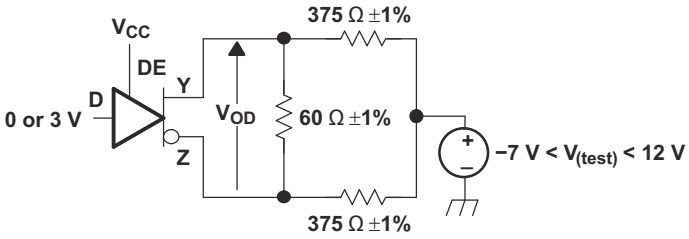


図 8-2. Driver V_{OD} With Common-Mode Loading Test Circuit

$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

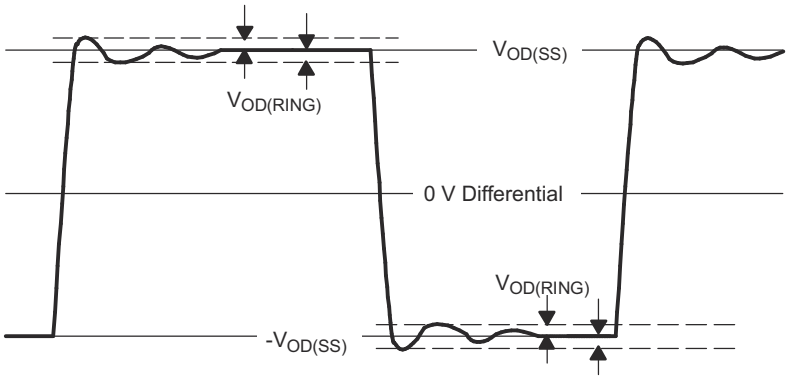
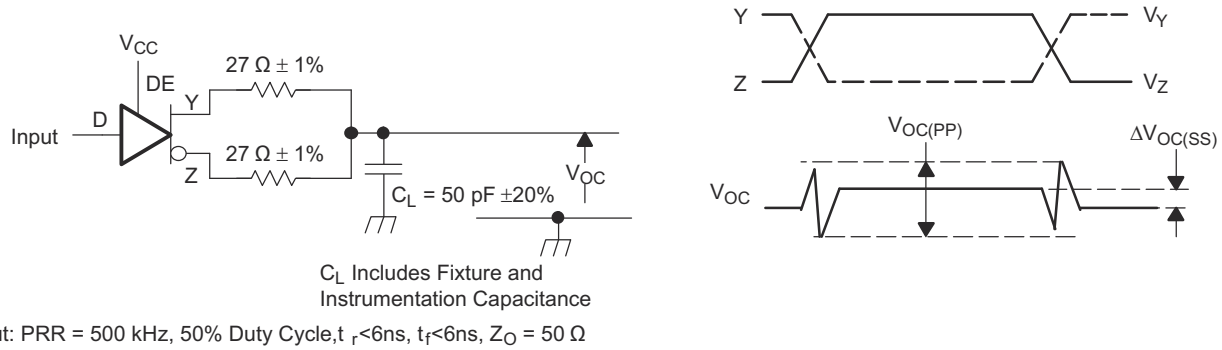
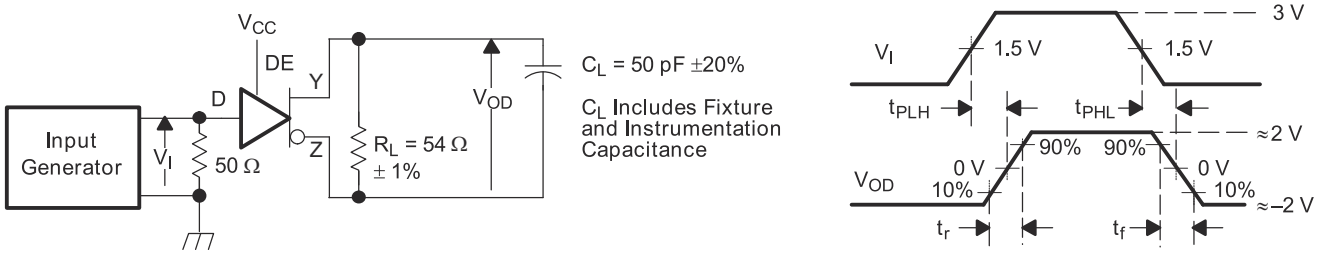


図 8-3. $V_{OD(RING)}$ Waveform and Definitions



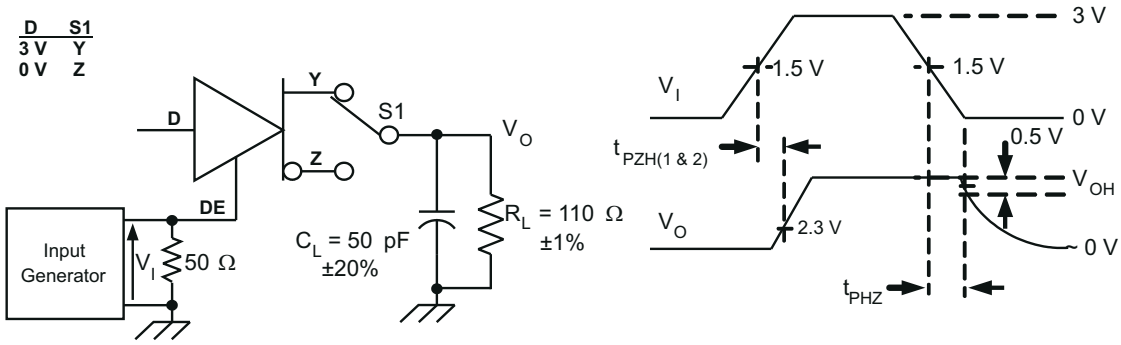
Input: PRR = 500 kHz, 50% Duty Cycle,t_r<6ns, t_f<6ns, Z_O = 50 Ω

図 8-4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



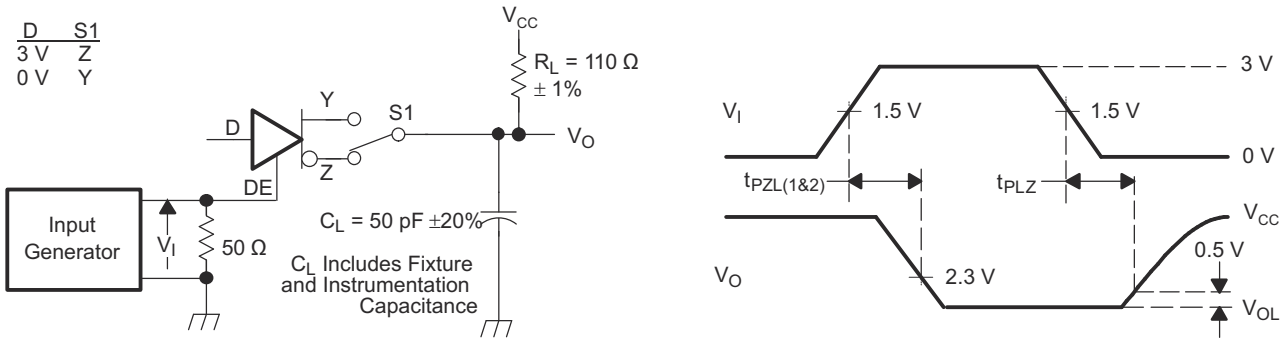
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

図 8-5. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500kHz, 50% Duty Cycle, t_r<6 ns, t_f < 6ns, Z_0 = 50 Ω
C_L Includes Fixture and Instrumentation Capacitance

図 8-6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

図 8-7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

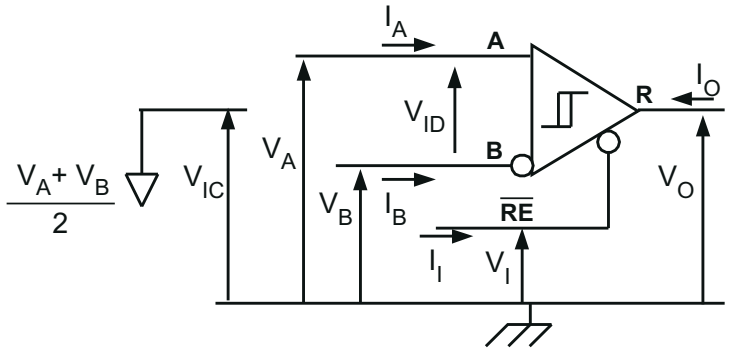


図 8-8. Receiver Voltage and Current Definitions

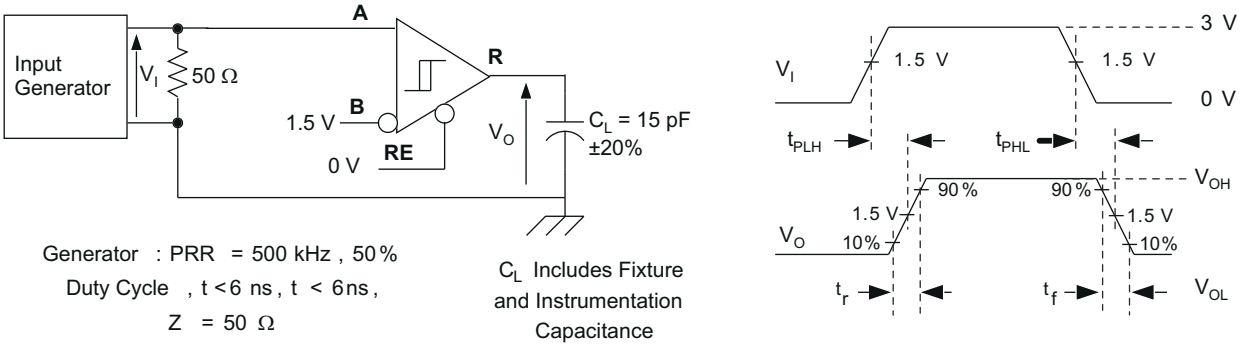
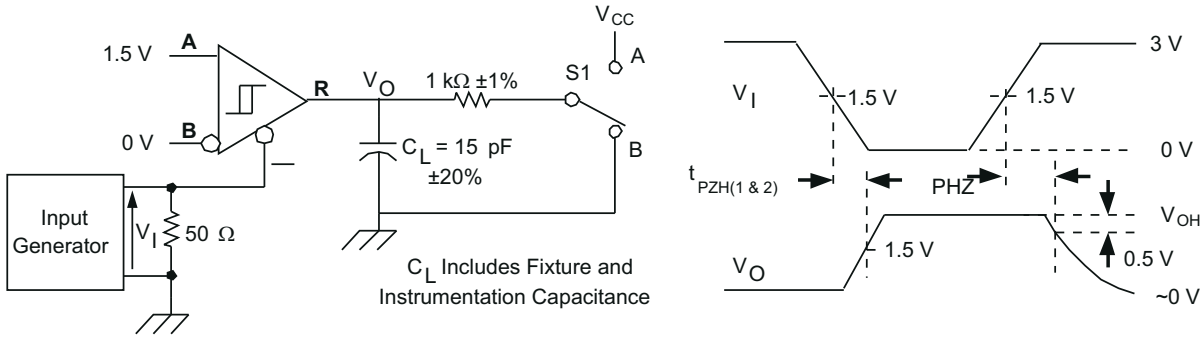
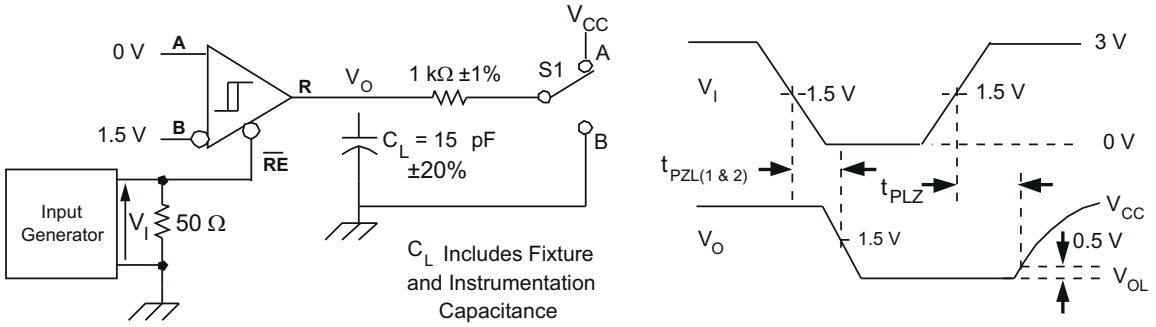


図 8-9. Receiver Switching Test Circuit and Voltage Waveforms



Generator: P_{RR} = 500 kHz, 50%, Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω

図 8-10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: P_{RR} = 500 kHz, 50%, Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω

図 8-11. Receiver Low-Level Enable and Disable Time Test Circuit and Voltage Waveforms

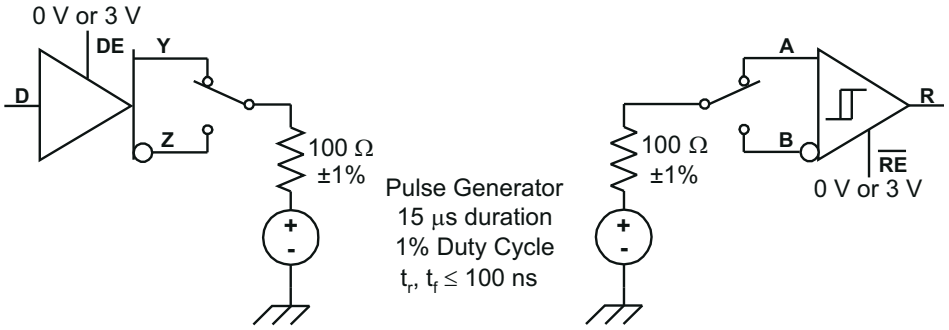


図 8-12. Test Circuit, Transient Overvoltage Test

9 Device Information

9.1 LI-Power Standby Mode

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

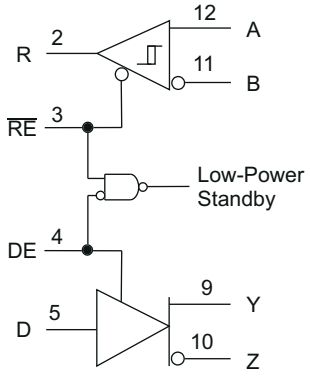


図 9-1. Low-Power Standby Logic Diagram

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by t_{PZH2} and t_{PZL2} in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled ($\overline{RE}$ transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by t_{PZH2} and t_{PZL2} in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

9.2 Function Tables

表 9-1. SN65HVD53, SN65HVD54, SN65HVD55 DRIVER

INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

表 9-2. SN65HVD53, SN65HVD54, SN65HVD55 RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \le -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.02$ V	L	?
-0.02 V $\le V_{ID}$	L	H
X	H or open	Z
Open Circuit	L	H
Idle circuit	L	H
Short Circuit, $V_{(A)} = V_{(B)}$	L	H

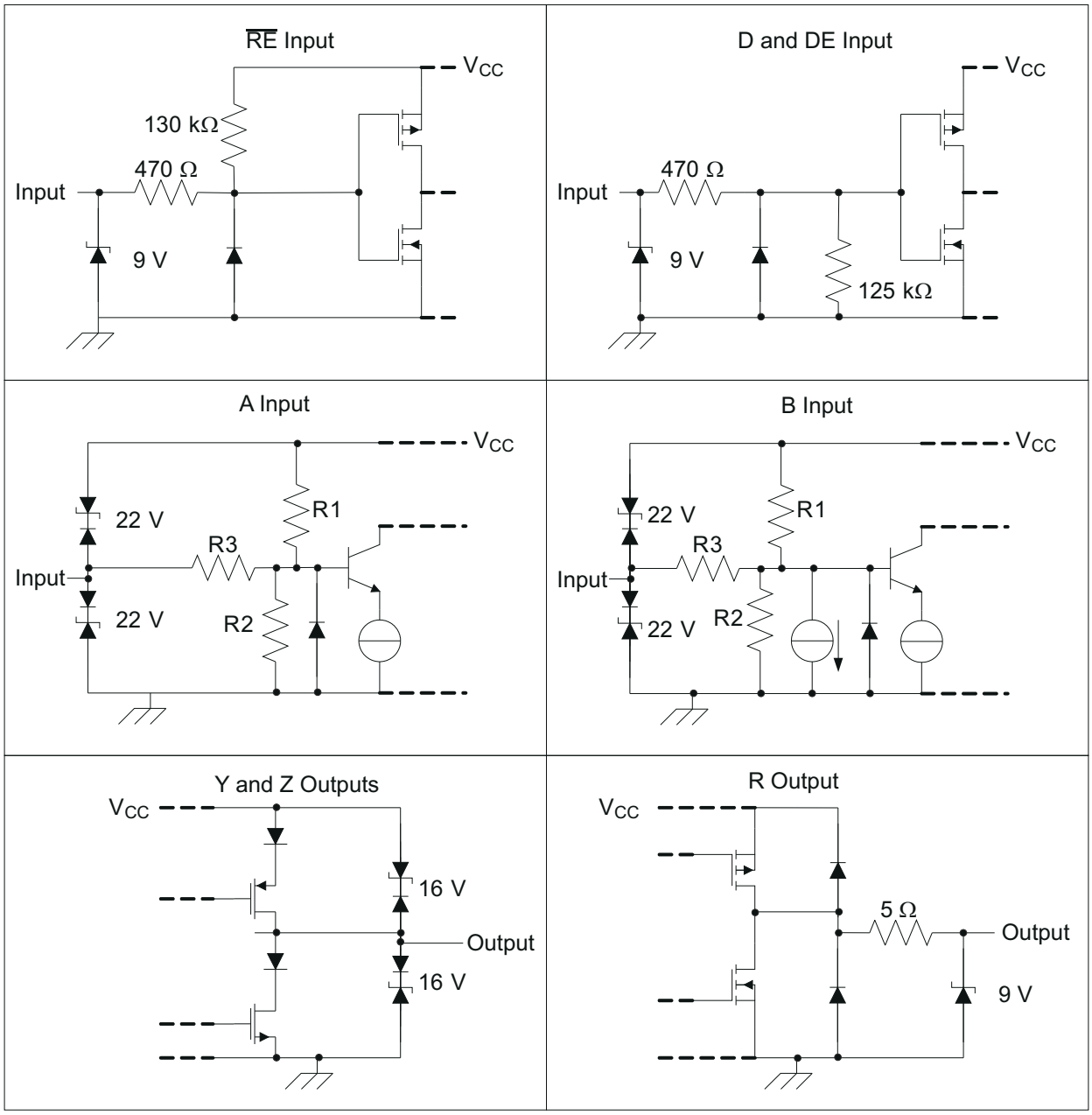
表 9-3. SN65HVD50, SN65HVD51, SN65HVD52 DRIVER

	OUTPUTS	
INPUT D	Y	Z
H	H	L
L	L	H
Open	L	H

表 9-4. SN65HVD50, SN65HVD51, SN65HVD52 RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \le -0.2$ V	L
-0.2 V $< V_{ID} < -0.02$ V	?
-0.02 V $\le V_{ID}$	H
Open Circuit	H
Idle circuit	H
Short Circuit, $V_{(A)} = V_{(B)}$	H

9.3 Equivalent Input and Output Schematic Diagrams



	R1/R2	R3
SN65HVD50, SN65HVD53	9 kΩ	45 kΩ
SN65HVD51, SN65HVD52, SN65HVD54, SN65HVD55	36 kΩ	180 kΩ

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives best *case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see 図 10-1.

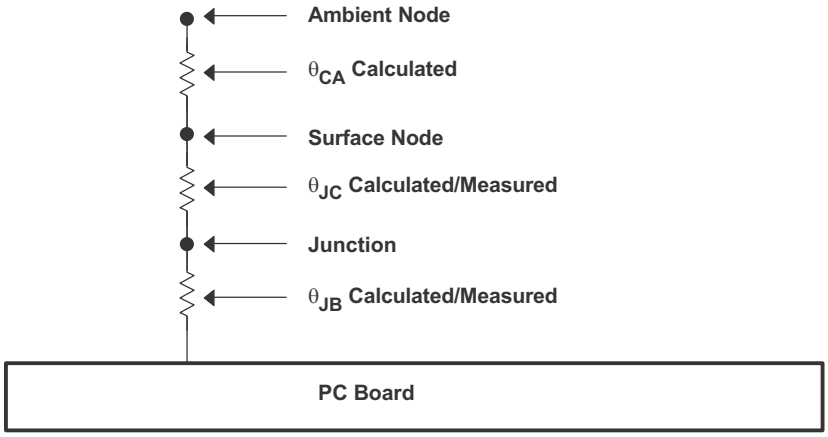


図 10-1. Thermal Resistance

11 Device and Documentation Support

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.3 商標

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD50D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP50	
SN65HVD50DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP50	Samples
SN65HVD51D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP51	
SN65HVD51DR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP51	
SN65HVD52D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP52	
SN65HVD52DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP52	Samples
SN65HVD53D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	65HVD53	
SN65HVD53DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD53	Samples
SN65HVD54DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD54	Samples
SN65HVD55D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	65HVD55	
SN65HVD55DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD55	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

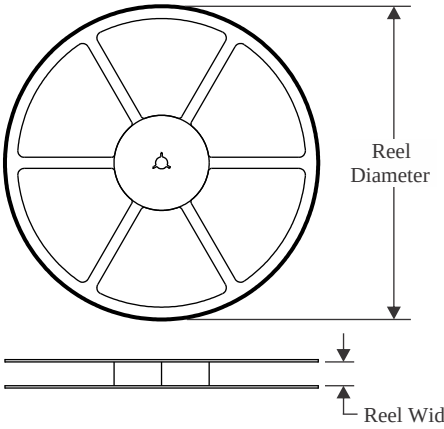
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

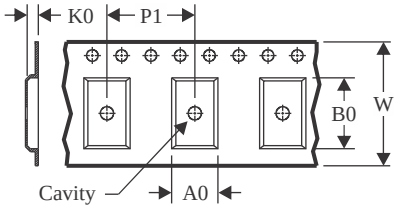
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

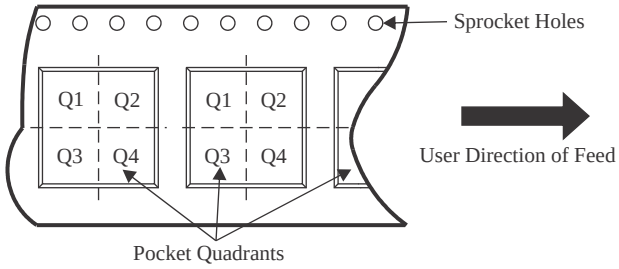


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

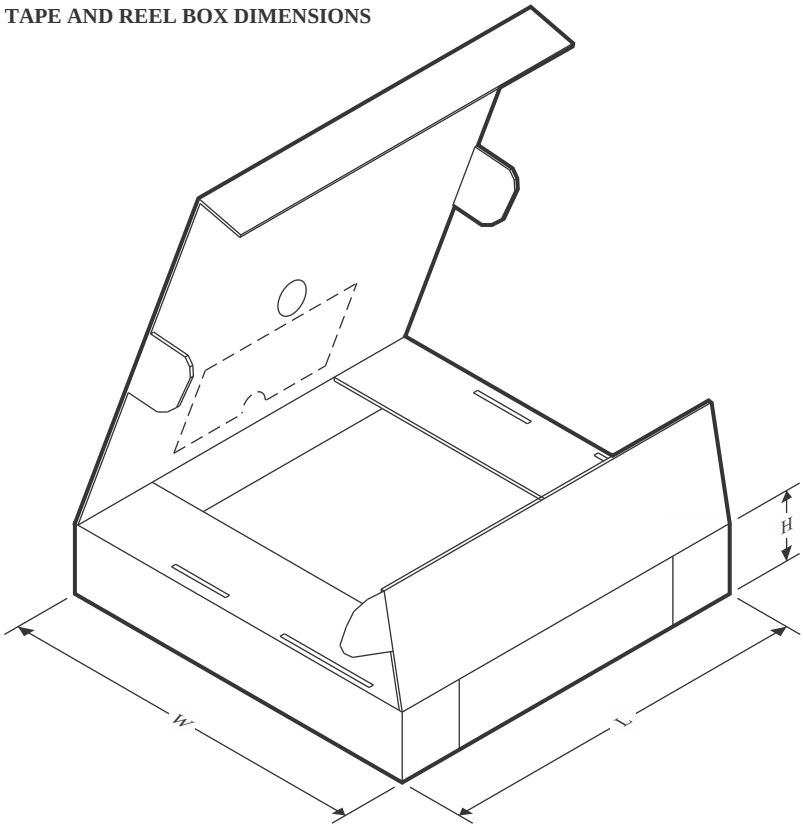
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

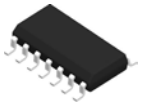
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD52DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD52DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD53DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD54DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD55DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD50DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD50DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD52DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD52DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD53DR	SOIC	D	14	2500	356.0	356.0	35.0
SN65HVD54DR	SOIC	D	14	2500	350.0	350.0	43.0
SN65HVD55DR	SOIC	D	14	2500	356.0	356.0	35.0

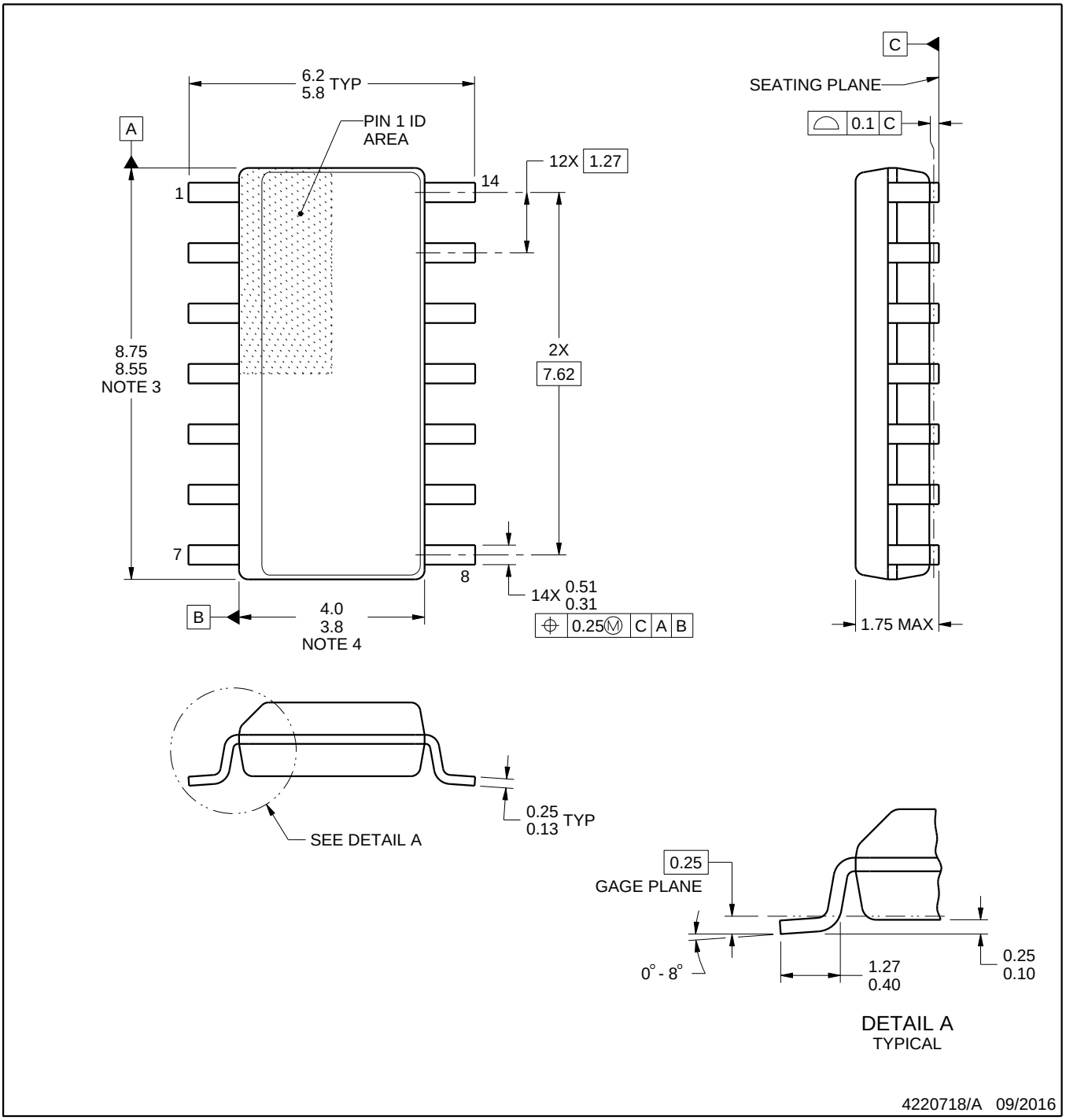


PACKAGE OUTLINE

D0014A

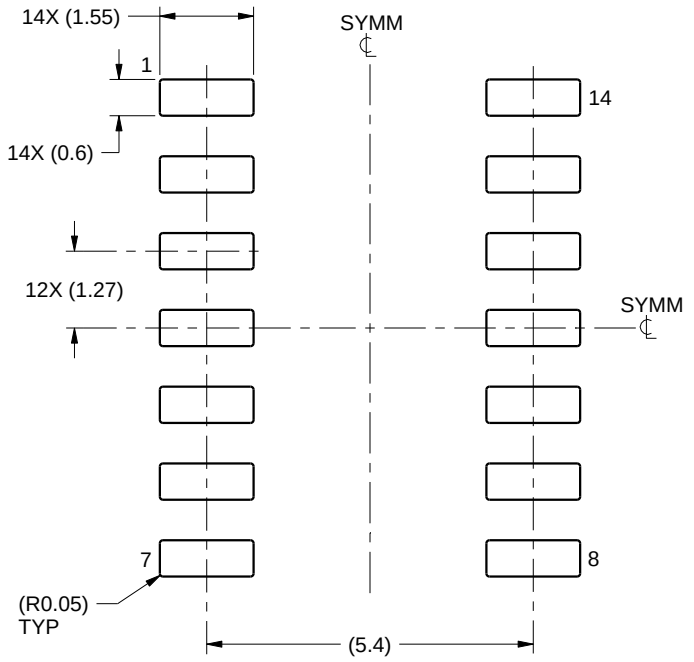
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

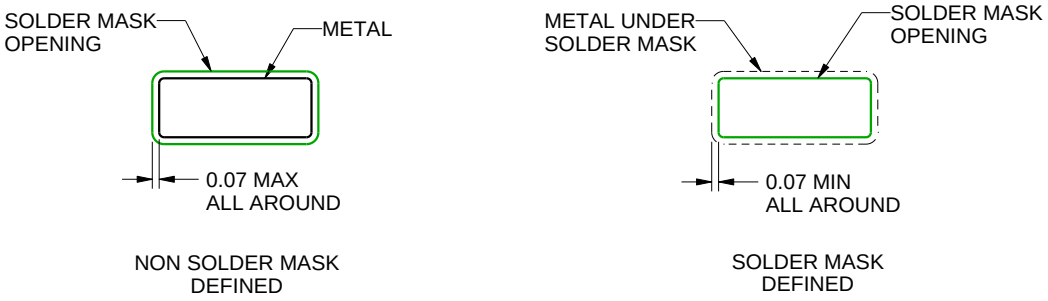


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

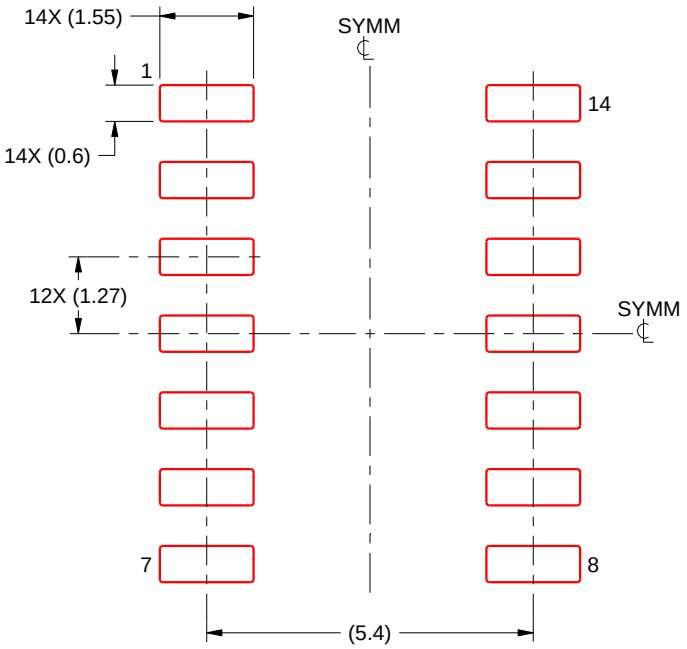
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

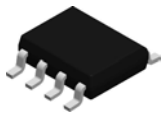


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

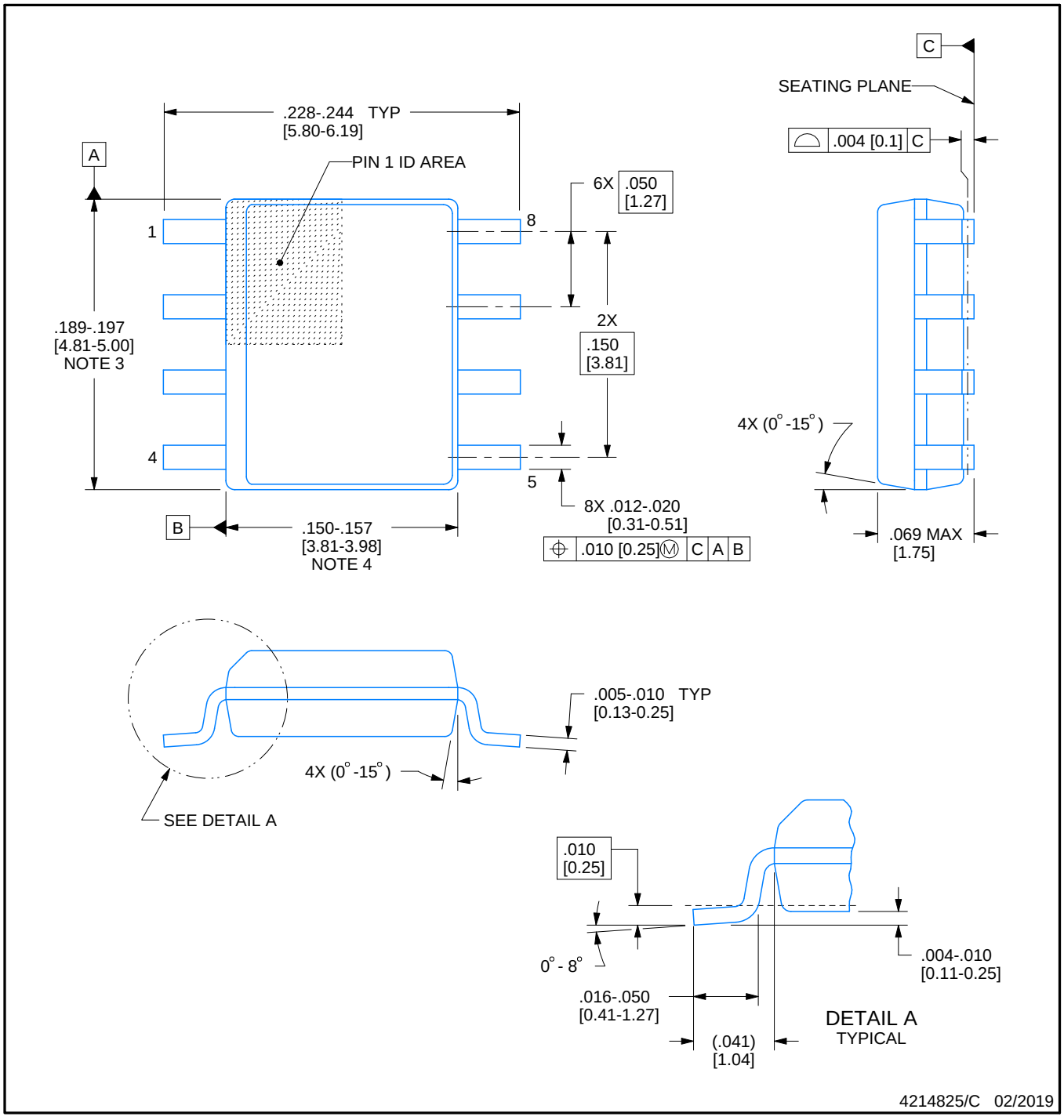


PACKAGE OUTLINE

D0008A

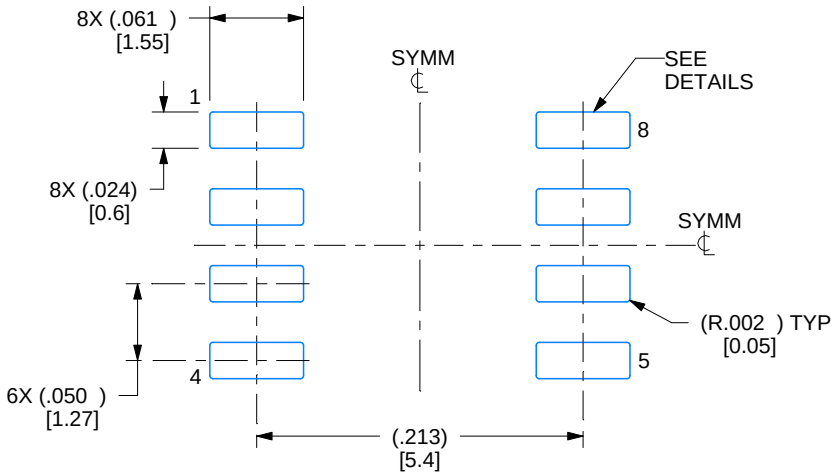
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

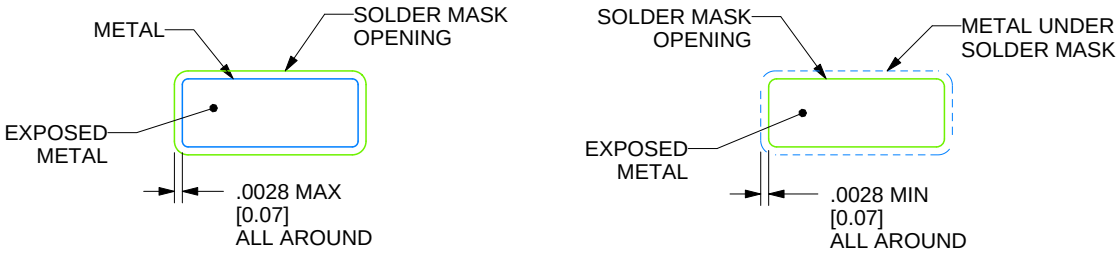


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

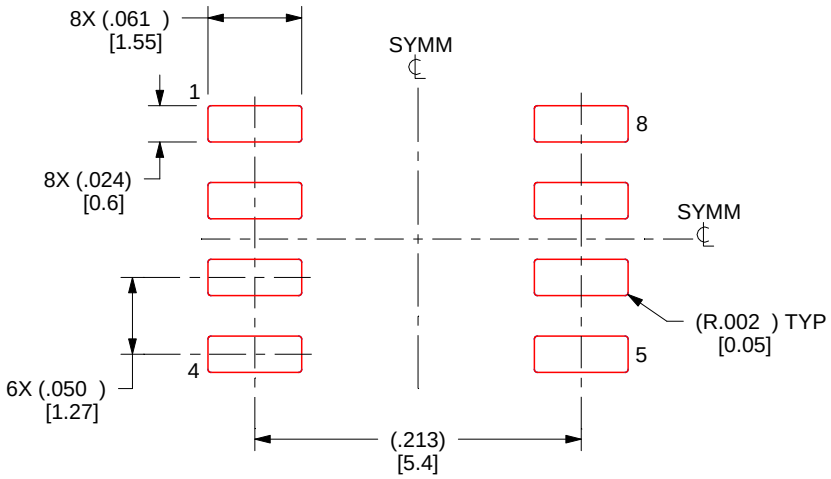
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265