TEXAS INSTRUMENTS
SN65LBC173A-EP
JAJSCO6 – NOVEMBER 2016

# SN65LBC173A-EP クワッドRS-485差動ライン・レシーバ

## 1 特長

- TIA/EIA-485、TIA/EIA-422、ISO 8482アプリケーション用に設計
- 最高50Mbpsの信号速度 (1)
- バスの短絡、開回路、アイドルバス状況に対するフェイルセーフ
- バス入力に対する6kVを超えるESD保護
- 同相バス入力範囲: -7V～12V
- 伝搬遅延時間: 18ns未満
- 低いスタンバイ時消費電力: 32µA未満
- AM26LS32、DS96F173、LTC488、SN75173用のピン互換アップグレード

## 2 アプリケーション

- 防衛、航空宇宙、および医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ/テスト施設
  - 単一の製造施設
  - 長期にわたる製品ライフ・サイクル
  - 製品変更通知の延長
  - 製品のトレーサビリティ

(1) ラインの信号速度とは1秒間の電圧遷移回数であり、bps (Bits Per Second)単位で表されます。

## 3 概要

SN65LBC173Aはクワッド差動ライン・レシーバで、tri-stateの出力を持ち、TIA/EIA-485 (RS-485)、TIA/EIA-422 (RS-422)、ISO 8482 (Euro RS-485)アプリケーション用に設計されています。

このデバイスは、負荷バランスされたマルチポイント・バス通信で、毎秒50メガビットまで、さらにそれ以上のデータ転送速度で使用するよう最適化されています。転送媒体には、より線ペア・ケーブル、プリント基板の導線、バックプレーンを使用できます。データ転送の最高速度および最大距離は、メディアの減衰特性と周囲からのノイズに依存します。

レシーバは、広い範囲の正および負の同相入力電圧で動作し、6kVのESD保護を実現しているため、過酷な環境における高速のマルチポイント・データ転送アプリケーションに適しています。これらのデバイスは LinBiCMOS®を使用して設計されており、低消費電力と堅牢性に貢献しています。

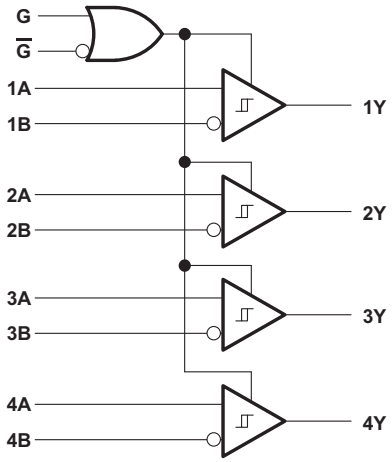
GおよびG̅入力によるイネーブル制御ロジックで、4つのドライバすべてについて正または負のロジックをイネーブルできます。ディセーブルまたは電源オフ時には、レシーバの入力はバスに対して高インピーダンスとなるため、システム負荷が減少します。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| SN65LBC173A-EP | SOIC (16) | 9.90mm×3.90mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**ロジック図**



# 目次

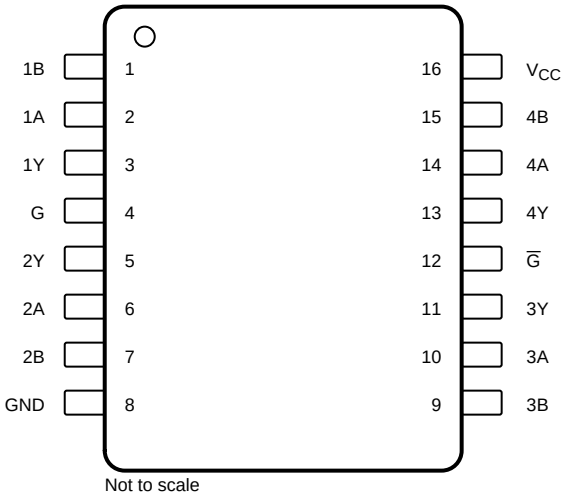


## 4 改訂履歴

| 日付 | 改訂内容 | 注 |
|---|---|---|
| 2016年11月 | * | 初版 |

# 5 Pin Configuration and Functions

**D Package**
**16-Pin SOIC**
**Top View**




Not to scale

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 2 | I | RS-485 differential input (noninverting). |
| 1B | 1 | I | RS-485 differential input (inverting). |
| 1Y | 3 | O | Logic level output. |
| 2A | 6 | I | RS-485 differential input (noninverting). |
| 2B | 7 | I | RS-485 differential input (inverting). |
| 2Y | 5 | O | Logic level output. |
| 3A | 10 | I | RS-485 differential input (noninverting). |
| 3B | 9 | I | RS-485 differential input (inverting). |
| 3Y | 11 | O | Logic level output. |
| 4A | 14 | I | RS-485 differential input (noninverting). |
| 4B | 15 | I | RS-485 differential input (inverting). |
| 4Y | 13 | O | Logic level output. |
| $\overline{G}$ | 12 | I | Active-low select. |
| G | 4 | I | Active-high select. |
| GND | 8 | — | Ground. |
| $V_{CC}$ | 16 | — | Power supply. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$(2) | –0.3 | 6 | V |
| Voltage at any bus input (DC) | –10 | 15 | V |
| Voltage at any bus input (transient pulse through 100 Ω, see 図 10) | –30 | 30 | V |
| Input voltage at G and $\overline{G}$, $V_I$ | –0.5 | $V_{CC}$ + 0.5 | V |
| Receiver output current, $I_O$ | –10 | 10 | mA |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | A and B to GND | ±6000 | V |
| | | | All pins | ±5000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | All pins | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.25 | V |
| | Voltage at any bus terminal | A, B | –7 | | 12 | V |
| $V_{IH}$ | High-level input voltage | G, $\overline{G}$ | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | | 0 | | 0.8 | V |
| | Output current | Y | –8 | | 8 | mA |
| $T_J$ | Junction temperature | | –55 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN65LBC173A-EP D (SOIC) 16 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 78 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 39.5 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 35.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 35.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating conditions

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input voltage threshold | | –7 V ≤ $V_{CM}$ ≤ 12 V ($V_{CM}$ = ($V_A$ + $V_B$ ) / 2) | | | –80 | –10 | mV |
| $V_{IT-}$ | Negative-going differential input voltage threshold | | | | –200 | –120 | | mV |
| $V_{HYS}$ | Hysteresis voltage ($V_{IT+}$ – $V_{IT-}$) | | | | | 40 | | mV |
| VIK | Input clamp voltage | | $I_I$ = –18 mA | | –1.5 | –0.8 | | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 200 mV, $I_{OH}$ = –8 mA | See 図 6 | 2.7 | 4.8 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = –200 mV, $I_{OL}$ = 8 mA | | | 0.2 | 0.4 | V |
| $I_{OZ}$ | High-impedance-state output current | | $V_O$ = 0 V to $V_{CC}$ | | –1 | | 1 | µA |
| $I_I$ | Line input current | | Other input at 0 V, $V_{CC}$ = 0 V or 5 V | $V_I$ = 12 V | | | 0.9 | mA |
| | | | | $V_I$ = –7 V | –0.7 | | | |
| $I_{IH}$ | High-level input current | Enable inputs G, $\overline{G}$ | | | | | 110 | µA |
| $I_{IL}$ | Low-level input current | | | | –100 | | | µA |
| $R_I$ | Input resistance | A, B inputs | | | 12 | | | kΩ |
| $I_{CC}$ | Supply current | | $V_{ID}$ = 5 V | G at 0 V, $\overline{G}$ at $V_{CC}$ | | | 32 | µA |
| | | | No load | G at $V_{CC}$, $\overline{G}$ at 0 V | | 11 | 16 | mA |

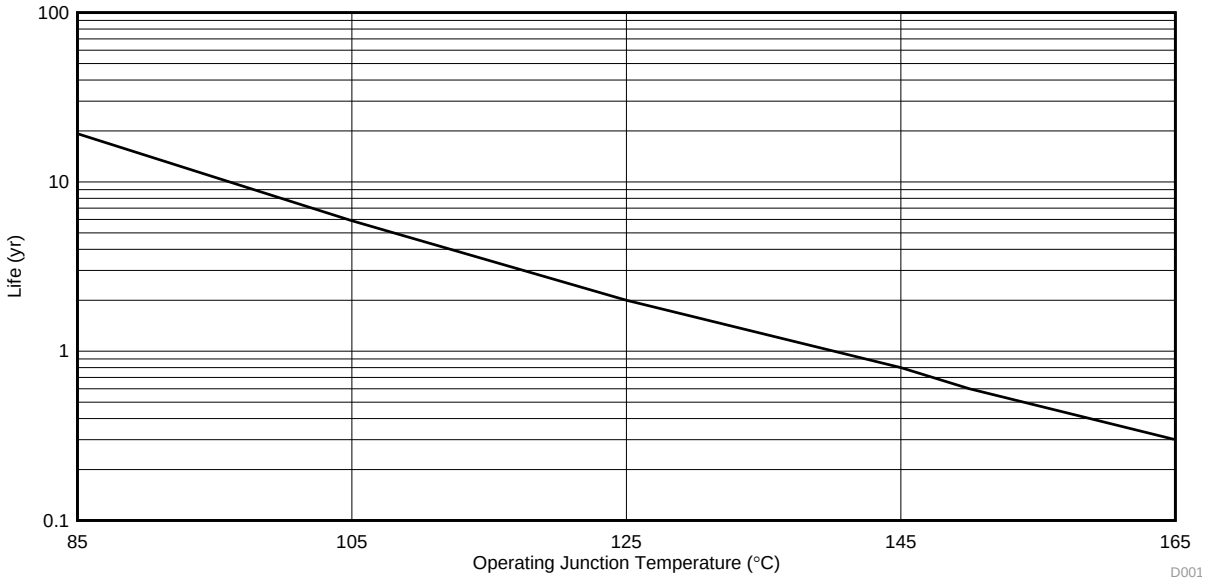
(1) All typical values are at $V_{CC}$ = 5 V and 25°C.

## 6.6 Switching Characteristics

over recommended operating conditions

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Differential output voltage rise time | $V_{ID}$ = –3 V to 3 V, See 図 7 | | 2 | 7 | ns |
| $t_f$ | Differential output voltage fall time | | | 2 | 7 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high level output | | 8 | 12 | 18 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low level output | | 8 | 12 | 18 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | See 図 8 | | 27 | 39 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-output-to-high impedance | | | 7 | 24 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | See 図 9 | | 29 | 39 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-output-to-high impedance | | | 12 | 18 | ns |
| $t_{sk(p)}$ | Pulse skew (\|$t_{PLH}$ – $t_{PHL}$\|) | | | 0.2 | 2 | ns |
| $t_{sk(o)}$ | Output skew(1) | | | | 3 | ns |
| $t_{sk(pp)}$ | Part-to-part skew(2) | | | | 3 | ns |

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.




(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

**図 1. SN65LBC173A-EP Wirebond Life Derating Chart**

## 6.7 Typical Characteristics

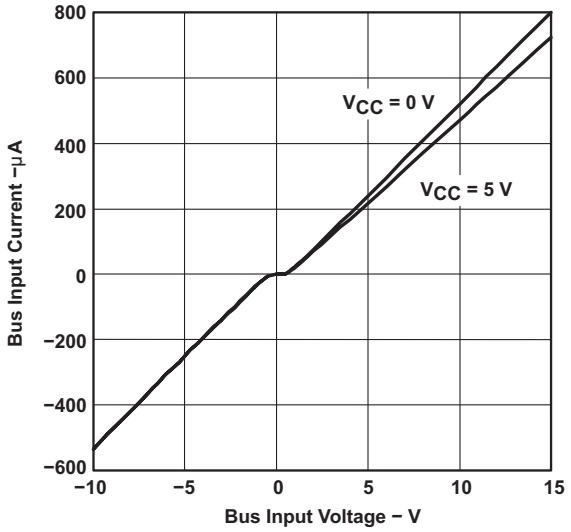



図 2. Bus Input Current vs Bus Input Voltage

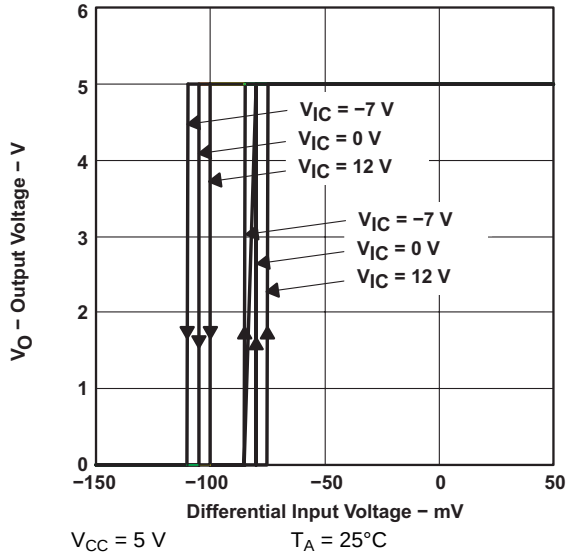



図 3. Output Voltage vs Differential Input Voltage

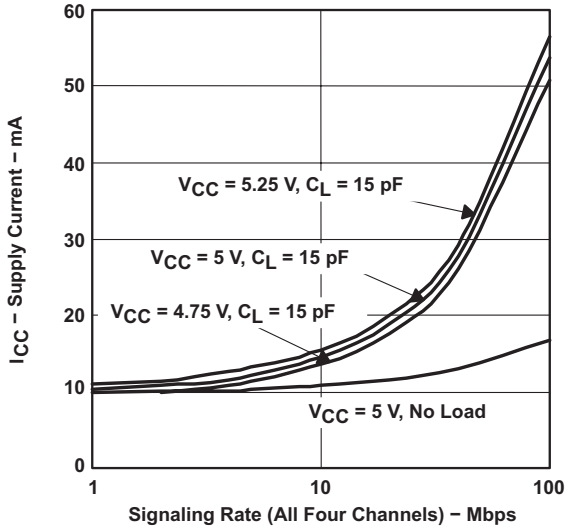



図 4. Supply Current vs Signaling Rate (All Four Channels)

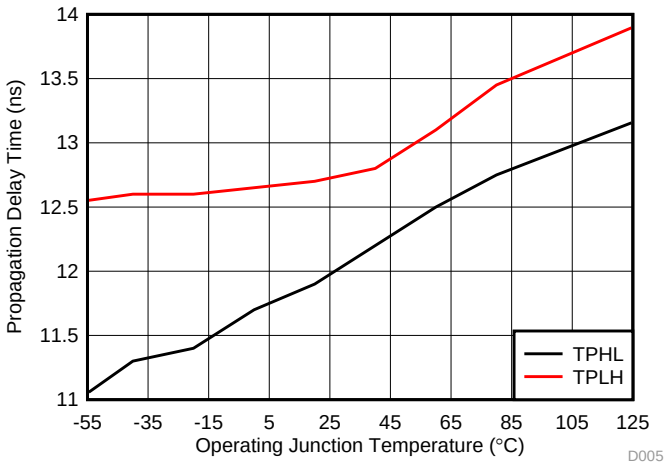



図 5. Propagation Delay Time vs Free-Air Temperature

# 7 Parameter Measurement Information

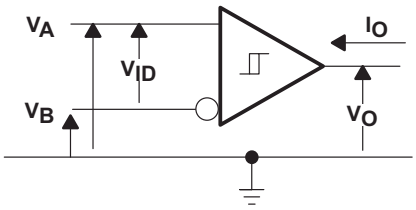
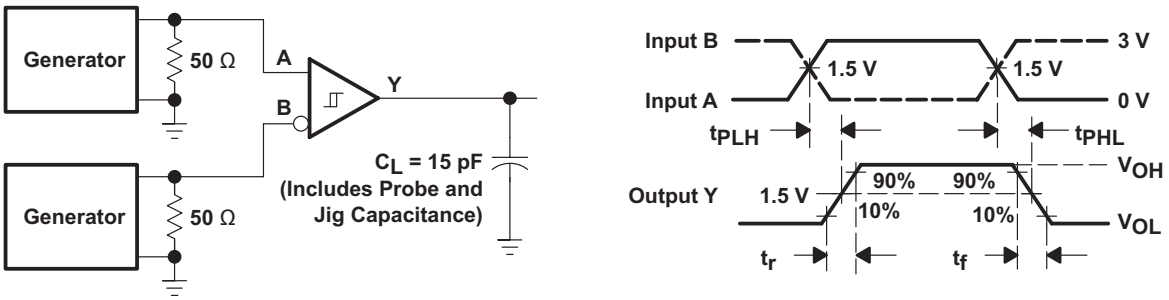
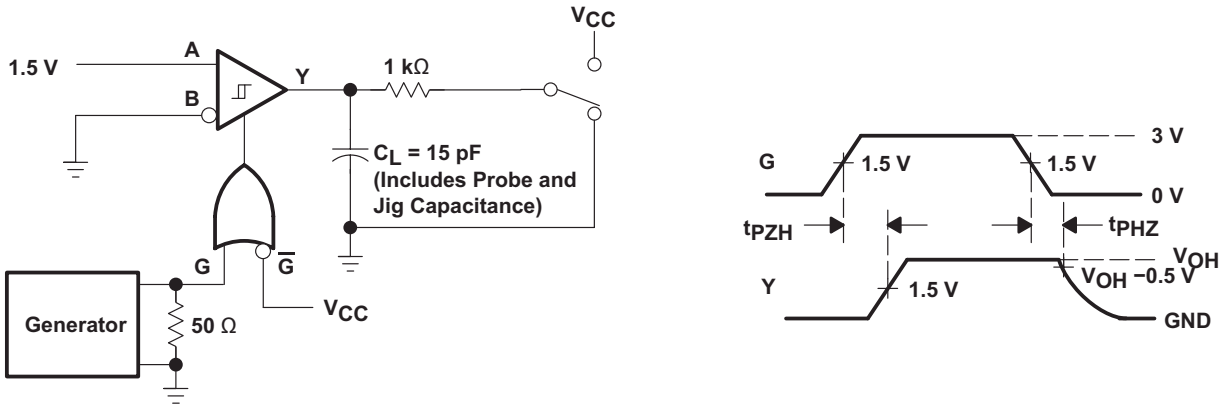



**図 6. Voltage and Current Definitions**




Generators: PRR = 1 MHz, 50% Duty Cycle,
$t_r$ <6 ns, $Z_O$ = 50 Ω

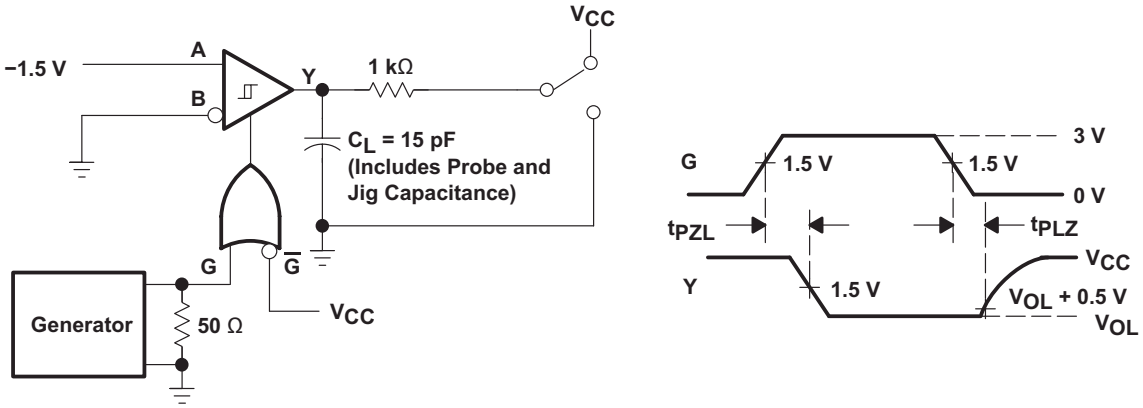
**図 7. Switching Test Circuit and Waveforms**




Generators: PRR = 1 MHz, 50% Duty Cycle,
$t_r$ <6 ns, $Z_O$ = 50 Ω

**図 8. Test Circuit Waveforms, $t_{PZH}$ and $t_{PHZ}$**

## Parameter Measurement Information (continued)




Generators: PRR = 1 MHz, 50% Duty Cycle,
$t_r$ <6 ns, $Z_O$ = 50 Ω

**図 9. Test Circuit Waveforms, $t_{PZL}$ and $t_{PLZ}$**

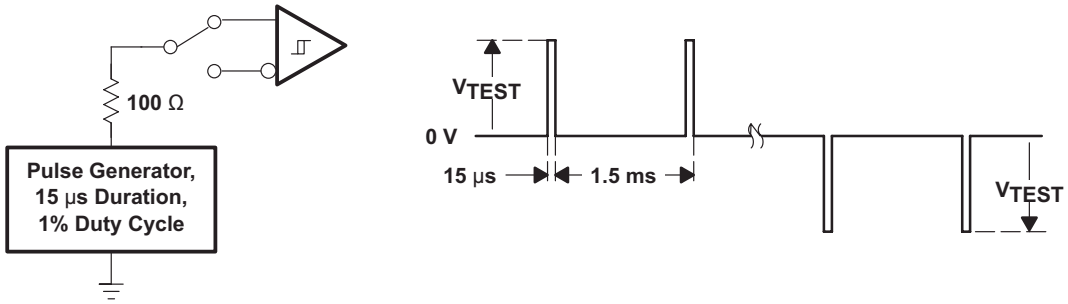



**図 10. Test Circuit and Waveform, Transient Over-Voltage Test**

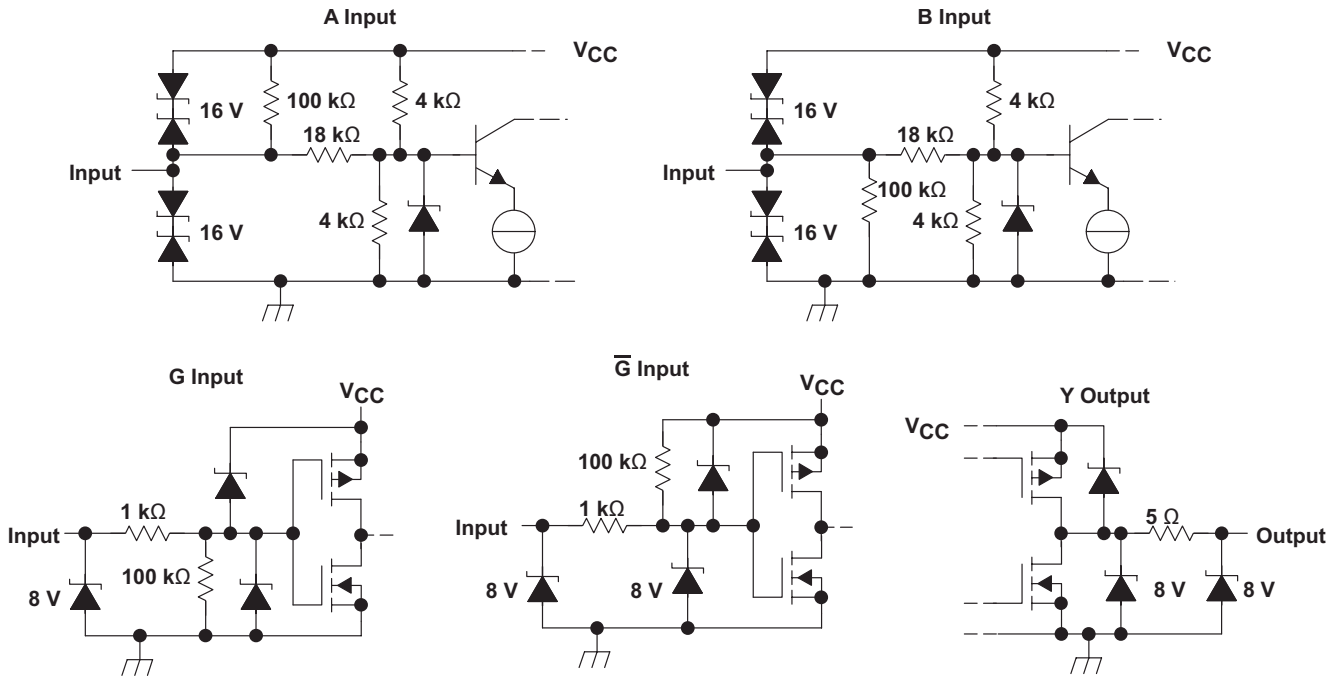



**図 11. Equivalent Input and Output Schematic Diagrams**

# 8 Detailed Description

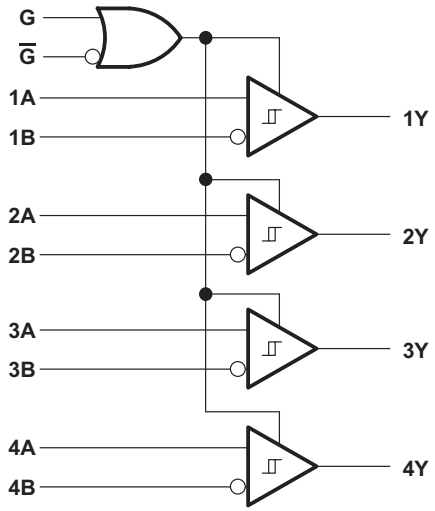
## 8.1 Overview

The SN65LBC173A is a quadruple differential line receiver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications. This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS®, facilitating low-power consumption and robustness.

The G and $\overline{G}$ inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

## 8.2 Functional Block Diagram





## 8.3 Feature Description

The device can be configured using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the $\overline{G}$ enables active low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

## 8.4 Device Functional Modes

The receivers implemented in these RS-485 device can be configured using the G and $\overline{G}$ logic pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

**表 1. Function Table(1)**

| INPUT | ENABLES | | OUTPUT |
|---|---|---|---|
| A - B ($V_{ID}$) | G | $\overline{G}$ | Y |
| $V_{ID} \le -0.2$ V | H | X | L |
| | X | L | |
| $-0.2$ V < $V_{ID}$ < -0.01 V | H | X | ? |
| | X | L | |
| $-0.01$ V ≤ $V_{ID}$ | H | X | H |
| | X | L | |
| X | L | H | Z |
| | OPEN | OPEN | |
| Short circuit | H | X | H |
| | X | L | |
| Open circuit | H | X | H |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

Extending SPI operation over RS-485 link.

## 9.2 Typical Application

The following block diagram shows an MCU host connected via RS-485 to a SPI slave device. This device can be an ADC, DAC, MCU, or other SPI slave peripheral.

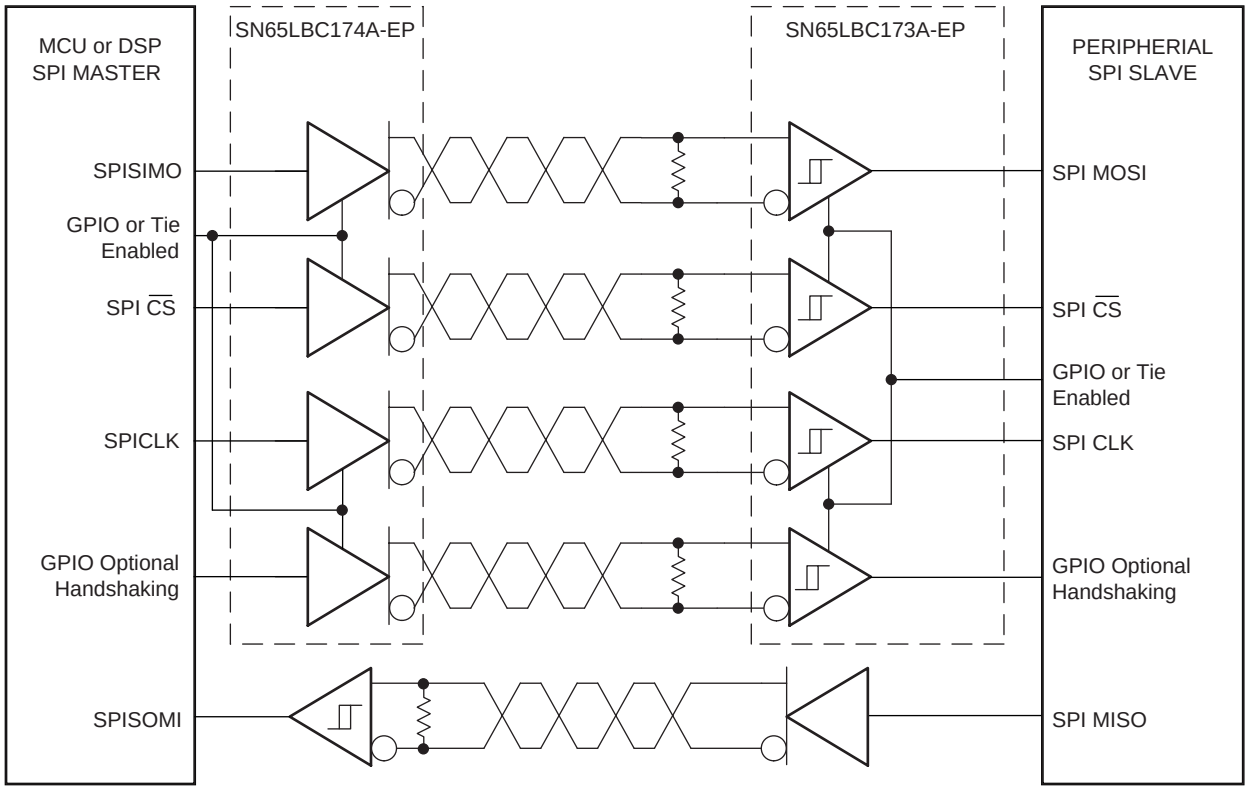





**図 12. DSP-to-DSP Link via Serial Peripheral Interface**

### 9.2.1 Design Requirements

This application can be implemented using standard SPI protocol on DSP or MCU devices. The interface is independent of the specific frame or data requirements of the host or slave device. An additional but not required handshake bit is provided that can be used for customer purposes.

### 9.2.2 Detailed Design Procedure

The interface design requirements are fairly straight forward in this single source/destination scenario. Trace lengths and cable lengths need to be matched to maximize SPI timing. If there is a benefit to put the interface to sleep, GPIOs can be used to control the enable signals of the transmitter and receiver. If GPIOs are not available, or constant uptime needed, both the enables on transmit and receive can be hard tied enabled.

## Typical Application (continued)

The link shown can operate at up to 50 Mbps, well within the capability of most SPI links.

### 9.2.3 Application Curves

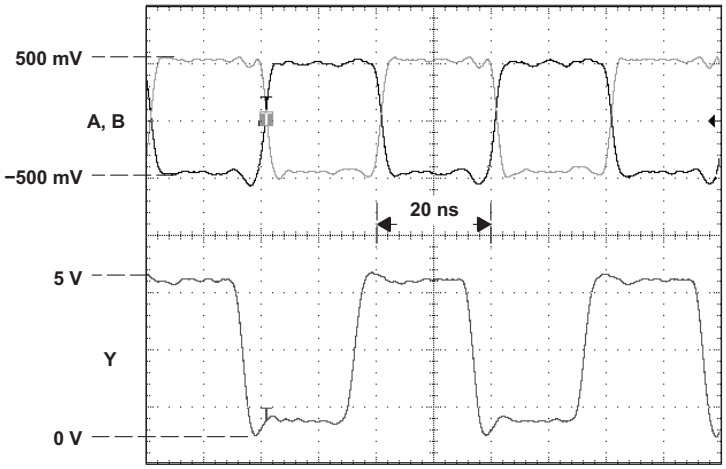



**図 13. Receiver Inputs and Outputs, 50-Mbps Signaling Rate**

# 10 Power Supply Recommendations

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.
- Place termination resistor as close as possible to the input pins (if end point node).
- Keep trace lengths from input pins to buss as short as possible to reduce stub lengths and reflections on any nodes that are not end points of bus.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

## 11.2 Layout Example

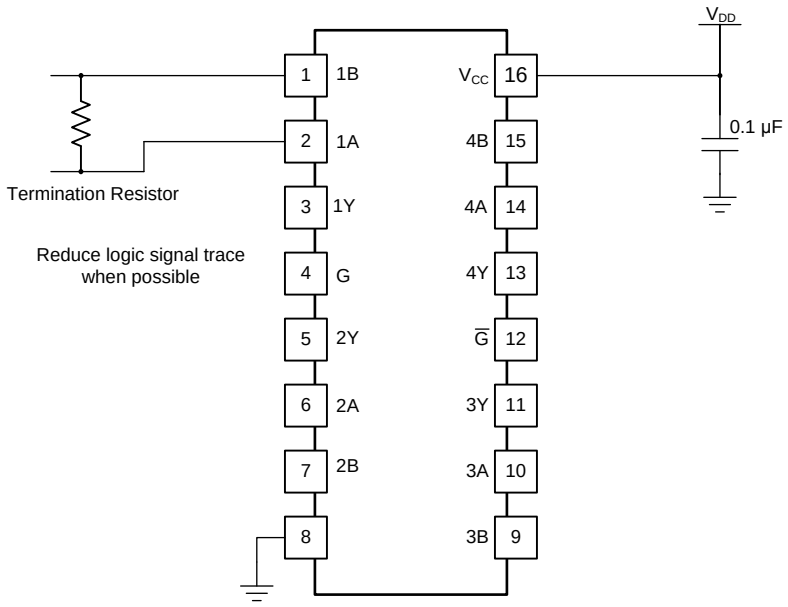



**図 14. Layout with PCB Recommendations**

# 12 デバイスおよびドキュメントのサポート

## 12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある*通知を受け取る*をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**設計サポート** ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 12.3 商標

E2E is a trademark of Texas Instruments.
LinBiCMOS is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 12.5 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC173AMDREP | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LBC173AEP | Samples |
| V62/13623-02XE | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LBC173AEP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

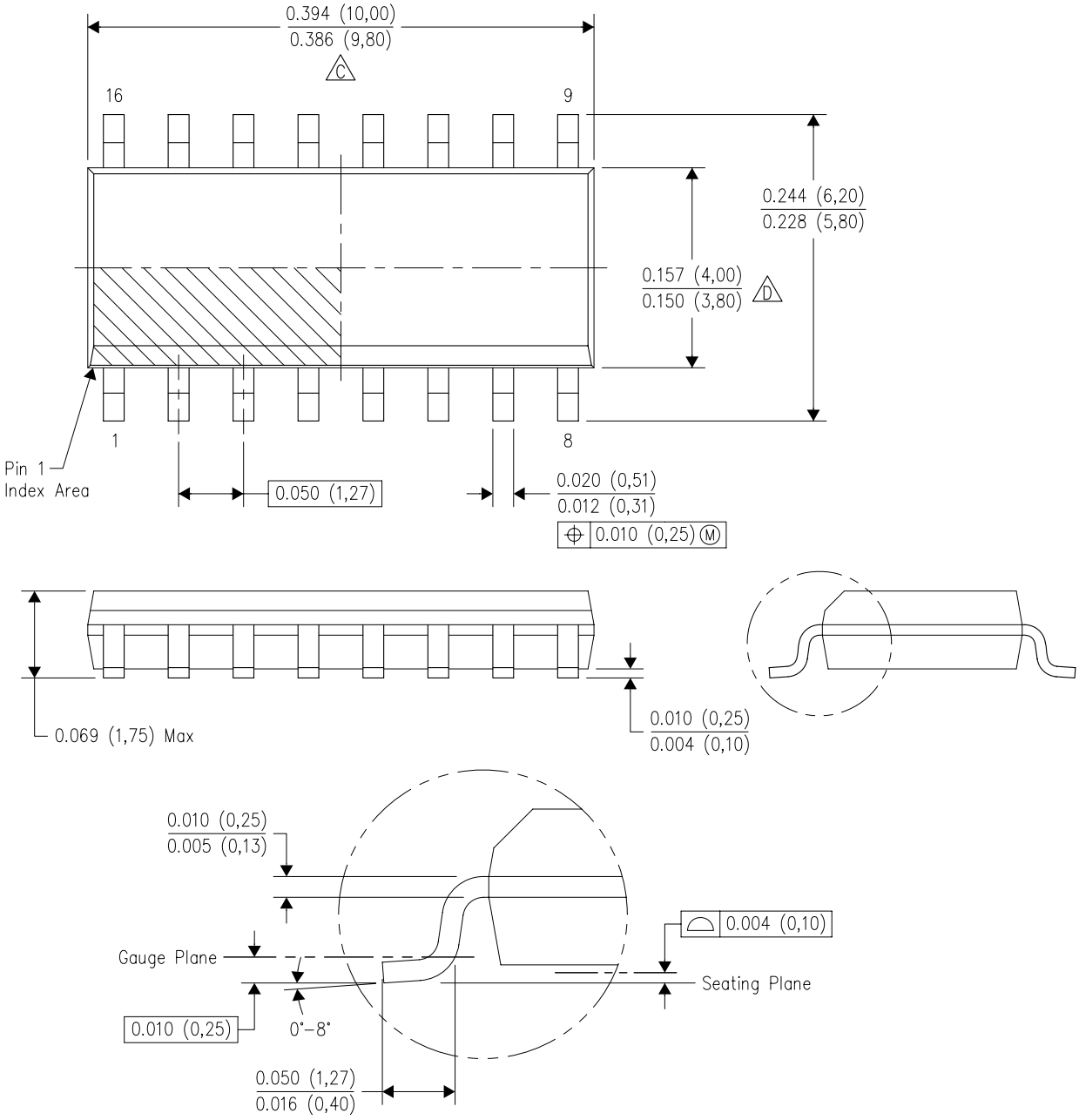
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

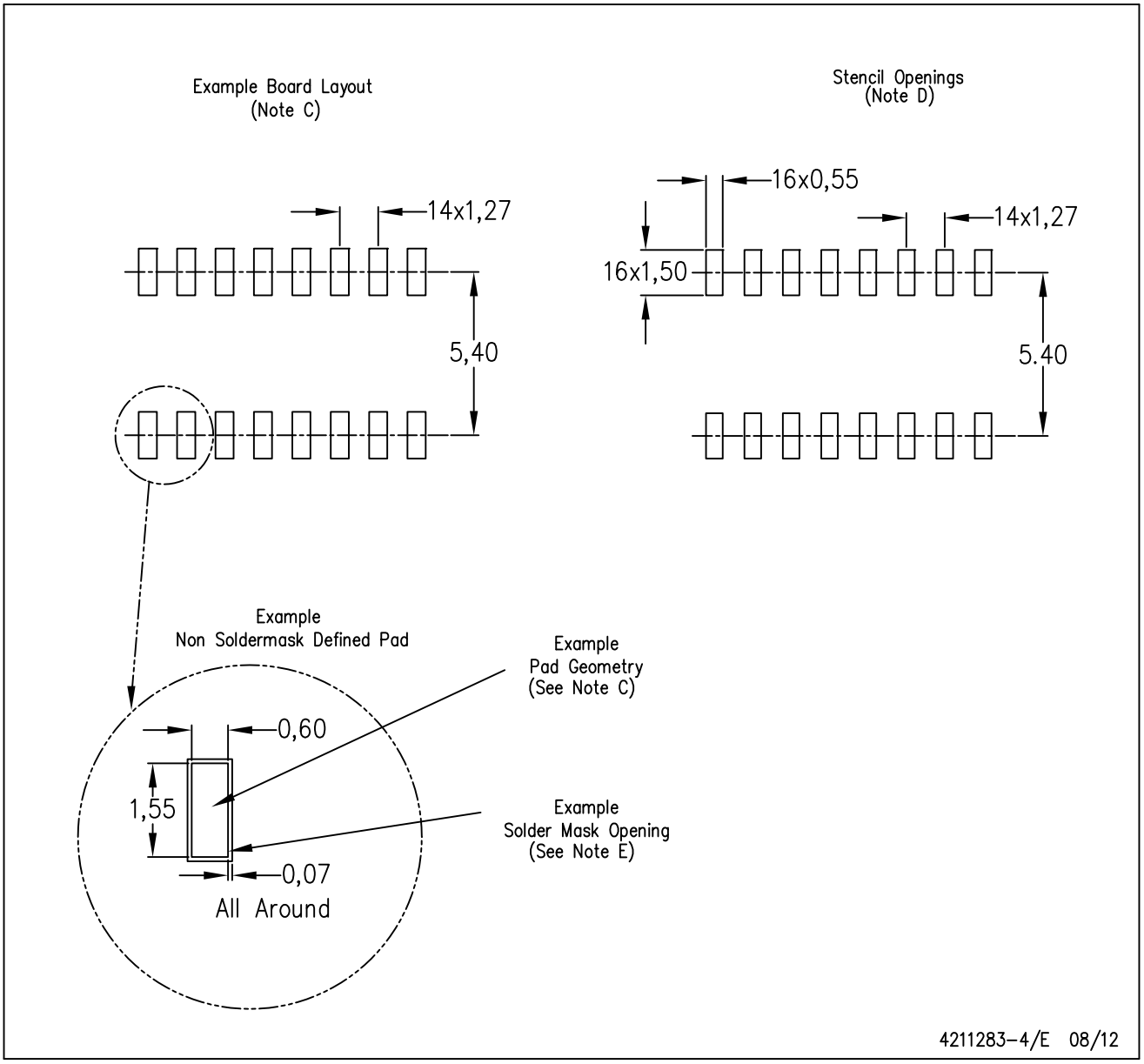
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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