SN65LBC174、SN75LBC174 クワッド、低消費電力差動ライン ドライバ

1 特長

- EIA-485 規格に適合または上回る性能
- ノイズの多い環境の、長いバス ラインでの高速マルチポイント伝送用に設計
- 毎秒最大 1,000 万転送以上のデータレートをサポート
- 同相入力電圧範囲：-7V～12V
- 正と負の電流制限
- 低消費電力：最大 1.5mA (出力ディセーブル)
- SN75174 との機能互換性

2 アプリケーション

- 化学およびガス センサ
- フィールド トランスミッタ：温度センサおよび圧力センサ
- モータ駆動：ブラシレス DC およびブラシ付き DC
- Modbus 使用の温度センサおよびコントローラ

3 概要

SN65LBC174 および SN75LBC174 は、3 ステート出力のモノリシック クワッド差動ライン ドライバです。どちらのデバイスも、米国電子工業会の規格 EIA-485 の要件を満たすように設計されています。これらのデバイスは、最大で毎秒 10 メガビット、さらにそれ以上のデータ転送速度での平衡マルチポイント バス伝送用に最適化されています。各ドライバは、広い正および負の同相出力電圧範囲、電流制限、サーマルシャットダウン保護機能を備えており、ノイズの多い環境でのパーティライン アプリケーションに適しています。これらのデバイスは LinBiCMOS™ を使用して設計されており、低消費電力と本質的な堅牢性を実現しています。

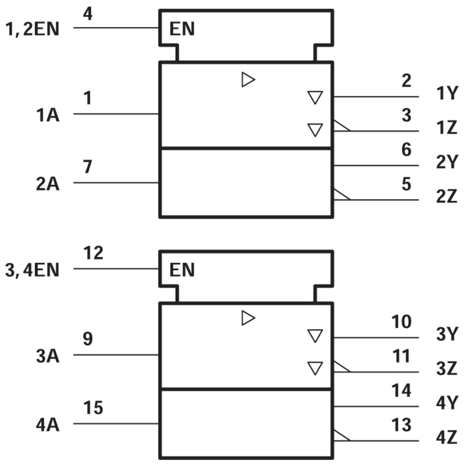
SN65LBC174 および SN75LBC174 には、正および負の電流制限とサーマル シャットダウンがあり、伝送バスラインのライン フォルト状況から保護します。これらのデバイスは、SN75LBC173 または SN75LBC175 クワッド ライン レシーバとともに使用したとき、最高のパフォーマンスを発揮します。SN65LBC174 および SN75LBC174 は、16 端子の DIP パッケージ (N) と、20 端子の幅広 SOIC (Small Outline Integrated Circuit) パッケージ (DW) で供給されます。

SN75LBC174 は 0℃～70℃の商用温度範囲で動作が規定されています。SN65LBC174 は –40℃～85℃の産業用温度範囲で動作が規定されています。

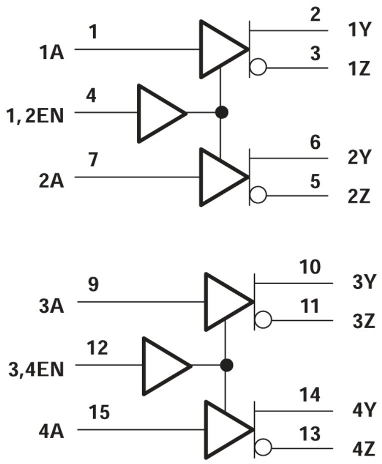
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN65LBC174	DW	12.8mm × 10.3mm
	N	19.3mm × 9.4mm
SN75LBC174	DW	12.8mm × 10.3mm
	N	19.3mm × 9.4mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理記号[†][1]



論理図 (正論理)

[†] この記号は ANSI/IEEE Std 91-1984 および IEC Publication 617-12 に準拠しています。
[1] ここに示すピン番号は N パッケージのものです。

Table of Contents

4 Pin Configuration and Functions

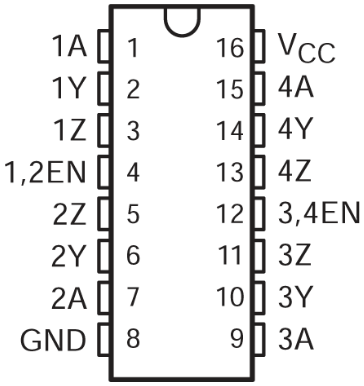
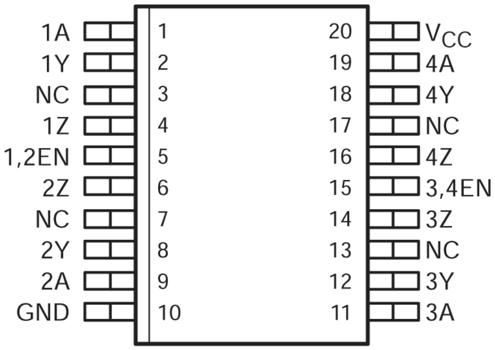


図 4-1. N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
1Z	3	O	Driver 1 inverted output
1,2EN	4	I	Active high driver enable channel 1 and 2
2Z	5	O	Driver 2 inverted output
2Y	6	O	Driver 2 output
2A	7	I	Driver 2 input
GND	8	-	Ground pin
3A	9	I	Driver 3 input
3Y	10	O	Driver 3 output
3Z	11	O	Driver 3 inverted output
3,4EN	12	I	Active high driver enable channel 3 and 4
4Z	13	O	Driver 4 inverted output
4Y	14	O	Driver 4 output
4A	15	I	Driver 4 input
V_{CC}	16	–	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



NC – No internal connection

図 4-2. DW Package (Top View)

表 4-2. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
NC	3	-	No Internal Connection
1Z	4	O	Driver 1 inverted output
1,2EN	5	I	Active high driver enable channel 1 and 2
2Z	6	O	Driver2 inverted output
NC	7	-	No Internal Connection
2Y	8	O	Driver 2 output
2A	9	I	Driver 2 input
GND	10	–	Ground pin
3A	11	I	Driver 3 input
3Y	12	O	Driver 3 output
NC	13	–	No Internal Connection
3Z	14	O	Driver 3 inverted output
3,4EN	15	I	Active high driver enable channel 3 and 4
4Z	16	O	Driver 4 inverted output
NC	17	–	No Internal Connection
4Y	18	O	Driver 4 output
4A	19	I	Driver 4 input
V_{CC}	20	–	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC} (see Note 1)	Supply voltage range, see Note (2)		–0.3	7	V
V_O	Output voltage range		–10	15	V
V	Voltage range at A, 1/2EN, 3/4EN		–0.3	V_{CC} +0.5	V
P_D	Continuous total power dissipation		Internally limited(2)		
T_A	Operating free-air temperature range:	SN65LBC174	–40	85	°C
		SN75LBC174	0	70	°C
T_{stg}	Storage temperature range		–65	150	°C
T_{lead}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature. NOTE 1: All voltage values are with respect to GND.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common-mode), V_O	Y or Z			12	V
				–7	
High-level output current, I_{OH}	Y or Z			–60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A	SN65LBC174	–40		85	°C
	SN75LBC174	0		70	

5.3 Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125mW	9.0mW/°C	720mW	585mW
N	1150mW	9.2mW/°C	736mW	598mW

5.4 Thermal Information

THERMAL METRIC[1]		DW	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18mA				-1.5	V
$\|V_{OD}\|$	Differential output voltage[2]	R_L = 54Ω, See 図 6-1	SN65LBC174	1.1	1.8	5	V
			SN75LBC174	1.5	1.8	5	
		R_L = 60Ω, See 図 6-2	SN65LBC174	1.1	1.7	5	
			SN75LBC174	1.5	1.7	5	
$\Delta\|V_{OD}\|$	Change in magnitude of common-mode output voltage[3]	R_L = 54Ω,	See 図 6-1			±0.2	V
V_{OC}	Common-mode output voltage			-1		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[3]					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = - 7V to 12V			± 100	μA
I_{OZ}	High-impedance-state output current	V_O = - 7V to 12V				± 100	μA
I_{IH}	High-level input current	V_I = 2.4V				-100	μA
I_{IL}	Low-level input current	V_I = 0.4V				-100	μA
I_{OS}	Short-circuit output current	V_O = -7V to 12V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.

(3) $\Delta_{|VOD|}$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54Ω,	See 図 6-3	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			9	15	25	ns
t_{PZH}	Output enable time to high level	R_L = 110Ω,	See 図 6-3		20	30	ns
t_{PZL}	Output enable time to low level	R_L = 110Ω,	See 図 6-5		21	30	ns
t_{PHZ}	Output disable time from high level	R_L = 110Ω,	See 図 6-4		48	70	ns
t_{PLZ}	Output disable time from low level	R_L = 110Ω,	See 図 6-5		21	30	ns

5.7 Typical Characteristics

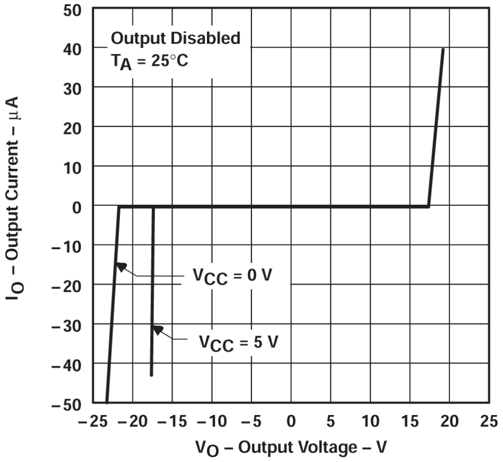


図 5-1. Output Current vs Output Voltage

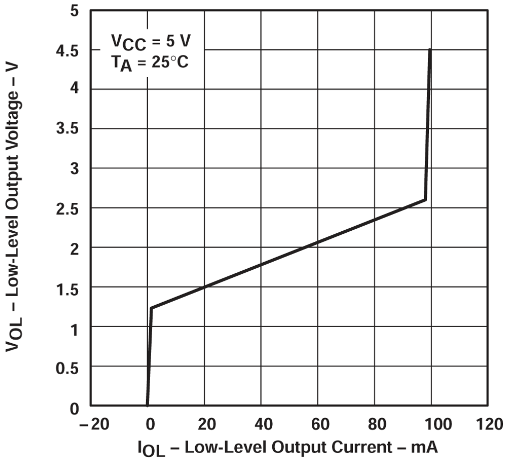


図 5-2. Low-level Output Voltage vs Low-level Output Current

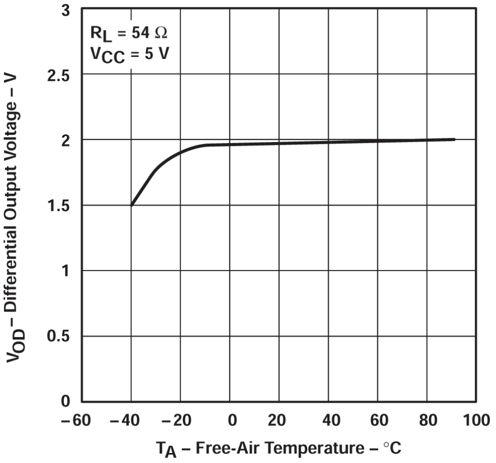


図 5-3. Differential Output Voltage vs Free-air Temperature

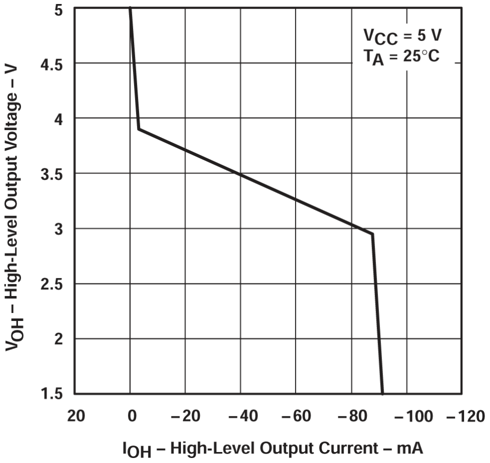


図 5-4. High-level Output Voltage vs High-level Output Current

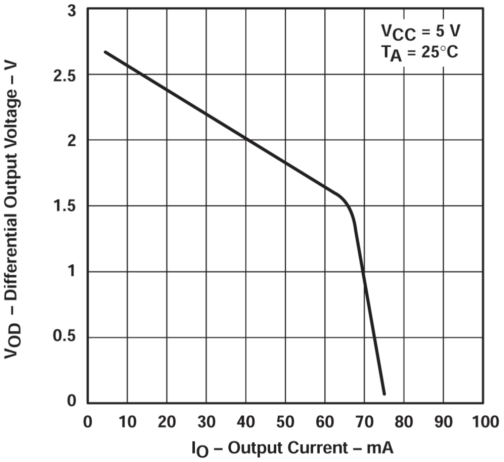


図 5-5. Differential Output Voltage vs Output Current

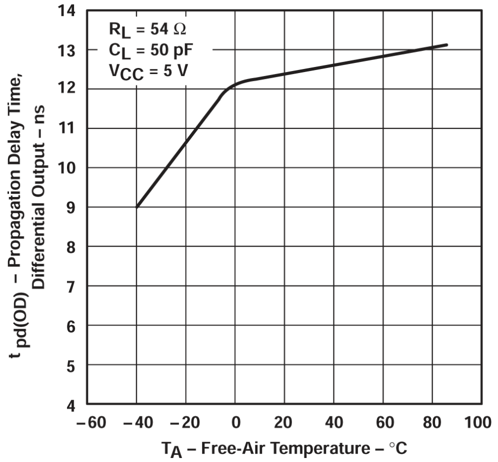


図 5-6. Propagation Delay Time, Differential Output vs Free-air Temperature

6 Parameter Measurement Information

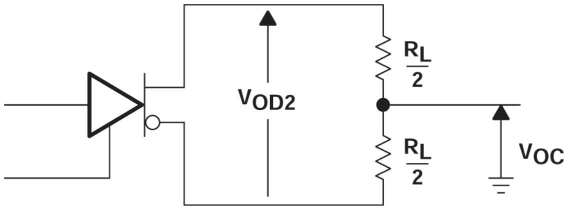


図 6-1. Differential and Common-Mode Output Voltages

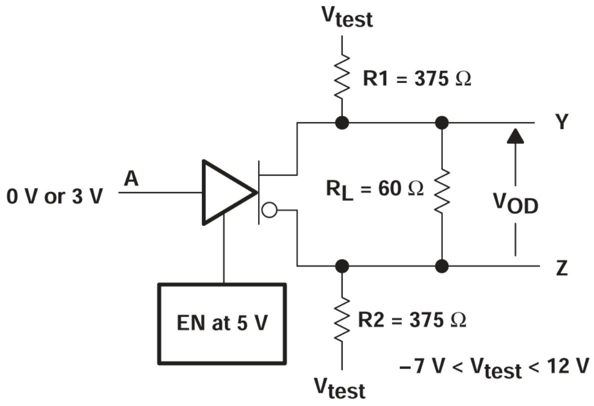
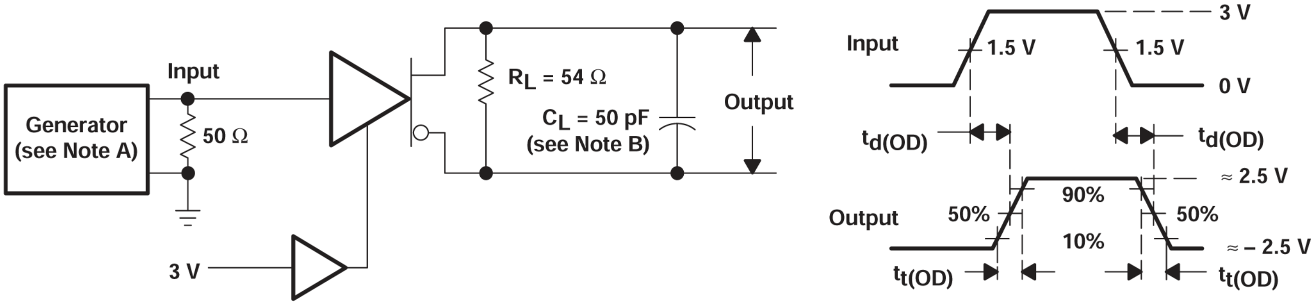


図 6-2. Driver V_{OD} Test Circuit



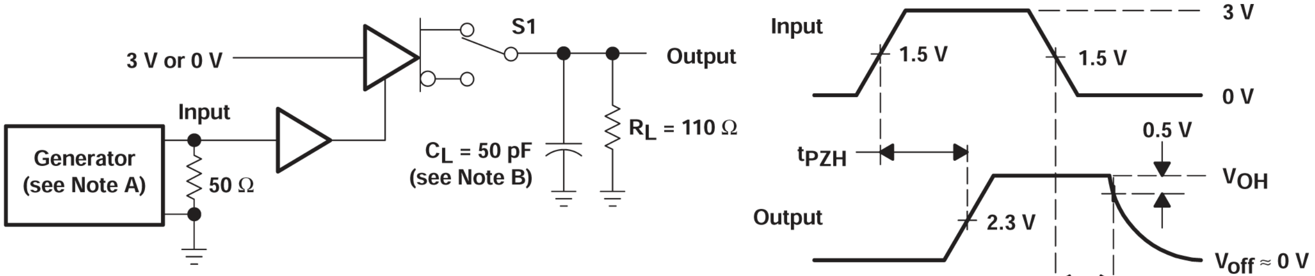
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle = 50%, t_r ≤ 5ns, t_f ≤ 5ns, Z_O = 50Ω.

B. C_L includes probe and stray capacitance.

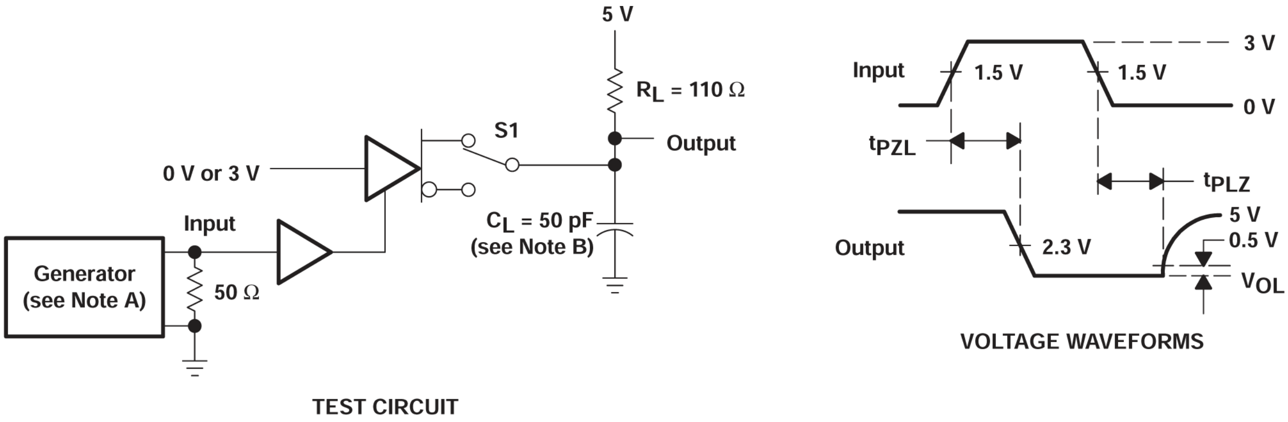
図 6-3. Time Waveforms for Driver Differential Output Test Circuit Delay and Transition



TEST CIRCUIT

VOLTAGE WAVEFORMS

図 6-4. t_{PZH} and t_{PHZ} Test Circuit and Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle = 50%, t_r ≤ 5ns, t_f ≤ 5ns, Z_O = 50Ω.

B. C_L includes probe and stray capacitance.

図 6-5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

7 Detailed Description

7.1 Thermal Characteristics of Ic Packages

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. Θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25mm long and 2-oz thick copper. The high-k board gives *best case* in−use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in Θ_{JA} can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. Including a bit for the PCB thermal resistance (especially for BGAs with thermal balls), and can be used for simple 1-dimensional network analysis of package system (see 図 7-1).

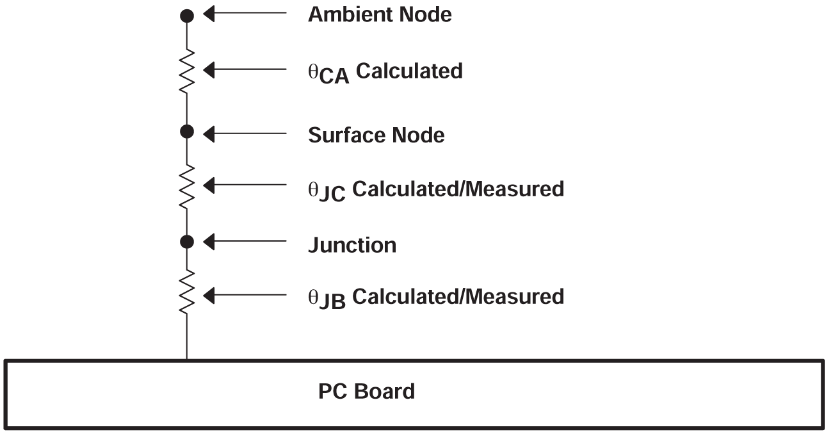


図 7-1. Thermal Resistance

7.2 Device Functional Modes

表 7-1. Functional Tables (Each Driver)

INPUT(1)	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

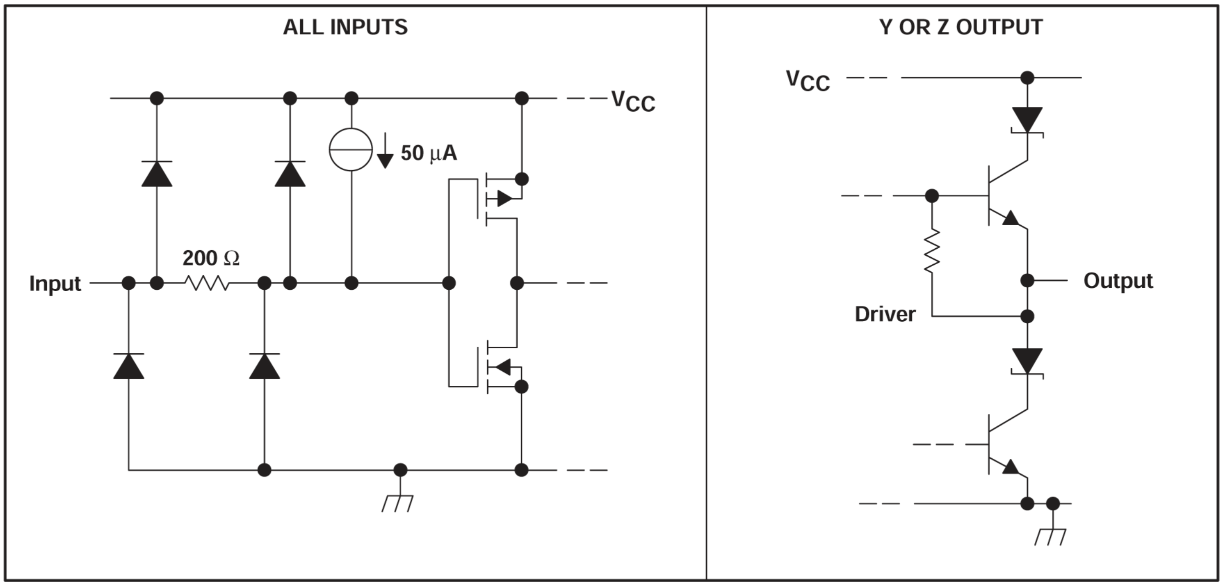


図 7-2. Schematic of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[更新の通知を受け取る] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

8.3 Trademarks

LinBiCMOS™ and TI E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (April 2006) to Revision F (April 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を変更 1
- Added the *Thermal Information* table........ 6
- Changed the $t_{t(OD)}$ MIN value from 10ns to 9ns in the *Switching Characteristics* 7

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC174DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174	Samples
SN65LBC174N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC174N	Samples
SN75LBC174N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC174N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN75LBC174 :

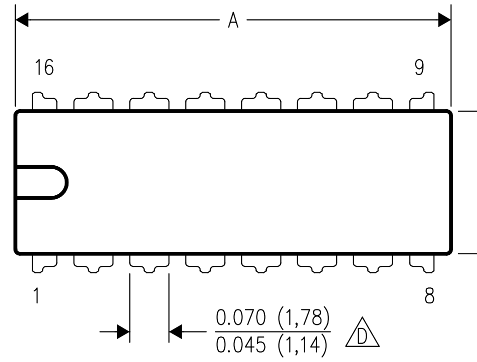
- Military : SN55LBC174

NOTE: Qualified Version Definitions:

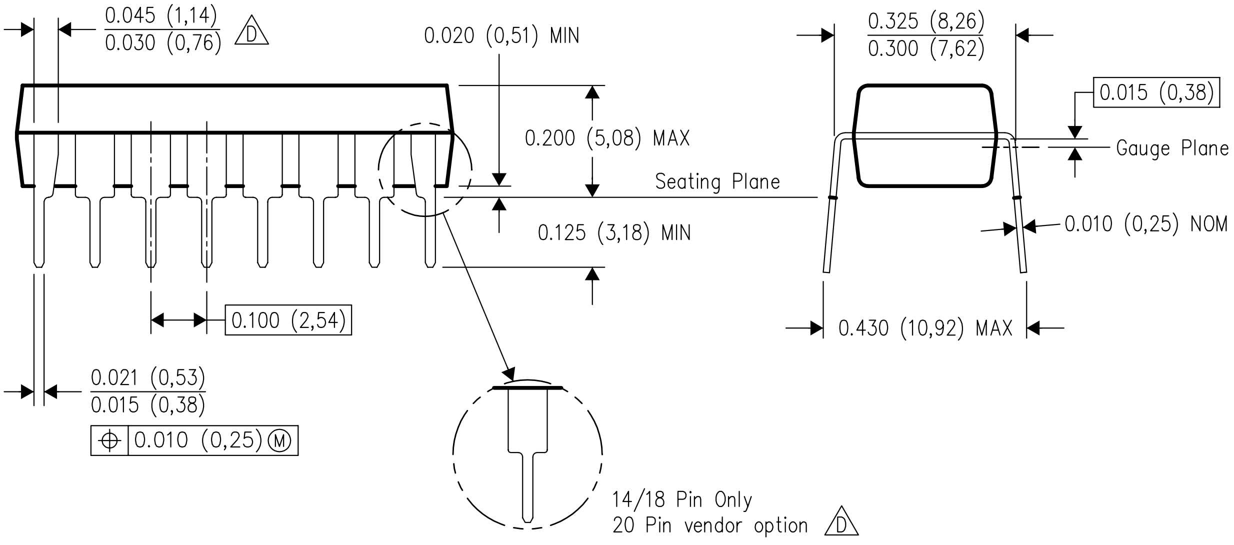
- Military - QML certified for Military and Defense Applications

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

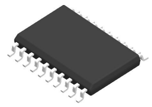


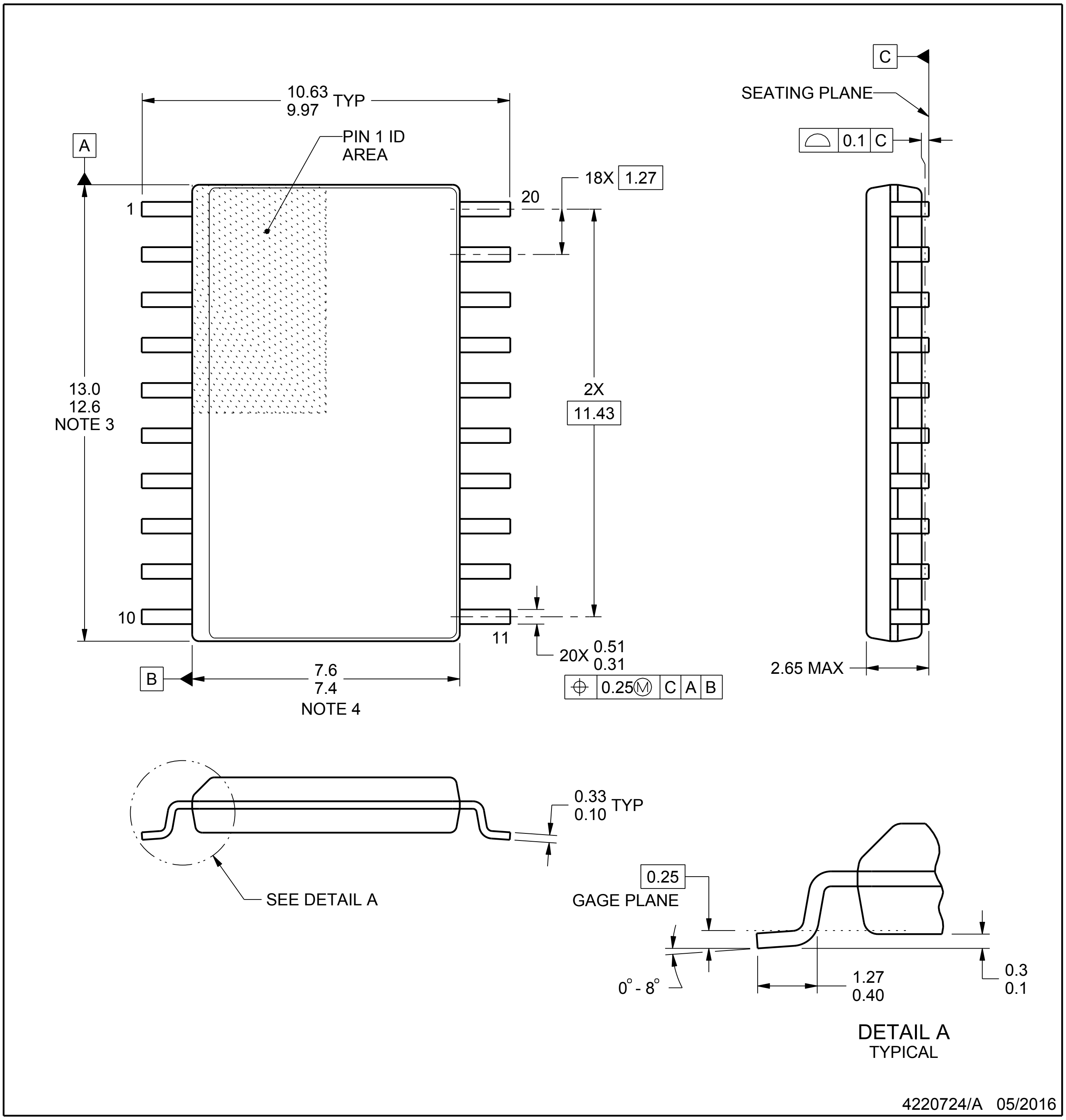
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

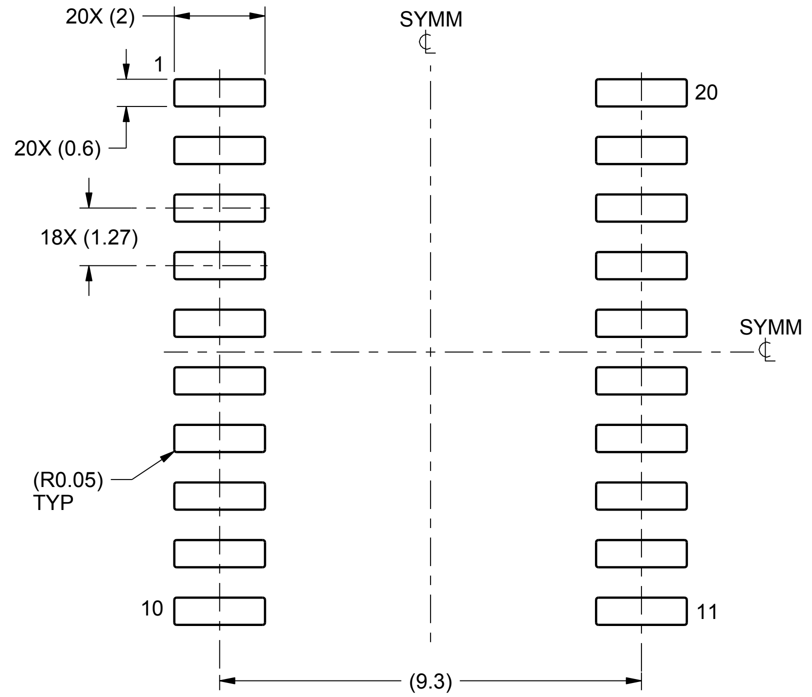
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.



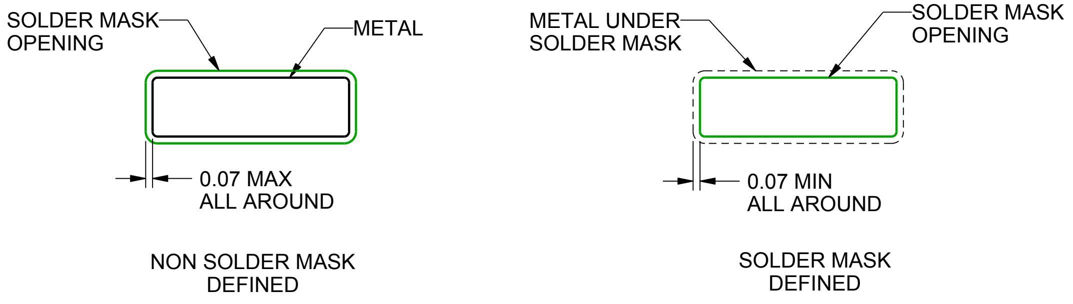


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

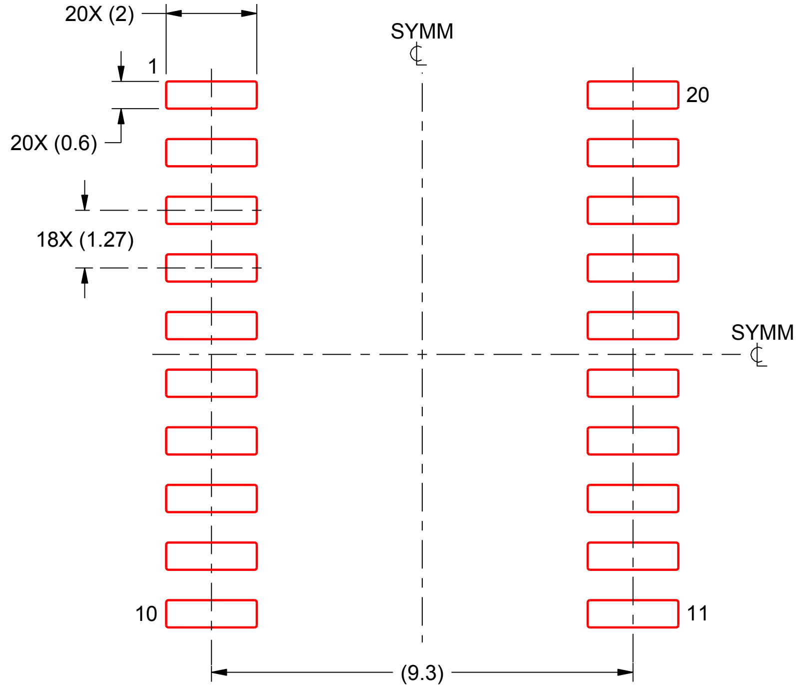


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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