

SN65LBC174A-EP クワッド RS-485 差動ライン・レシーバ

1 特長

- VID V62/07611
- TIA/EIA-485、TIA/EIA-422、ISO 8482 アプリケーション用に設計
- 最大 30Mbps の信号速度⁽¹⁾
- 伝搬遅延時間：11ns 未満
- 低いスタンバイ時消費電力：1.5mA 以下
- ドライバの正および負の電流制限
- 活線挿抜アプリケーションでパワーアップ/パワーダウン時のグリッチなし
- サーマル・シャットダウン保護機能
- SN75174、MC3487、DS96174、LTC487、MAX3042 と互換の業界標準ピン配置
- 防衛、航空宇宙、および医療アプリケーションをサポート
 - 管理されたベースライン
 - 単一のアセンブリ/テスト施設
 - 単一の製造施設
 - 軍用温度範囲 (-55°C ~ 125°C) で利用可能
 - 長い製品ライフ・サイクル
 - 製品変更通知期間の延長
 - 製品のトレーサビリティ

2 アプリケーション

- 最高 30Mbps の信号レートでの伝送
- アビオニクス、レーダー
- ミサイル用 GPS ナビゲーション
- 産業用輸送
- ノイズの多い環境の高速マルチポイント・データ伝送アプリケーション

3 概要

SN65LBC174A-EP は TRI-STATE 出力付きクワッド差動ライン・レシーバであり、TIA/EIA-485 (RS-485)、TIA/EIA-422 (RS-422)、ISO 8482 アプリケーション用に設計されています。

このデバイスは、最大 30Mbps の信号レートでの平衡マルチポイント・バス伝送用に最適化されています。伝送媒体にはプリント基板のトレース、バックプレーン、ケーブルを使用できます。データ転送の最高速度および最大距離は、メディアの減衰特性と周囲からのノイズに依存します。

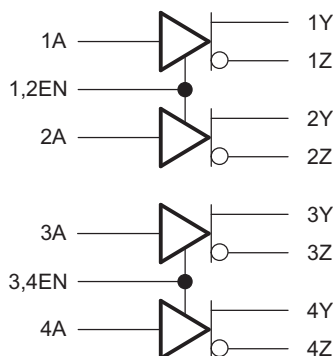
製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
SN65LBC174A-EP	SOIC (20)	7.50 × 12.80
	SOIC (16)	7.50 × 10.30

(1) ラインの信号レートとは、1 秒あたりの電圧遷移回数を bps (ビット/秒) 単位で表したものです。

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ロジック図 (正論理)



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2006年12月発行のものから更新

	Page
• データシートを上位基準に更新	1
• Added pinout drawing for 16-pin DW	3
• Added 16-pin DW and updated the Pin Functions table	4
• Added ESD value for 16-pin DW package	5
• Added updated thermal metrics	5

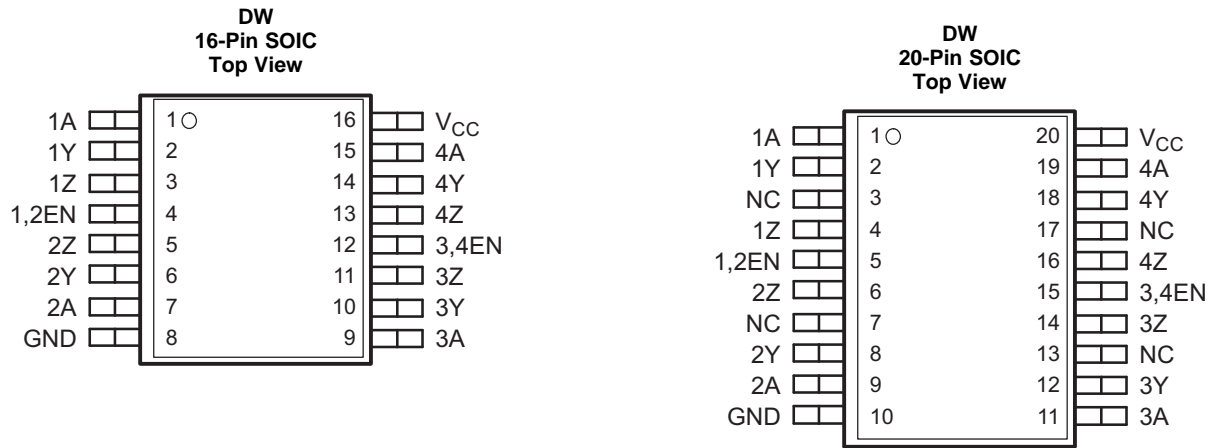
5 概要（続き）

各ドライバは電流制限およびサーマル・シャットダウン回路を備えているため、ノイズの多い環境の高速マルチポイント・アプリケーションに適しています。このデバイスは LinBiCMOS™ 技術を採用して設計されているため、低消費電力で堅牢性の高いソリューションを簡単に構築できます。

2 つのイネーブル (EN) 入力を備えているため、ドライバを対にしてイネーブルできます。また、2 つのイネーブル入力を外部で接続することで、4 つのドライバ全部を 1 つの信号でイネーブル制御することもできます。ディセーブルまたは電源オフ時には、ドライバの出力はバスに対して高インピーダンスになるため、システムの負荷を低減できます。

SN65LBC174A-EP は、 -55°C ～ 125°C の温度範囲で動作が規定されています。

6 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	16 PINS	20 PINS		
1A	1	1	Digital input	Port 1 A data input
1Y	2	2	Bus output	Bus port 1 Y (complementary to 1 Z)
NC	—	3	No Connect	Physically not connected in package
1Z	3	4	Bus output	Bus port 1 Z (complementary to 1 Y)
1,2EN	4	5	Digital input	Bus output port 1 and 2 driver enable
2Z	5	6	Bus output	Bus port 2 Z (complementary to 2 Y)
NC	—	7	No Connect	Physically not connected in package
2Y	6	8	Bus output	Bus port 2 Y (complementary to 2 Z)
2A	7	9	Digital input	Port 2 A data input
GND	8	10	Ground	Device ground
3A	9	11	Digital input	Port 3 A data input
3Y	10	12	Bus output	Bus port 3 Y (complementary to 3 Z)
NC	—	13	No Connect	Physically not connected in package
3Z	11	14	Bus output	Bus port 3 Z (complementary to 3 Y)
3,4EN	12	15	Digital input	Bus output port 3 and 4 driver enable
4Z	13	16	Bus output	Bus port 4 Z (complementary to 4 Y)
NC	—	17	No Connect	Physically not connected in package
4Y	14	18	Bus output	Bus port 4 Y (complementary to 4 Z)
4A	15	19	Digital input	Port 4 A data input
V _{CC}	16	20	V _{CC}	Device power

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾	-0.3	6	V
	Voltage at any bus (dc)	-10	15	V
	Voltage at any bus (transient pulse through 100 Ω , See Figure 14)	-30	30	V
V_I	Input voltage at any A or EN terminal	-0.5	$V_{CC} + 0.5$	V
T_{stg}	Storage temperature ⁽³⁾	-65	150	°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s		260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to GND.
- (3) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.

7.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Y, Z (20-pin DW)	±13,000	V
			Y, Z (16-pin DW)	±10,000	
			All other pins	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at any bus terminal	Y, Z	-7		12	V
V_{IH}	High-level input voltage	A, EN	2		V_{CC}	V
V_{IL}	Low-level input voltage	A, EN	0		0.8	V
	Output current		-60		60	mA
T_A	Operating free-air temperature		-55		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN65LBC174A-EP		UNIT	
	DW (SOIC)			
	20 PINS	16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.3	60.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	24.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	26.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.8	25.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

7.5 Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA		-1.5	-0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$ V_{OD(SS)} $	Steady-state differential output voltage magnitude ⁽²⁾	No load (open circuit)		3		V_{CC}	V
		$R_L = 54 \Omega$, See Figure 7		0.8	1.6	2.5	
		With common-mode loading, See Figure 8		0.8	1.6	2.5	
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See Figure 7		-0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 9		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 9		-0.04		0.04	V
I_I	Input current	A, G, \bar{G}		-70		70	μ A
I_{OS}	Short-circuit output current	$V_{TEST} = -7$ V to 12 V, See Figure 13	$V_I = 0$ V	-200		200	mA
I_{OZ}	High-impedance-state output current		$V_I = V_{CC}$			50	
$I_{O(OFF)}$	Output current with power off		EN at 0 V	-10		10	μ A
I_{CC}	Supply current		$V_I = 0$ V or V_{CC} , No load	All drivers enabled			25
			All drivers disabled			1.5	

(1) All typical values are at $V_{CC} = 5$ V and 25°C.

(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibility of lower output signal into account in determining the maximum signal transmission distance.

7.6 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$T_A = 25^\circ\text{C}$	4.0	8	11	ns
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	4.0		16	
t_{PHL}	Propagation delay time, high- to low-level output	$T_A = 25^\circ\text{C}$	4.0	8	11	ns
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	4.0		16	
t_r	Differential output voltage rise time	$T_A = 25^\circ\text{C}$	3	7.5	11	ns
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	3		24	
t_f	Differential output voltage fall time	$T_A = 25^\circ\text{C}$	3	7.5	11	ns
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	3		24	
$t_{sk(p)}$	Pulse skew $ t_{PLH} - t_{PHL} $			0.6		ns
$t_{sk(o)}$	Output skew ⁽¹⁾			2		ns
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾			3		ns
t_{PZH}	Propagation delay time, high impedance to high-level output	See Figure 11			25	ns
t_{PHZ}	Propagation delay time, high-level output to high impedance				25	ns
t_{PZL}	Propagation delay time, high impedance to low-level output	See Figure 12			30	ns
t_{PLZ}	Propagation delay time, low-level output to high impedance				20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.7 Typical Characteristics

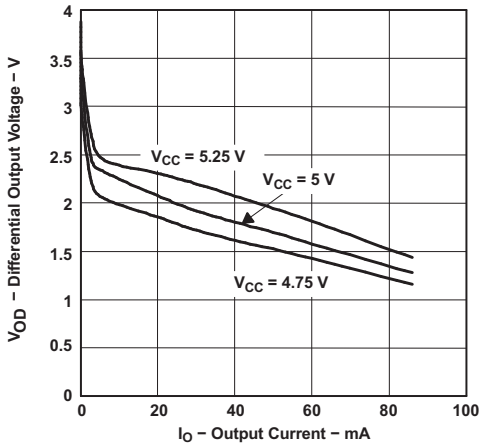


Figure 1. Differential Output Voltage vs Output Current

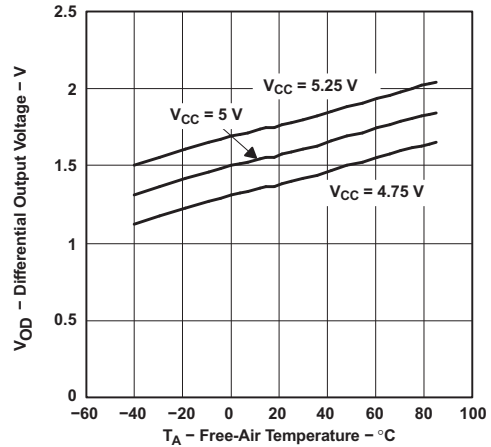


Figure 2. Differential Output Voltage vs Free-Air Temperature

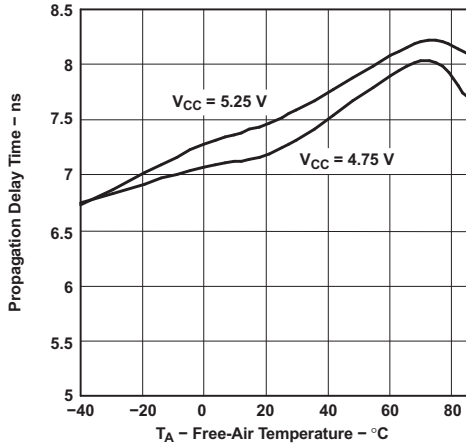


Figure 3. Propagation Delay Time vs Free-Air Temperature

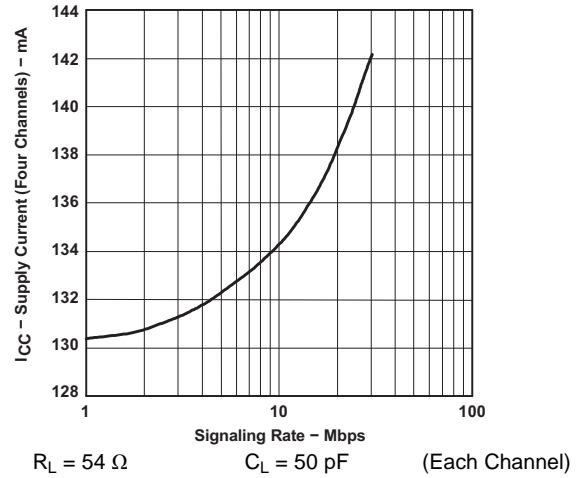


Figure 4. Supply Current (Four Channels) vs Signaling Rate

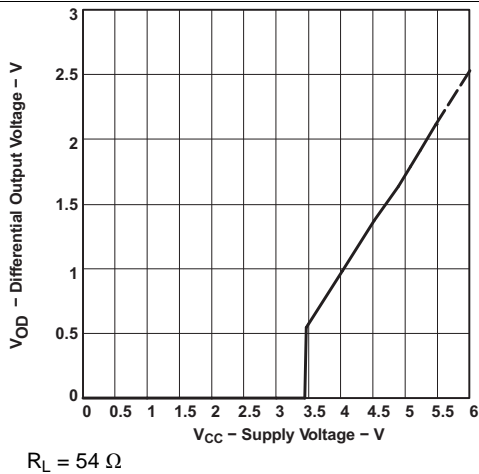


Figure 5. Differential Output Voltage vs Supply Voltage

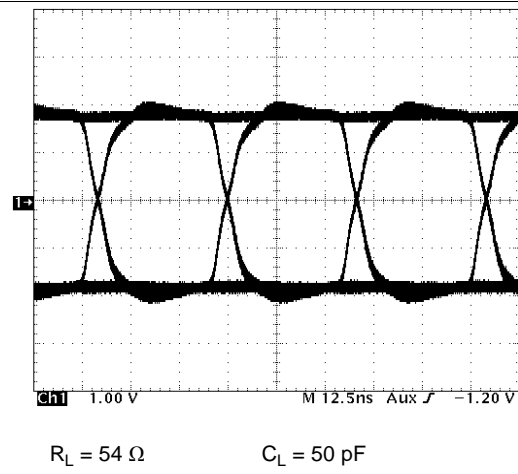


Figure 6. Eye Pattern, Pseudo-Random Data at 30 Mbps

8 Parameter Measurement Information

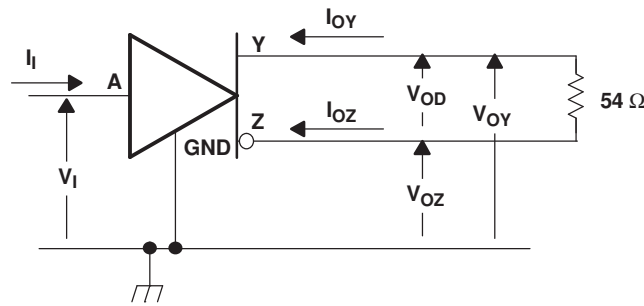


Figure 7. Test Circuit, V_{OD} Without Common-Mode Loading

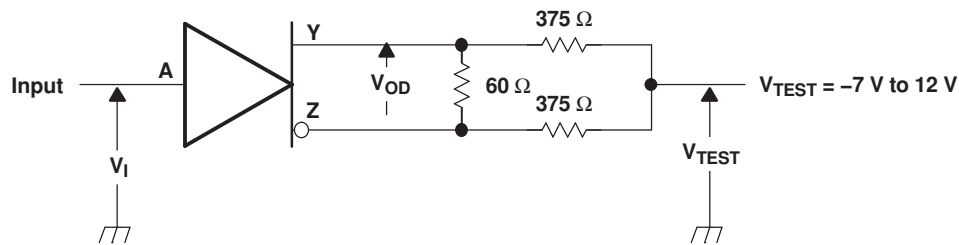
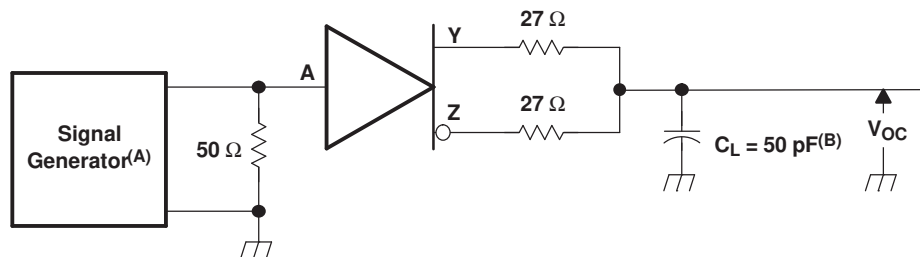


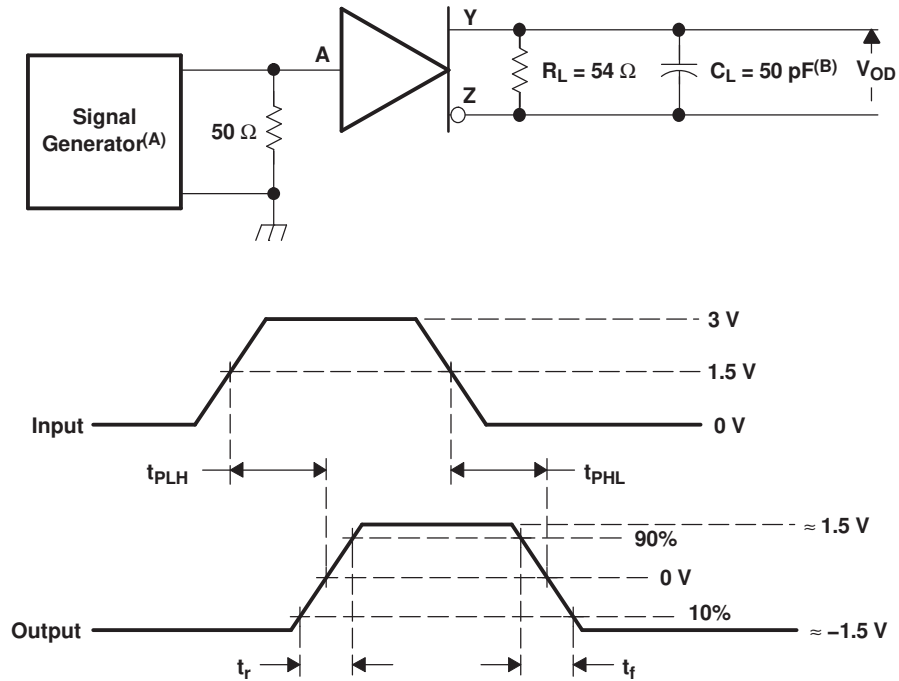
Figure 8. Test Circuit, V_{OD} With Common-Mode Loading



PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50 \Omega$
Includes probe and jig capacitance.

Figure 9. V_{OC} Test Circuit

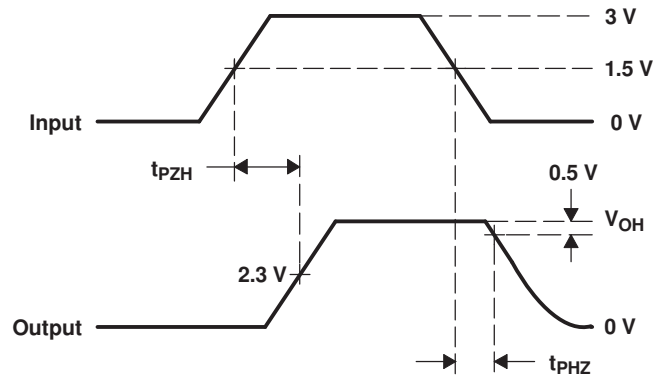
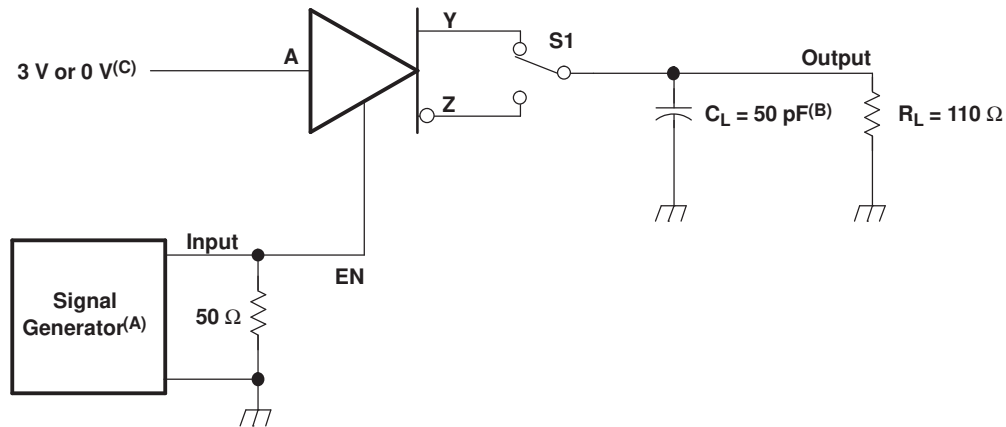
Parameter Measurement Information (continued)



PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$
 Includes probe and jig capacitance.

Figure 10. Output Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)



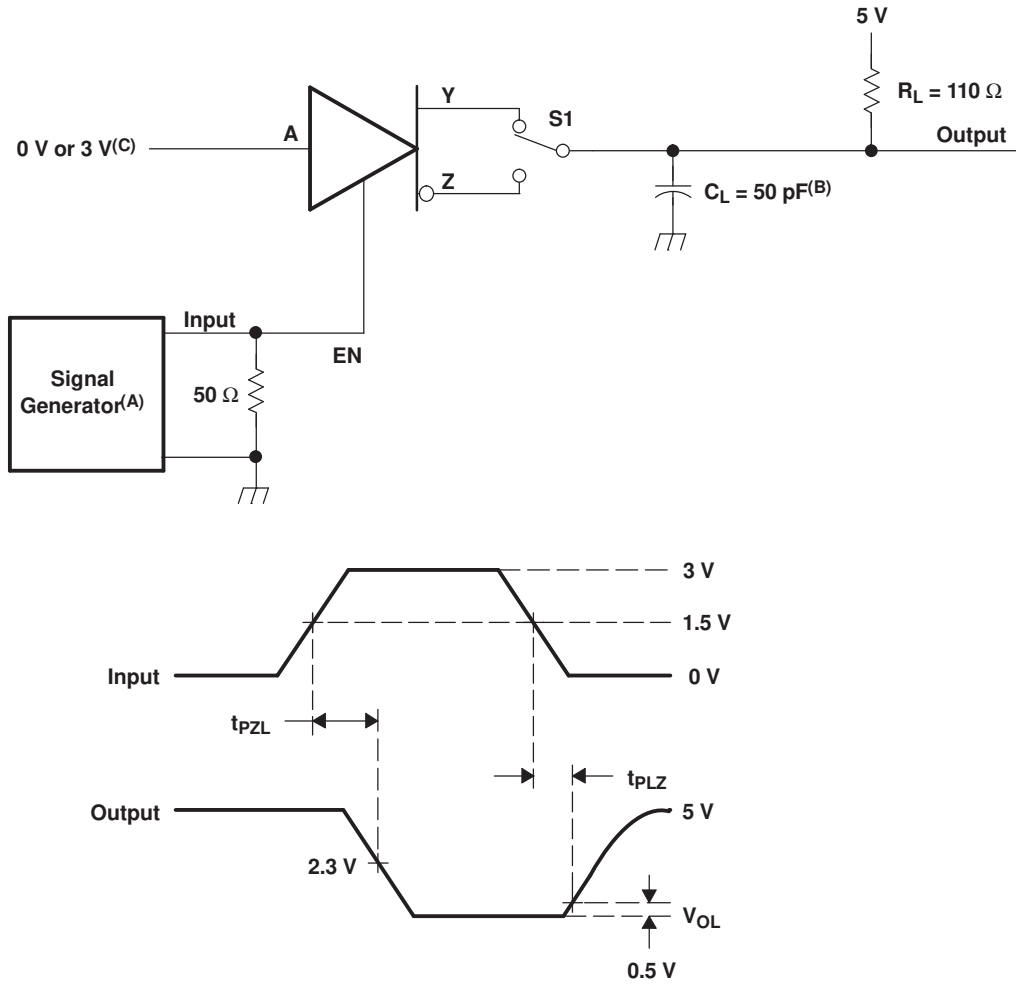
PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50 \Omega$

Includes probe and jig capacitance.

3 V if testing Y output, 0 V if testing Z output.

Figure 11. Enable Timing Test Circuit and Waveforms, T_{PZH} and T_{PHZ}

Parameter Measurement Information (continued)



PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50 \Omega$
 Includes probe and jig capacitance.
 3 V if testing Y output, 0 V if testing Z output.

Figure 12. Enable Timing Test Circuit and Waveforms, T_{PZL} and T_{PLZ}

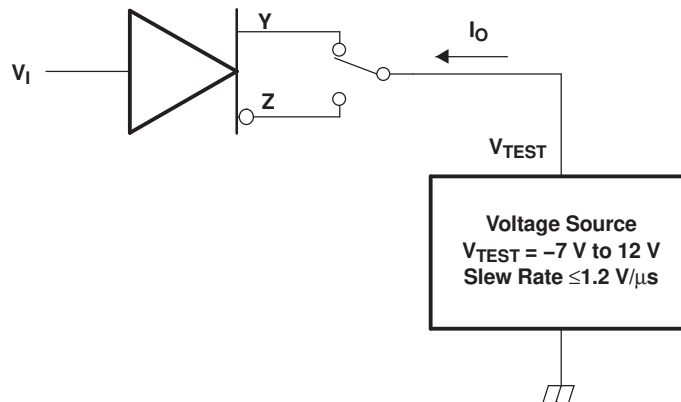


Figure 13. Test Circuit, Short-Circuit Output Current

Parameter Measurement Information (continued)

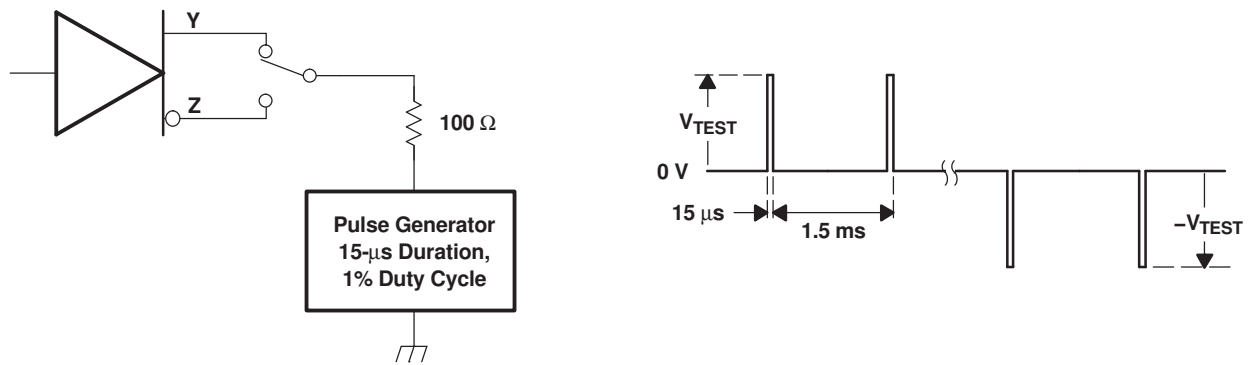


Figure 14. Test Circuit Waveform, Transient Overvoltage Test

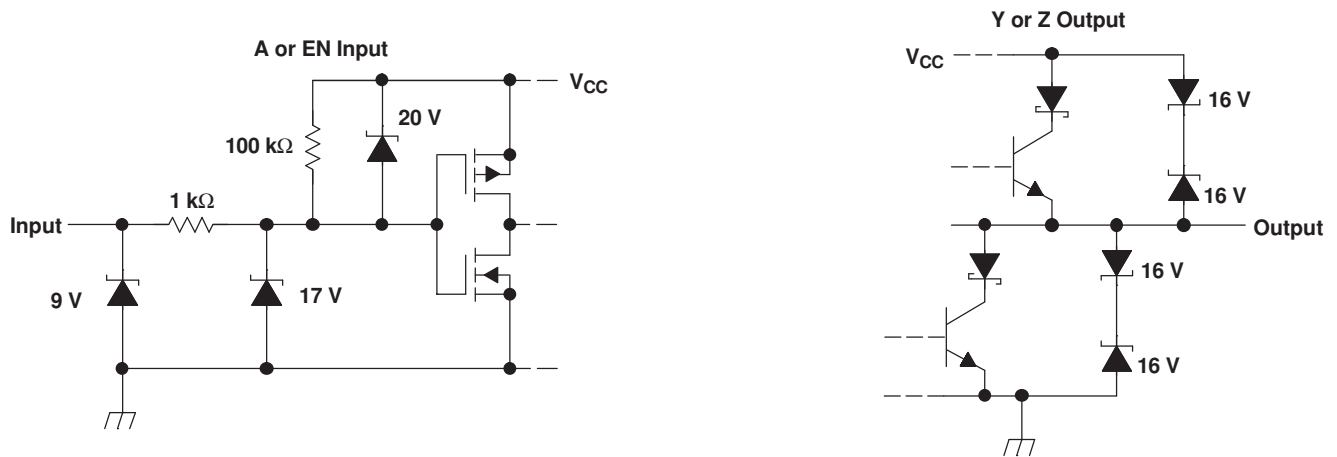


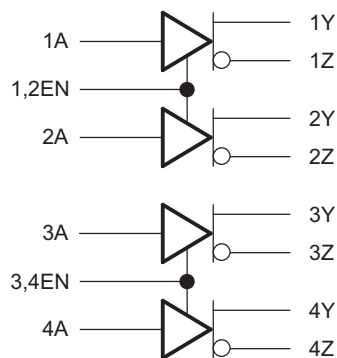
Figure 15. Equivalent Input and Output Schematic Diagrams

9 Detailed Description

9.1 Overview

The SN65LBC174A-EP is a quadruple differential line driver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications. This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 30 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment. The transmitter features ESD protection to 12 kV on driver outputs, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS, facilitating low-power consumption and robustness. Two EN inputs provide pair-wise enable control, or these can be tied together externally to enable all four drivers with the same signal.

9.2 Functional Block Diagram



9.3 Feature Description

The device can be configured using the enable inputs to enable driver pairs 1 and 2, and/or 3 and 4. The high voltage or logic 1 on the EN pin enables the devices differential outputs.

9.4 Device Functional Modes

The drivers implemented in the RS-485 device can be configured using the EN logic pins set to enabled or disabled. This allows users to transmit or idle the bus as desired.

**Table 1. Function Table⁽¹⁾
(Each Driver)**

INPUT A	ENABLE G	OUTPUTS	
		Y	Z
L	H	L	H
H	H	H	L
OPEN	H	H	L
L	OPEN	L	H
H	OPEN	H	L
OPEN	OPEN	H	L
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

10 Application and Implementation

NOTE

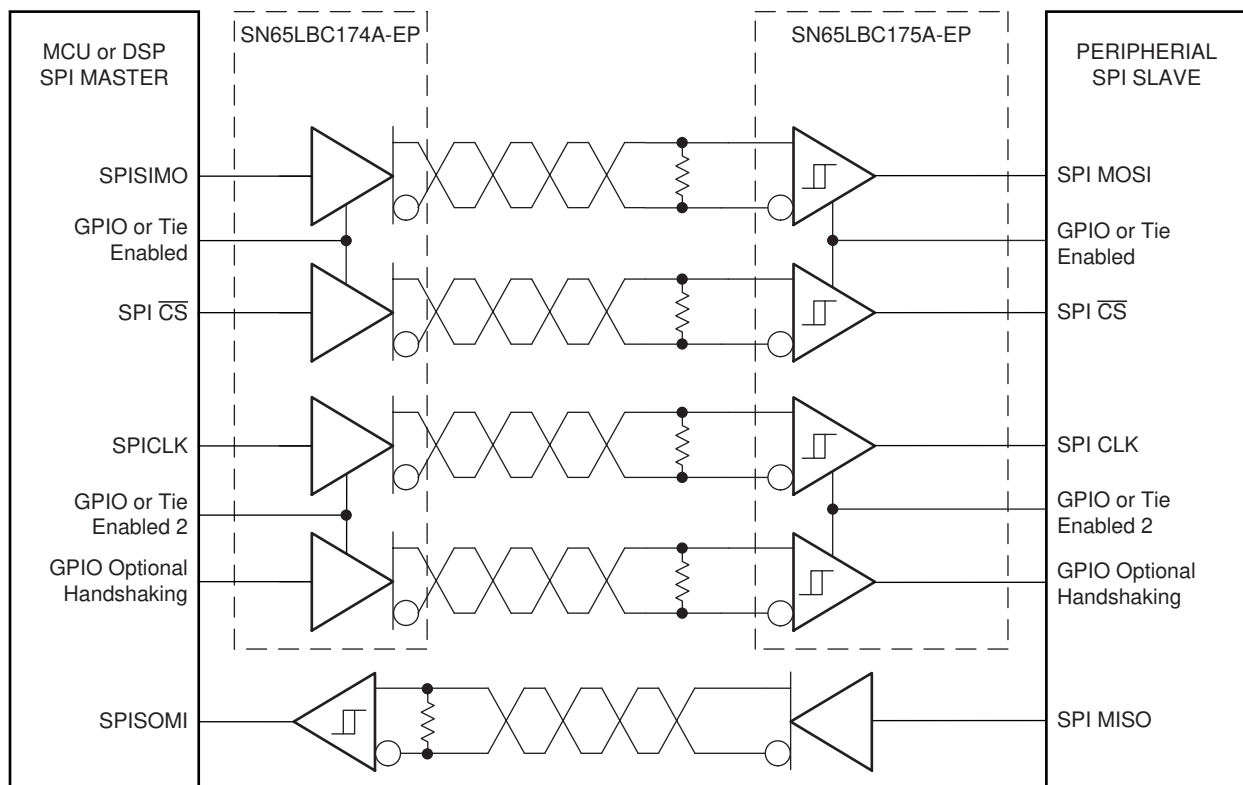
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Extending SPI operation over RS-485 link.

10.2 Typical Application

The following block diagram shows an MCU host connected via RS-485 to a SPI slave device. This device can be an ADC, DAC, MCU, or other SPI slave peripheral.



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Figure 16. Typical Application Circuit, MCU Master to Slave Link Via Serial Peripheral Interface

10.2.1 Design Requirements

This application can be implemented using standard SPI protocol on DSP or MCU devices. The interface is independent of the specific frame or data requirements of the host or slave device. An additional but not required handshake bit is provided that can be used for customer purposes.

Typical Application (continued)

10.2.2 Detailed Design Procedure

The interface design requirements are fairly straight forward in this single source/destination scenario. Trace lengths and cable lengths need to be matched to maximize SPI timing. If there is a benefit to put the interface to sleep, GPIOs can be used to control the enable signals of the transmitter and receiver. If GPIOs are not available, or constant uptime needed, both the enables on transmit and receive can be hard tied enabled. The link shown can operate at up to 30 Mbps, well within the capability of most SPI links.

10.2.3 Application Curve

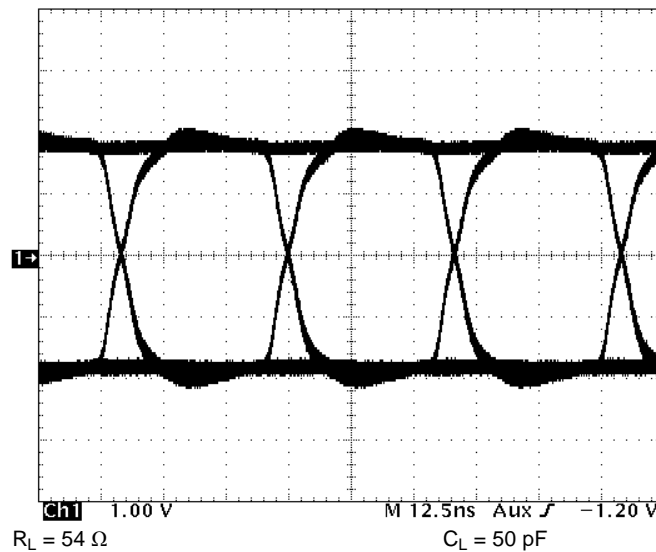


Figure 17. Eye Pattern, Pseudo-Random Data at 30 Mbps

11 Power Supply Recommendations

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.
- Place termination resistor as close as possible to the input pins (if end point node).
- Keep trace lengths from input pins to bus as short as possible to reduce stub lengths and reflections on any nodes that are not end points of bus.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

12.2 Layout Example

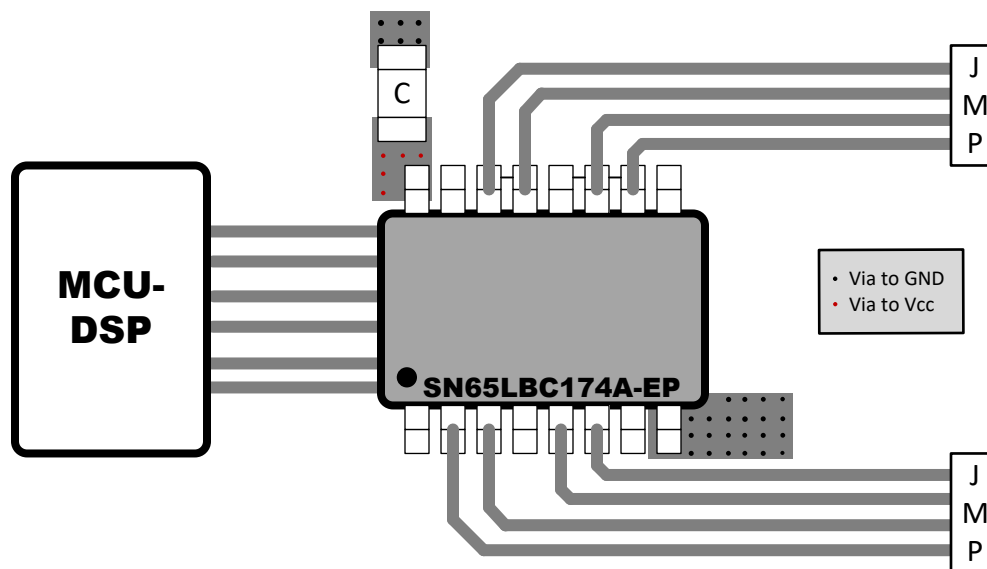


Figure 18. Layout With PCB Recommendations

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.2 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.3 商標

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13.4 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
65LBC174AM16DWREP	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	65LBC174EP	Samples
SN65LBC174AMDWREP	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	65LBC174EP	Samples
V62/07611-01XE	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	65LBC174EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
65LBC174AM16DWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65LBC174AMDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
65LBC174AM16DWREP	SOIC	DW	16	2000	350.0	350.0	43.0
SN65LBC174AMDWREP	SOIC	DW	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

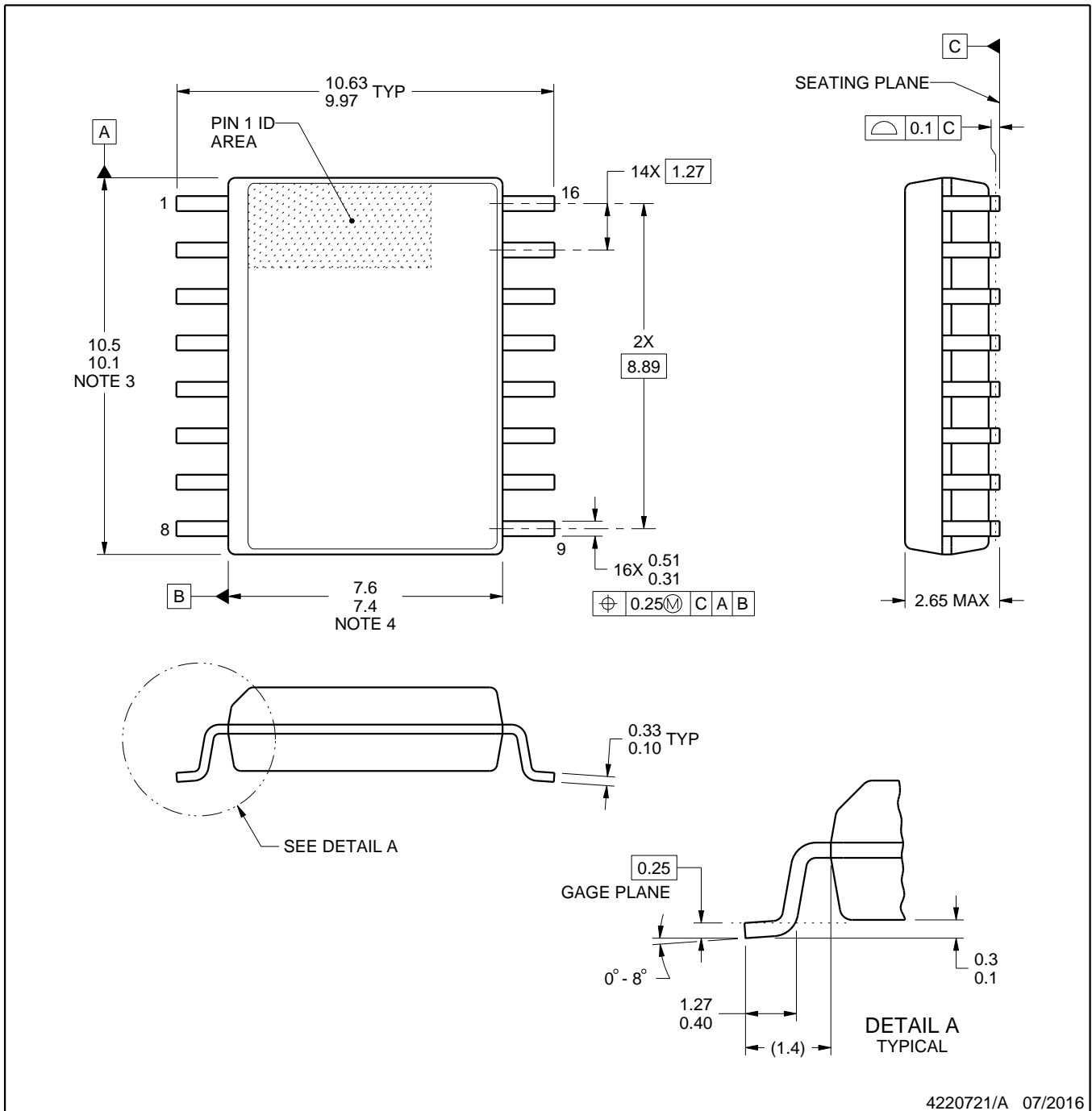


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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