SNx5LBC179A 低消費電力、差動ライン・ドライバとレシーバのペア

1 特長

- 最大 30 Mbps の信号速度(1) 向けに設計された、高速で低消費電力の LinBiCMOS™ 回路
- 12kV HBM を超えるバス・ピンの ESD 保護
- ディセーブル時の非常に低い消費電流要件:最大 700µA
- -7V～12V の同相電圧範囲
- 低消費電流:最大 15mA
- ANSI 標準 TIA/EAI-485-A および ISO8482 と互換:1987(E)
- 正および負の出力電流制限
- ドライバのサーマル・シャットダウン保護 [1]

2 概要

SN65LBC179A および SN75LBC179A 差動ドライバ / レシーバ・ペアは、伝送ラインの特性を考慮し、長いケーブルを使用する双方向データ通信向けに設計されたモノリシック IC です。これらは、ANSI 標準 TIA/EIA-485-A および ISO 8482:1987(E) と互換性のある平衡型、つまり差動の電圧モード・デバイスです。A バージョンは、消費電力を大幅に増やすことなく、従来製品に比べてスイッチング性能が向上しています。

SN65LBC179A および SN75LBC179A は、差動ライン・ドライバと差動入力ライン・レシーバを組み合わせて、5V 単電源で動作します。ドライバの差動出力とレシーバの差動入力は、全二重動作のために個別の端子に接続されており、電源オフ (V_{CC} = 0) 時にバスの負荷が最小化されるように設計されています。これらのデバイスは正と負の同相電圧範囲が広いため、ポイント・ツー・ポイントまたはマルチポイントのデータ・バス・アプリケーションに適しています。またこれらのデバイスは、ライン・フォルト状態からの保護のために、正と負の電流制限機能とサーマル・シャットダウン機能を備えています。

SN65LBC179A は -40℃～85℃の産業用温度範囲で動作が規定されています。SN75LBC179A は 0℃～70℃の商業用温度範囲で動作が規定されています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN65LBC179ASN75LBC179A	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

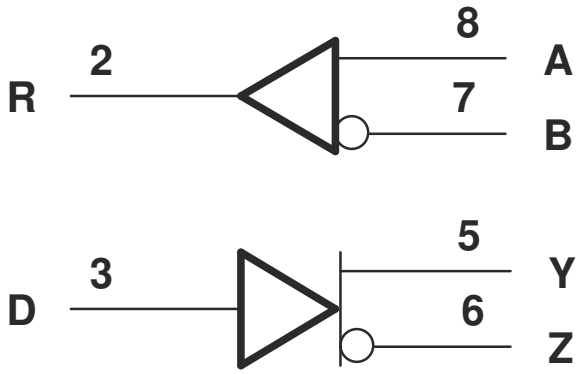

図 2-1. 論理図 (正論理)

[1] (1)TIA/EIA-485-A による信号速度の定義では、遷移時間がビット長の 30% に制限されており、このデバイスの標準的な特性に示すように、この要件を必要とせずにより高い信号速度を実現できます。

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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2011) to Revision E (January 2023) — **Page**

- ドキュメントを最新のテキサス・インスツルメンツのフォーマットに変更 ... 1
- Added the *Thermal Information* table ... 5
- Changed the *Typical Characteristics* graphs ... 7

Changes from Revision C (June 2001) to Revision D (September 2011) — **Page**

- Added Receiver output current to the Abs Max Table ... 4
- Changed ESD - All terminals, Class 3, A From: 4 kV To: 3 kV ... 4
- Changed the D Output and R Output schematics ... 12

4 Pin Configuration and Functions

SN65LBC179AD (Marked as BL179A)
SN65LBC179AP (Marked as 65LBC179A)
SN75LBC179AD (Marked as LB179A)
SN75LBC179AP (Marked as 75LBC179A)
(TOP VIEW)

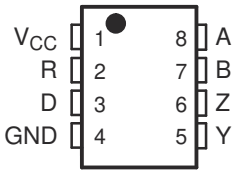


表 4-1. Pin Functions

NO	Name	Type	Description
1	V_{CC}	Supply	4.75V to 5.25V Supply
2	R	O	Receive data output
3	D	I	Driver data input
4	GND	GND	Device ground
5	Y	O	Digital bus output, Y (Complementary to Z)
6	Z	O	Digital bus output, Z (Complementary to Y)
7	B	I	Bus input, B (complementary to A)
8	A	I	Bus input, A (complementary to B)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage range(2)		–0.3 V to 6 V
	Voltage range	A, B, Y, or Z(2)	–10 V to 15 V
		D or R(2)	–0.3 V to V_{CC} + 0.5 V
I_O	Receiver output current		±20 mA
	Electrostatic discharge	Bus terminals and GND, Class 3, A(3)	12 kV
		Bus terminals and GND, Class 3, B(3)	400 V
		All terminals, Class 3, A	3 kV
		All terminals, Class 3, B	400 V
	Continuous total power dissipation(4)		Internally limited
	Total power dissipation		See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.
(3) Tested in accordance with MIL-STD-883C, Method 3015.7
(4) The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

5.2 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1100 mW	8.08 mW/°C	640 mW	520 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D	2		V_{CC}	V
V_{IL}	Low-level input voltage	D	0		0.8	V
V_{ID}	Differential input voltage(1)		–12(2)		12	V
V_O, V_I, V_{IC}	Voltage at any bus terminal (separately or common-mode)	A, B, Y, or Z	–7		12	V
I_{OH}	High-level output current	Y or Z	–60			mA
		R	–8			
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_A	Operating free-air temperature	SN65LBC179A	–40		85	°C
		SN75LBC179A	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.
(2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

5.4 Thermal Information

THERMAL METRIC[1]		P (PDIP)	D (SOIC) SN65 Device	D (SOIC) SN75 Device	UNIT
		8-Pins	8-Pins	8-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.7	116.7	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	54.7	56.3	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	63.4	53.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23	8.8	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.7	62.2	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5	–0.8		V
$\lvert V_{OD}\rvert$	Differential output voltage	R_L = 54 Ω, See 図 6-1	SN65LBC179A	1	1.5	3	V
			SN75LBC179A	1.1	1.5	3	
		R_L = 60 Ω, –7 <$V_{(tot)}$ < 12, See 図 6-2	SN65LBC179A	1	1.5	3	V
			SN75LBC179A	1.1	1.5	3	
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage [2]	See 図 6-1 and 図 6-2		–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 図 6-1		1.8	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage[2]			–0.1		0.1	V
I_O	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V	–10	±1	10	μA
I_{IH}	High-level input current	V_I = 2.V		–100			μA
I_{IL}	Low-level input current	V_I = 0.8 V		–100			μA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V		–250	±70	250	mA
I_{CC}	Supply current	No load,	V_I = 0 or V_{CC}		8.5	15	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Δ | V_{OD} | and Δ | V_{OC} | are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.6 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See 図 6-3	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	6	12	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0.3	1	ns
t_r	Differential output signal rise time		4	7.5	11	ns
t_f	Differential output signal fall time		4	7.5	11	ns

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		–0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See 図 6-1		4	4.9		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, See 図 6-1			0.1	0.8	V
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V	Other input at 0 V		0.4	1	mA
		V_{IH} = 12 V, V_{CC} = 0			0.5	1	
		V_{IH} = –7 V, V_{CC} = 5 V		–0.8	–0.4		
		V_{IH} = –7 V, V_{CC} = 0		–0.8	–0.3		

5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, See 図 6-4	7	13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output		7	13	20	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			0.5	1.5	ns
t_r	Rise time, output			2.1	3.3	ns
t_f	Fall time, output	See 図 6-4		2.1	3.3	ns

5.9 Typical Characteristics

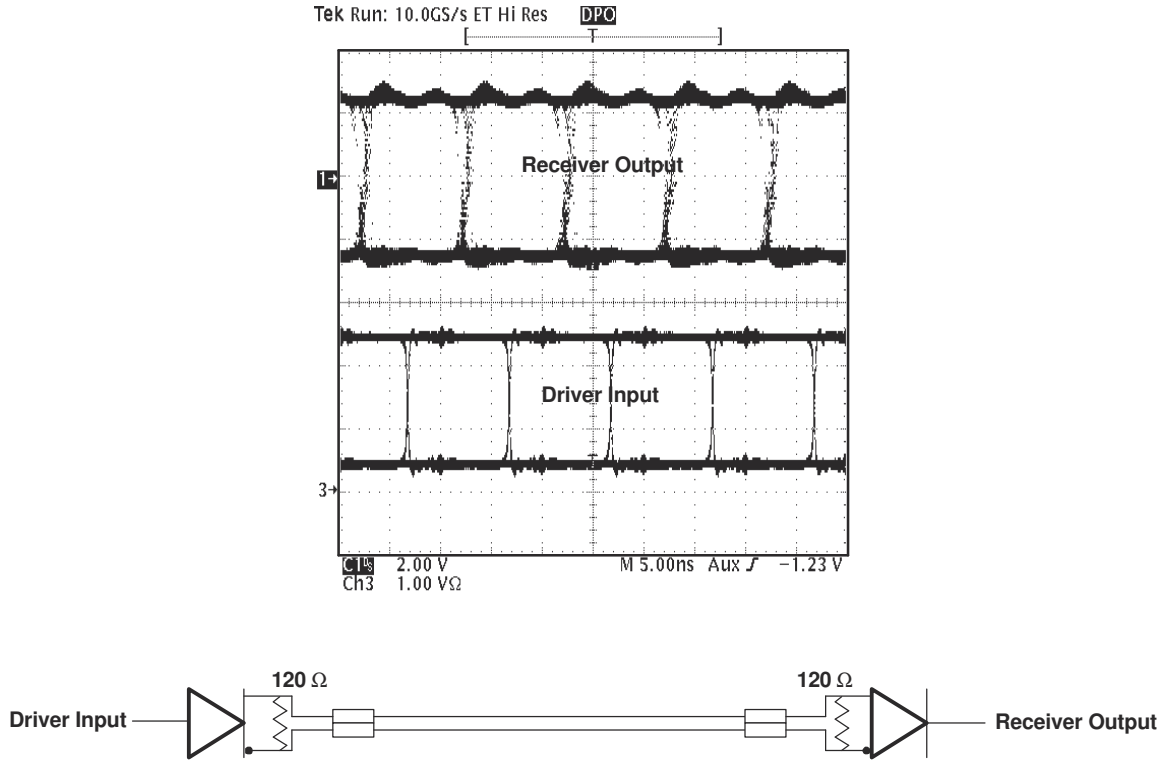


図 5-1. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

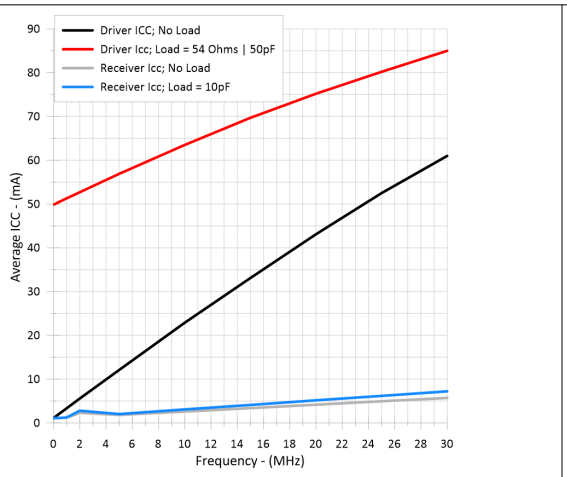


図 5-2. Average Supply Current vs Frequency

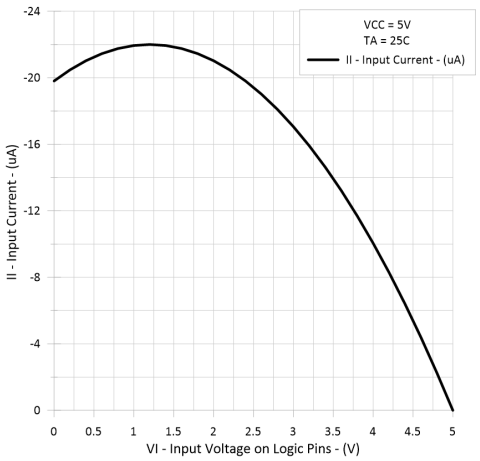


図 5-3. Logic Input Current vs Input Voltage

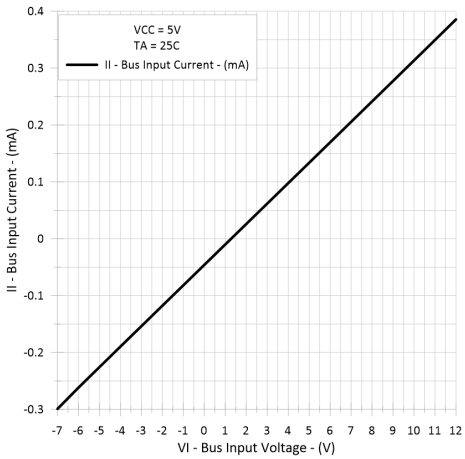


図 5-4. Input Current vs Input Voltage

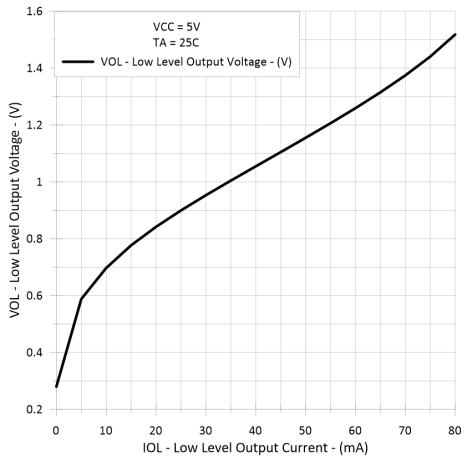


図 5-5. Low-Level Output Voltage vs Low-Level Output Current

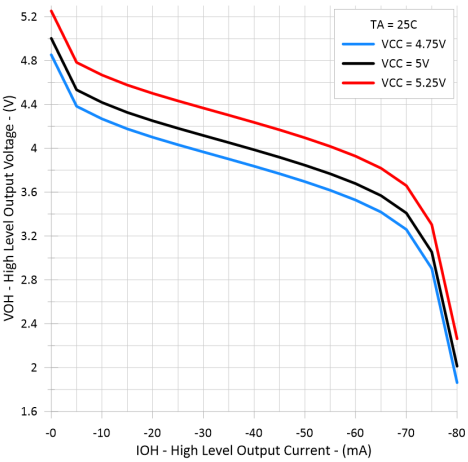


図 5-6. Driver High-Level Output Voltage vs HIGH-Level Output Current

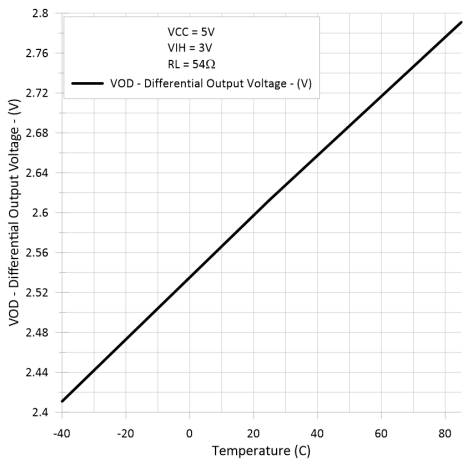


図 5-7. Driver Differential Output Voltage vs Average Case Temperature

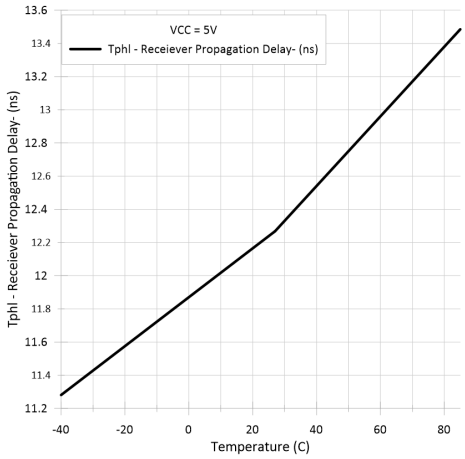


図 5-8. Receiver Propagation Time vs Case Temperature

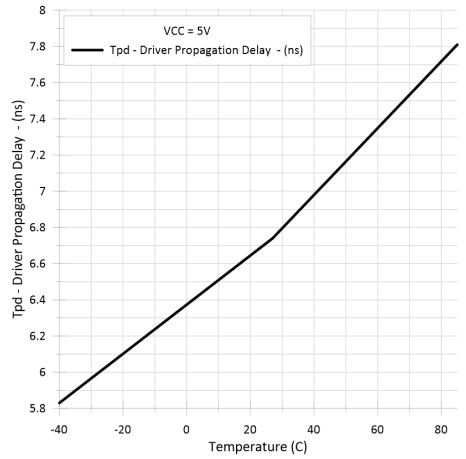


図 5-9. Driver Propagation Delay Time vs Case Temperature

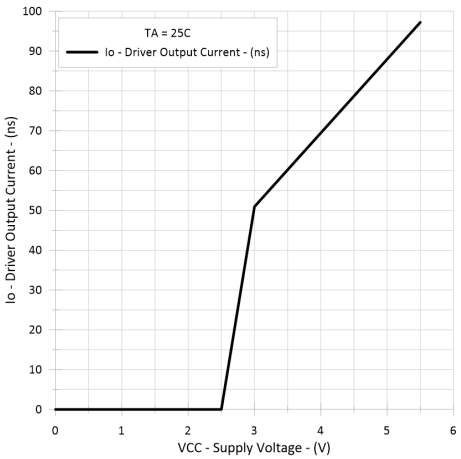


図 5-10. Driver Output Current vs Supply Voltage

6 Parameter Measurement Information

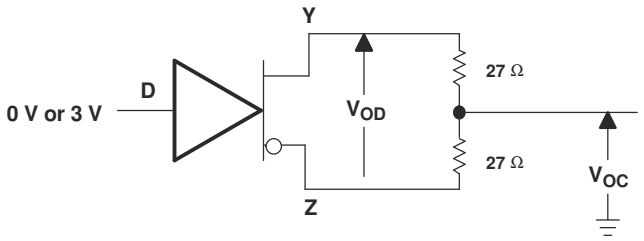


図 6-1. Driver V_{OD} and V_{OC}

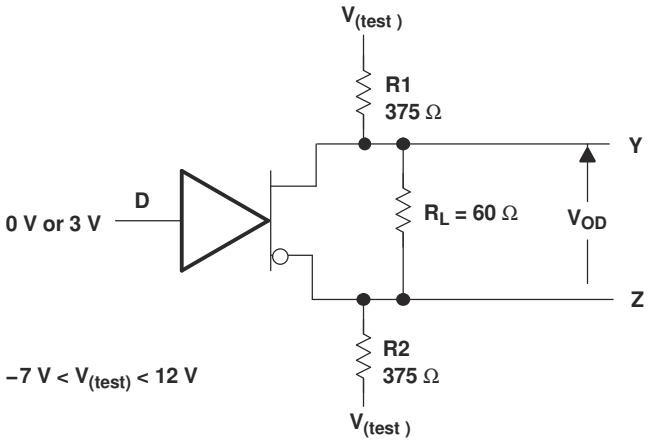
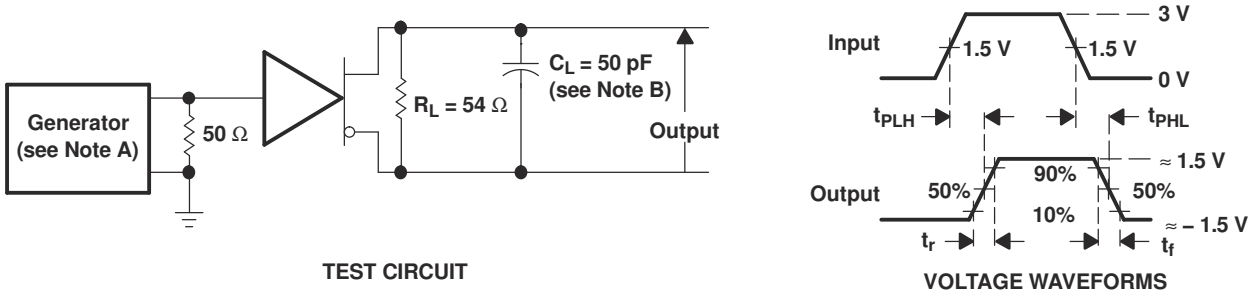


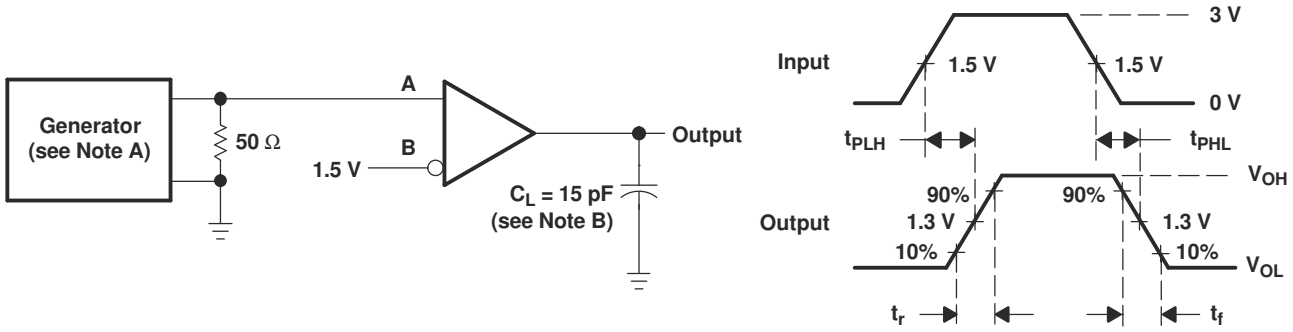
図 6-2. Driver V_{OD} With Common-Mode Loading



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

図 6-3. Driver Test Circuits and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. CL includes probe and jig capacitance.

図 6-4. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

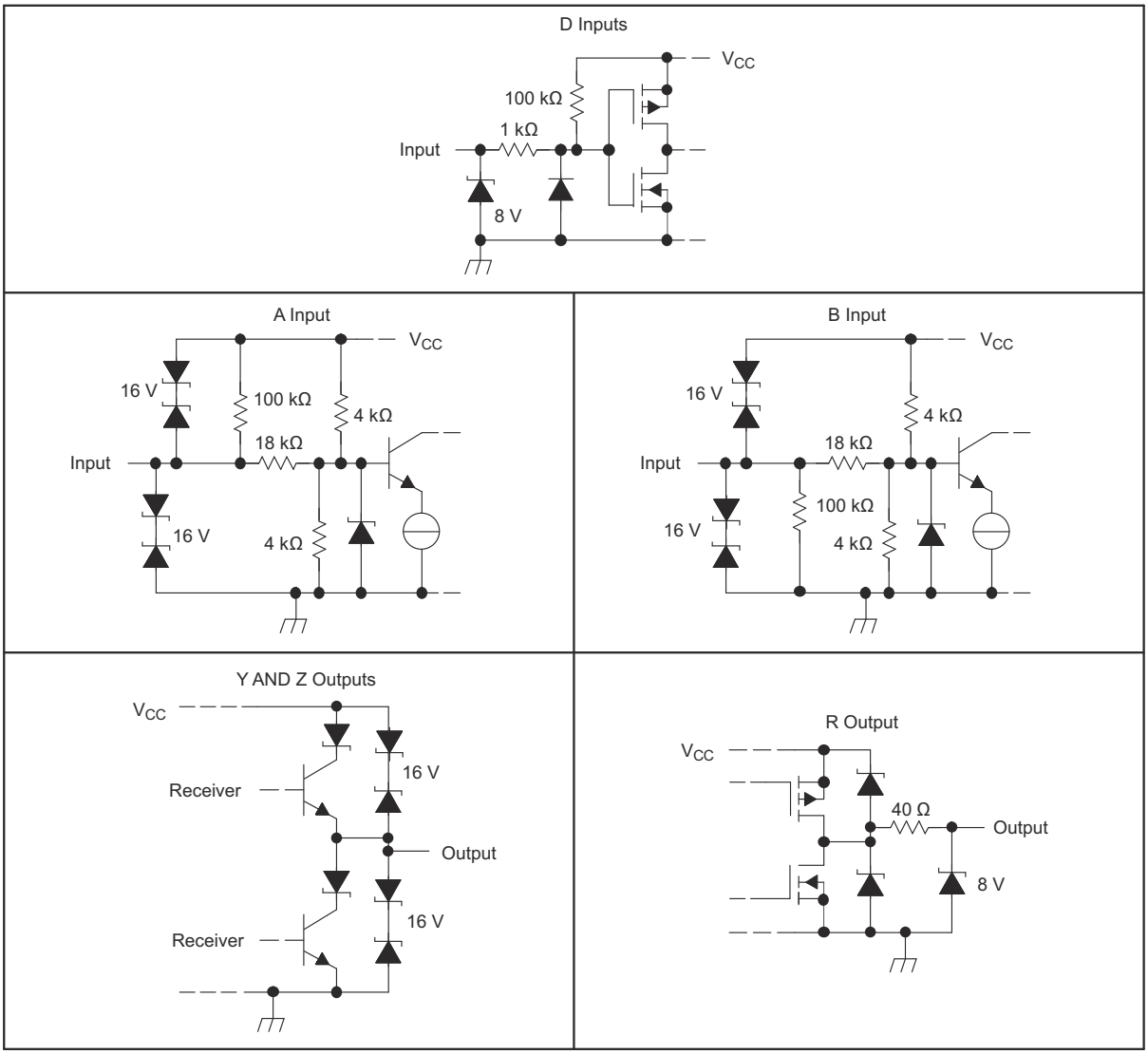
7.1.1 FUNCTION TABLE

DRIVER			RECEIVER	
INPUT D	OUTPUTS(1)		DIFFERENTIAL INPUTS A – B	OUTPUT R
	Y	Z	$V_{ID} \geq 0.2$ V	H
H	H	L	-0.2 V < V_{ID} < 0.2 V	?
L	L	H	$V_{ID} \leq$ -0.2 V	L
OPEN	H	L	Open circuit	H

(1) H = high level, L = low level, ? = indeterminate

7.1.2 Schematics

Schematics of Inputs and Output



8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

8.3 商標

LinBiCMOS™ and TI E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC179ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A	Samples
SN65LBC179ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A	Samples
SN65LBC179AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC179A	Samples
SN75LBC179AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC179A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

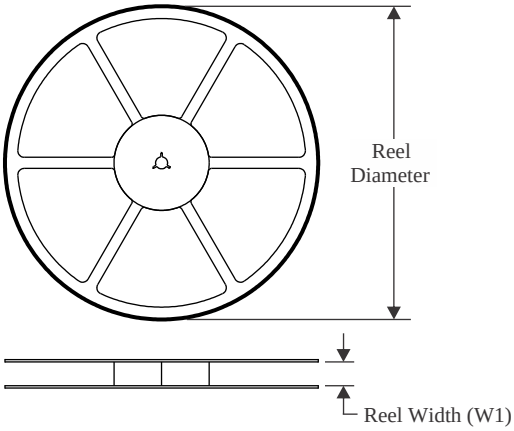
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

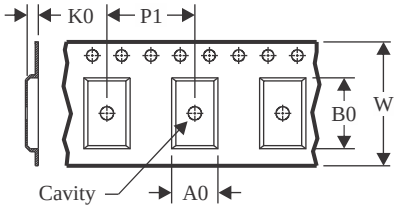
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

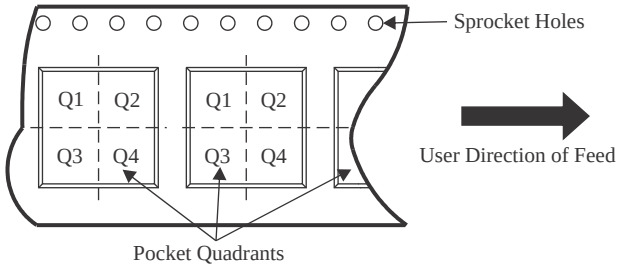


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

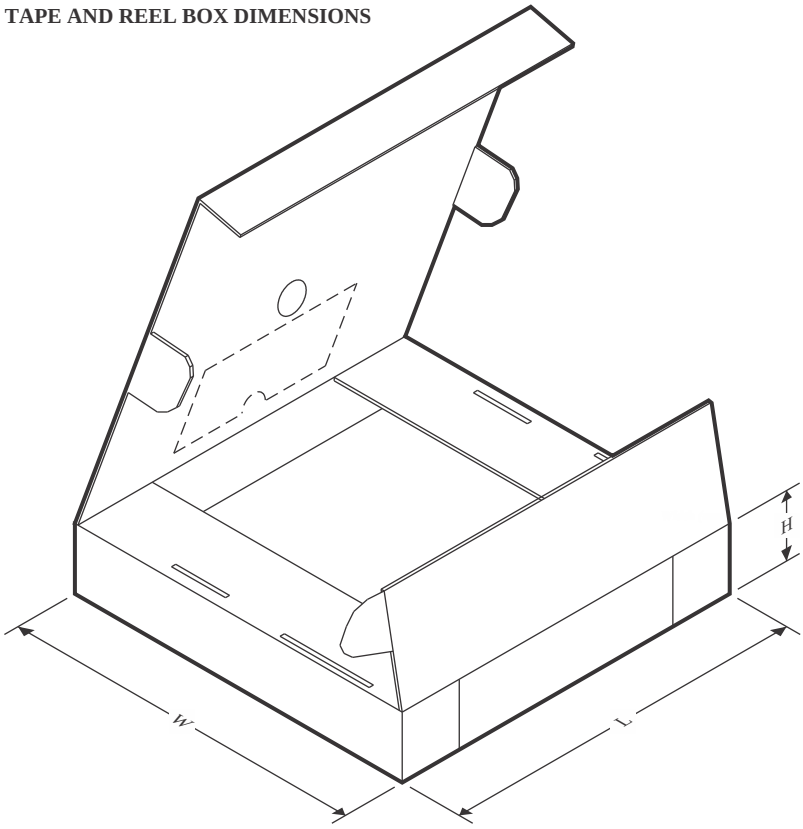
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC179ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

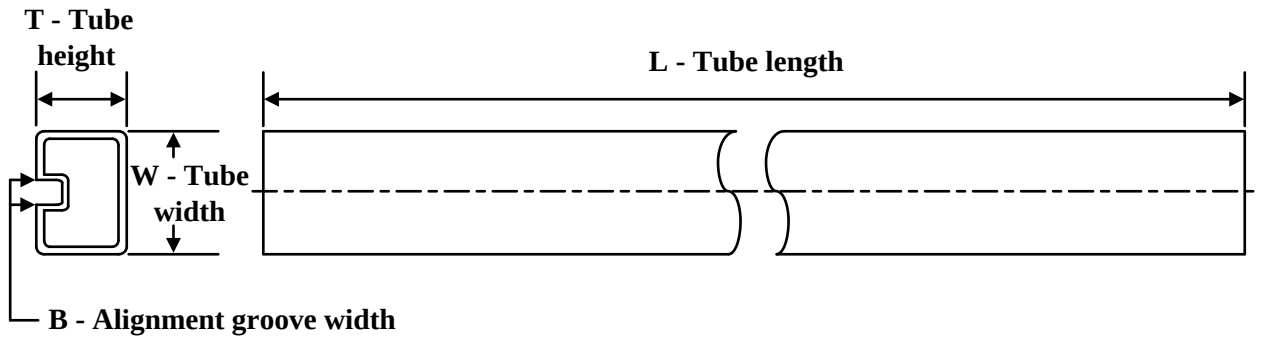
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC179ADR	SOIC	D	8	2500	356.0	356.0	35.0

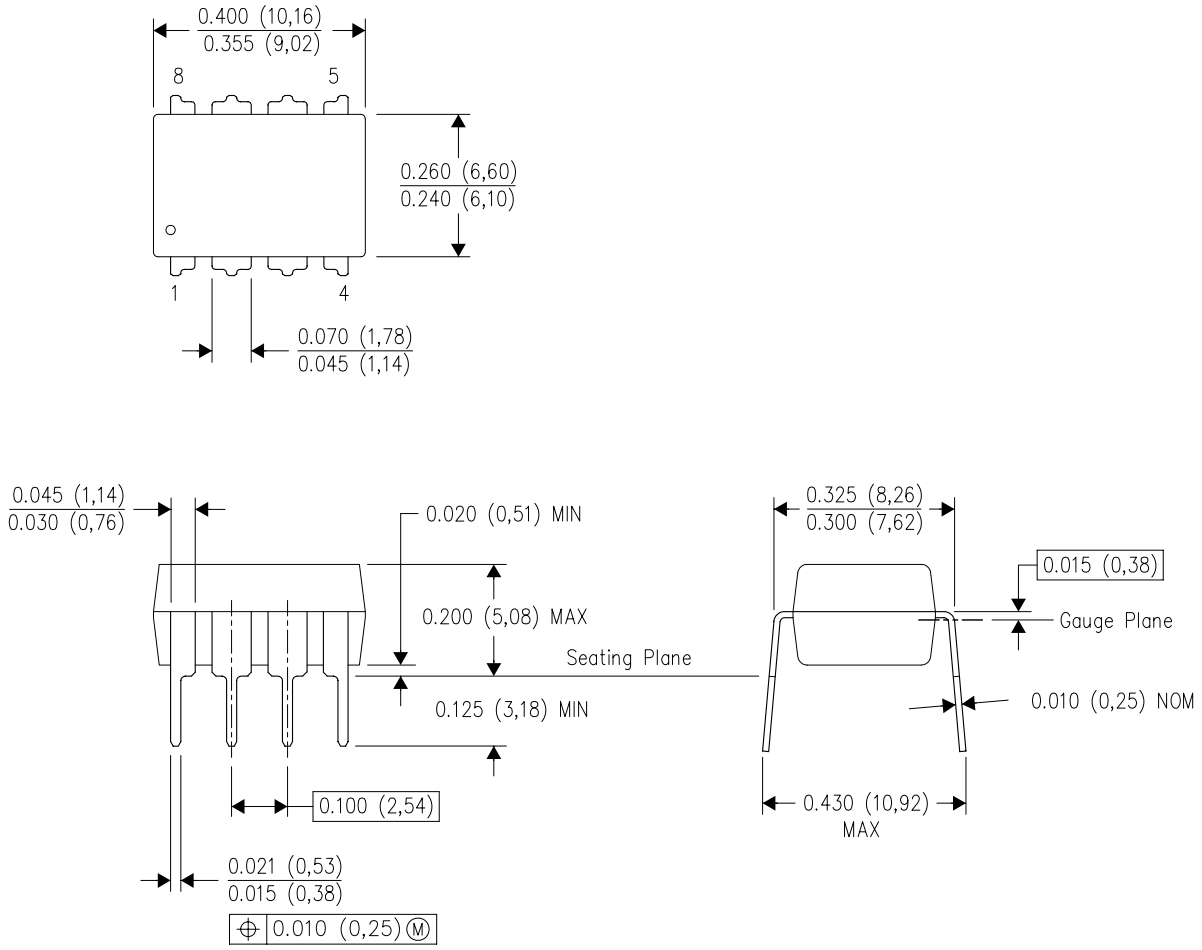
TUBE



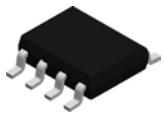
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC179AP	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC179AP	P	PDIP	8	50	506	13.97	11230	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

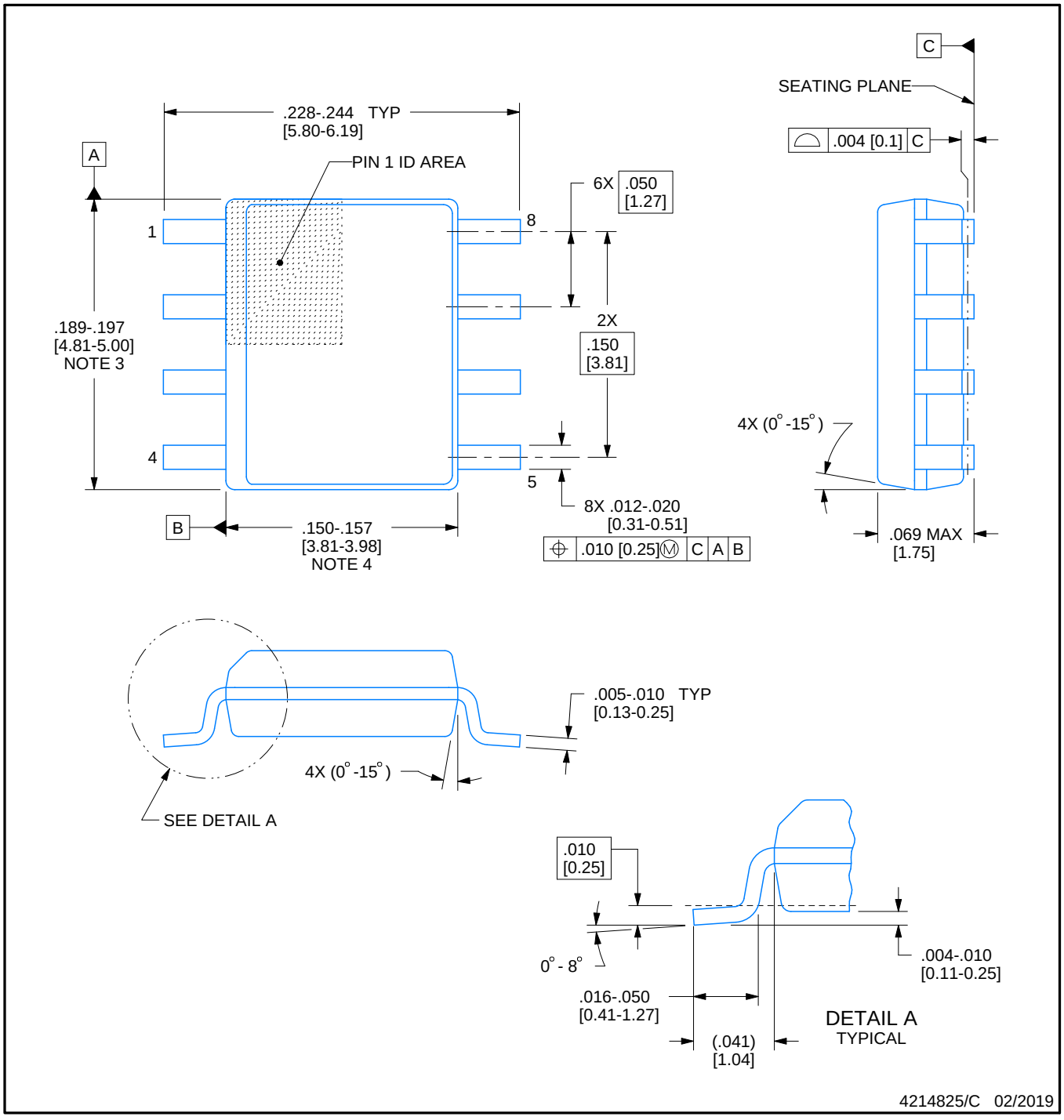


PACKAGE OUTLINE

D0008A

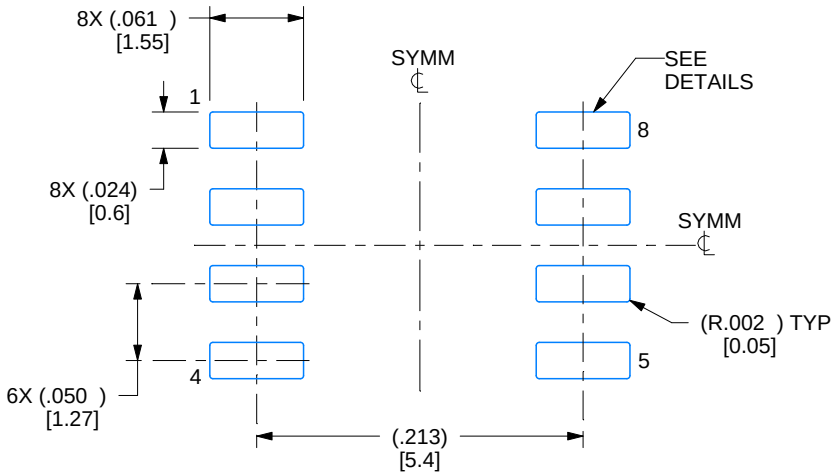
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

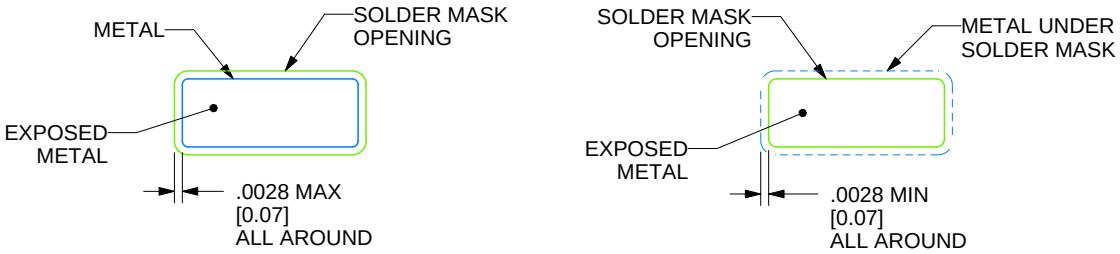


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

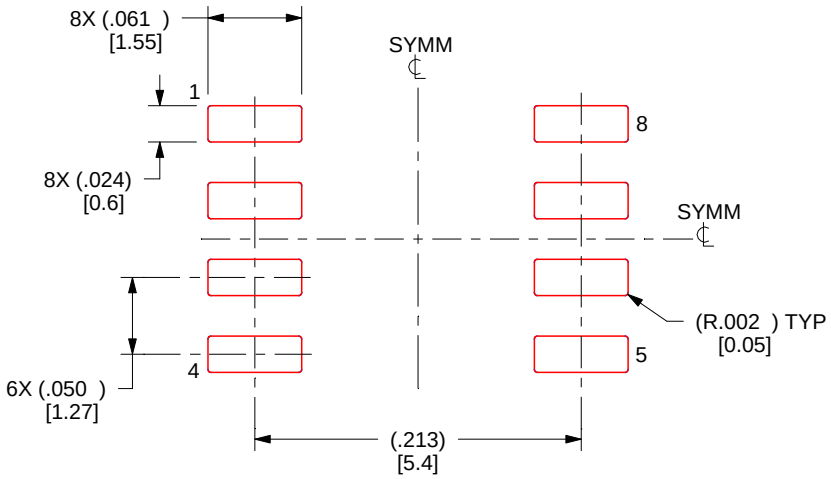
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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