

# SN74AHC367 3 ステート出力搭載、ヘキサ バッファおよびラインドライバ

## 1 特長

- 動作範囲 : 2V ~ 5.5V  $V_{CC}$
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

## 2 アプリケーション

- デジタル信号のイネーブルまたはディセーブル
- インジケータ LED の制御
- 通信モジュールとシステム・コントローラの変換

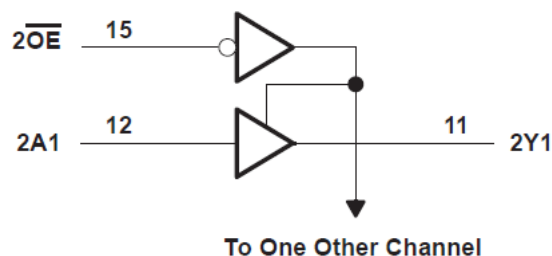
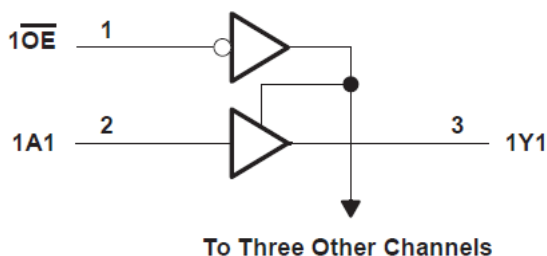
## 3 概要

'AHC367 デバイスは、 $V_{CC} = 2V \sim 5.5V$  で動作するように設計された、ヘキサ バッファおよびラインドライバです。

### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	パッケージ サイズ <sup>(2)</sup>	本体サイズ <sup>(3)</sup>
SN74AHC367	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.4mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ サイズ (長さ×幅) は公称値で、該当する場合はピンも含まれます。
- 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



論理図 (正論理)



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision E (February 2002) to Revision F (November 2023)

Page

• 「アプリケーション」セクション、「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加 .....	1
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## 5 Pin Configurations and Functions

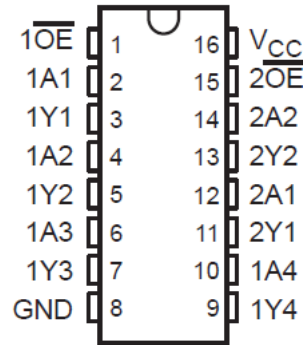


図 5-1. D, DB, DGV, N, or PW Package (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Output Enable 1
2	1A1	I	1A1 Input
3	1Y1	O	1Y1 Output
4	1A2	I	1A2 Input
5	1Y2	O	1Y2 Output
6	1A3	I	1A3 Input
7	1Y3	O	1Y3 Output
8	GND	—	Ground Pin
9	1Y4	O	1Y4 Output
10	1A4	I	1A4 Input
11	2Y1	O	2Y1 Output
12	2A1	I	2A1 Input
13	2Y2	O	2Y2 Output
14	2A2	I	2A2 Input
15	2 $\overline{OE}$	I	Output Enable 2
16	V <sub>CC</sub>	—	Power Pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage range	-0.5	7	V
V <sub>O</sub> <sup>(2)</sup>	Output voltage range	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0)	-20	mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0)	±20	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±75	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-Body Model (A114-A), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	V
		Charged-Device Model (C101), per JESD22-C101 <sup>(2)</sup>	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 3 V	2.1	
		V <sub>CC</sub> = 5.5 V	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 3 V	0.9	
		V <sub>CC</sub> = 5.5 V	1.65	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	-50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	-4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V	20	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC367					UNIT
		D	DB	DGV	N	PW	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	73	82	120	67	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN74AHC367		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			± 0.1	± 1	μA	
I <sub>OZ</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = V <sub>CC</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	5.5 V			± 0.25	± 2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4	40	μA	
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3	10	10	pF	
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		5.1			pF	

## 6.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		4.7 <sup>1</sup>	8.3 <sup>1</sup>	1	10	ns
t <sub>PHL</sub>					4.7 <sup>1</sup>	8.3 <sup>1</sup>	1	10	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		5.1 <sup>1</sup>	10.5 <sup>1</sup>	1	12.5	ns
t <sub>PZL</sub>					5.1 <sup>1</sup>	10.5 <sup>1</sup>	1	12.5	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		4 <sup>1</sup>	10.5 <sup>1</sup>	1	12.5	ns
t <sub>PLZ</sub>					4.91	10.51	1	12.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		6.1	11.8	1	13.5	ns
t <sub>PHL</sub>					6.2	11.8	1	13.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		6.4	14	1	16	ns
t <sub>PZL</sub>					6.8	14	1	16	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		6.2	13.6	1	15.5	ns
t <sub>PLZ</sub>					7.3	13.6	1	15.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$		3.4 <sup>1</sup>	5.9 <sup>1</sup>	1	7	ns
$t_{PHL}$					3.6 <sup>1</sup>	5.9 <sup>1</sup>	1	7	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		3.6 <sup>1</sup>	7.2 <sup>1</sup>	1	8.5	ns
$t_{PZL}$					3.8 <sup>1</sup>	7.2 <sup>1</sup>	1	8.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		2.6 <sup>1</sup>	7.2 <sup>1</sup>	0	8.5	ns
$t_{PLZ}$					2.6 <sup>1</sup>	7.2 <sup>1</sup>	0	8.5	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$		4.3	7.9	1	9	ns
$t_{PHL}$					4.5	7.9	1	9	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		4.6	9.2	1	10.5	ns
$t_{PZL}$					4.9	9.2	1	10.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		3.4	9.2	0	10.5	ns
$t_{PLZ}$					4.5	9.2	0	10.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.8 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

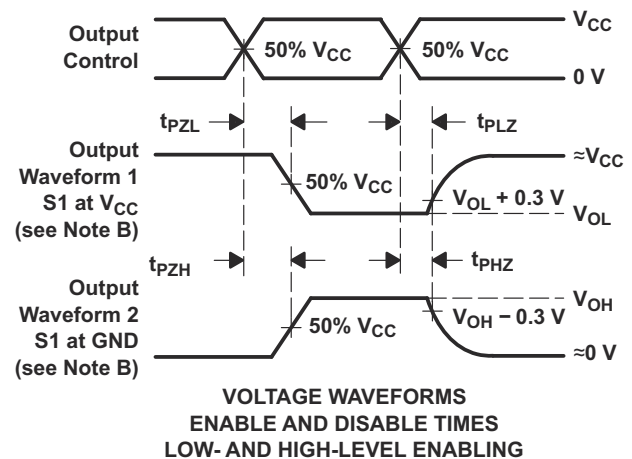
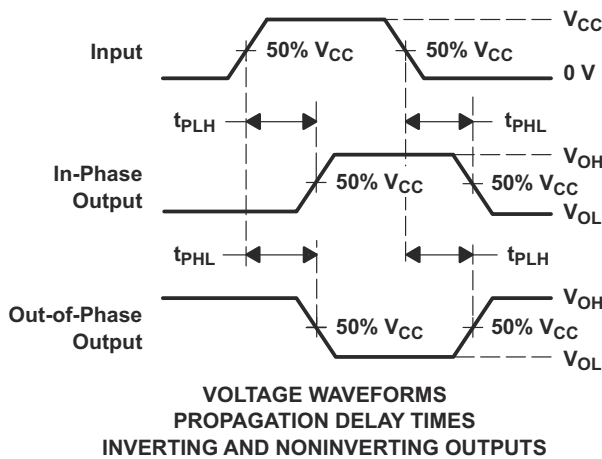
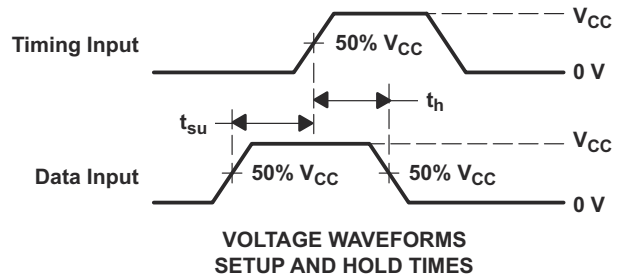
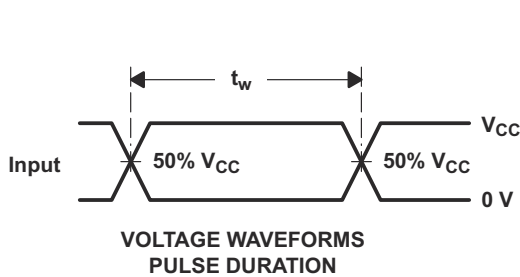
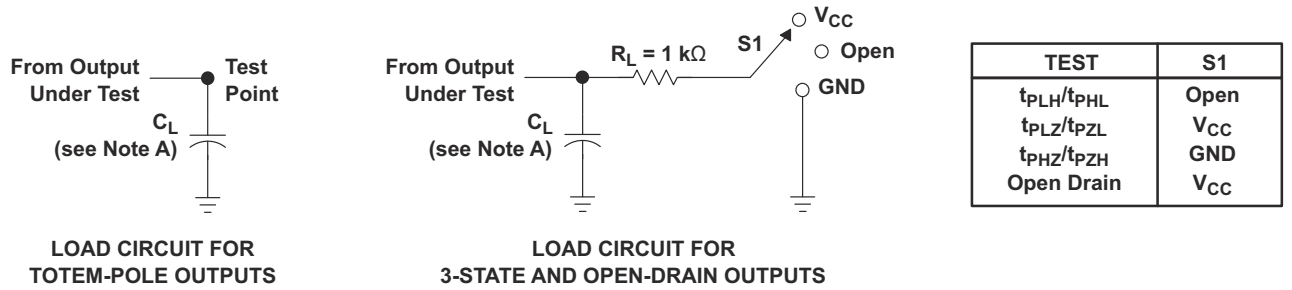
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.2		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

## 6.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	22.4	pF

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'AHC367 devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ( $\overline{1OE}$  and  $\overline{2OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



图 8-1. Logic Diagram (Positive Logic)

### 8.3 Device Functional Modes

表 8-1. Function Table  
(Each Buffer/ Driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Block Diagram. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74AHC367 is used to directly control the  $\overline{\text{RESET}}$  pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

### 9.2 Typical Application

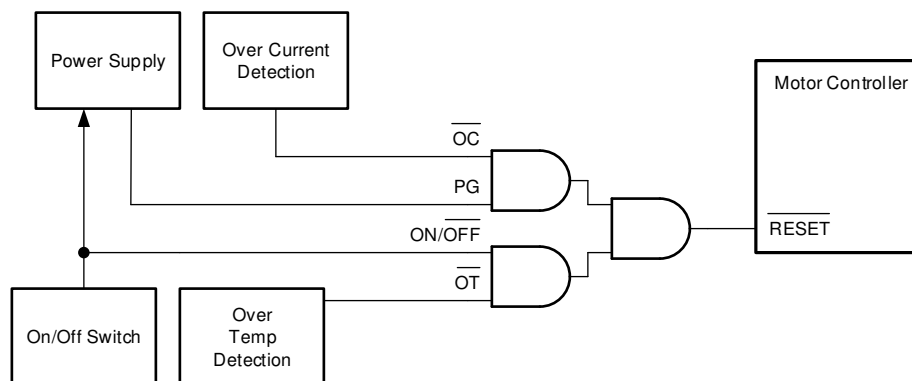


図 9-1. Typical Application Block Diagram

### 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

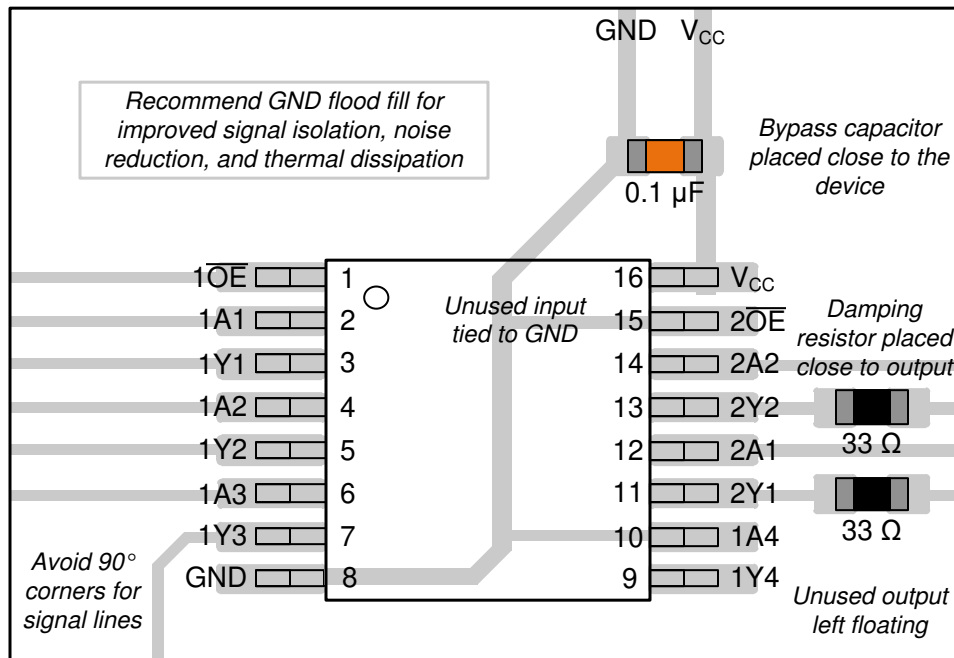


図 9-2. Example Layout for the SN74AHC367

## 10 Device and Documentation Support

### 10.1 Documentation Support (Analog)

#### 10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 10-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC367	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

#### 10.3 サポート・リソース

**テキサス・インスツルメンツ E2E™ サポート・フォーラム** は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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#### 10.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.  
すべての商標は、それぞれの所有者に帰属します。

#### 10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

#### 10.6 用語集

**テキサス・インスツルメンツ用語集** この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC367DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC367	<a href="#">Samples</a>
SN74AHC367N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC367N	<a href="#">Samples</a>
SN74AHC367PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA367	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

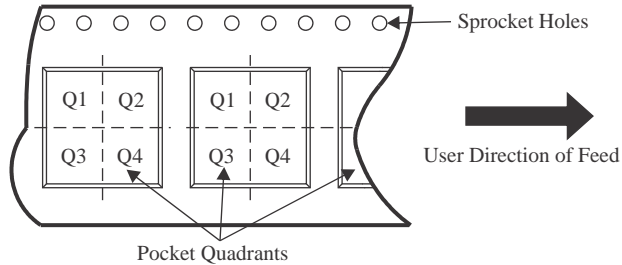
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


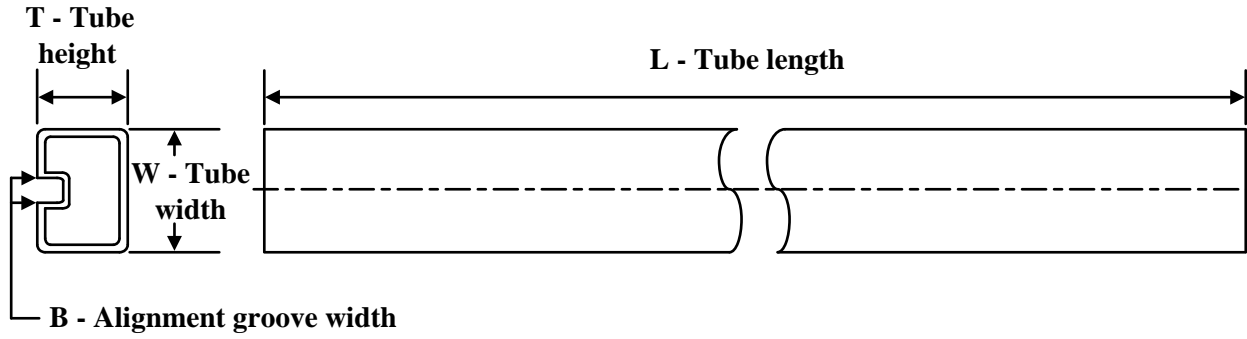
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC367DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC367PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC367DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC367PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC367N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC367N	N	PDIP	16	25	506	13.97	11230	4.32



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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