

SN74AHCT174 クリア搭載、ヘキサ D タイプ・フリップ・フロップ

1 特長

- 入力は TTL 電圧互換
- シングル レール 出力を備えた 6 つのフリップ フロップ を内蔵
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- バッファ / ストレージ・レジスタ
- シフト・レジスタ
- パターン・ジェネレータ

3 概要

これらのポジティブ エッジトリガ D タイプ フリップ フロップ はダイレクト クリア (**CLR**) 入力を備えています。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ ⁽²⁾	本体サイズ ⁽³⁾
SN74AHCT174	D (SOIC, 16)	9.9mm × 6mm	9.00mm × 3.90mm
	DB (SSOP, 16)	6.2mm × 7.8mm	6.2mm × 5.3mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	NS (SOP, 16)	10.2mm × 7.8mm	10.2mm × 5.3mm
	PW (TSSOP, 16)	5mm × 6.4mm	5.00mm × 4.40mm

- (1) 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。

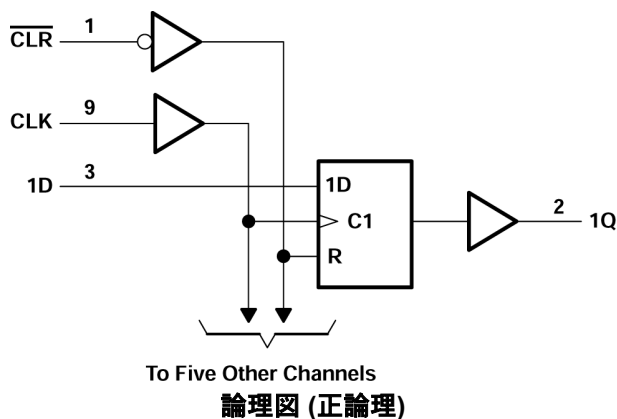


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4 Pin Configuration and Functions

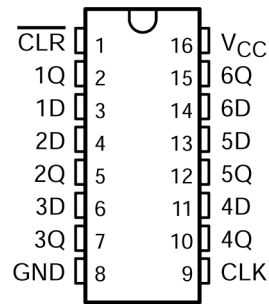


図 4-1. Package SN74AHCT174 D, DB, DGV, N, NS, or PW Package (Top View)

表 4-1. Pin Functions

PIN		I/O (1)	DESCRIPTION
NO.	NAME		
1	CLR	I	Clear all channels, active low
2	1Q	O	Channel 1, Q output
3	1D	I	Channel 1, D input
4	2D	I	Channel 2, D input
5	2Q	O	Channel 2, Q output
6	3D	I	Channel 3, D input
7	3Q	O	Channel 3, Q output
8	GND	—	Ground
9	CLK	I	Clock all channels, rising edge triggered
10	4Q	O	Channel 4, Q output
11	4D	I	Channel 4, D input
12	5Q	O	Channel 5, Q output
13	5D	I	Channel 5, D input
14	6D	I	Channel 6, D input
15	6Q	O	Channel 6, Q output
16	V _{CC}	—	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ¹	Input voltage range	-0.5	7	V
V _O ¹	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)	-20	mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})	±20	mA
I _O	Continuous output current	(V _O = 0 to V _{CC})	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

(over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74AHCT174		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-8	mA
I _{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall time		20	ns/V
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHCT174						UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		16 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	73	82	120	67	64	135.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25 °C			SN74AHCT174		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		V
	I _{OH} = -8 mA		3.94			3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	μA
ΔI _{CC} ⁽¹⁾	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5	μA
C _i	V _I = V _{CC} or GND	5 V		2	10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

5.6 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T _A = 25°C		SN74AHCT174		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	5		5		ns
		CLK high or low	5		5		
t _{su}	Setup time before CLK ↑	Data	5		5		ns
		CLR inactive	3.5		3.5		
t _h	Hold time, data after CLK ↑		0		0		ns

5.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN74AHCT174		UNIT
				MIN	TYP	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	100 ⁽¹⁾	135 ⁽¹⁾		80		MHz
			C _L = 50 pF	80	115		65		
t _{PHL}	CLR	Any Q	C _L = 15 pF		7.6 ⁽¹⁾	10.4 ⁽¹⁾	1	13	ns
t _{PLH}	CLK	Any Q	C _L = 15 pF		5.8 ⁽¹⁾	7.8 ⁽¹⁾	1	9	ns
t _{PHL}					5.8 ⁽¹⁾	7.8 ⁽¹⁾	1	9	
t _{PHL}	CLR	Any Q	C _L = 50 pF		8.1	11.4	1	13	ns
t _{PLH}	CLK	Any Q	C _L = 50 pF		6.3	8.8	1	10	ns
t _{PHL}					6.3	8.8	1	10	
t _{sk(o)}			C _L = 50 pF			1 ⁽²⁾		1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C ⁽¹⁾

PARAMETER	DESCRIPTION	SN74AHCT174			UNIT
		MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.8		V

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JAJ5QB5H – JUNE 1998 – REVISED JULY 2024

 $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}^{(1)}$

PARAMETER		SN74AHCT174			UNIT
		MIN	TYP	MAX	
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

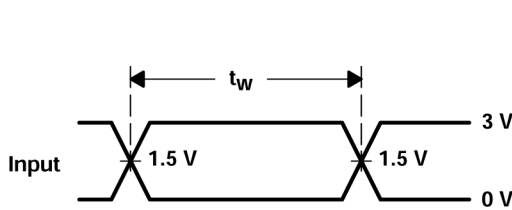
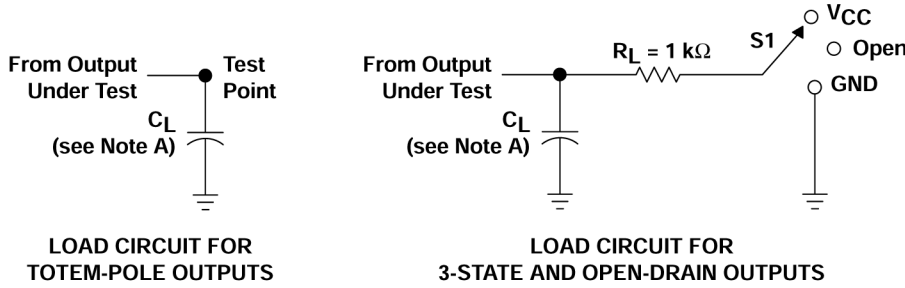
(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

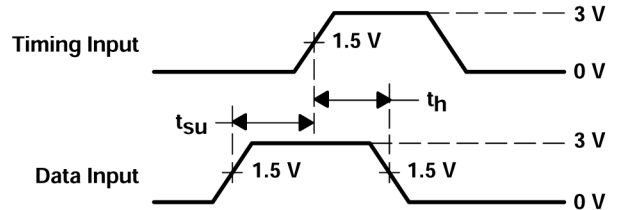
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	28	pF

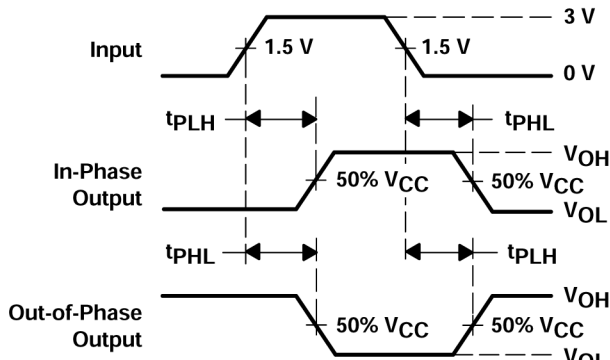
6 Parameter Measurement Information



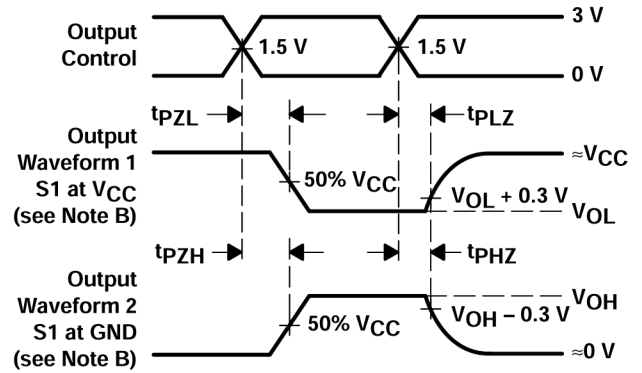
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

图 6-1. Load Circuit and Voltage Waveforms

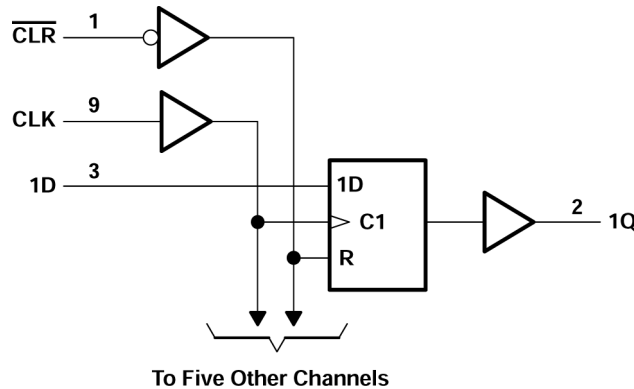
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

7 Detailed Description

7.1 Overview

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

7.2 Functional Block Diagram



☒ 7-1. Logic Diagram (Positive Logic)

Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS ⁽¹⁾			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q _o

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

8 Application and Implementation

注

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8.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [セクション 5.3](#).

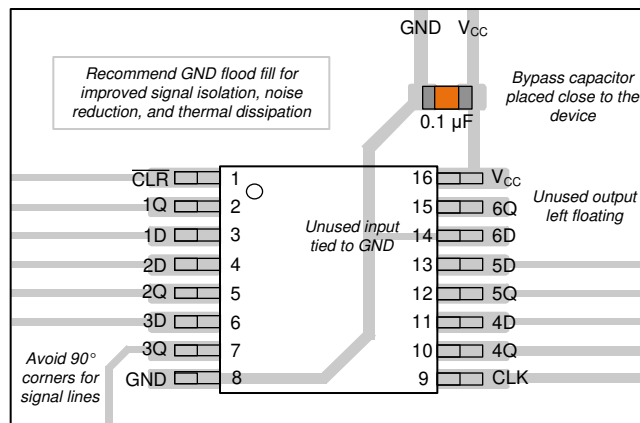
Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1.0 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.2.2 Layout Example



☒ 8-1. Example layout for the SN74AHCT174 in the PW package.

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT174	Click here	Click here	Click here	Click here	Click here

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (May 2023) to Revision H (July 2024)	Page
• 「パッケージ情報」表にパッケージ サイズを追加.....	1
• Deleted machine model from <i>ESD Ratings</i> table.....	4
• Updated RθJA value: PW = 108 to 135.9, all values in °C/W.....	4
• Added <i>Application and Implementation</i> section.....	9
• Added <i>Device and Documentation Support</i> section	10

Changes from Revision F (April 2002) to Revision G (May 2023)

Page

- 「アプリケーション」「パッケージ情報」表、「ピン機能」表、「熱に関する情報」表を追加 **1**
-

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT174D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	AHCT174	
SN74AHCT174DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB174	Samples
SN74AHCT174DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT174	Samples
SN74AHCT174N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT174N	Samples
SN74AHCT174NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT174	Samples
SN74AHCT174PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HB174	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

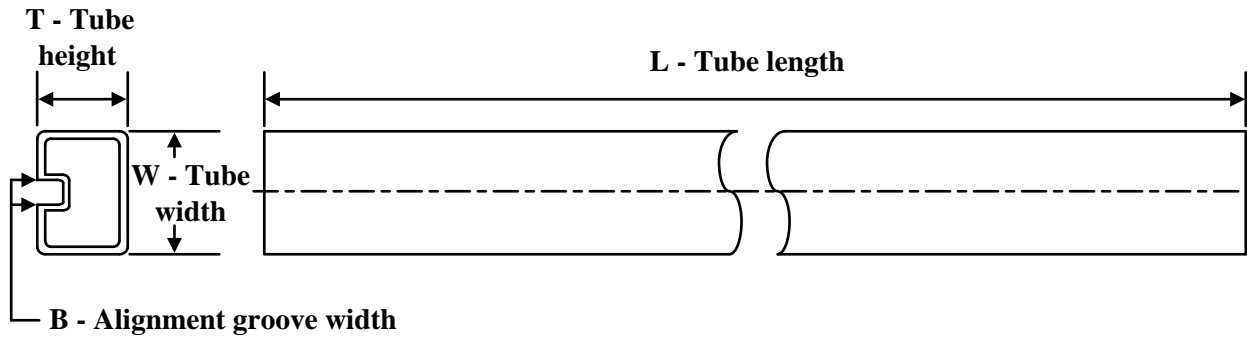
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT174DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT174DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT174NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT174PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT174PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT174DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHCT174DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT174NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74AHCT174PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHCT174PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT174N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT174N	N	PDIP	16	25	506	13.97	11230	4.32



PACKAGE OUTLINE

NS0016A

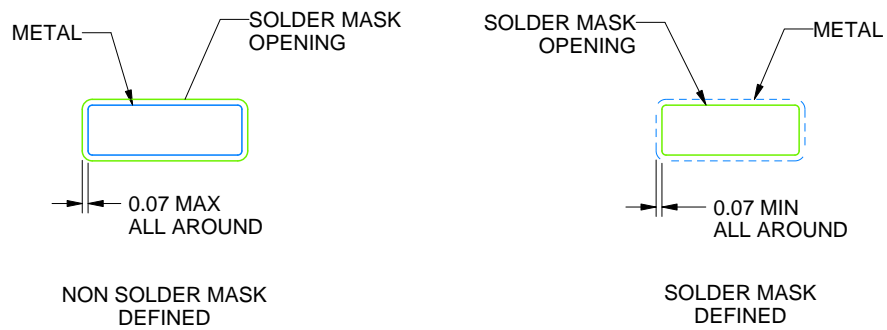
SOP - 2.00 mm max height

SOP



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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