

## SN74AHCT245-Q1 車載用、3 ステート出力、オクタール・バス・トランシーバ

### 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1: -40°C ~ +125°C, T<sub>A</sub>
- 入力は TTL 電圧互換
- JESD 17 準拠で 250mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン・モデル (A115-A)
  - 1000V、デバイス帯電モデル (C101)

### 2 アプリケーション

- デジタル信号のイネーブルまたはディセーブル
- コントローラ・リセット時の信号保持
- スイッチのデバウンス

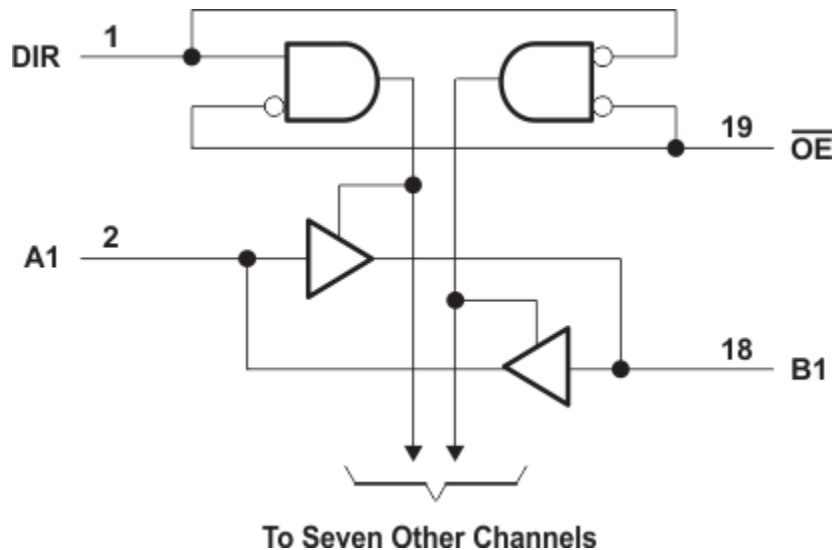
### 3 概要

SN74AHCT245-Q1 オクタール・バス・トランシーバは、データ・バス間の非同期双方向通信用に設計されています。これらの部品は、4.5V ~ 5.5V で動作します。

#### パッケージ情報<sup>(1)</sup>

部品番号	パッケージ	本体サイズ (公称)
SN74AHCT245-Q1	PW (TSSOP, 20)	6.50mm × 4.40mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図



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## 4 Revision History

DATE	REVISION	NOTES
August 2022	*	Initial Release

## 5 Pin Configuration and Functions

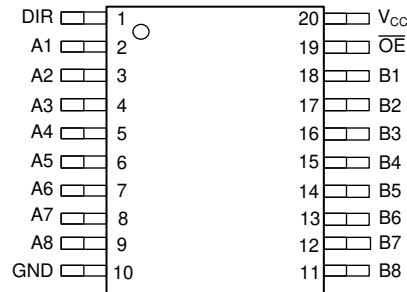


图 5-1. SN74AHCT245-Q1: PW Package, 20-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
DIR	1	—	Direction Pin
A1	2	I/O	A1 Input/Output
A2	3	I/O	A2 Input/Output
A3	4	I/O	A3 Input/Output
A4	5	I/O	A4 Input/Output
A5	6	I/O	A5 Input/Output
A6	7	I/O	A6 Input/Output
A7	8	I/O	A7 Input/Output
A8	9	I/O	A8 Input/Output
GND	10	—	Ground Pin
B8	11	I/O	B8 Input/Output
B7	12	I/O	B7 Input/Output
B6	13	I/O	B6 Input/Output
B5	14	I/O	B5 Input/Output
B4	15	I/O	B4 Input/Output
B3	16	I/O	B3 Input/Output
B2	17	I/O	B2 Input/Output
B1	18	I/O	B1 Input/Output
OE	19	I	Output Enable
VCC	20	—	Power Pin

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	Control inputs	-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±75	mA

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range		-65	150	°C
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup>		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B		±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN74AHCT245-Q1		UNIT
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level Input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input Transition rise and fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT245-Q1		UNIT
		PW		
		20 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.8		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	36.8		
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.8		
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.5		
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.3		
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4	4.5		4.4		V
	I <sub>OH</sub> = –8 mA		3.94			3.7		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	V
	I <sub>OH</sub> = 8 mA				0.36		0.44	
I <sub>I</sub>	OE or DIR	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±0.1		±1	μA
I <sub>OZ</sub>	A or B inputs <sup>(1)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±.25		±2.5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4		40	μA
ΔI <sub>CC</sub> <sup>(2)</sup>		One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V		1.35		1.5	mA
C <sub>i</sub>	OE or DIR	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	2.5	10			pF
C <sub>io</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4				pF

(1) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				TYP	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	$C_L = 15\text{ pF}$	4.5	7.7	1	10	ns
$t_{PHL}$				4.5	7.7	1	10	
$t_{PZH}$	OE	A or B	$C_L = 15\text{ pF}$	8.9	13.8	1	16	ns
$t_{PZL}$				8.9	13.8	1	16	
$t_{PHZ}$	OE	A or B	$C_L = 15\text{ pF}$	9.2	14.4	1	16.5	ns
$t_{PLZ}$				9.2	14.4	1	16.5	
$t_{PLH}$	A or B	B or A	$C_L = 50\text{ pF}$	5.3	8.7	1	11	ns
$t_{PHL}$				5.3	8.7	1	11	
$t_{PZH}$	OE	A or B	$C_L = 50\text{ pF}$	9.7	14.8	1	17	ns
$t_{PZL}$				9.7	14.8	1	17	
$t_{PHZ}$	OE	A or B	$C_L = 50\text{ pF}$	10	15.4	1	17.5	ns
$t_{PLZ}$				10	15.4	1	17.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1			ns

## 6.7 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER	SN74AHCT245-Q1			UNIT
	MIN	TYP	MAX	
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

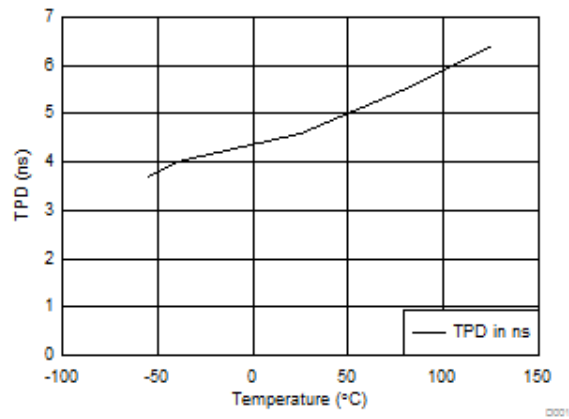
(1) Characteristics are for surface-mount packages only.

## 6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

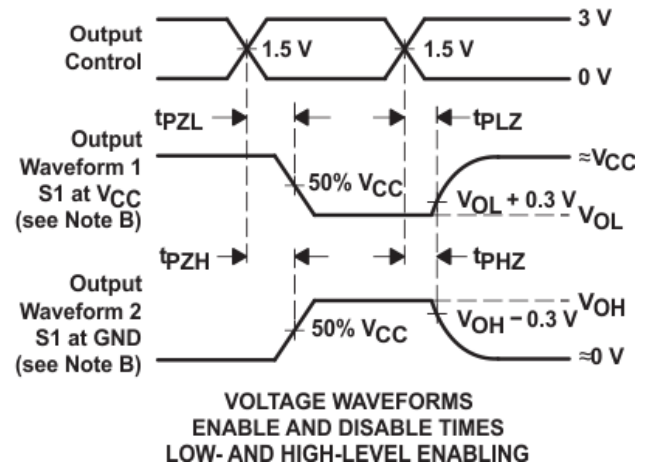
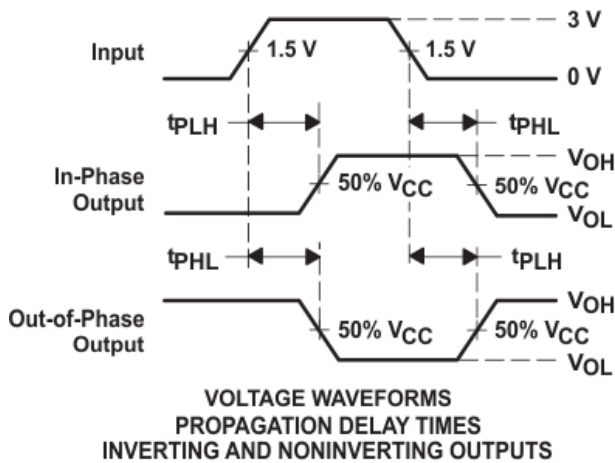
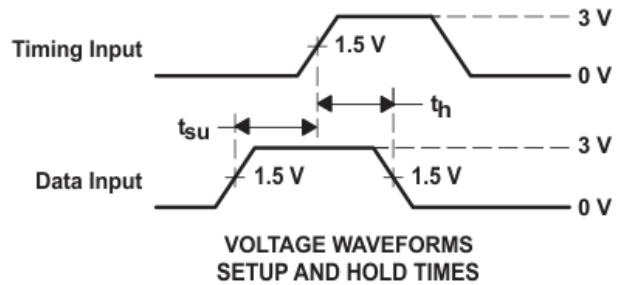
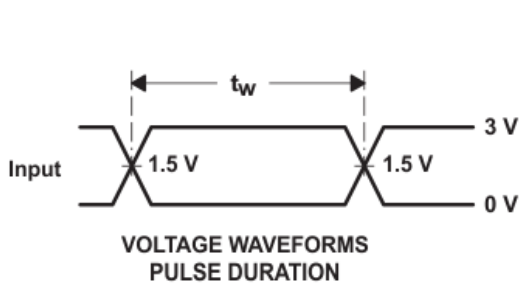
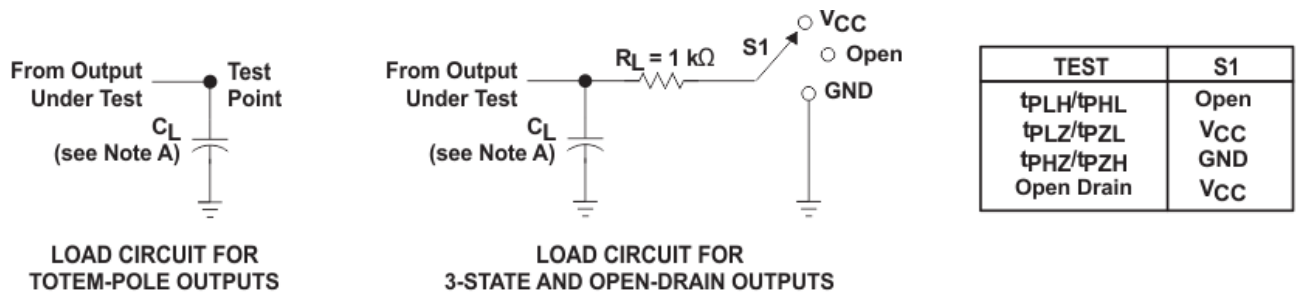
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	13	pF

## 6.9 Typical Characteristics



6-1. SN74AHCT245 TPD vs Temperature, 15 pF Load

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

 **7-1. Load Circuit and Voltage Waveforms**



## 8 Detailed Description

### 8.1 Overview

The SNx7AHT245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SN74AHCT245-Q1 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses effectively are isolated. For the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram

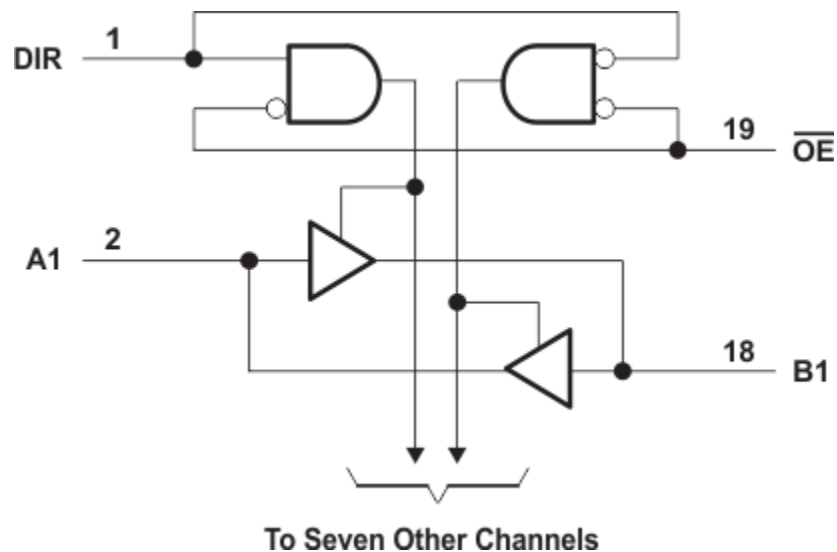


图 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

- $V_{CC}$  is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
  - Inputs accept  $V_{IH}$  levels of 2 V
- Slow edge rates minimize output ringing

### 8.4 Device Functional Modes

表 8-1. Function Table  
(Each Transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The SN74AHCT245 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of  $0.8 V_{IL}$  and  $2 V_{IH}$ . This feature makes it ideal for translating up from 3.3 V to 5 V. The following figure shows this type of translation.

### 9.2 Typical Application

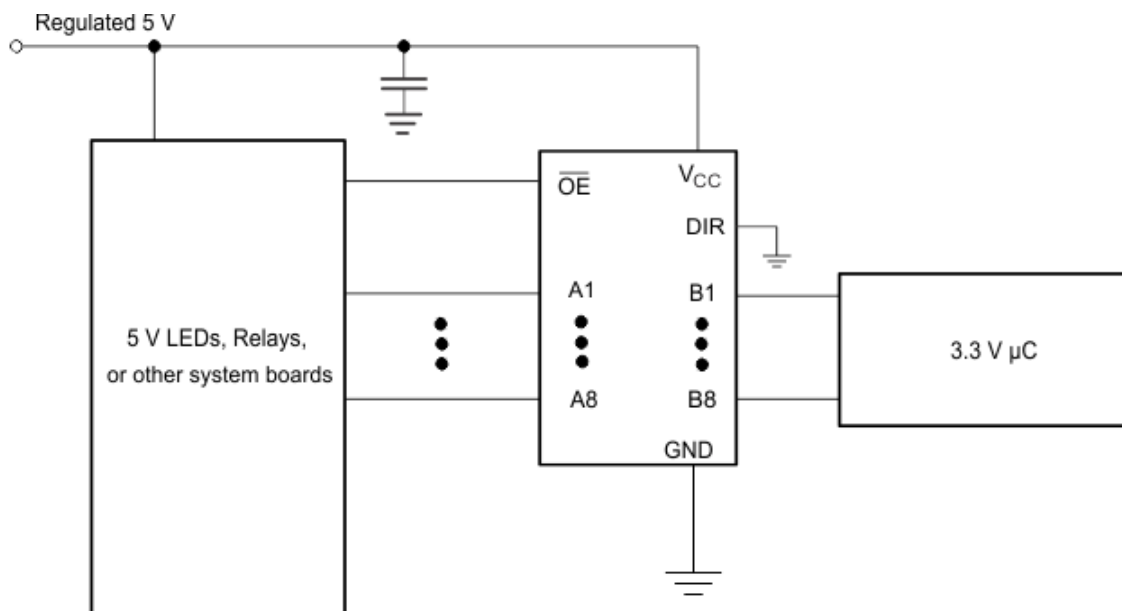


図 9-1. Typical Application Diagram

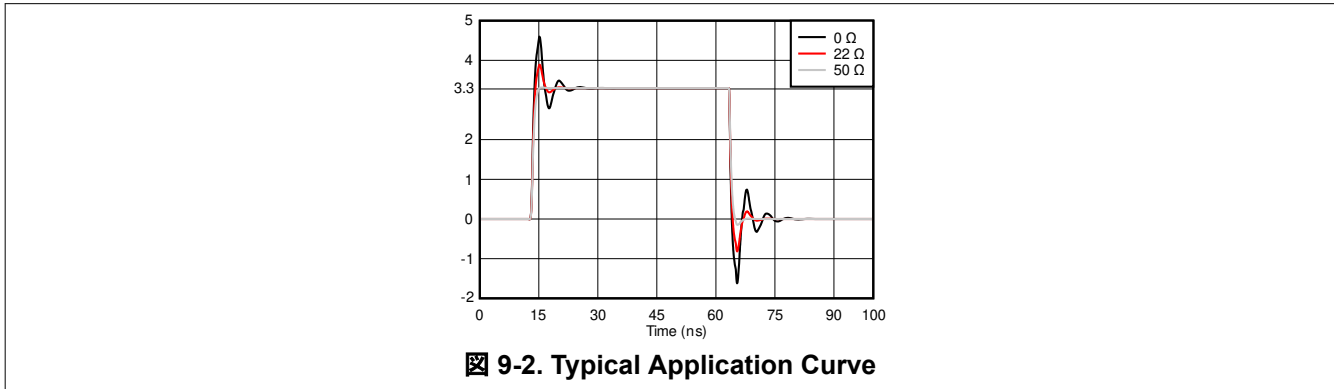
#### 9.2.1 Design Requirements

This device uses CMOS technology and has a balanced output drive. Take care to avoid bus contention, because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommend output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{f}$  is recommended; if there are multiple VCC pins, then 0.01  $\mu\text{f}$  or 0.022  $\mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu\text{f}$  and a 1  $\mu\text{f}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

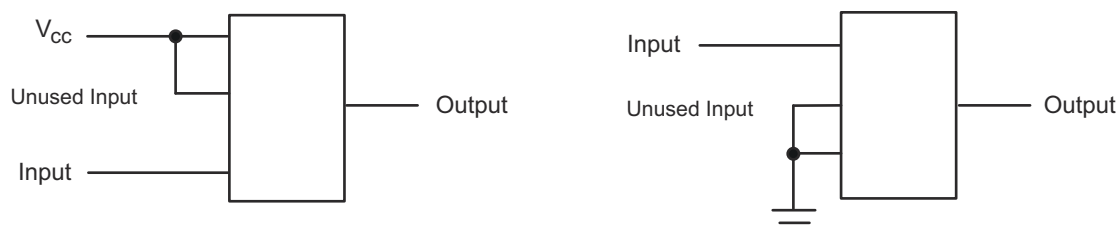
## 11 Layout

### 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 11-1](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 11.2 Layout Example



**11-1. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.2 サポート・リソース

**TI E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT245QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT245Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AHCT245-Q1 :**

- Catalog : [SN74AHCT245](#)
- Military : [SN54AHCT245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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