

SNx4AHCT373 3 ステート出力、オクタール・トランスペアレント D タイプ・ラッチ

1 特長

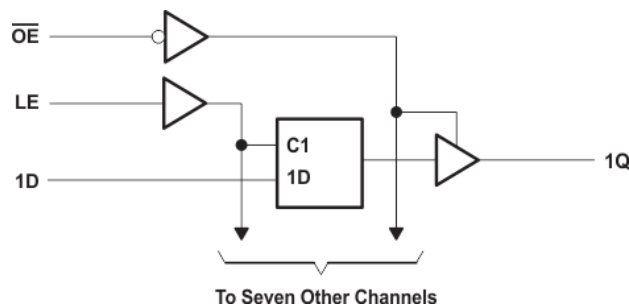
- 入力は TTL 電圧互換
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 概要

'AHCT373 デバイスはオクタール・トランスペアレント D タイプ・ラッチです。ラッチ・イネーブル (LE) 入力が HIGH の場合、Q 出力はデータ (D) 入力に従います。LE を LOW にすると、D 入力のロジック・レベルで Q 出力がラッチされます。

製品情報

部品番号	パッケージ ¹	本体サイズ ²
SN54AHCT373	J (CDIP, 20)	24.2mm × 6.92mm
	W (CFP, 20)	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm
SN74AHCT373	DB (SSOP, 20)	7.20mm × 5.30mm
	DW (SOIC, 20)	12.80mm × 7.50mm
	NS (SOP, 20)	12.6mm × 5.3mm
	N (PDIP, 20)	25.40mm × 6.35mm
	PW (TSSOP, 20)	6.50mm × 4.40mm



論理図 (正論理)



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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (July 2023) to Revision N (August 2023)	Page
<ul style="list-style-type: none"> 「製品情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 	1

4 Pin Configuration and Functions

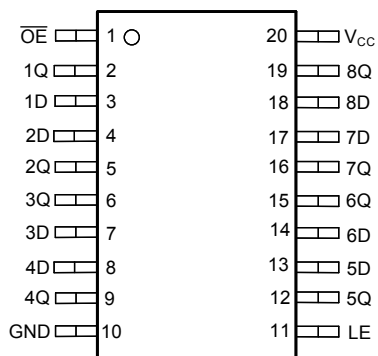


图 4-1. SN54AHCT373 J or W Package;
SN74AHCT373 DB, DGV, DW, N, NS, or PW
Package (Top View)

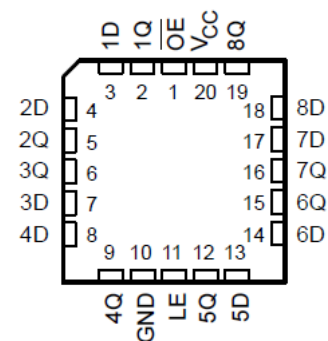


图 4-2. SN54AHCT373 FK Package (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OE	I	Output Enable
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground
11	LE	I	Latch Enable
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	V _{CC}	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽¹⁾	-0.5	7	V
V _O	Output voltage range ⁽¹⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±75	mA
T _{stg}	Storage temperature	-65	150	°C

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		Value	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHCT373						UNIT
	DW	DB	DGV	N	NS	PW	
	20 PINS						
R _{θJA} Junction-to-ambient thermal resistance	58	70	92	69	60	83	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT373		SN74AHCT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1			0.1	V	
	I _{OL} = 8 mA				0.36			0.44		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			± 0.25			± 2.5	μA	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			± 0.1			± 1 ⁽¹⁾	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4			40	μA	
ΔI _{CC†}	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35			1.5	mA	
C _i	V _I = V _{CC} or GND	5 V			4			10	pF	
C _o	V _O = V _{CC} or GND	5 V			9				pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		T _A = 25°C		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, \overline{LE} high	6.5		6.5		6.5		ns
t _{su}	Setup time, data before \overline{LE} ↓	1.5		1.5		1.5		ns
t _h	Hold time, data after \overline{LE} ↓	3.5		3.5		3.5		ns

5.7 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT373		SN74AHCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	$C_L = 15 \text{ pF}$		5.1 ⁽¹⁾	8.5 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	ns
t_{PHL}					5.1 ⁽¹⁾	8.5 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	
t_{PLH}	LE	Q	$C_L = 15 \text{ pF}$		7.7 ⁽¹⁾	12.3 ⁽¹⁾	1 ⁽¹⁾	13.5 ⁽¹⁾	1	13.5	ns
t_{PHL}					7.7 ⁽¹⁾	12.3 ⁽¹⁾	1 ⁽¹⁾	13.5 ⁽¹⁾	1	13.5	
t_{PZH}	$\overline{\text{OE}}$	Q	$C_L = 15 \text{ pF}$		6.3 ⁽¹⁾	10.9 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	ns
t_{PZL}					6.3 ⁽¹⁾	10.9 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	
t_{PHZ}	$\overline{\text{OE}}$	Q	$C_L = 15 \text{ pF}$		6 ⁽¹⁾	10.2 ⁽¹⁾	1 ⁽¹⁾	11 ⁽¹⁾	1	11	ns
t_{PLZ}					6 ⁽¹⁾	10.2 ⁽¹⁾	1 ⁽¹⁾	11 ⁽¹⁾	1	11	
t_{PLH}	D	Q	$C_L = 50 \text{ pF}$		5.9	9.5	1	10.5	1	10.5	ns
t_{PHL}					5.9	9.5	1	10.5	1	10.5	
t_{PLH}	LE	Q	$C_L = 50 \text{ pF}$		8.5	13.3	1	14.5	1	14.5	ns
t_{PHL}					8.5	13.3	1	14.5	1	14.5	
t_{PZH}	$\overline{\text{OE}}$	Q	$C_L = 50 \text{ pF}$		7.1	11.9	1	13.5	1	13.5	ns
t_{PZL}					7.1	11.9	1	13.5	1	13.5	
t_{PHZ}	$\overline{\text{OE}}$	Q	$C_L = 50 \text{ pF}$		6.8	11.2	1	12	1	12	ns
t_{PLZ}					6.8	11.2	1	12	1	12	
$t_{sk(o)}$			$C_L = 50 \text{ pF}$			1 ⁽²⁾			1	ns	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

$V_{CC} = 5 V$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74AHCT373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	-1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

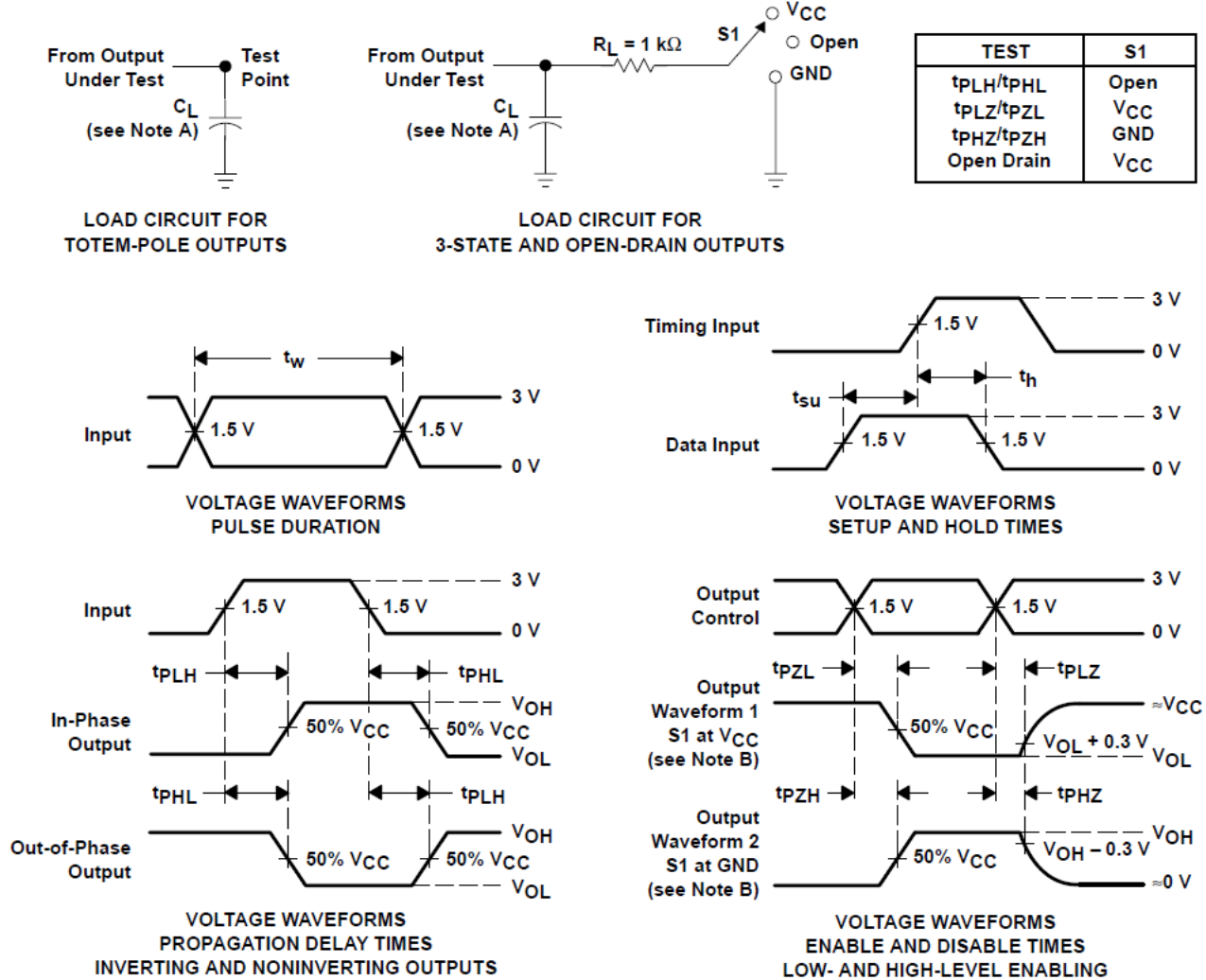
(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5 V$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance No load, $f = 1 \text{ MHz}$	17	pF

6 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

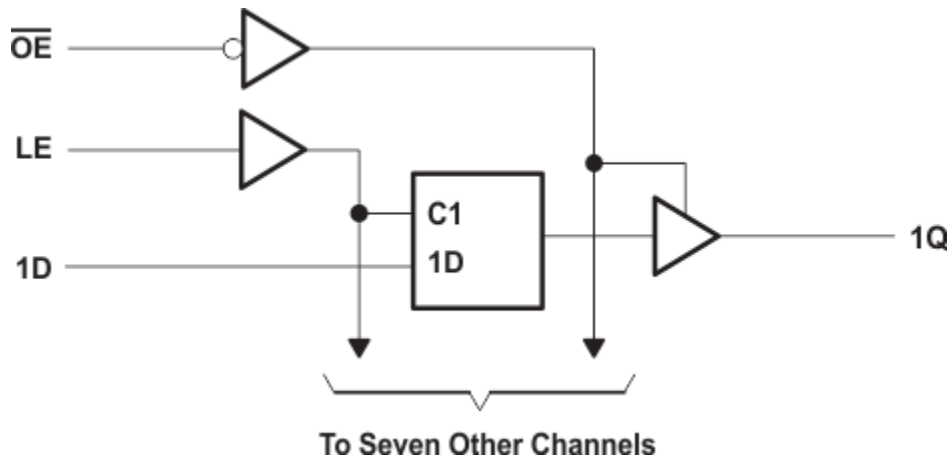


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table
(Each Latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT373	Click here	Click here	Click here	Click here	Click here
SN74AHCT373	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686701Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701Q2A SNJ54AHCT373FK	Samples
5962-9686701QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QR A SNJ54AHCT373J	Samples
5962-9686701QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QS A SNJ54AHCT373W	Samples
SN74AHCT373DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373	Samples
SN74AHCT373DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373	Samples
SN74AHCT373N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT373N	Samples
SN74AHCT373NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373	Samples
SN74AHCT373PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373	Samples
SNJ54AHCT373FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701Q2A SNJ54AHCT373FK	Samples
SNJ54AHCT373J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QR A SNJ54AHCT373J	Samples
SNJ54AHCT373W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QS A SNJ54AHCT373W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT373, SN74AHCT373 :

● Catalog : [SN74AHCT373](#)

● Military : [SN54AHCT373](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT373NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT373DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHCT373DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT373NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHCT373PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686701QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT373N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT373FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT373W	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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