SN74AUC1G126シングル・バス・バッファ・ゲート、3ステート出力

1 特長

- JESD 78, Class II準拠で100mA超のラッチアップ性能
- JESD22を超えるESD保護
  - 2000V、人体モデル(A114-A)
  - 200V、マシン・モデル(A115-A)
  - 1000V、荷電デバイス・モデル(C101)
- TIの NanoFree™パッケージで供給
- 1.8Vでの動作に最適化されており、3.6VのI/O許容電圧により、ミクスト・モード・シグナル動作をサポート
- I_{off}により部分的パワーダウン・モードおよびバック・ドライブ保護をサポート
- 1V未満で動作可能
- 最大t_{pd} 2.5ns (1.8V時)
- 低消費電力、最大I_{CC} 10µA
- 1.8Vにおいて±8mAの出力駆動能力

2 アプリケーション

- AVレシーバ
- オーディオ・ドック: ポータブル
- Blu-ray™プレーヤ/ホーム・シアター
- 組み込みPC
- MP3プレーヤ/レコーダ(ポータブル・オーディオ)
- パーソナル・デジタル・アシスタント(PDA)
- 電源: AC/DC電源、シングル・コントローラ
- ソリッド・ステート・ドライブ(SSD): クライアントおよびエンタープライズ
- テレビ: LCD、デジタル、高解像度(HD)
- タブレット: エンタープライズ
- ビデオ・アナリティクス: サーバー
- ワイヤレス・ヘッドセット、キーボード、マウス

3 概要

SN74AUC1G126バス・バッファ・ゲートは、0.8V～2.7VのV$_{CC}$に対応していますが、特に1.65V～1.95VのV$_{CC}$での動作に適した設計となっています。

SN74AUC1G126は、3ステート出力に対応したシングル・ライン・ドライバです。出力イネーブル(OE)入力がLOWのとき、この出力はディスエーブルになります。

電源投入時または切断時の高インピーダンス状態を確保するには、OEをプルダウン抵抗経由でGNDに接続する必要があります。この抵抗の最小値は、ドライバの電流ソース能力によって決まります。

NanoFree™パッケージは、デバイス・パッケージの概念を大きく変える技術であり、ダイをパッケージとして使用します。

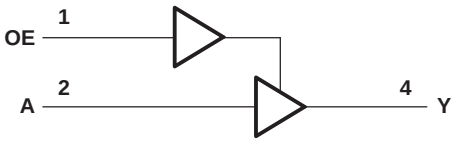
このデバイスは、I_{off}を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off}回路が出力をディスエーブルにすることにより、電源切断時にデバイスに電流が逆流することによる損傷を回避します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
SN74AUC1G126DBV	SOT-23 (5)	2.90mm×1.60mm
SN74AUC1G126DCK	SC70 (5)	2.00mm×1.25mm
SN74AUC1G126YZP	DSBGA (5)	1.388mm×0.888mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ロジック図 (正論理)



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision K (June 2017) から **Revision L** に変更 **Page**

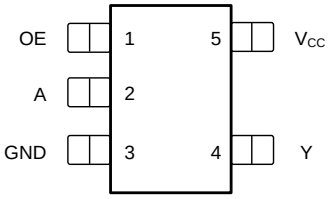
- YZPパッケージの本体サイズを更新。 ... 1
- Added junction temperature to *Absolute Maximum Ratings* ... 4
- Add *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations*, and *Layout* sections ... 12

Revision J (July 2007) から **Revision K** に変更 **Page**

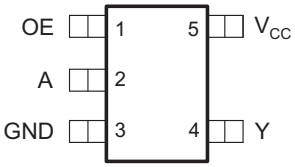
- データシート全体でDRYパッケージを 削除 ... 1
- 「*アプリケーション*」、「*製品情報*」の表、「*ESD定格*」の表、「*熱に関する情報*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- このデータシートの末尾にある「*メカニカル、パッケージ、および注文情報*」を参照し、「*注文情報*」表を 削除 ... 1

5 Pin Configuration and Functions

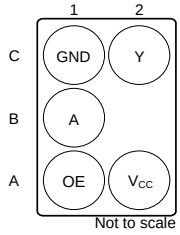
DBV Package
5-Pin SOT-23
Top View



DCK Package
5-Pin SC70
Top View



YZP Package
5-Pin DSBGA
Bottom View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV, DCK	YZP		
A	2	B1	I	Logic input
GND	3	C1	—	Ground
OE	1	A1	I	Output enable
V_{CC}	5	A2	—	Positive supply
Y	4	C2	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	3.6	V
Input voltage, V_I(2)		–0.5	3.6	V
Voltage applied to any output in the high-impedance or power-off state, V_O(2)		–0.5	3.6	V
Output voltage, V_O(2)		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–50	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O			±20	mA
Continuous current through V_{CC} or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–0.7	mA
		V_{CC} = 1.1 V		–3	
		V_{CC} = 1.4 V		–5	
		V_{CC} = 1.65 V		–8	
		V_{CC} = 2.3 V		–9	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		0.7	mA
		V_{CC} = 1.1 V		3	
		V_{CC} = 1.4 V		5	
		V_{CC} = 1.65 V		8	
		V_{CC} = 2.3 V		9	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.6 V		20	ns/V
		V_{CC} = 1.65 V to 1.95 V		10	
		V_{CC} = 2.3 V to 2.7 V		3	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AUC1G126			UNIT
		DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	132	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA, V_{CC} = 0.8 V to 2.7 V	V_{CC} – 0.1			V
		I_{OH} = –0.7 mA, V_{CC} = 0.8 V		0.55		
		I_{OH} = –3 mA, V_{CC} = 1.1 V	0.8			
		I_{OH} = –5 mA, V_{CC} = 1.4 V	1			
		I_{OH} = –8 mA, V_{CC} = 1.65 V	1.2			
		I_{OH} = –9 mA, V_{CC} = 2.3 V	1.8			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, V_{CC} = 0.8 V to 2.7 V			0.2	V
		I_{OL} = 0.7 mA, V_{CC} = 0.8 V		0.25		
		I_{OL} = 3 mA, V_{CC} = 1.1 V			0.3	
		I_{OL} = 5 mA, V_{CC} = 1.4 V			0.4	
		I_{OL} = 8 mA, V_{CC} = 1.65 V			0.45	
		I_{OL} = 9 mA, V_{CC} = 2.3 V			0.6	
I_I	Inflection-point current	A or OE input: V_I = V_{CC} or GND, V_{CC} = 0 to 2.7 V			±5	µA
I_{off}	Off-state current	V_I or V_O = 2.7 V, V_{CC} = 0			±10	µA
I_{OZ}	High-impedance-state output current	V_O = V_{CC} or GND, V_{CC} = 2.7 V			±10	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, V_{CC} = 0.8 V to 2.7 V I_O = 0			10	µA
C_i	Input capacitance	V_I = V_{CC} or GND, V_{CC} = 2.5 V		2.5		pF
C_o	Output capacitance	V_O = V_{CC} or GND, V_{CC} = 2.5 V		5.5		pF

(1) All typical values are at T_A = 25°C.

6.6 Switching Characteristics: C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see 表 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time	A-to-Y	V_{CC} = 0.8 V		4.5		ns
			V_{CC} = 1.2 V ± 0.1 V	0.8		3.6	
			V_{CC} = 1.5 V ± 0.1 V	0.6		2.3	
			V_{CC} = 1.8 V ± 0.15 V	0.6	1	1.6	
			V_{CC} = 2.5 V ± 0.2 V	0.5		1.4	
t_{en}	Enable time	OE-to-Y	V_{CC} = 0.8 V		4.9		ns
			V_{CC} = 1.2 V ± 0.1 V	0.7		3.8	
			V_{CC} = 1.5 V ± 0.1 V	0.7		2.5	
			V_{CC} = 1.8 V ± 0.15 V	0.3	0.9	1.9	
			V_{CC} = 2.5 V ± 0.2 V	0.3		1.5	
t_{dis}	Disable time	OE-to-Y	V_{CC} = 0.8 V		4.9		ns
			V_{CC} = 1.2 V ± 0.1 V	2.2		4.7	
			V_{CC} = 1.5 V ± 0.1 V	1.8		4.1	
			V_{CC} = 1.8 V ± 0.15 V	1.6	2.4	3.5	
			V_{CC} = 2.5 V ± 0.2 V	1		2.7	

6.7 Switching Characteristics: C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see 表 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time	A-to-Y	V_{CC} = 1.8 V ± 0.15 V	1	1.5	2.5	ns
			V_{CC} = 2.5 V ± 0.2 V	0.9		1.7	
t_{en}	Enable time	OE-to-Y	V_{CC} = 1.8 V ± 0.15 V	1.1	1.6	2.5	ns
			V_{CC} = 2.5 V ± 0.2 V	0.9		1.9	
t_{dis}	Disable time	OE-to-Y	V_{CC} = 1.8 V ± 0.15 V	1.3	2.6	3.1	ns
			V_{CC} = 2.5 V ± 0.2 V	1		2.1	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	Inputs disabled	V_{CC} = 0.8 V		14		pF
				V_{CC} = 1.2 V		14		
				V_{CC} = 1.5 V		14		
				V_{CC} = 1.8 V		15		
				V_{CC} = 2.5 V		16		
			Outputs disabled	V_{CC} = 0.8 V		1.5		
				V_{CC} = 1.2 V		1.5		
				V_{CC} = 1.5 V		1.5		
				V_{CC} = 1.8 V		2		
				V_{CC} = 2.5 V		2.5		

7 Typical Characteristics

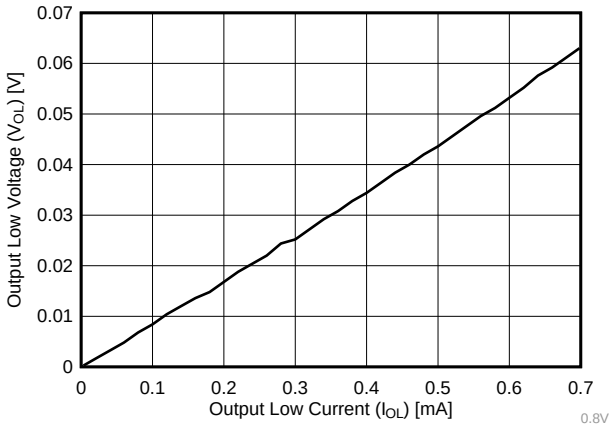


図 1. Typical Output Low Voltage of 0.8 V (25°C)

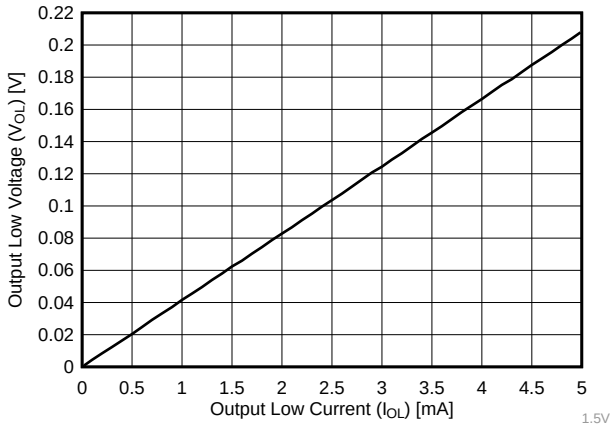


図 2. Typical Output Low Voltage of 1.5 V (25°C)

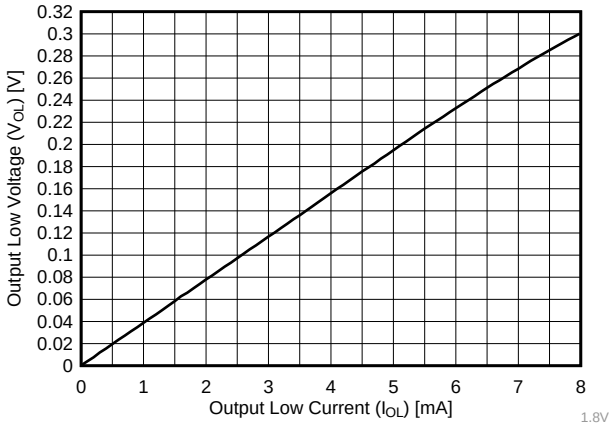


図 3. Typical Output Low Voltage of 1.8 V (25°C)

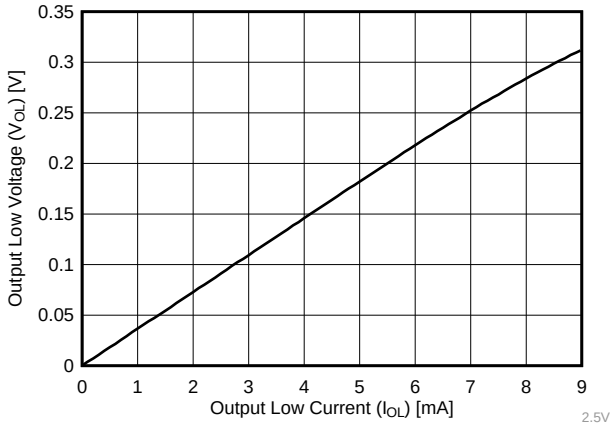


図 4. Typical Output Low Voltage of 2.5 V (25°C)

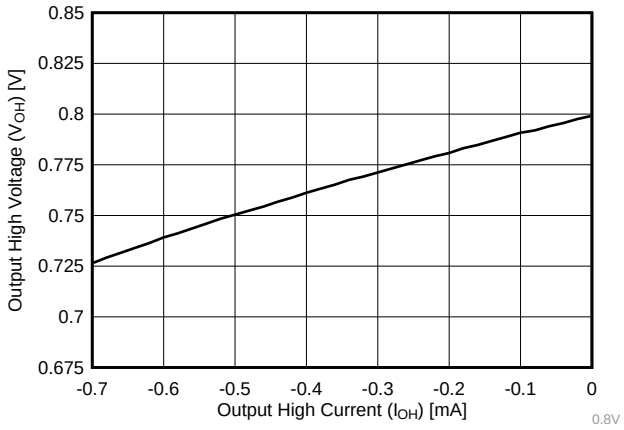


図 5. Typical Output High Voltage of 0.8 V (25°C)

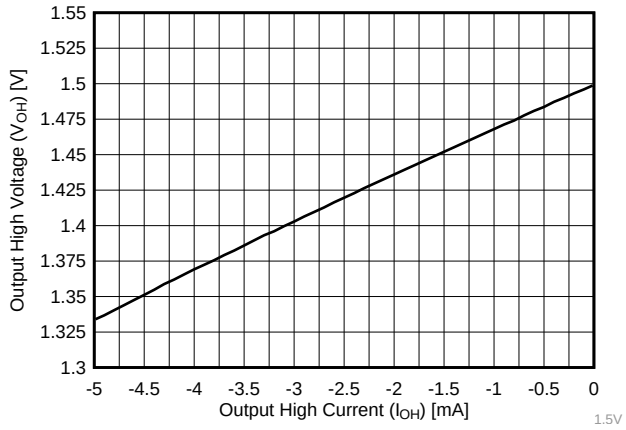


図 6. Typical Output High Voltage of 1.5 V (25°C)

Typical Characteristics (continued)

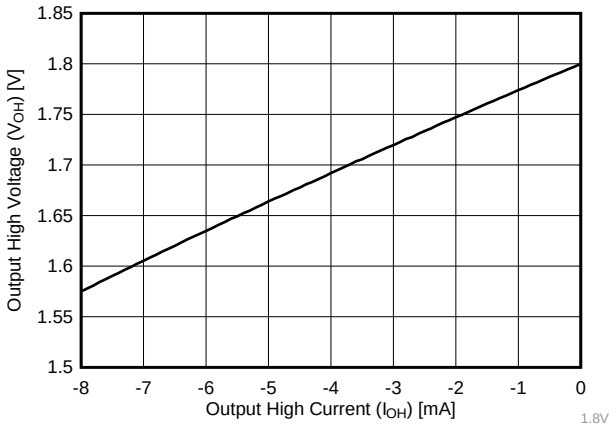


図 7. Typical Output High Voltage of 1.8 V (25°C)

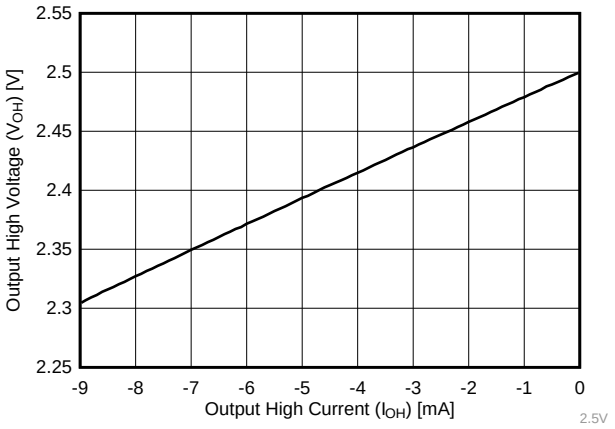
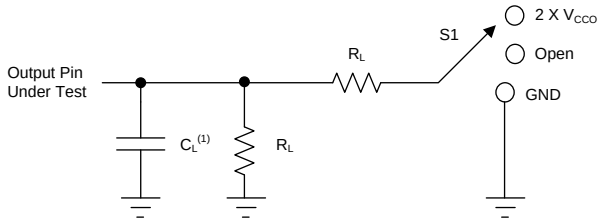


図 8. Typical Output High Voltage of 2.5 V (25°C)

8 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators that have the following characteristics:

- PRR ≤ 10 MHz
- Z_O = 50 Ω



(1) C_L includes probe and jig capacitance.

図 9. Load Circuit

表 1. Loading Conditions for Parameter

TEST	S1
t_{PLH} (1), t_{PHL} (1)	Open
t_{PLZ} (2), t_{PZL} (3)	2 × V_{CC}
t_{PHZ} (2), t_{PZH} (3)	GND

表 2. Loading Conditions for V_{CC}

V_{CC}	C_L	R_L	V_Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 kΩ	0.15 V

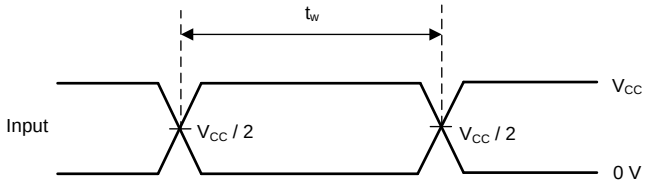
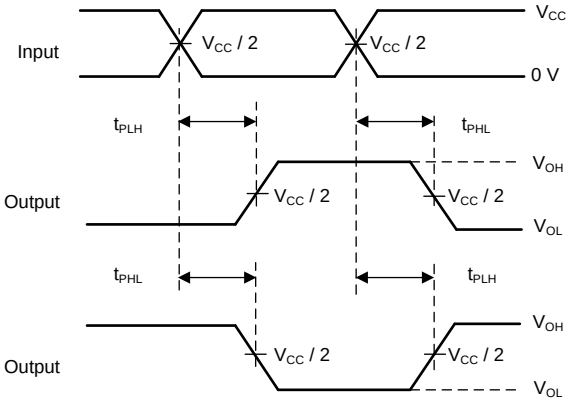


図 10. Voltage Waveforms: Pulse Duration



(1) All outputs are measured one at a time, with one transition per measurement.

図 11. Voltage Waveforms: Propagation Delay Times, Inverting and Noninverting Outputs

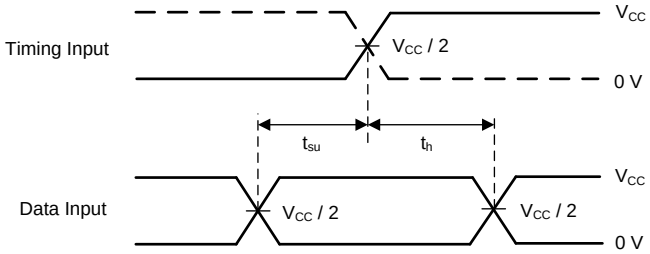
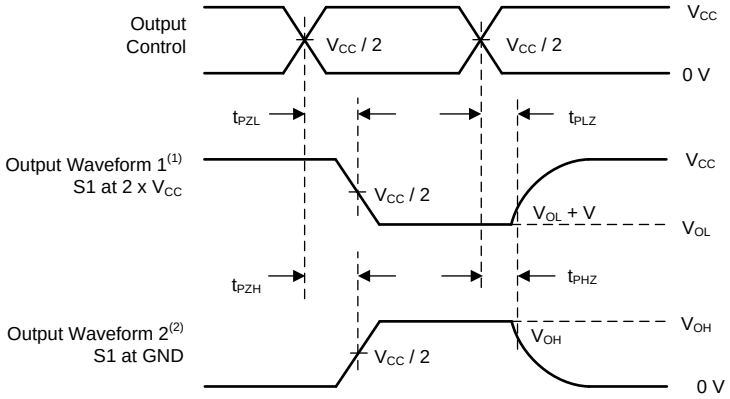


図 12. Voltage Waveforms: Setup and Hold Times



(1) Waveform 1 is for an output with internal conditions such as the output is low, except when disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such as the output is high, except when disabled by the output control.

(3) All outputs are measured one at a time, with one transition per measurement.

図 13. Voltage Waveforms: Enable and Disable Times, Low- and High-Level Enabling

9 Detailed Description

9.1 Overview

The SN74AUC1G126 device contains one buffer gate device with output enable control, and performs the Boolean function Y = A. This device is specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow, preventing damage to the device.

To ensure the high-impedance state during power up or power down, OE must be tied to GND through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagram

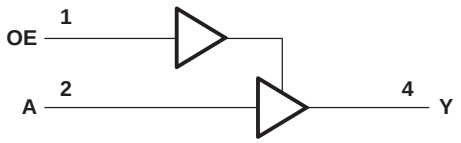


図 14. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in *Absolute Maximum Ratings* must be followed at all times.

9.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in *Absolute Maximum Ratings*, and the maximum input leakage current, given in *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

9.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in 図 15.

注意

Voltages beyond the values specified in *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

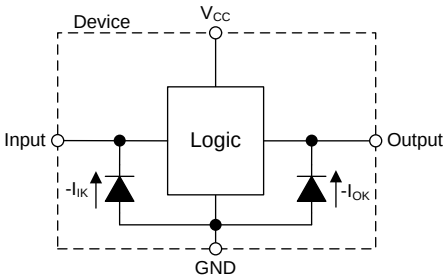


図 15. Electrical Placement of Clamping Diodes for Each Input and Output

9.3.4 Special Features

9.3.4.1 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

9.3.4.2 Overvoltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as the input signals remain below the maximum input voltage value specified in *Recommended Operating Conditions*.

9.3.4.3 Output Enable

This device has an output enable (OE) pin that functions according to 表 3. When the outputs of the device are disabled, the outputs are placed into a high impedance state where the output will neither source nor sink current. High-impedance outputs are also commonly referred to as three-state or tri-state outputs. The maximum leakage for the output in this state is defined by I_{OZ} in the *Electrical Characteristics* table.

9.4 Device Functional Modes

表 3 lists the functional modes of the SN74AUC1G126 device.

表 3. Function Table

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AUC1G126 device is an output enabled CMOS buffer that can be used in LED indicator applications that require less than 9 mA. The device can produce up to 9 mA of drive current at 2.5 V. The inputs to the device are also overvoltage tolerant up to 3.6 V, allowing the inputs to translate down to any valid V_{CC}.

10.2 Typical Application

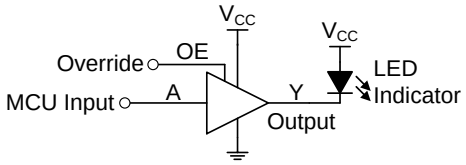


図 16. Application Schematic with MCU driving an LED Indicator

10.2.1 Design Requirements

This device uses CMOS technology, and has a balanced output drive. The output drive strength of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

注

Take care of the output drive to avoid bus contention, because the output can drive currents that exceed maximum limits.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Rise time and fall time specifications ($\Delta t/\Delta V$) are shown in the *Recommended Operating Conditions* table.
   - Specified high (V_{IH}) and low voltage (V_{IL}) levels are shown in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I maximum) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents must not exceed (I_O max) per output and must not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

10.2.3 Application Curve

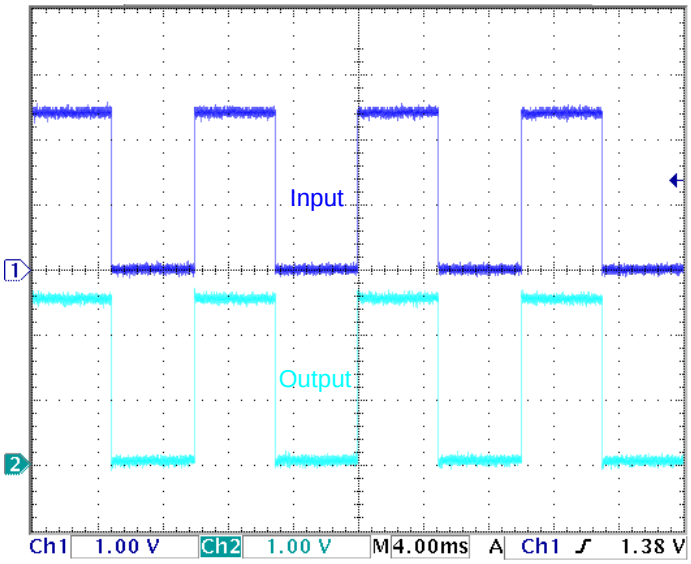


図 17. Example Oscilloscope Waveform

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power pin for best results.

12 Layout

12.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 図 18 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

12.2 Layout Example

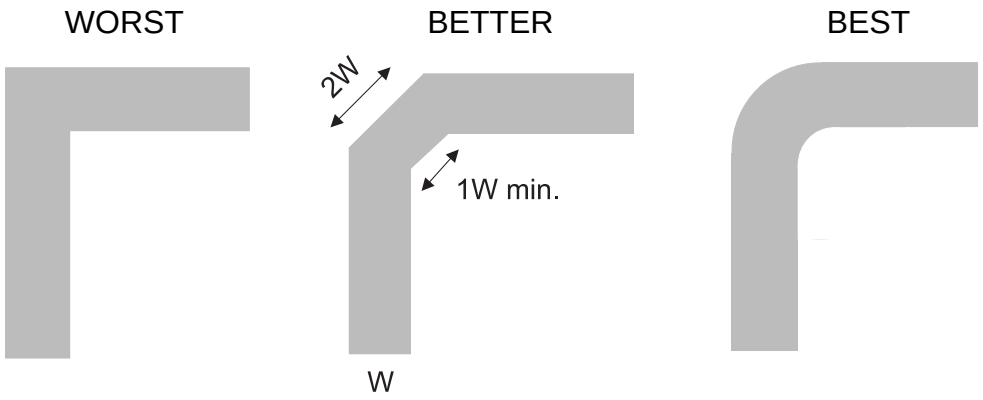


図 18. Trace Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ、『低速またはフローティングCMOS入力の影響』アプリケーション・レポート

13.2 ドキュメントの更新通知を受け取る方法

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13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AUC1G126DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UNR	Samples
SN74AUC1G126DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U26R	Samples
SN74AUC1G126DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UNR	Samples
SN74AUC1G126YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(UN, UNN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

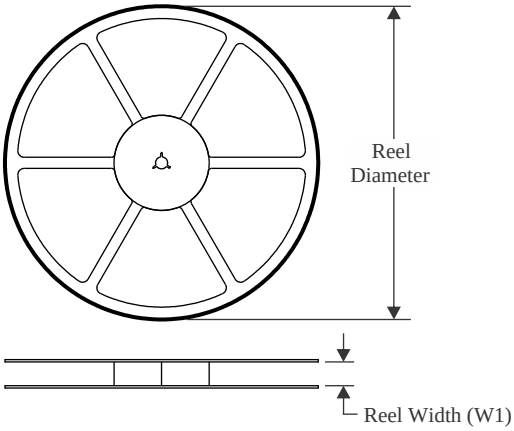
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

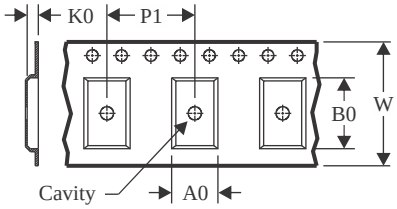
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

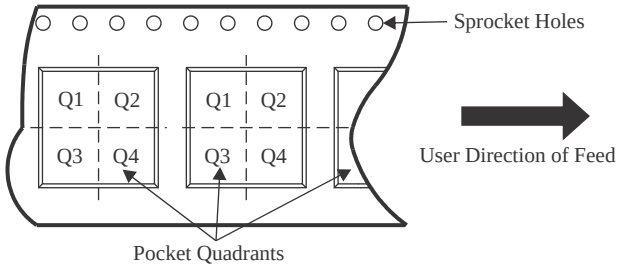


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

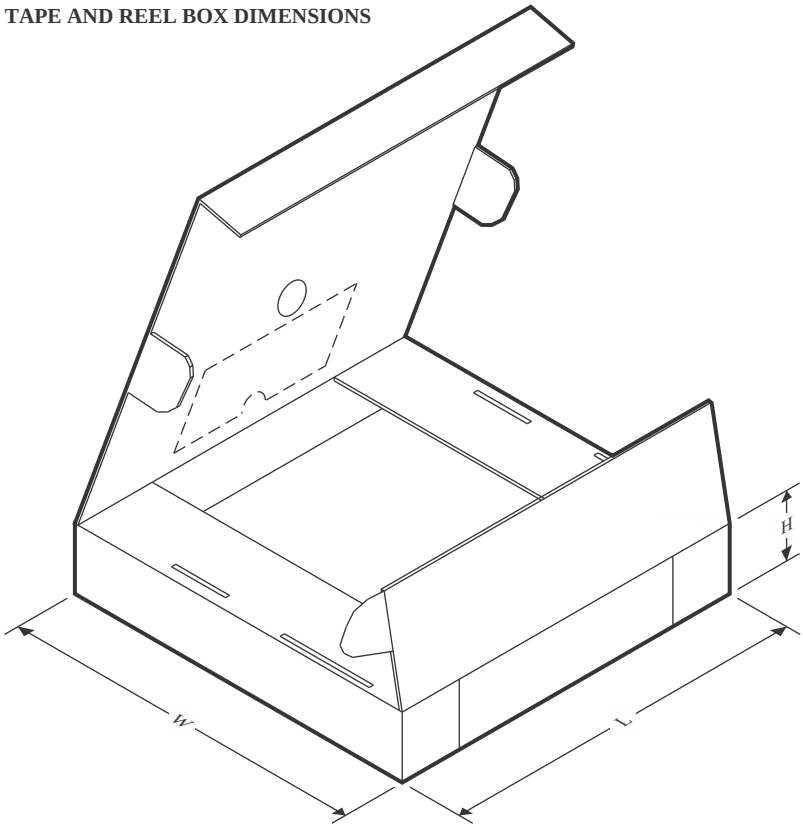
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G126DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC1G126DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUC1G126YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

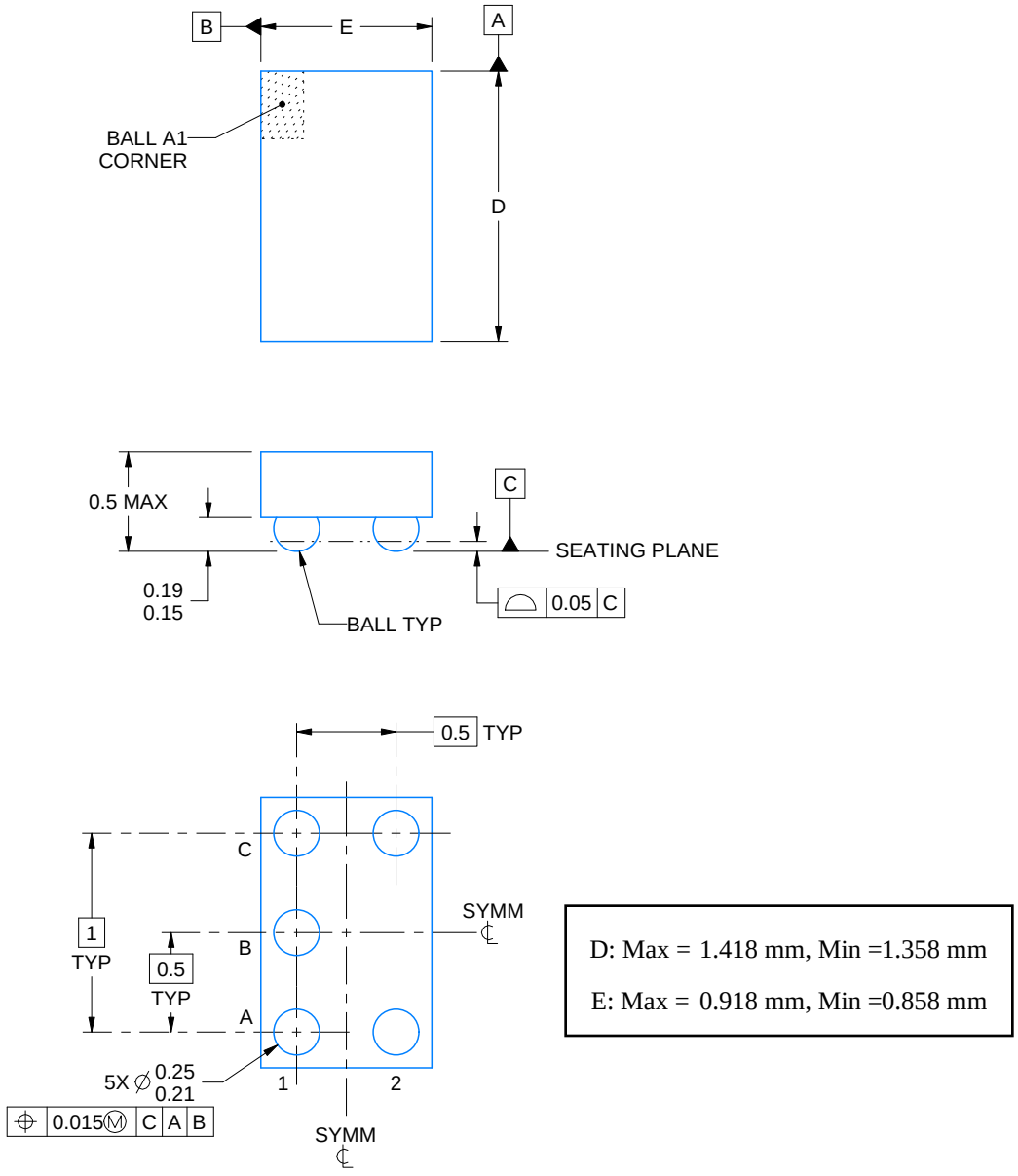
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC1G126DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUC1G126DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUC1G126YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



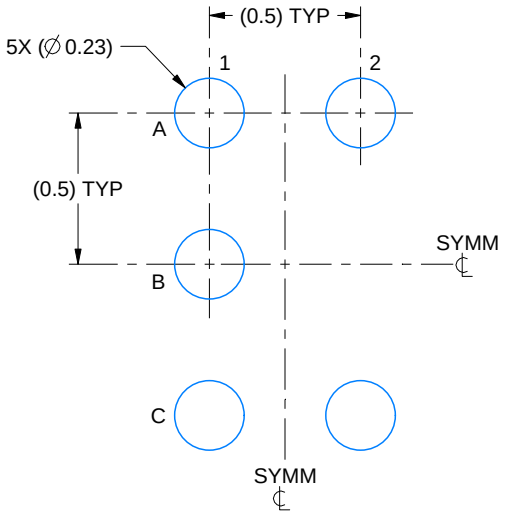
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

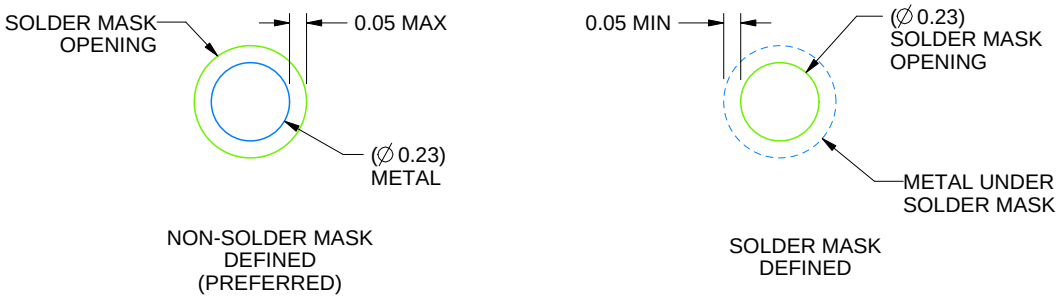
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

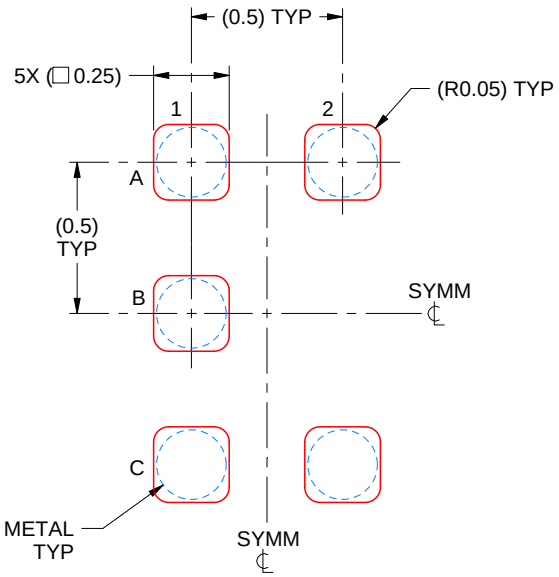


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

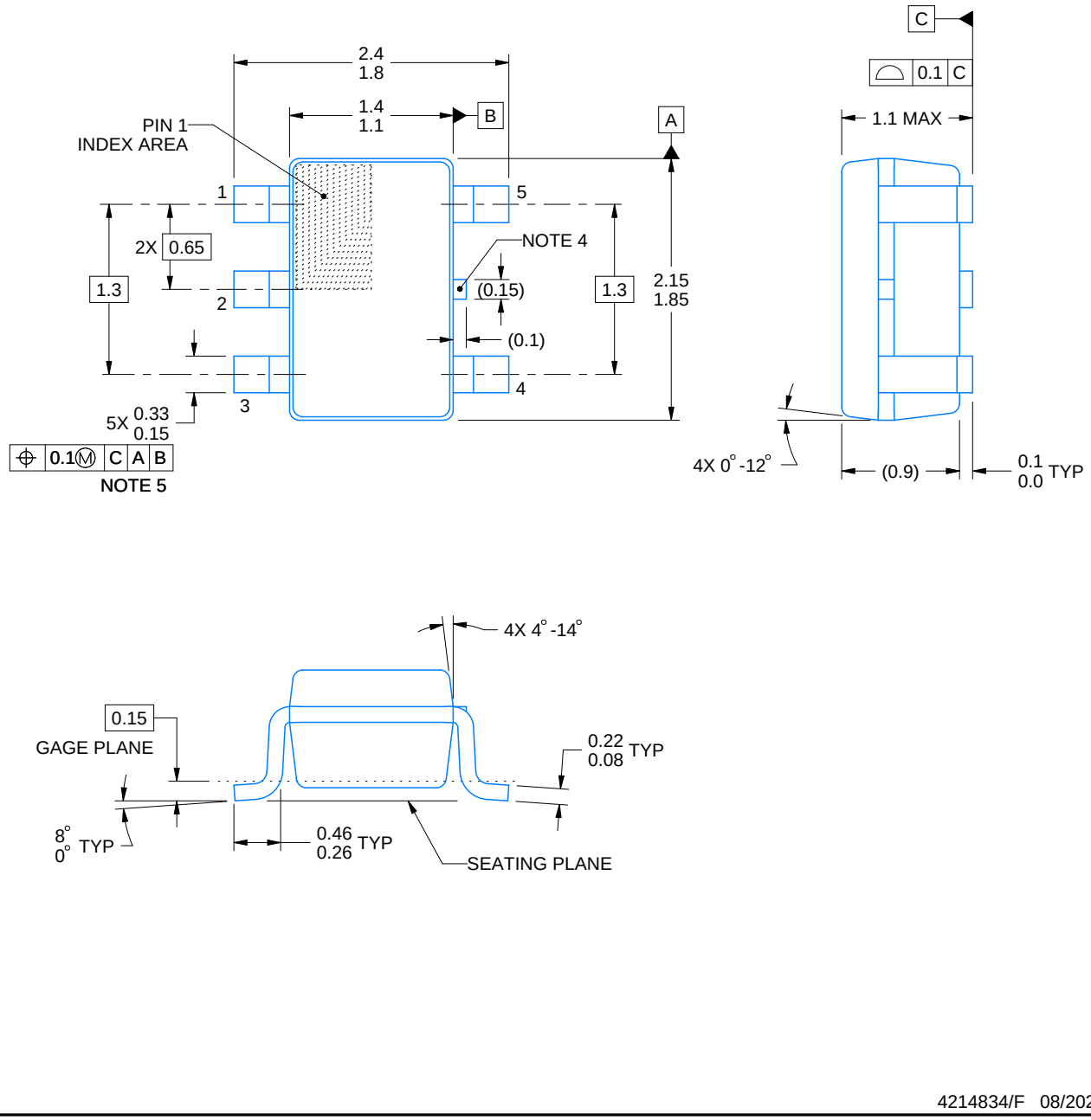
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

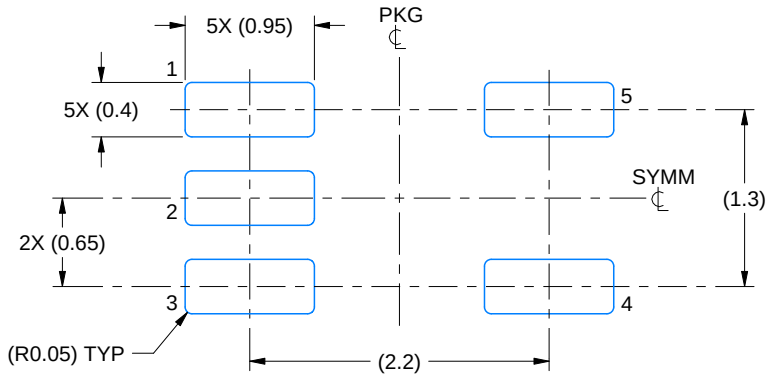
SMALL OUTLINE TRANSISTOR



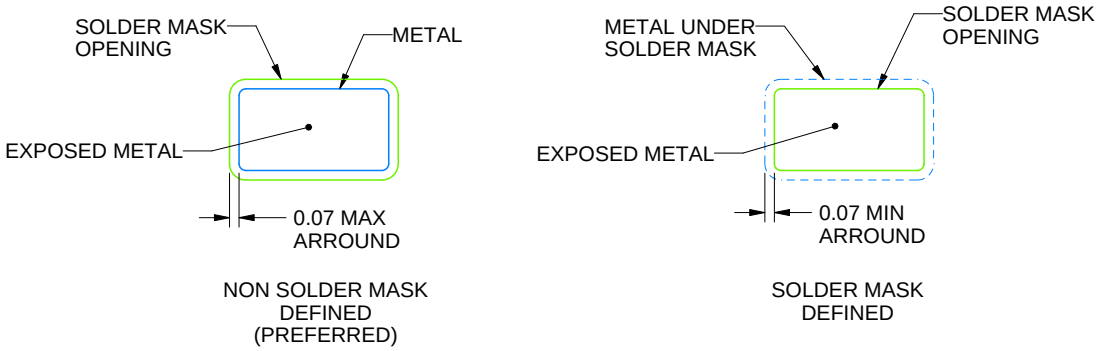
4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

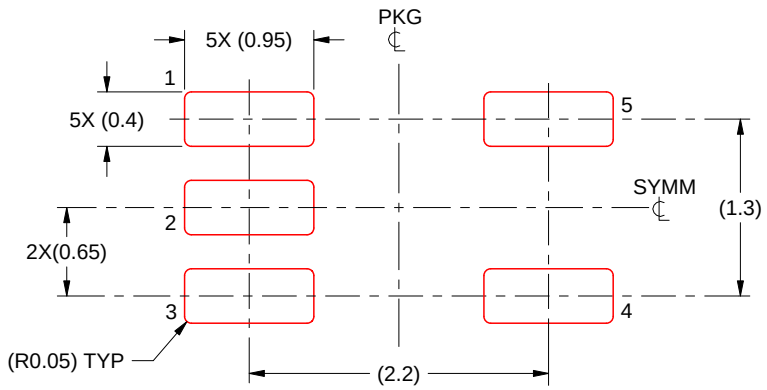


SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

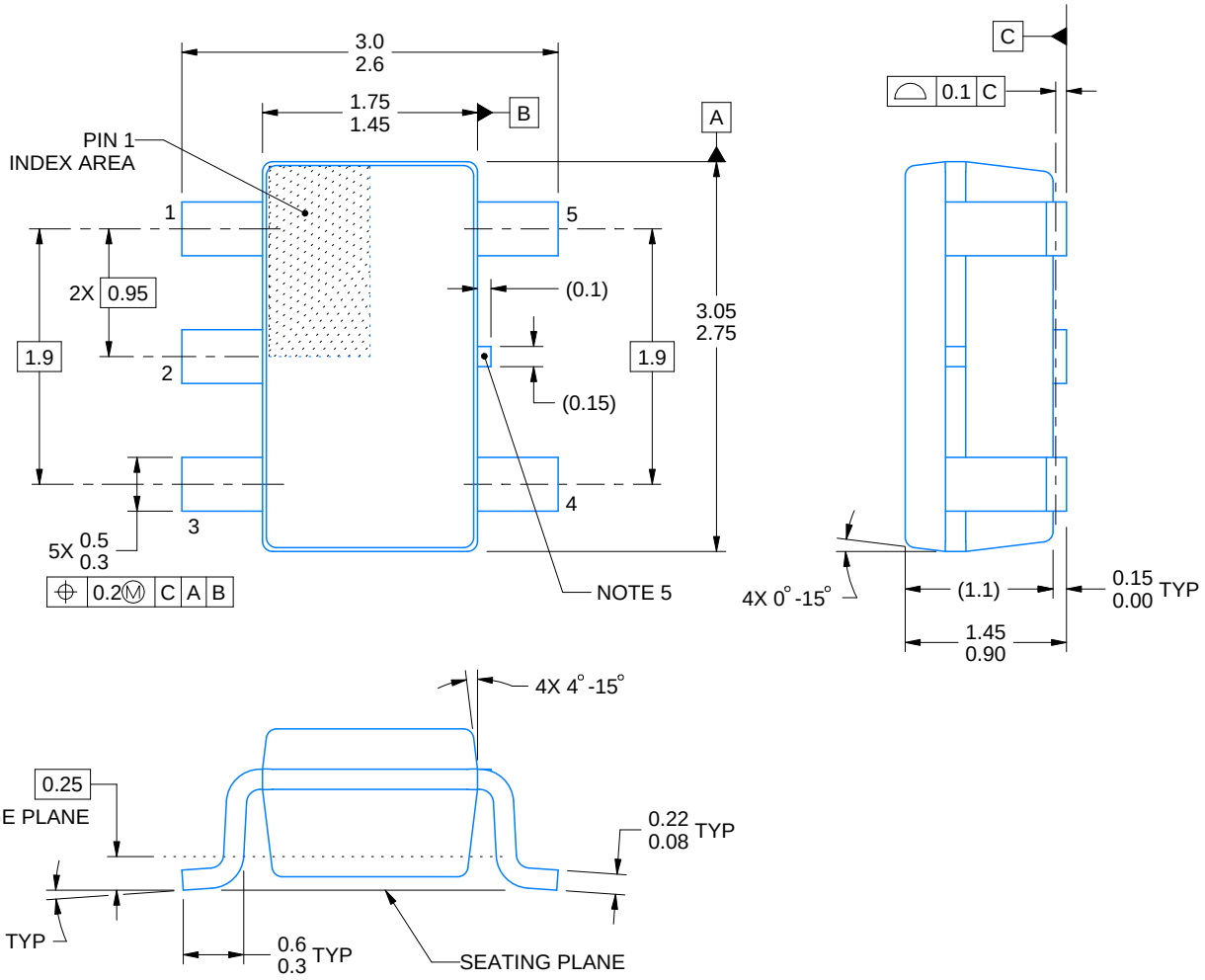
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

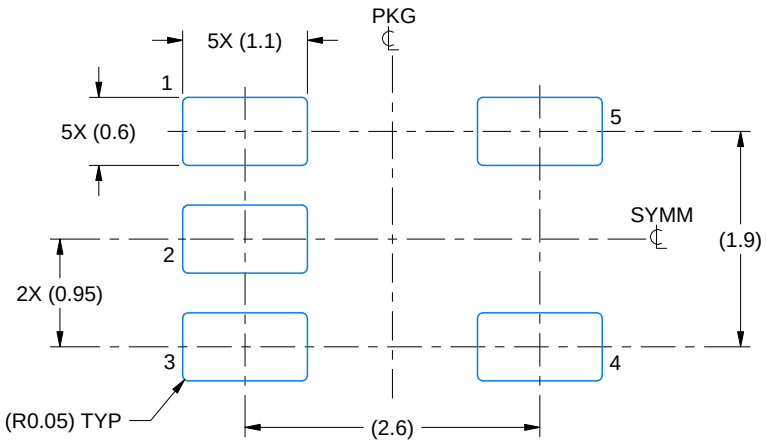
SMALL OUTLINE TRANSISTOR



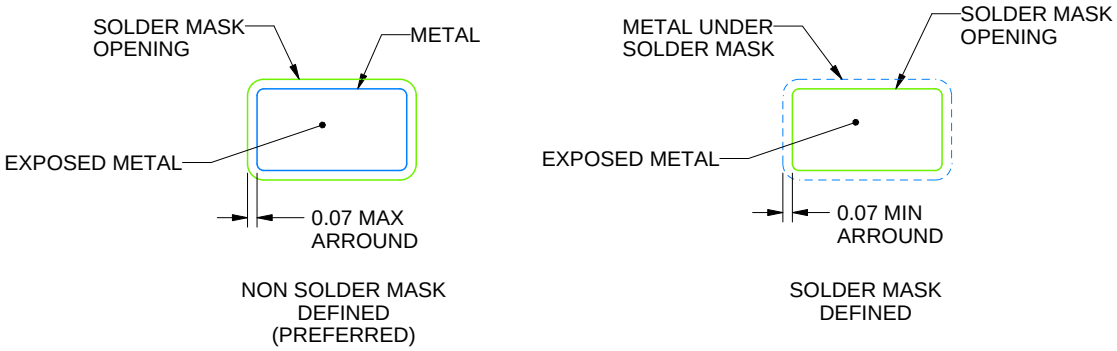
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

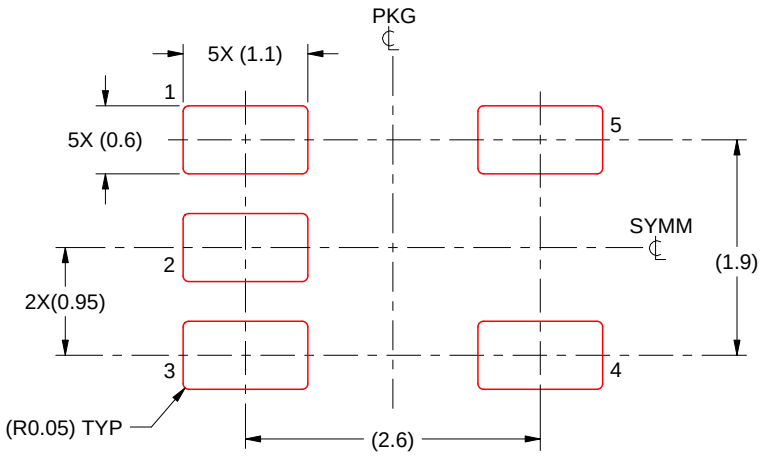


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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