

SN74AUP1T97 単一電源電圧レベル・シフト、 9つの設定可能なゲート論理機能付き

1 特長

- テキサス・インスツルメンツの NanoStar™ パッケージで提供
- 単一電源電圧レベル・シフト
- 1.8V ~ 3.3V ($V_{CC} = 3.3V$ の場合)
- 2.5V ~ 3.3V ($V_{CC} = 3.3V$ の場合)
- 1.8V ~ 2.5V ($V_{CC} = 2.5V$ の場合)
- 3.3V ~ 2.5V ($V_{CC} = 2.5V$ の場合)
- 9つの設定可能なゲート論理機能
- シュミット・トリガ入力により、入力ノイズを除去し出力信号の整合性を向上
- I_{off} により、低リーク電流 (0.5 μ A) の部分的パワーダウン・モードをサポート
- 非常に小さい静的および動的消費電力
- 提供している鉛フリー・パッケージ: SON (DRY または DSF)、SOT-23 (DBV)、SC-70 (DCK)、NanoStar WCSP
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- ESD 性能は JESD 22 に準拠しテスト済み
 - 2000V、人体モデル (A114-B、Class II)
 - 1000V、荷電デバイス・モデル (C101)
- 関連デバイス: SN74AUP1T98、SN74AUP1T57、SN74AUP1T58

2 概要

AUP テクノロジは、バッテリー駆動機器またはバッテリー・バックアップ機器で使用するために設計された、業界で最も消費電力が小さい論理方式です。SN74AUP1T97 は、1.8V LVCMOS 信号に適合する入力スイッチング・レベルを持つロジック・レベル変換アプリケーション向けに設計されており、3.3V と 2.5V のどちらの V_{CC} 単一電源でも動作します。

V_{CC} 範囲が 2.3V ~ 3.6V と広いため、システム動作中にバッテリー電圧が低下してもこの範囲で正常に動作できます。

シュミット・トリガ入力 (正と負の入力遷移の間隔 $\Delta V_T = 210mV$) により、スイッチング遷移時のノイズ耐性を向上させることができます。これは、アナログ・ミクスト・モード設計では特に便利です。シュミット・トリガ入力は入力ノイズを除去し、出力信号の整合性を確保し、遅い入力信号遷移を許容します。

SN74AUP1T97 は、A、B、C 入力を V_{CC} またはグラウンドに接続することで、必要なゲート機能を実行するように簡単に設定できます (「機能選択」表を参照)。最

大 9 つの一般的なロジック・ゲート機能を実行できます。

I_{off} は、パワー・ダウン条件 ($V_{CC} = 0V$) を可能にする機能であり、ポータブルおよびモバイル・アプリケーションで重要です。 $V_{CC} = 0V$ の場合、0V ~ 3.6V の範囲の信号をデバイスの入力と出力に印加できます。これらの条件でデバイスが損傷することはありません。

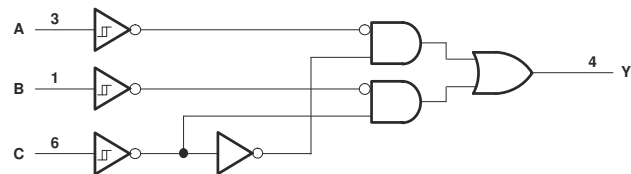
SN74AUP1T97 は、高駆動出力によるラインの反射、オーバーシュート、アンダーシュートを低減するため、4mA という最適化された電流駆動能力を持つように設計されています。

ダイをパッケージとして使用する NanoStar パッケージ技術は、IC パッケージの概念を大きく覆すものです。

製品情報

型番	パッケージ ⁽¹⁾ (1 ページ)	本体サイズ (公称)
SN74AUP1T97DBV	SOT-23 (6)	2.9mm × 1.6mm
SN74AUP1T97DCK	SC70 (6)	2.0mm × 1.25mm
SN74AUP1T97DRY	SON (6)	1.45mm × 1.0mm
SN74AUP1T97DSF	SON (6)	1.0mm × 1.0mm
SN74AUP1T97YFP	DSBGA (6)	1.0mm × 1.4mm
SN74AUP1T97YZP	DSBGA (6)	1.75mm × 1.25mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



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3 Revision History

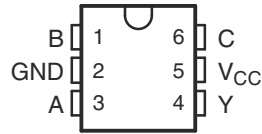
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。


Changes from Revision I (May 2010) to Revision J (September 2020)

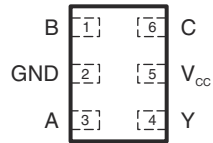
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- 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加1
- 「注文情報」表を削除 (このデータシートの末尾にある「メカニカル、パッケージ、および注文情報」を参照)1
- 文書全体にわたって表、図、相互参照の採番方法を更新.....

4 Pin Configuration and Functions




4-1. DBV OR DCK Package 6-Pin SOT-23 or SC70 Top View




4-2. DRY OR DSF Package 6-Pin SON Top View




4-3. YFP OR YZP Package 6-Pin DSBGA Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	4.6	V
V _I	Input voltage ⁽²⁾		-0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	4.6	V
V _O	Output voltage range in the high or low state ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge		
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _I	Input voltage		0	3.6	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.3 V		-3.1	mA
		V _{CC} = 3 V		-4	
I _{OL}	Low-level output current	V _{CC} = 2.3 V		3.1	mA
		V _{CC} = 3 V		4	
T _A	Operating free-air temperature		-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AUP1T97				UNIT
		DBV (SOT-23)	DCK (SC70)	DRY (SON)	DSF (SON)	
		6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	165	259	340	300	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance					°C/W
R _{θJB}	Junction-to-board thermal resistance					°C/W
ψ _{JT}	Junction-to-top characterization parameter					°C/W
ψ _{JB}	Junction-to-board characterization parameter					°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance					°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AUP1T97		UNIT
		YFP (DSBGA)	YZP (DSBGA)	
		6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	123	123	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance			°C/W
R _{θJB}	Junction-to-board thermal resistance			°C/W
ψ _{JT}	Junction-to-top characterization parameter			°C/W
ψ _{JB}	Junction-to-board characterization parameter			°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance			°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
		3 V to 3.6 V	0.75		1.16	0.75	1.19	
V _{T-} Negative-going input threshold voltage		2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
		3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV _T Hysteresis (V _{T+} - V _{T-})		2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
		3 V to 3.6 V	0.25		0.56	0.15	0.56	
V _{OH}	I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1		V	
	I _{OH} = -2.3 mA	2.3 V	2.05		1.97			
	I _{OH} = -3.1 mA		1.9		1.85			
	I _{OH} = -2.7 mA	3 V	2.72		2.67			
	I _{OH} = -4 mA		2.6		2.55			

5.6 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OL}	I _{OL} = 20 μA	2.3 V to 3.6 V			0.1		0.1	V
	I _{OL} = 2.3 mA	2.3 V			0.31		0.33	
	I _{OL} = 3.1 mA				0.44		0.45	
	I _{OL} = 2.7 mA	3 V			0.31		0.33	
	I _{OL} = 4 mA				0.44		0.45	
I _I	All inputs V _I = 3.6 V or GND	0 V to 3.6 V			0.1		0.5	μA
I _{off}	V _I or V _O = 0 V to 3.6 V	0 V			0.1		0.5	μA
ΔI _{off}	V _I or V _O = 3.6 V	0 V to 0.2 V			0.2		0.5	μA
I _{CC}	V _I = 3.6 V or GND, I _O = 0	2.3 V to 3.6 V			0.5		0.9	μA
ΔI _{CC}	One input at 0.3 V or 1.1 V, Other inputs at 0 or V _{CC} , I _O = 0	2.3 V to 2.7 V					4	μA
	One input at 0.45 V or 1.2 V, Other inputs at 0 or V _{CC} , I _O = 0	3 V to 3.6 V					12	
C _i	V _I = V _{CC} or GND	3.3 V		1.5				pF
C _o	V _O = V _{CC} or GND	3.3 V		3				pF

5.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see [6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

5.8 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see [6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

5.9 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

5.10 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see [6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

5.11 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

5.12 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

SN74AUP1T97

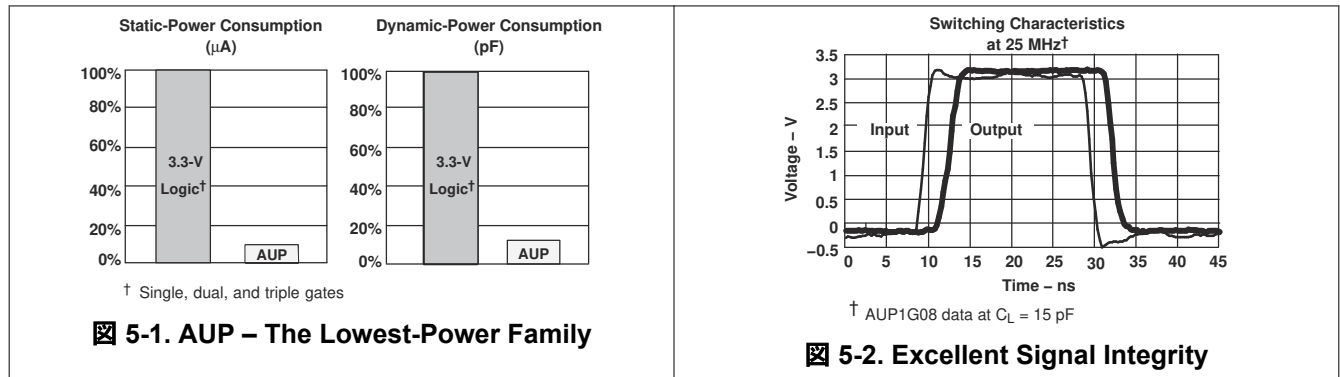
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5.13 Operating Characteristics

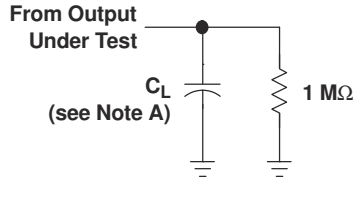
T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	4	5	pF

5.14 Typical Characteristics

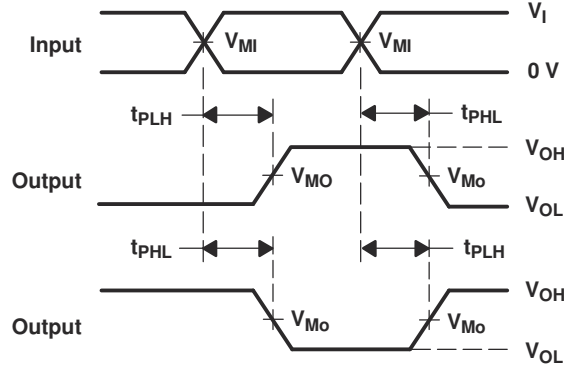


6 Parameter Measurement Information



LOAD CIRCUIT

	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	$V_I/2$	$V_I/2$
V_{MO}	$V_{CC}/2$	$V_{CC}/2$



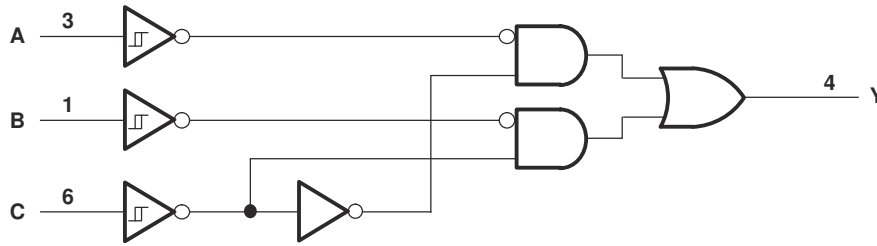
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, slew rate $\geq 1\text{ V/ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

6-1. Load Circuit and Voltage Waveforms

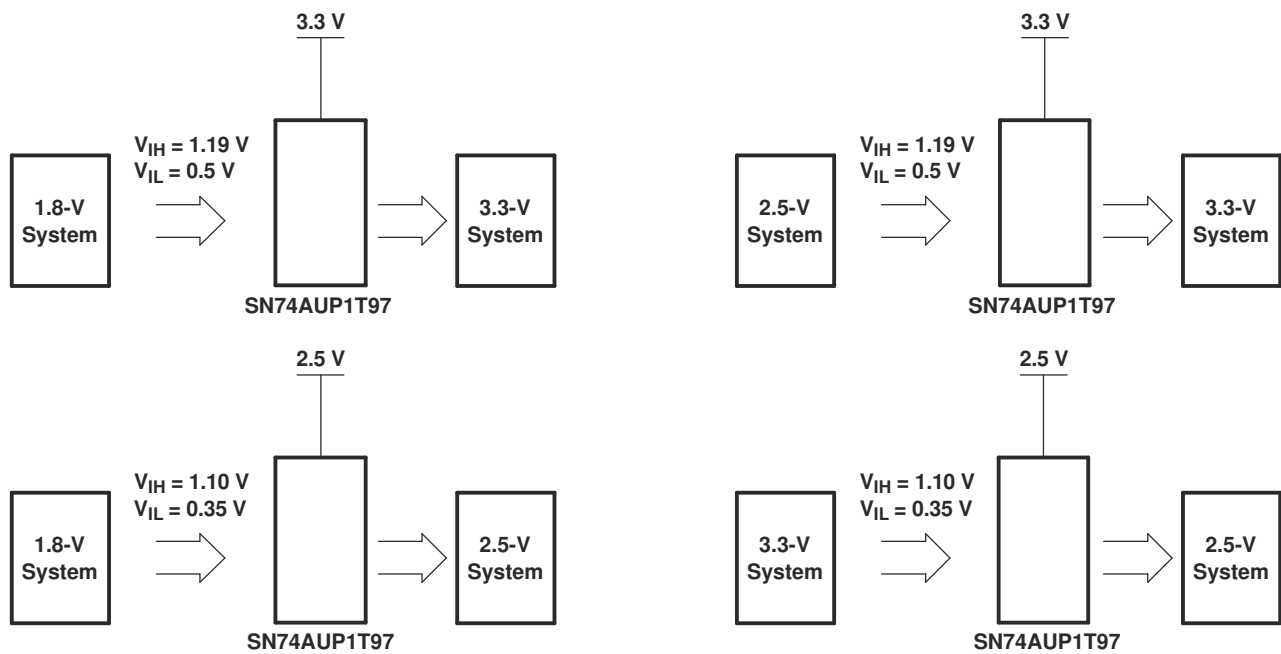
7 Detailed Description

7.1 Functional Block Diagram

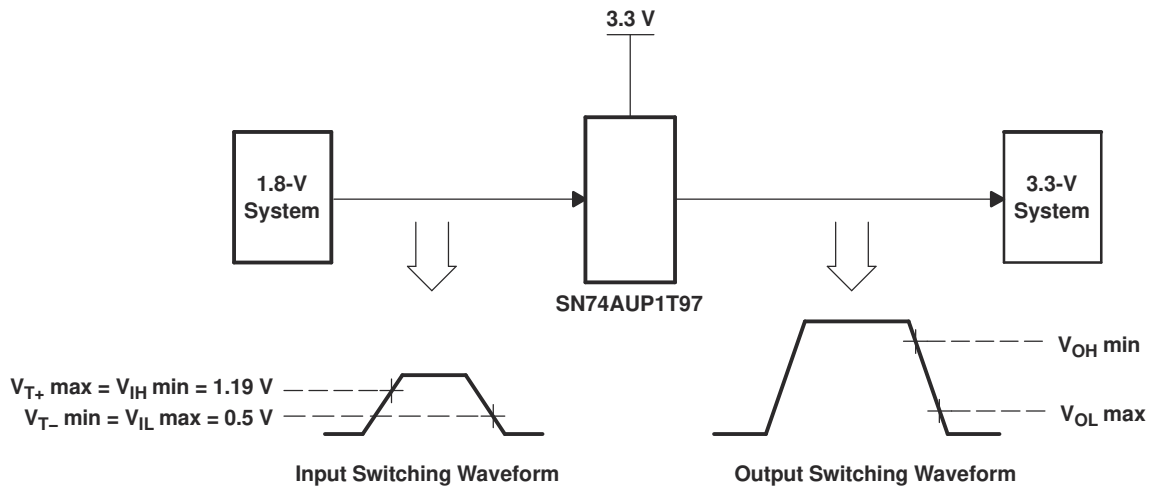


7-1. Logic Diagram (Positive Logic)

7.2 Feature Description



7-2. Possible Voltage-Translation Combinations



7-3. Switching Thresholds for 1.8-V to 3.3-V Translation

7.3 Device Functional Modes

表 7-1 lists the functional modes of the SN74AUP1T97.

表 7-1. Function Table

INPUTS			OUTPUT Y
C	B	A	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

7.3.1 Logic Configurations

表 7-2. Function Selection Table

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	7-4
2-input AND gate	7-5
2-input OR gate with one inverted input	7-6
2-input NAND gate with one inverted input	7-6
2-input AND gate with one inverted input	7-7
2-input NOR gate with one inverted input	7-7
2-input OR gate	7-8
Inverter	7-9
Noninverted buffer	7-10

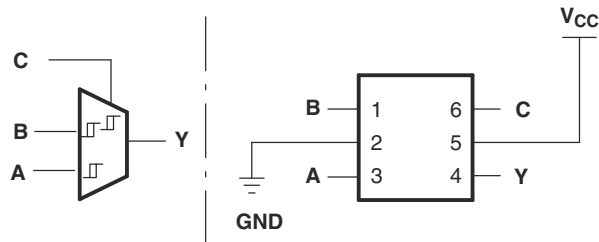


图 7-4. 157: 2-to-1 Data Selector/MUX
When C is L, Y = B
When C is H, Y = A

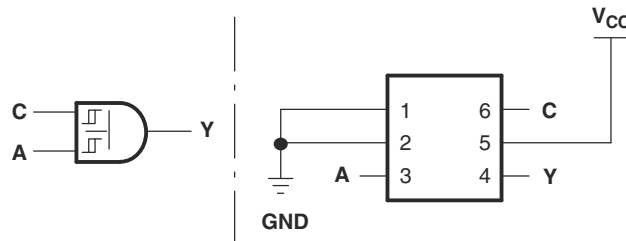
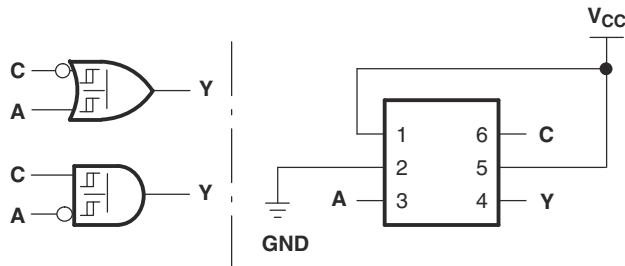
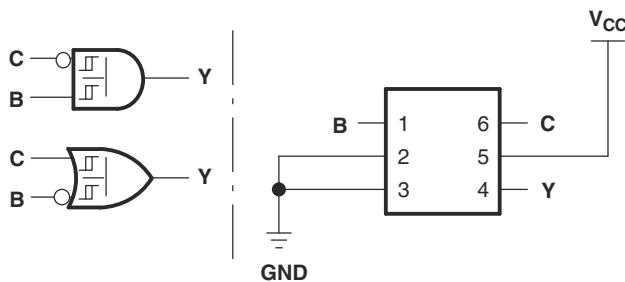


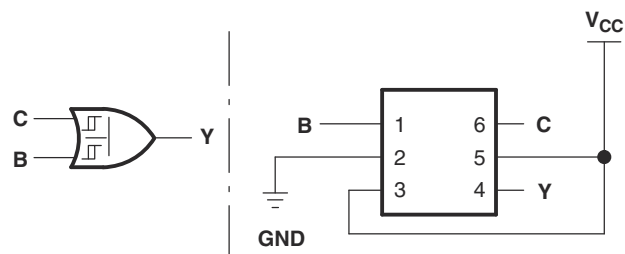
图 7-5. 08: 2-Input AND Gate



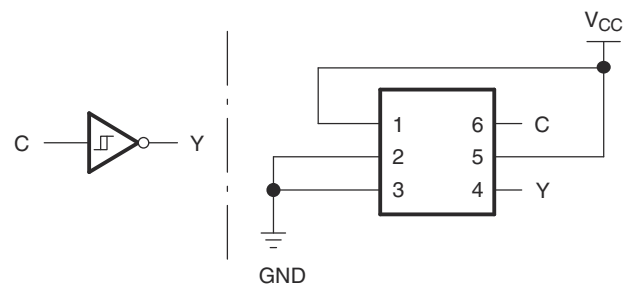
7-6. 14+32/14+00: 2-Input OR/NAND Gate With One Inverted Input



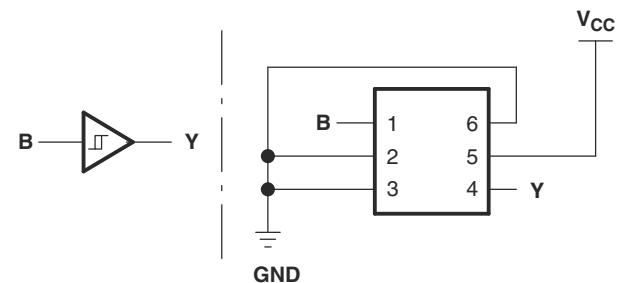
7-7. 14+08/14+02: 2-Input AND/NOR Gate With One Inverted Input



7-8. 32: 2-Input OR Gate



7-9. 04/14: Inverter



7-10. 17/34: Noninverted Buffer

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

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8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T97DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT4R	Samples
SN74AUP1T97DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HT4F, HT4R)	Samples
SN74AUP1T97DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(THF, THR)	Samples
SN74AUP1T97DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(THF, THR)	Samples
SN74AUP1T97DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TH	Samples
SN74AUP1T97DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TH	Samples
SN74AUP1T97YFPR	ACTIVE	DSBGA	YFP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TH2, THN)	Samples
SN74AUP1T97YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TH2, THN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T97DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T97DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T97DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T97DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T97DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1T97YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1T97YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T97DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T97DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1T97DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T97DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T97DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1T97YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1T97YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

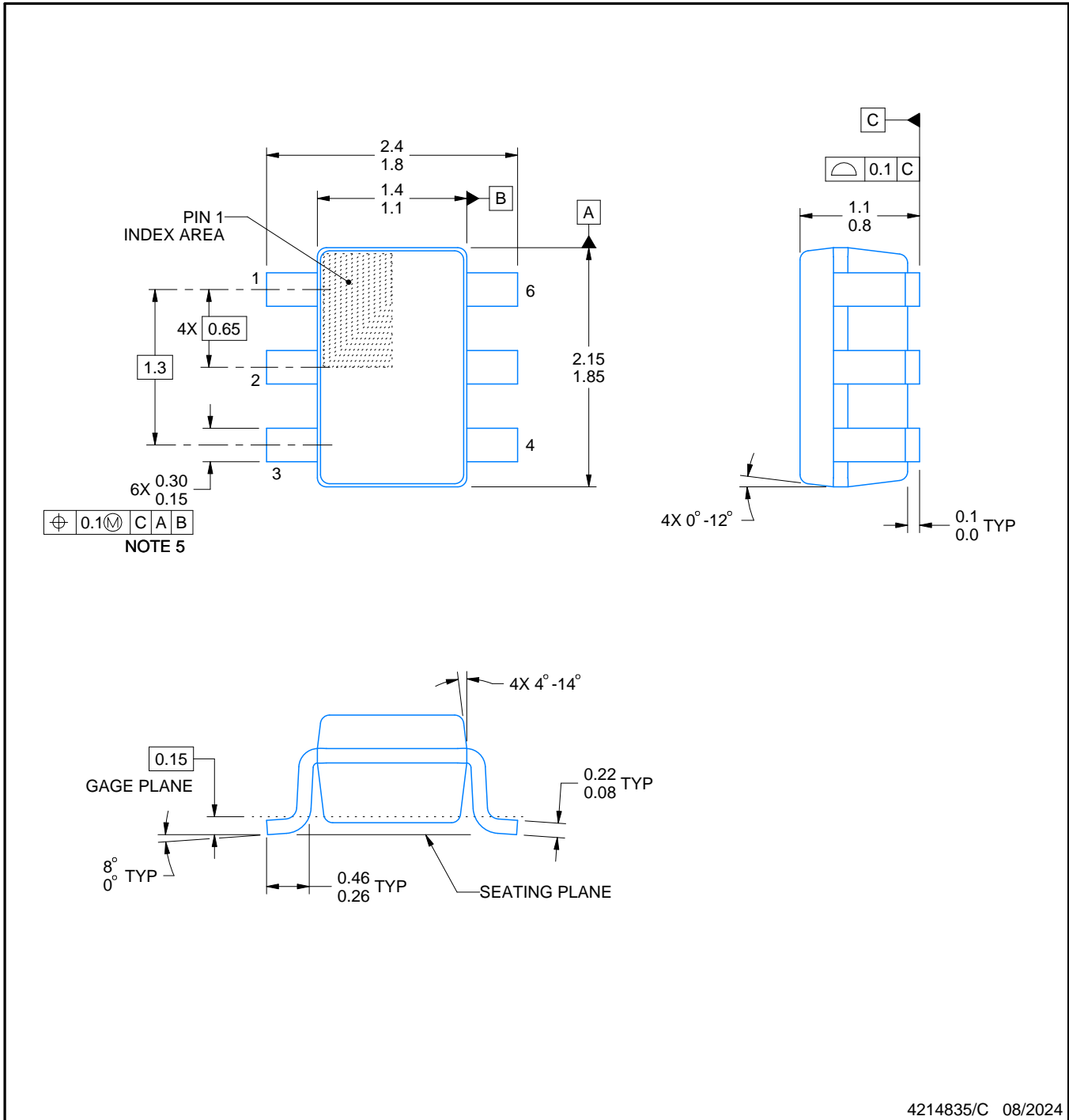
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

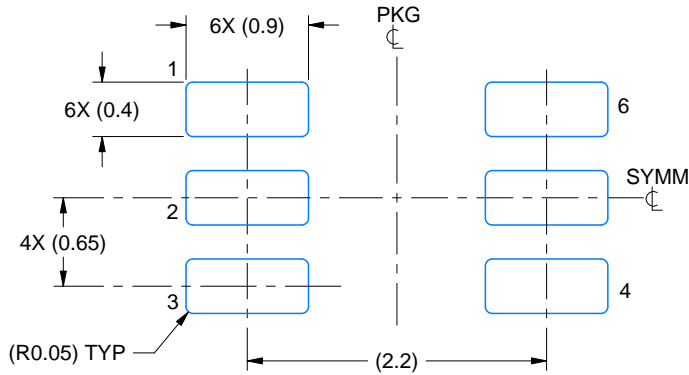
SMALL OUTLINE TRANSISTOR



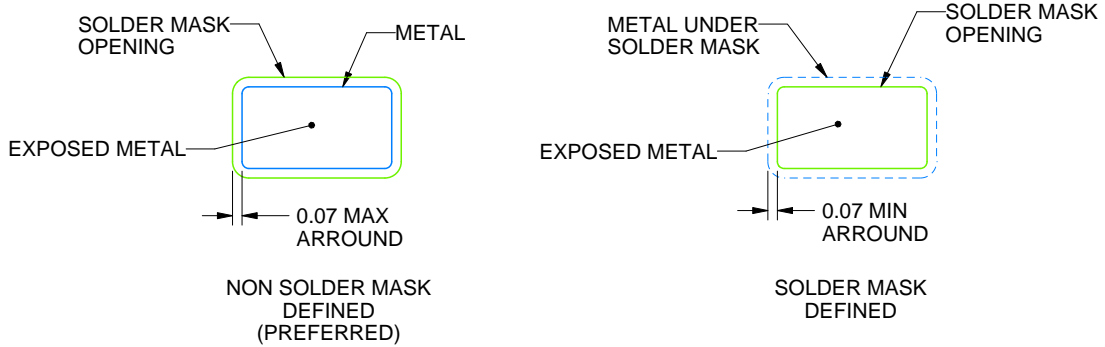
4214835/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

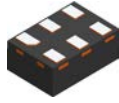
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

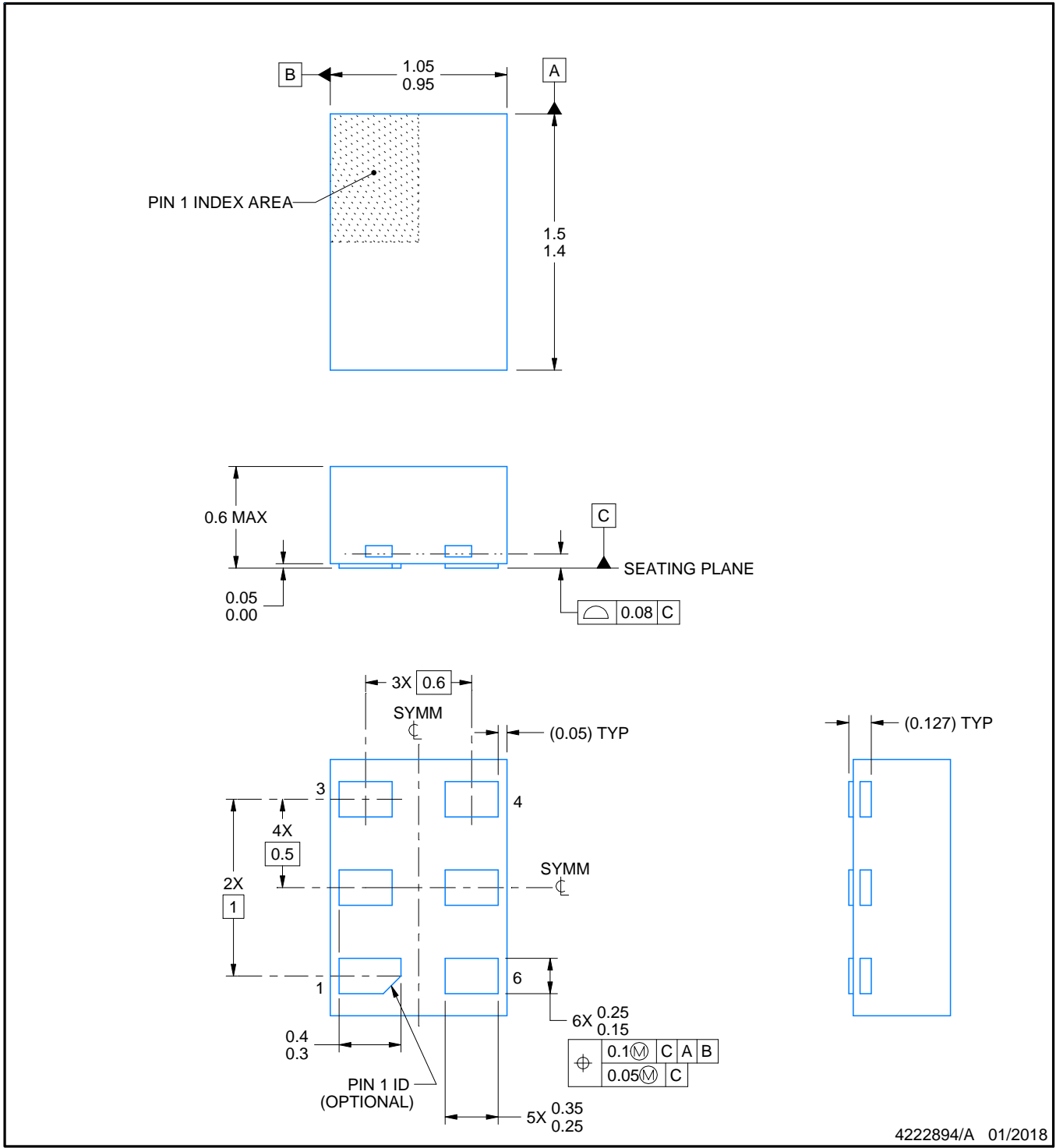
DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

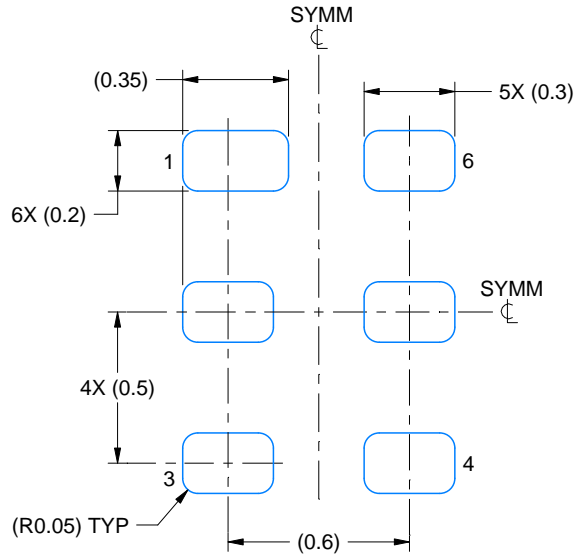
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

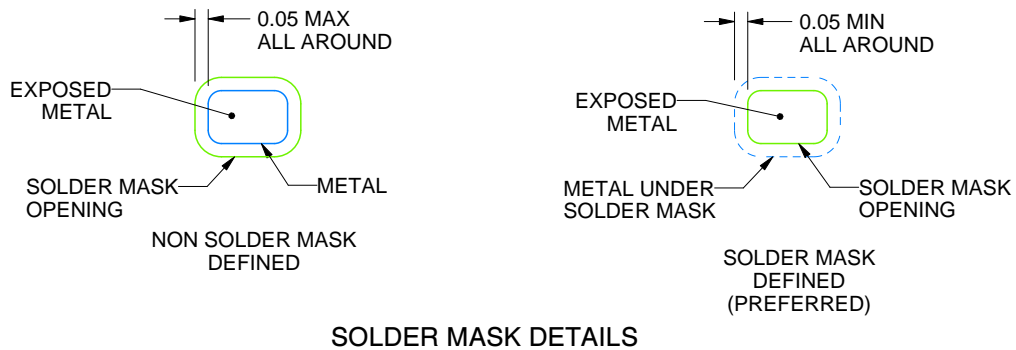
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

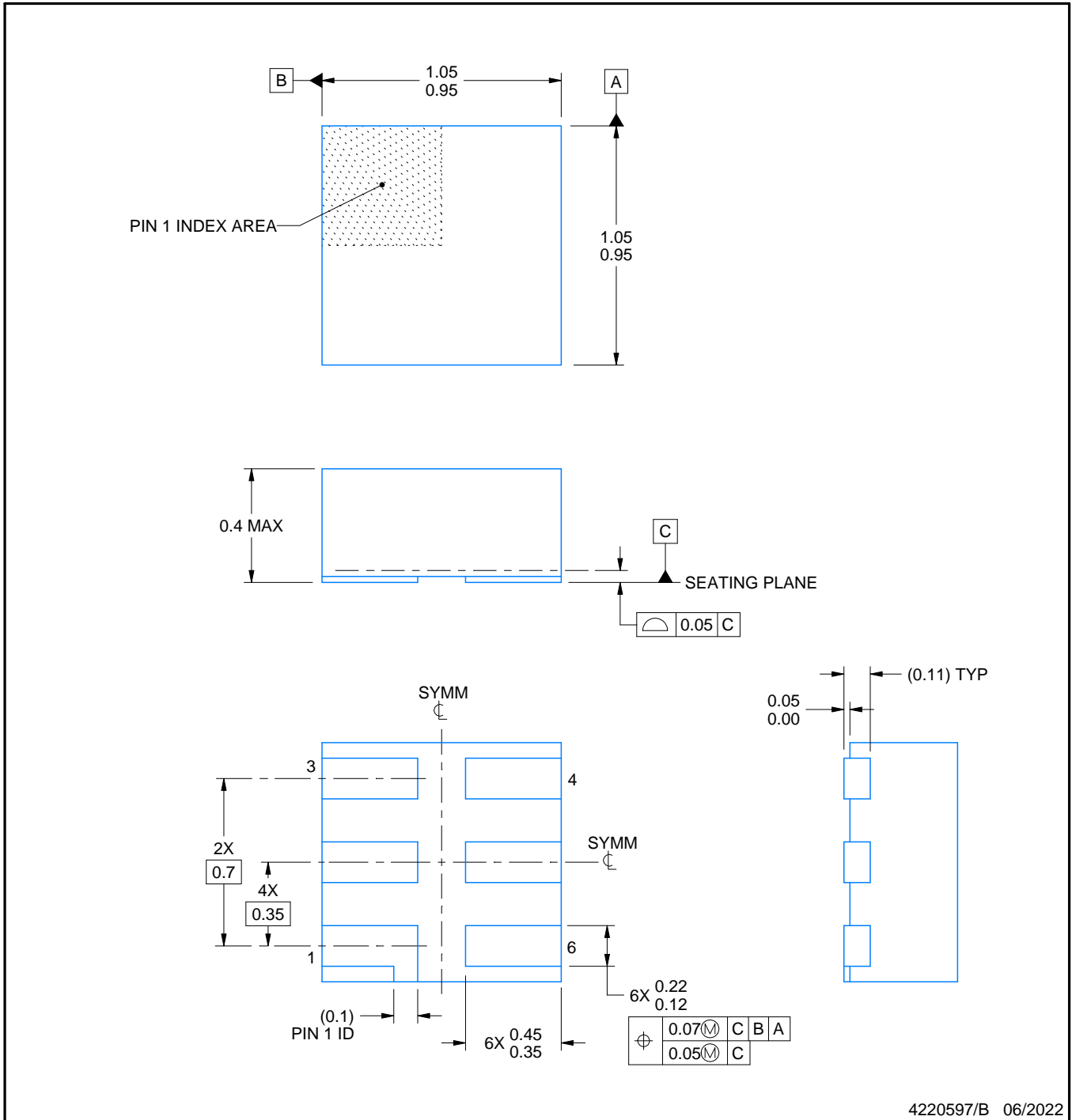


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



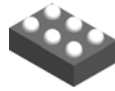
SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

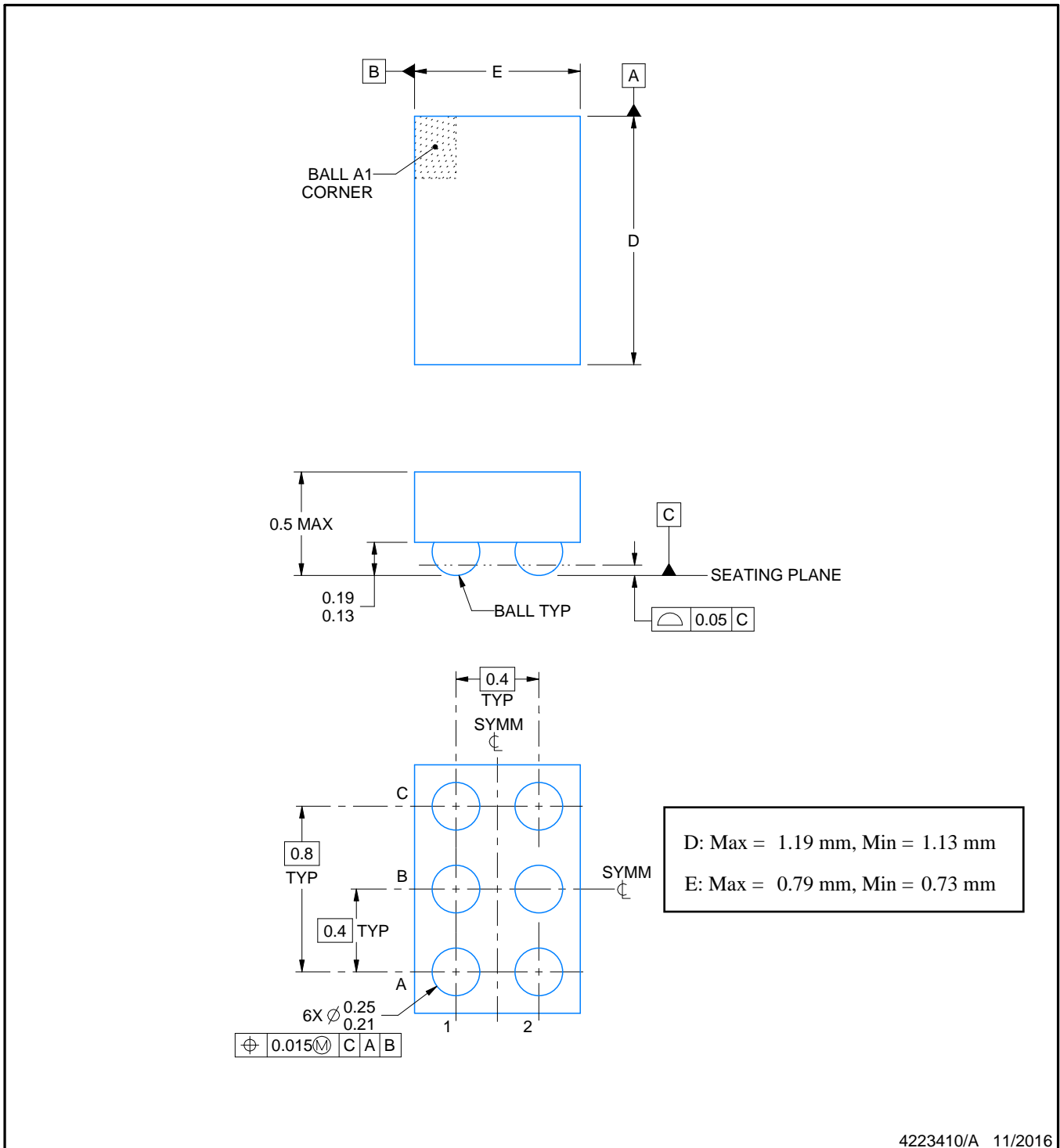
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

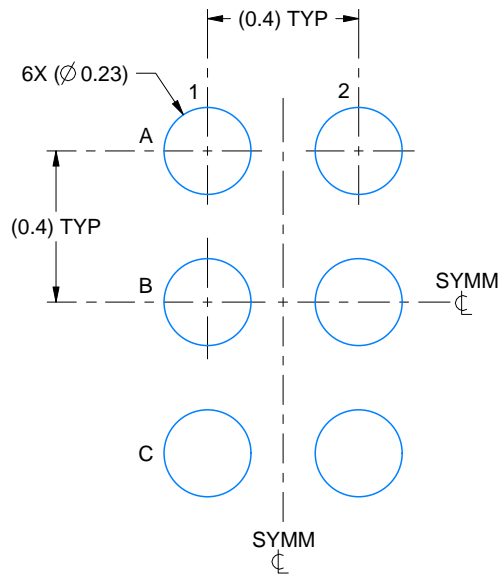
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

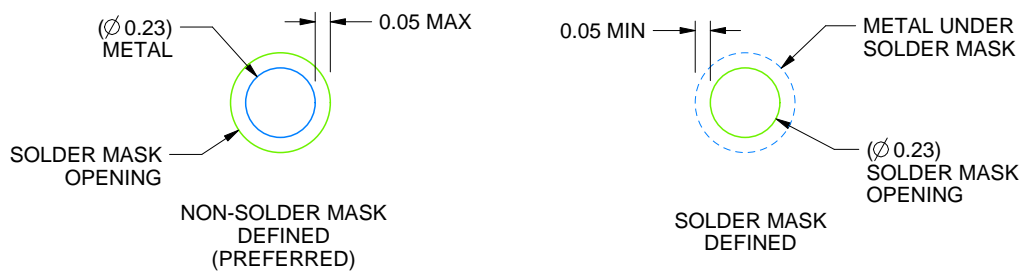
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

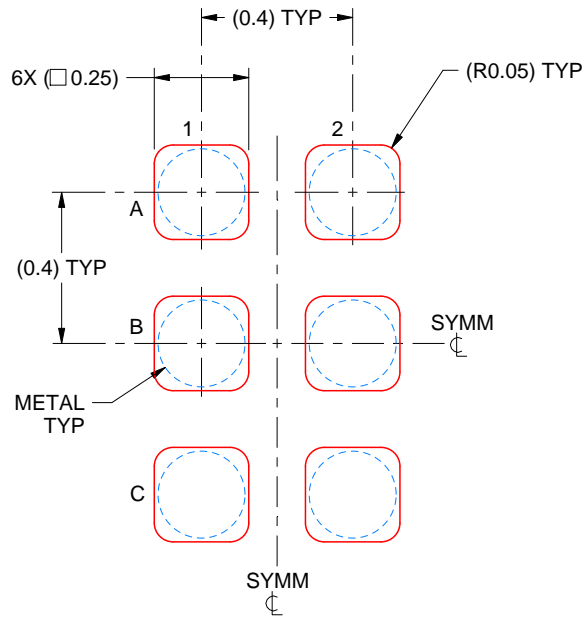
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

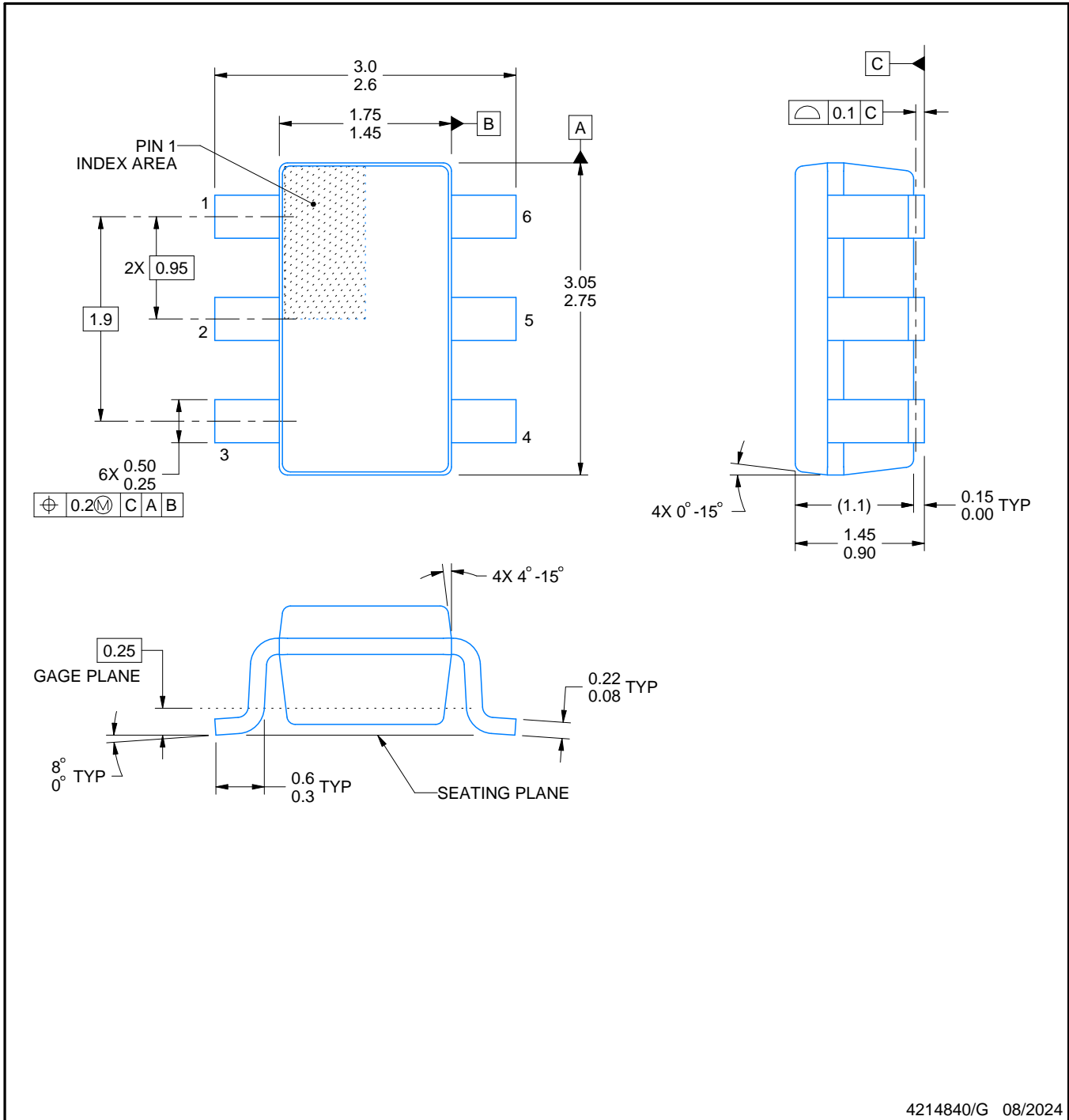
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



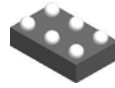
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

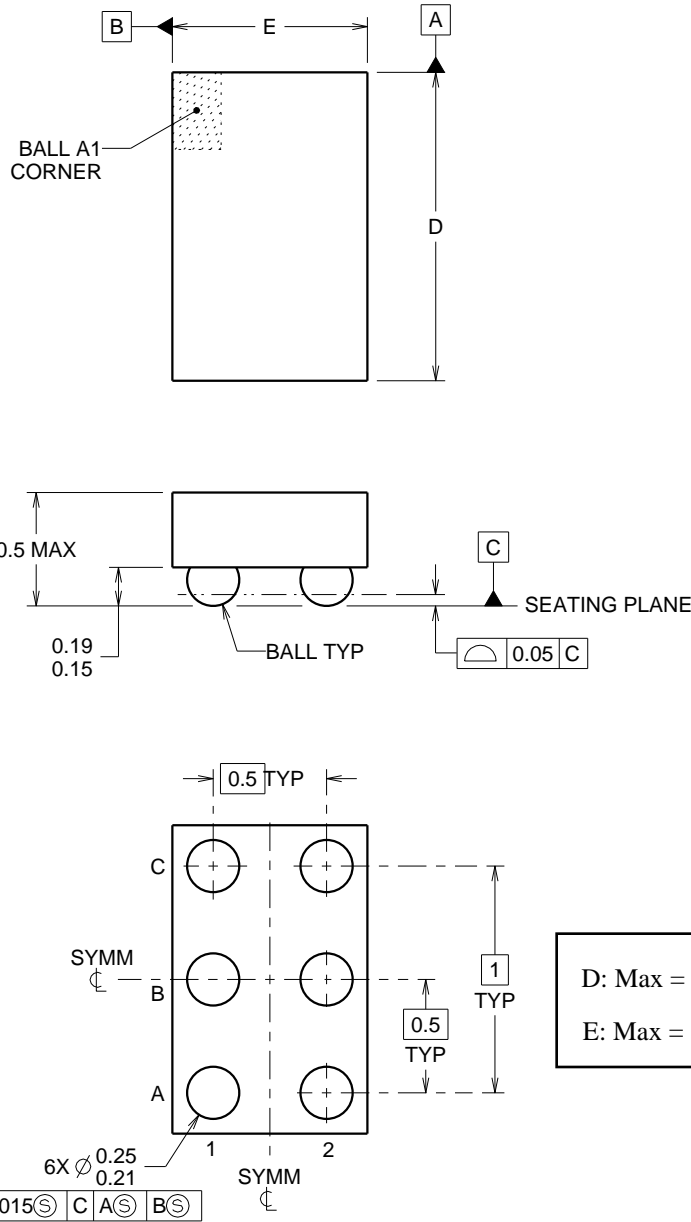
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm
 E: Max = 0.918 mm, Min = 0.858 mm

4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

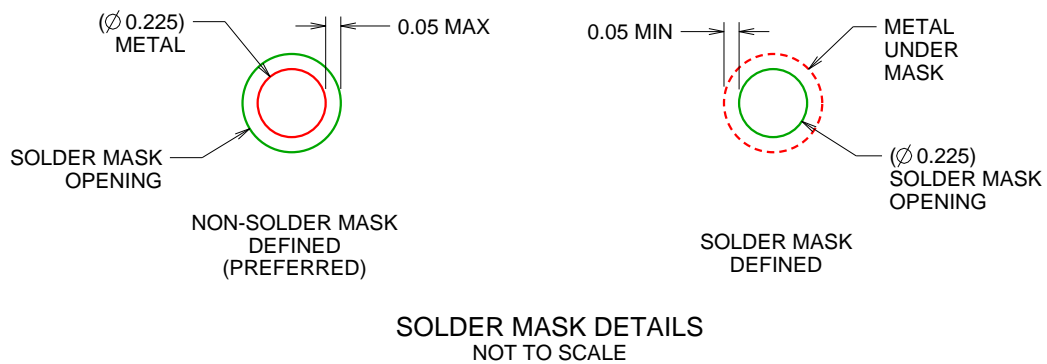
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



4219524/A 06/2014

NOTES: (continued)

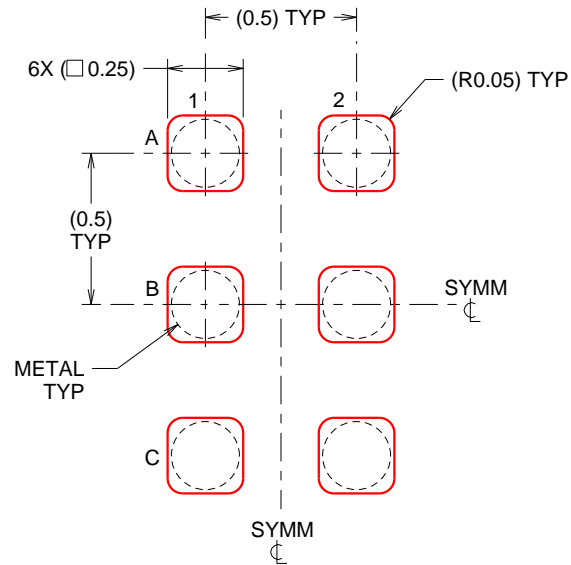
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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