

# SN74CB3Q3253 デュアル1 : 4 FETマルチプレクサ/デマルチプレクサ、 2.5V~3.3V低電圧高帯域バス・スイッチ

## 1 特長

- 高帯域データパス(最高500MHz)<sup>(1)</sup>
  - デバイスの電源オン時とオフ時の両方で5V許容のI/O
  - 動作範囲全体にわたって小さく平坦なオン抵抗( $r_{on}$ )特性( $r_{on} = 4\Omega$ 、標準値)
  - データI/Oポートのレール・ツー・レール・スイッチング
    - 3.3V  $V_{CC}$ で0~5Vのスイッチング
    - 2.5V  $V_{CC}$ で0~3.3Vのスイッチング
  - 伝播遅延がゼロに近い双方向データ・フロー
  - 低い入力/出力容量により負荷および信号歪みが最小化( $C_{io(OFF)} = 3.5pF$ 、標準値)
  - 高いスイッチング周波数( $f_{OE} = 20MHz$ 、最大値)
  - データおよび制御入力にアンダーシュート・クランプ・ダイオードを搭載
  - 低い消費電力( $I_{CC} = 0.6mA$ 、標準値)
  - 2.3V~3.6Vの範囲の $V_{CC}$ で動作
  - データI/Oは0~5Vの信号レベルに対応(0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V)
  - 制御入力をTTLまたは5V/3.3V CMOS出力で駆動可能
  - $I_{off}$ により部分的パワーダウン・モードをサポート
  - JESD 78, Class II準拠で100mA超のラッチアップ性能
  - ESD性能はJESD 22に準拠しテスト済み
    - 人体モデルで2000V (A114-B, クラス II)
    - 荷電デバイス・モデルで1000V (C101)
  - デジタルとアナログの両方のアプリケーションに対応: USBインターフェイス、差動信号インターフェイス・バス絶縁、低歪の信号ゲーティング
- <sup>(1)</sup> CB3Qファミリの性能特性の詳細情報については、TIのアプリケーション・レポート『CBT-C、CB3T、CB3Q信号スイッチ・ファミリ』(SCDA008)を参照してください。

## 2 アプリケーション

- ビデオ放送: IPベースのマルチ・フォーマット・トランスコーダ
- ビデオ通信システム

## 3 概要

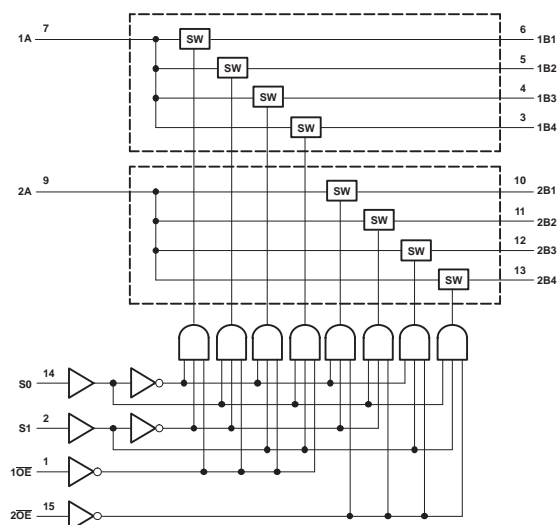
SN74CB3Q3253デバイスは高帯域のFETバス・スイッチで、チャージ・ポンプを使用してバス・トランジスタのゲート電圧を上昇させ、低い平坦なオン抵抗( $r_{on}$ )を実現します。オン抵抗が低く平坦であるため、伝搬遅延を最小限に抑えることができ、データ入出力(I/O)ポートでのレール・ツー・レール・スイッチングをサポートします。

### 製品情報

型番	パッケージ	本体サイズ(公称)
SN74CB3Q3253DBQ	SSOP (16)	4.90mm×3.90mm
SN74CB3Q3253DGV	TVSOP (16)	3.60mm×4.40mm
SN74CB3Q3253RGY	VQFN (16)	4.00mm×3.50mm
SN74CB3Q3253PW	TSSOP (16)	5.00mm×4.40mm

<sup>(1)</sup> 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### ロジック図(正論理)



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## 4 改訂履歴

### Revision B (June 2015) から Revision C に変更

Page

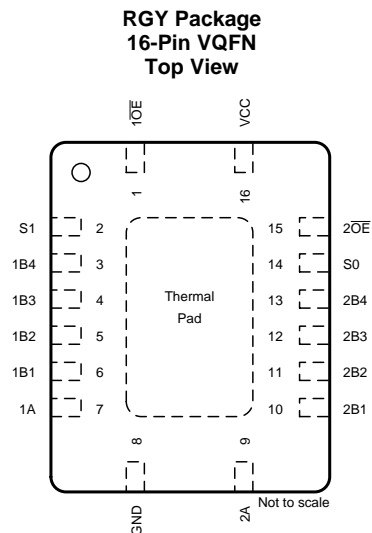
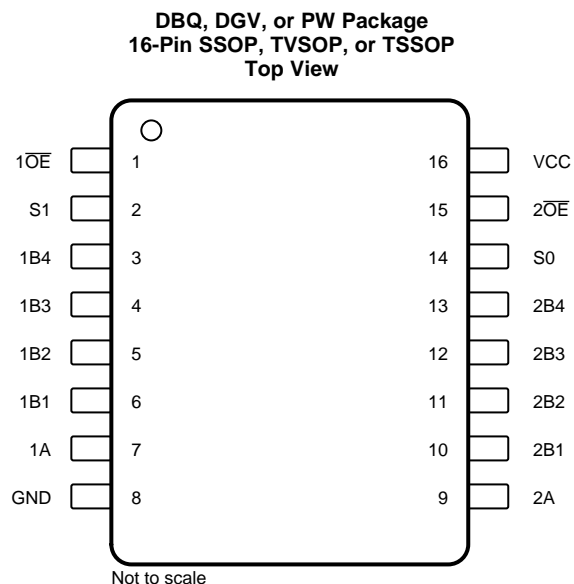
•	Changed the pinout image appearance .....	3
•	Updated the <i>Thermal Information</i> table .....	5

### Revision A (November 2003) から Revision B に変更

Page

•	「注文情報」表を削除 .....	1
•	「アプリケーション」セクション、「製品情報」表、「ピン構成および機能」表、「保管条件」表、「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ...	1

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{1OE}$	1	I	Output Enable 1 Active-Low
S1	2	I	Select Pin 1
1B4	3	I/O	Channel 1 I/O 4
1B3	4	I/O	Channel 1 I/O 3
1B2	5	I/O	Channel 1 I/O 2
1B1	6	I/O	Channel 1 I/O 1
1A	7	I/O	Channel 1 common
GND	8	—	Ground
2A	9	I/O	Channel 2 common
2B1	10	I/O	Channel 2 I/O 1
2B2	11	I/O	Channel 2 I/O 2
2B3	12	I/O	Channel 2 I/O 3
2B4	13	I/O	Channel 2 I/O 4
S0	14	I	Select Pin 0
$\overline{2OE}$	15	I	Output Enable 2 Active-Low
V <sub>CC</sub>	16	—	Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	4.6	V
V <sub>IN</sub>	Control input voltage <sup>(2)(3)</sup>	-0.5	7	V
V <sub>I/O</sub>	Switch I/O voltage <sup>(2)(3)(4)</sup>	-0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0	-50	mA
I <sub>I/O</sub>	I/O port clamp current	V <sub>I/O</sub> < 0	-50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>		±64	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	+2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	+1000
			V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	5.5
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	5.5
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0	0.7
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	0.8
V <sub>I/O</sub>	Data input/output voltage	0	5.5	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74CB3Q3253				UNIT
	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	
	16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	114.3	126	112.7	45.7	°C/W
R <sub>θJC(top)</sub> Junction-to-case (top) thermal resistance	65.4	51.3	47.5	59.6	°C/W
R <sub>θJB</sub> Junction-to-board thermal resistance	56.8	57.8	57.85	23.3	°C/W
ψ <sub>JT</sub> Junction-to-top characterization parameter	18.3	5.9	6	2.2	°C/W
ψ <sub>JB</sub> Junction-to-board characterization parameter	56.4	57.3	57.3	23.4	°C/W
R <sub>θJC(bot)</sub> Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 3.6 V,	I <sub>I</sub> = -18 mA			-1.8	V
I <sub>IN</sub> Control inputs	V <sub>CC</sub> = 3.6 V,	V <sub>IN</sub> = 0 to 5.5 V			±1	μA
I <sub>OZ</sub> <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±1	μA
I <sub>off</sub>	V <sub>CC</sub> = 0,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0			1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V,	I <sub>I/O</sub> = 0, Switch ON or OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND		0.6	2	mA
ΔI <sub>CC</sub> <sup>(4)</sup> Control inputs	V <sub>CC</sub> = 3.6 V,	One input at 3 V, Other inputs at V <sub>CC</sub> or GND			30	μA
I <sub>CCD</sub> <sup>(5)</sup> Per control input	V <sub>CC</sub> = 3.6 V, Control input switching at 50% duty cycle	A and B ports open, OE input		0.15	0.16	mA/ MHz
		S input		0.04	0.05	
C <sub>in</sub> Control inputs	V <sub>CC</sub> = 3.3 V,	V <sub>IN</sub> = 5.5 V, 3.3 V, or 0		2.5	3.5	pF
C <sub>io(OFF)</sub>	A port	V <sub>CC</sub> = 3.3 V, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0		8	11	pF
	B port	V <sub>CC</sub> = 3.3 V, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0		3.5	4.5	pF
C <sub>io(ON)</sub>	V <sub>CC</sub> = 3.3 V,	Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0		13	17	pF
r <sub>on</sub> <sup>(6)</sup>	V <sub>CC</sub> = 2.3 V, TYP at V <sub>CC</sub> = 2.5 V	V <sub>I</sub> = 0, I <sub>O</sub> = 30 mA		4	10	Ω
		V <sub>I</sub> = 1.7 V, I <sub>O</sub> = -15 mA		4.5	11	
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0, I <sub>O</sub> = 30 mA		3.5	8	
		V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA		4	10	

(1) V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

(2) All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.

(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see [Figure 2](#)).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

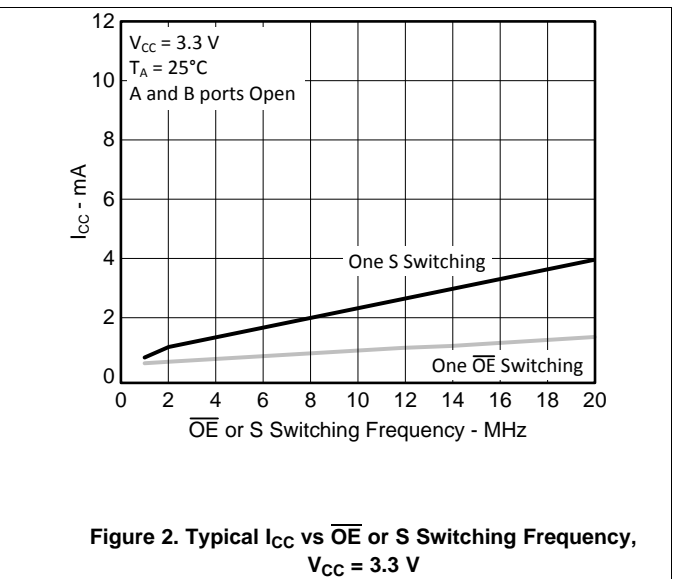
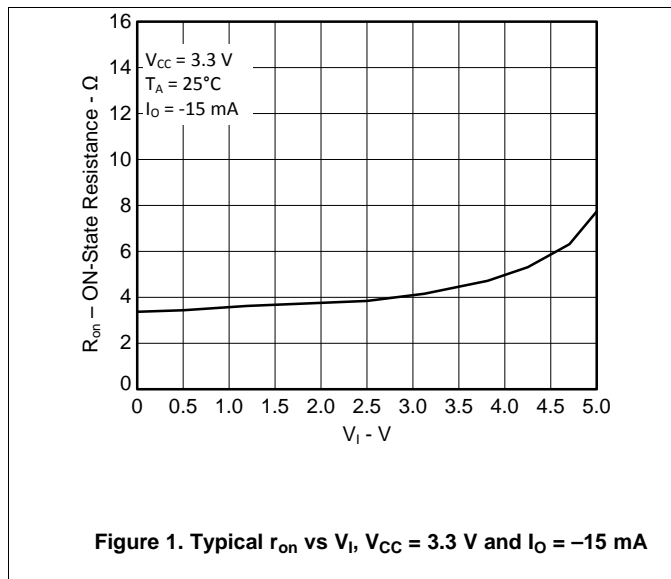
### 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

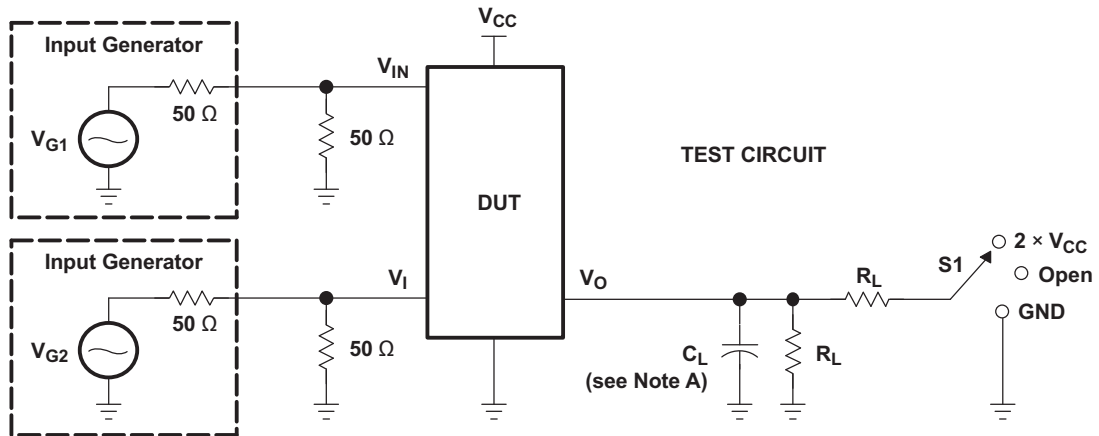
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f <sub>OE</sub> or f <sub>S</sub> <sup>(1)</sup>	OE or S	A or B		10		20	MHz
t <sub>pd</sub> <sup>(2)</sup>	A or B	B or A		0.12		0.18	ns
t <sub>pd(s)</sub>	S	A	1.5	6.7	1.5	5.9	ns
t <sub>en</sub>	S	B	1.5	6.7	1.5	5.9	ns
	OE	A or B	1.5	6.7	1.5	5.9	
t <sub>dis</sub>	S	B	1	6.1	1	6.1	ns
	OE	A or B	1	6.1	1	6.1	

- (1) Maximum switching frequency for control input (V<sub>O</sub> > V<sub>CC</sub>, V<sub>I</sub> = 5 V, R<sub>L</sub> ≥ 1 MΩ, C<sub>L</sub> = 0).
- (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

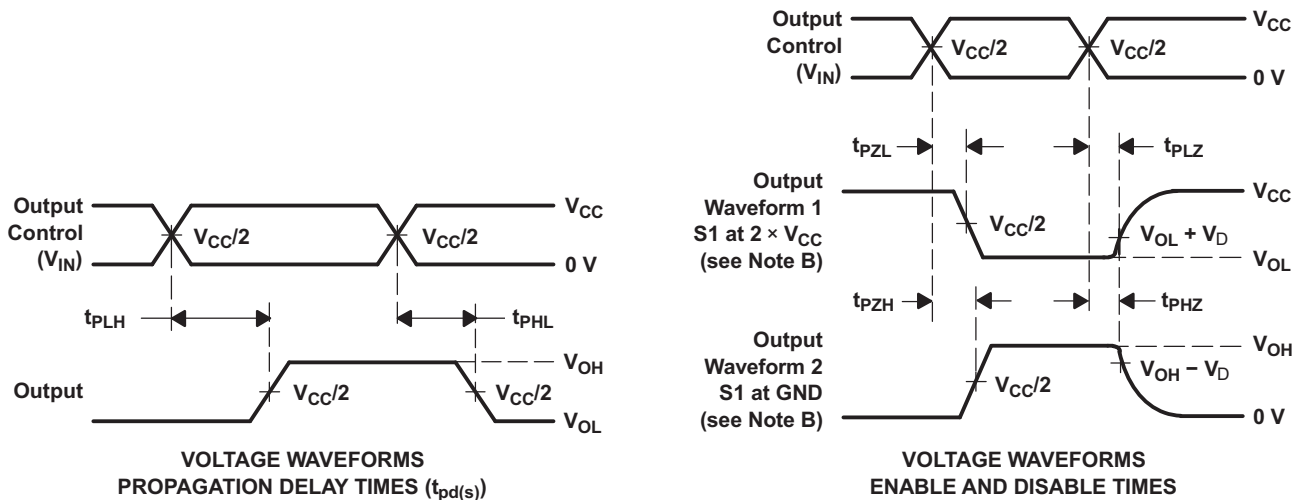
### 6.7 Typical Characteristics



## 7 Parameter Measurement Information



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	2.5 V ± 0.2 V	Open	500 Ω	V <sub>CC</sub> or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	GND	500 Ω	V <sub>CC</sub>	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

## 8 Detailed Description

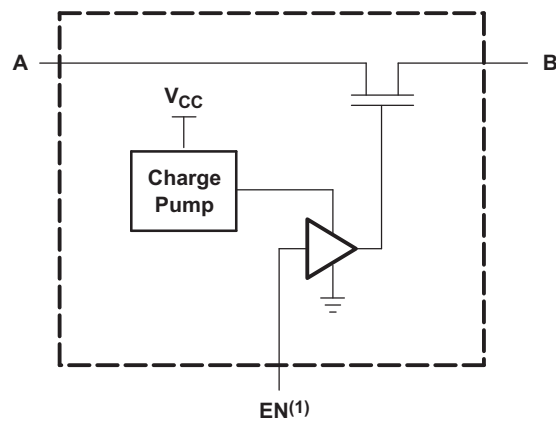
### 8.1 Overview

The SN74CB3Q3253 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3253 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3253 device is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When  $\overline{OE}$  is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

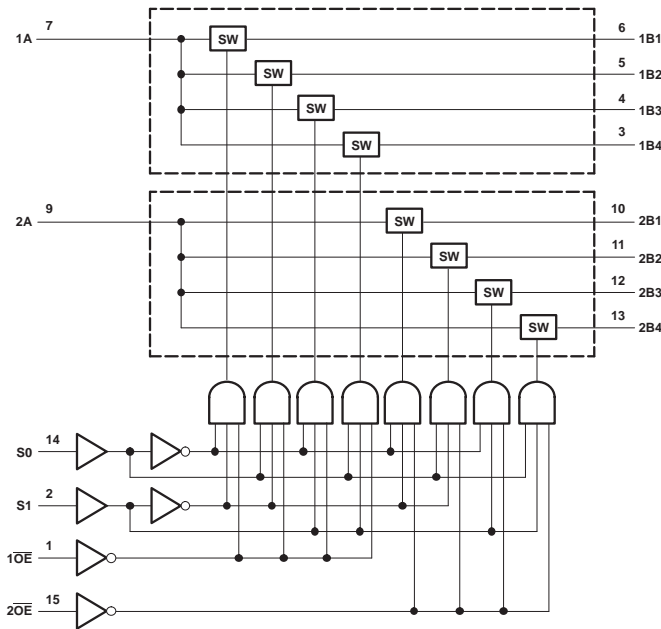


(1) EN is the internal enable signal applied to the switch.

**Figure 4. Simplified Schematic, Each FET Switch (SW)**



## 8.2 Functional Block Diagram



## 8.3 Feature Description

The SN74CB3Q3253 device has a high-bandwidth data path (up to 500 MHz) and has 5-V tolerant I/Os with the device powered up or powered down. It also has low and flat ON-state resistance ( $r_{on}$ ) characteristics over operating range ( $r_{on} = 4 \Omega$  Typical)

This device also has rail-to-rail switching on data I/O ports for 0- to 5-V switching with 3.3-V  $V_{CC}$  and 0- to 3.3-V switching with 2.5-V  $V_{CC}$  as well as bidirectional data flow with near-zero propagation delay and low input and output capacitance that minimizes loading and signal distortion ( $C_{iO(OFF)} = 3.5 \text{ pF}$  Typical)

The SN74CB3Q3253 also provides a fast switching frequency ( $f_{OE} = 20 \text{ MHz}$  Maximum) with data and control inputs that provide undershoot clamp diodes as well as low power consumption ( $I_{CC} = 0.6 \text{ mA}$  Typical)

The  $V_{CC}$  operating range is from 2.3 V to 3.6 V and the data I/Os support 0- to 5-V signal levels of (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)

The control inputs can be driven by TTL or 5-V and 3.3-V CMOS outputs as well as  $I_{off}$  Supports Partial-Power-Down Mode Operation

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74CB3Q3253.

**Table 1. Function Table  
(Each Multiplexer/Demultiplexer)**

INPUTS			INPUT/OUTPUT	FUNCTION
$\overline{OE}$	S1	S0	A	
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect

## 9 Application and Implementation

### NOTE

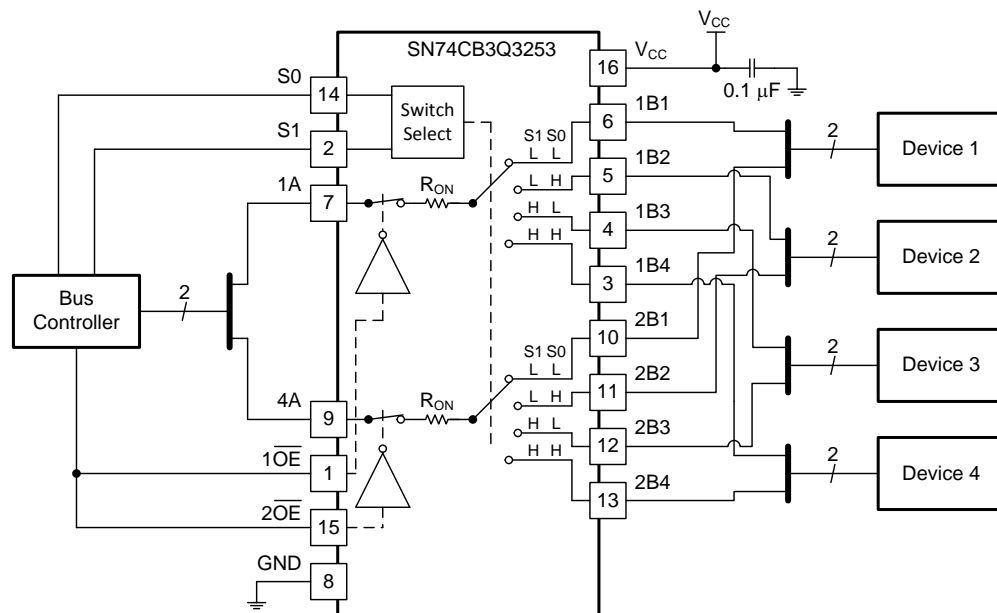
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74CB3Q3253 device can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration.

### 9.2 Typical Application

The application shown here is a 4-bit bus being multiplexed between two devices. the  $\overline{OE}$  and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.



**Figure 5. Typical Application of the SN74CB3Q3253**

#### 9.2.1 Design Requirements

The 0.1-µF capacitor should be placed as close as possible to the device.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#).
  - Inputs and outputs are overvoltage tolerant allowing them to go as high as 4.6 V at any valid  $V_{CC}$ .
2. Recommended Output Conditions:
  - Load currents should not exceed  $\pm 128$  mA per channel.
3. Frequency Selection Criterion:
  - Maximum frequency tested is 500 MHz.
  - Added trace resistance and capacitance can reduce maximum frequency capability; use layout practices as directed in [Layout](#).

## Typical Application (continued)

### 9.2.3 Application Curve

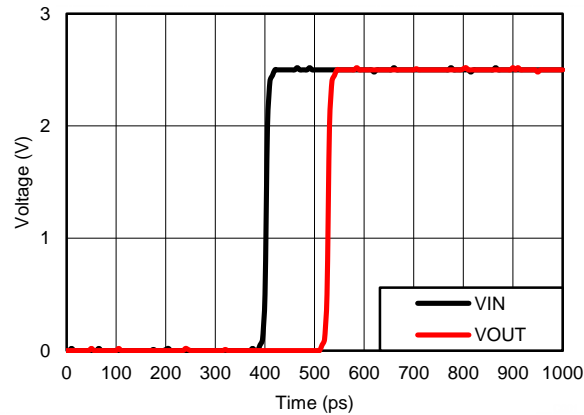


Figure 6. Propagation Delay ( $t_{pd}$ ) Simulation Result at  $V_{CC} = 2.5\text{ V}$

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Absolute Maximum Ratings](#) table.

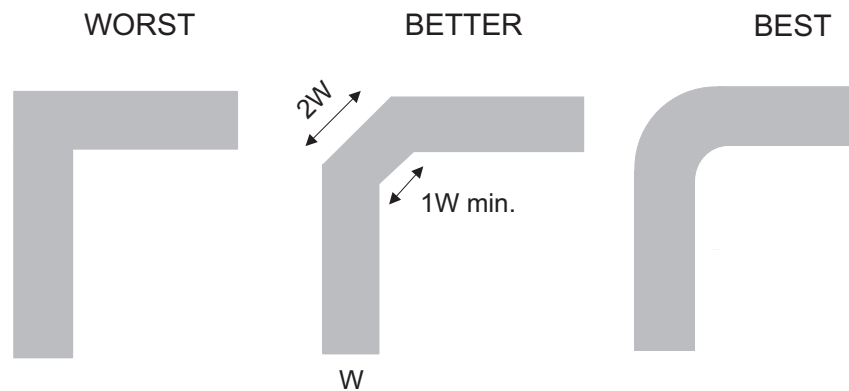
Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu\text{F}$  bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 7](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 11.2 Layout Example



**Figure 7. Trace Example**

## 12 デバイスおよびドキュメントのサポート

### 12.1 ドキュメントのサポート

#### 12.1.1 関連資料

関連資料については、以下を参照してください。

- 『低速またはフローティングCMOS入力の影響』、[SCBA004](#)
- 『テキサス・インスツルメンツ製信号スイッチの的確な選択』、[SZZA030](#)

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**設計サポート** TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3Q3253DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253	<a href="#">Samples</a>
SN74CB3Q3253DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253	<a href="#">Samples</a>
SN74CB3Q3253PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	BU253	
SN74CB3Q3253PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253	<a href="#">Samples</a>
SN74CB3Q3253RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3253DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3Q3253DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3253PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3253RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3253DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CB3Q3253DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CB3Q3253PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CB3Q3253RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



# EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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