

## SN74CBTLV1G125-Q1 低電圧シングル FET バス・スイッチ

### 1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - デバイス温度グレード 1:
    - 40°C ~ +125°C、 $T_A$
- 2つのポート間を5 $\Omega$ スイッチで接続
- データI/Oポートのレール・ツー・レール・スイッチング
- $I_{off}$ により部分的パワーダウン・モード動作をサポート

### 2 アプリケーション

- 換気扇

### 3 概要

SN74CBTLV1G125は、シングル高速ライン・スイッチです。このスイッチは、出力イネーブル( $\overline{OE}$ )入力がHIGHのときディセーブルになります。

このデバイスは、 $I_{off}$ を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。 $I_{off}$ 機能により、電源オフ時に損傷を引き起こすような電流がデバイスに逆流しないことが保証されます。デバイスは、電源オフ時は絶縁されています。

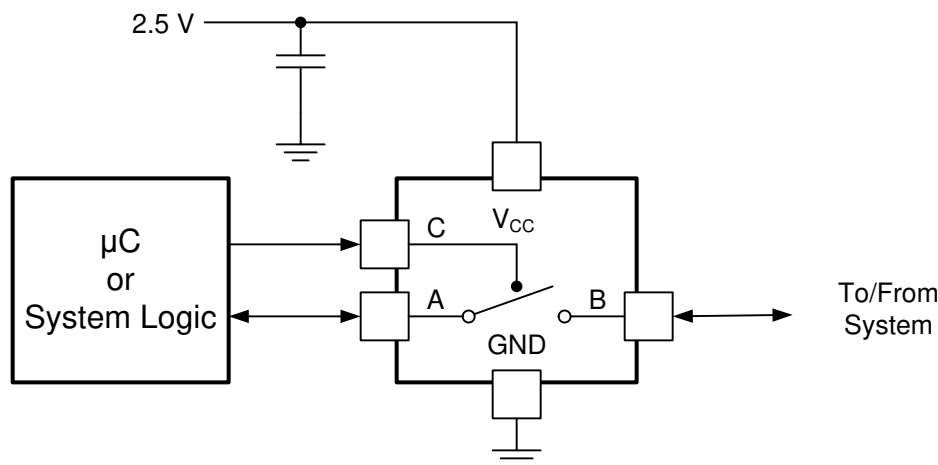
電源オンまたは電源オフ時に高インピーダンス状態を確保するため、 $\overline{OE}$ はプルアップ抵抗経路で $V_{CC}$ に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決定されます。

#### 製品情報<sup>(1)</sup>

発注型番	パッケージ	本体サイズ
SN74CBTLV1G125-Q1	SOT-23 (DBV) (5)	2.90mmx1.60mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

#### アプリケーション回路図



## 目次

1	特長 .....	1	8.4	Device Functional Modes .....	7
2	アプリケーション .....	1	<b>9</b>	<b>Application and Implementation</b> .....	<b>8</b>
3	概要 .....	1	9.1	Application Information .....	8
4	改訂履歴 .....	2	9.2	Typical Application .....	8
5	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>9</b>
6	<b>Specifications</b> .....	<b>4</b>	<b>11</b>	<b>Layout</b> .....	<b>9</b>
6.1	Absolute Maximum Ratings .....	4	11.1	Layout Guidelines .....	9
6.2	ESD Ratings .....	4	11.2	Layout Example .....	9
6.3	Recommended Operating Conditions .....	4	<b>12</b>	<b>デバイスおよびドキュメントのサポート</b> .....	<b>10</b>
6.4	Thermal Information .....	4	12.1	デバイス・サポート .....	10
6.5	Electrical Characteristics .....	5	12.2	ドキュメントの更新通知を受け取る方法 .....	10
6.6	Switching Characteristics .....	5	12.3	コミュニティ・リソース .....	10
<b>7</b>	<b>Parameter Measurement Information</b> .....	<b>6</b>	12.4	商標 .....	10
<b>8</b>	<b>Detailed Description</b> .....	<b>7</b>	12.5	静電気放電に関する注意事項 .....	10
8.1	Overview .....	7	12.6	Glossary .....	10
8.2	Functional Block Diagram .....	7	<b>13</b>	<b>メカニカル、パッケージ、および注文情報</b> .....	<b>10</b>
8.3	Feature Description .....	7			

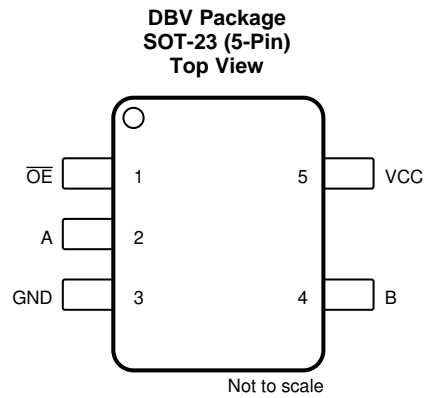
## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (December 2018) から Revision B に変更	Page
• 「特長」で「車載アプリケーション向けに認定済み」を「車載アプリケーション向けに AEC-Q100 認定済み」に変更 .....	1
• Changed the <i>ESD Ratings</i> table notes .....	4
• Changed the $T_A$ MAX value From: 85°C To 125°C in the <i>Recommended Operating Conditions</i> .....	4

2009年8月発行のものから更新	Page
• 「アプリケーション」一覧、「製品情報」表、「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 .....	1

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Active low enable
A	2	I/O	Switch I/O
GND	3	-	Ground
B	4	I/O	Switch I/O
V <sub>CC</sub>	5	-	Power Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
	Continuous channel current		128	mA
I <sub>IK</sub>	Input clamp current		-50	mA
		V <sub>I/O</sub> < 0		
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±2000
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74CBTLV1G125-Q1	UNIT
		SOT-23 (DBV)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	249.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	174.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	83.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	67.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	83.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 3\text{ V}$ , $I_I = -18\text{ mA}$				-1.2	V
$I_I$		$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND				±1	μA
$I_{off}$		$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to 3.6 V, $\overline{OE} = 3.6\text{ V}$				15	μA
		$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to 3.6 V, $\overline{OE} = 0\text{ V}$				100	
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND				10	μA
$\Delta I_{CC}$ <sup>(2)</sup>	Control inputs	$V_{CC} = 3.6\text{ V}$ , One input at 3 V, Other inputs at $V_{CC}$ or GND				300	μA
$C_i$	Control inputs	$V_I = 3\text{ V}$ or 0				2.5	pF
$C_{io(OFF)}$		$V_O = 3\text{ V}$ or 0, $\overline{OE} = V_{CC}$				7	pF
$r_{on}$ <sup>(3)</sup>	$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 32\text{ mA}$	7	10	Ω	
			$I_I = 24\text{ mA}$	7	10		
	$V_I = 1.7\text{ V}$	$I_I = 15\text{ mA}$	15	25			
		$V_I = 0$	$I_I = 32\text{ mA}$	5	7		
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 24\text{ mA}$	5	7		
			$V_I = 2.4\text{ V}$	$I_I = 15\text{ mA}$	10		15

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(3) Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

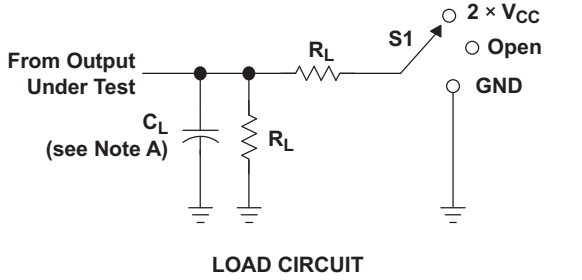
## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$ <sup>(1)</sup>	A or B	B or A	0.15		0.25		ns
$t_{en}$	$\overline{OE}$	A or B	0.5	8	0.5	7.5	ns
$t_{dis}$	$\overline{OE}$	A or B	0.5	8	0.5	7.5	ns

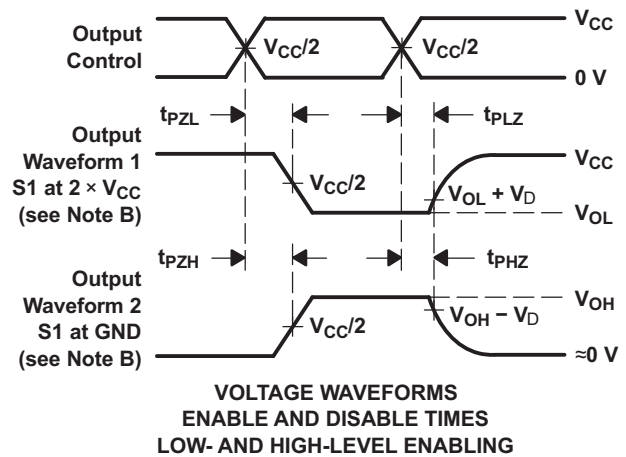
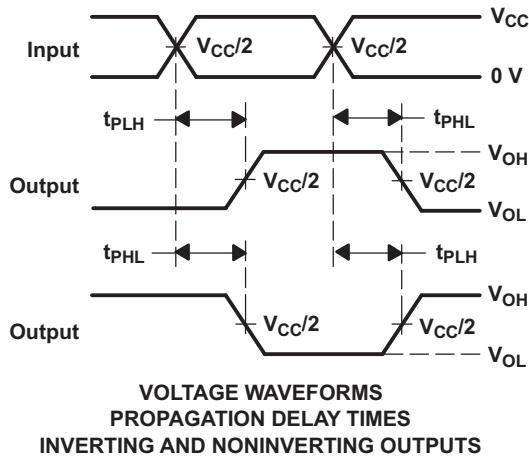
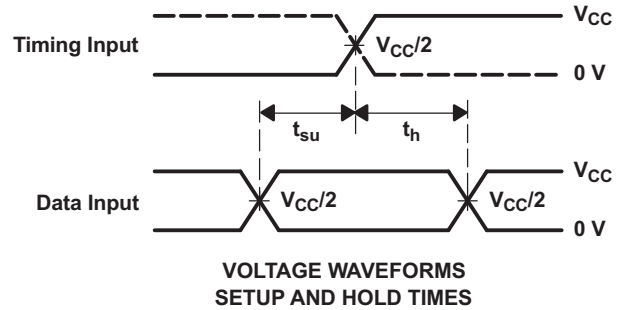
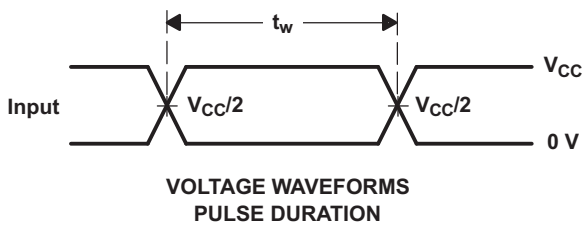
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

## 7 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_D$
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	50 pF	500 $\Omega$	0.3 V



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

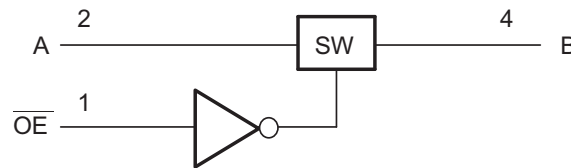
**Figure 1. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74CBTLV1G125 device is a 1-channel 1:1 high-speed FET switch. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. The  $\overline{\text{OE}}$  pin is an active low logic control pin that controls the data flow. The FET is disabled when the output-enable ( $\overline{\text{OE}}$ ) input is high. This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The SN74CBTLV1G125 features 5- $\Omega$  switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs.  $I_{\text{off}}$  supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on.

### 8.4 Device Functional Modes

Table 1 shows the functional modes of SN74CBTLV1G125.

Table 1. Function Table

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74CBTLV1G125 can be used to switch a signal path. The switch is bidirectional, so the A and B pins can be used as either inputs or outputs. This switch is typically used when there is one signal path that needs to be isolated at certain times.

### 9.2 Typical Application

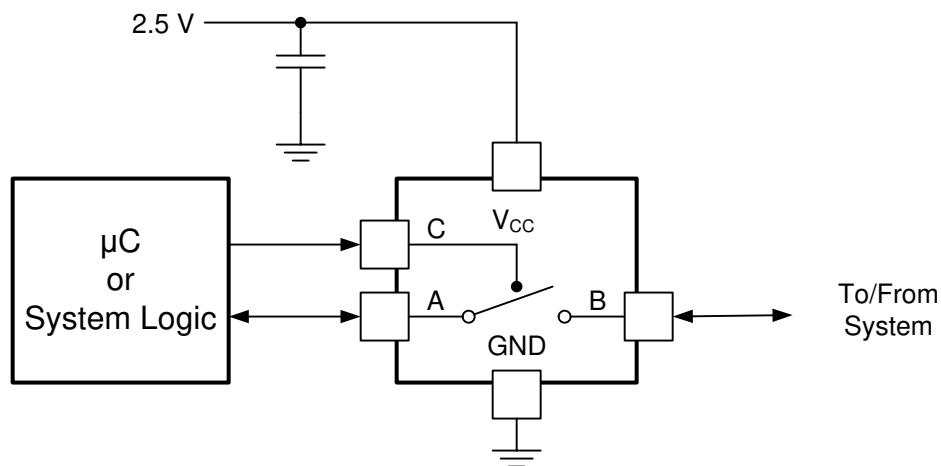


Figure 2. Typical Application

#### 9.2.1 Design Requirements

The SN74CBTLV1G125 device can be properly operated without any external components. TI recommends pulling up the digital control pin (OE) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin. A floating digital pin could cause excess current consumption refer to [Implications of Slow or Floating CMOS Inputs](#).

#### 9.2.2 Detailed Design Procedure

When  $\overline{OE}$  is high, the active bus. This means that there is a low impedance path between the A and B pins. The 0.1- $\mu$ F capacitor on VCC is a decoupling capacitor and should be placed as close as possible to the device.



## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the Recommended Operating Conditions table. Each VCC terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  bypass capacitor is recommended. If multiple pins are labeled VCC, then a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each VCC because the VCC pins are tied together internally. For devices with dual supply pins operating at different voltages, for example VCC and VDD, a 0.1- $\mu\text{F}$  bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight, and therefore; some traces must turn corners. Figure 3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 11.2 Layout Example

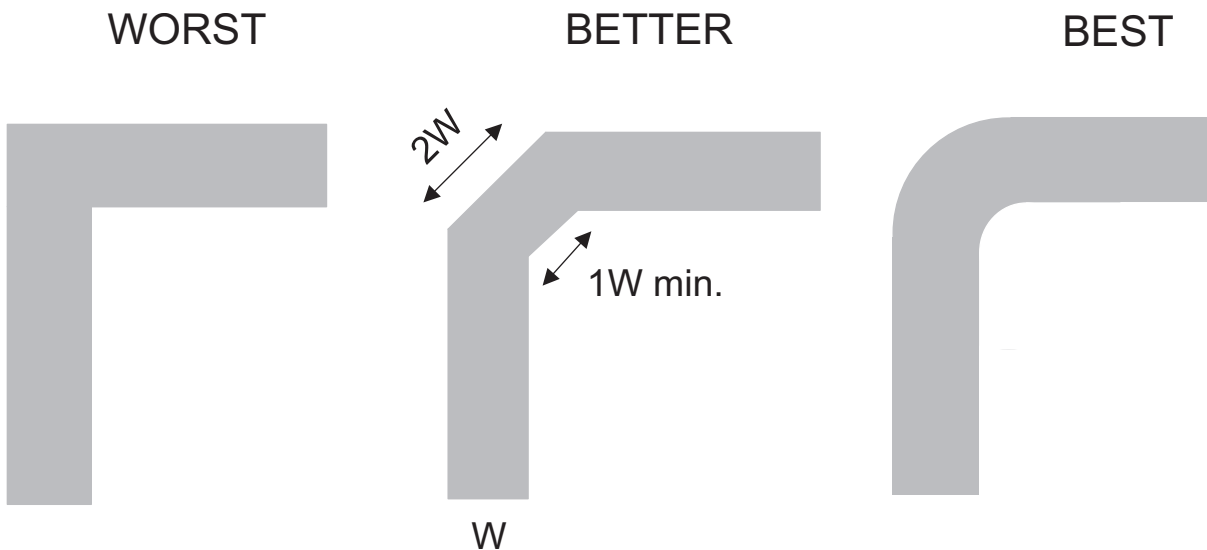


Figure 3. Example Layout

## 12 デバイスおよびドキュメントのサポート

### 12.1 デバイス・サポート

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E ( Engineer-to-Engineer )* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.4 商標

E2E is a trademark of Texas Instruments.

### 12.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV1G125DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCTO	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV1G125DBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV1G125DBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0

# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/J 02/2024

## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Reference JEDEC MO-178.
- Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated