

デュアル2ラインから4ラインへのデコーダ/デマルチプレクサ

1 特長

- 4.5V~5.5V の動作電源電圧範囲
- 出力は最大 10 個の LSTTL 負荷を駆動可能
- 低い消費電力、最大 I_{CC} 80 μ A
- $t_{pd} = 10ns$ (標準値)
- 5V で $\pm 4mA$ の出力駆動能力
- 低い入力電流、最大 1 μ A
- 入力は TTL 電圧互換
- 高速メモリ・デコーダおよびデータ伝送システム専用に設計
- 2 つのイネーブル入力を備え、カスケード接続やデータ受信を簡素化

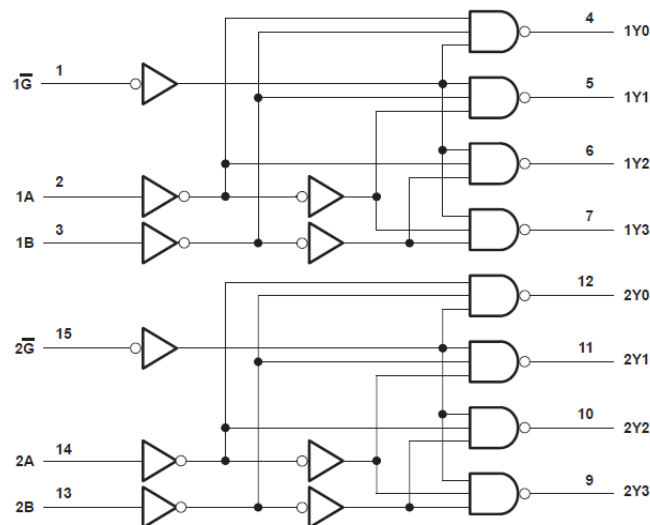
2 概要

'HCT139 デバイスは、伝搬遅延時間を極めて短くする必要がある、高性能のメモリ・デコーディングやデータ・ルーティングのアプリケーション用に設計されています。

製品情報 (1)

発注型番	パッケージ	本体サイズ (公称)
SN74HCT139	N (PDIP, 16)	19.31mm × 6.35mm
	D (SOIC, 16)	9.90mm × 3.90mm
	DB (SSOP, 16)	6.2mm × 5.3mm
	PW (TSSOP, 16)	5.00mm × 4.40mm
SNJ54HCT139	J (CDIP, 16)	24.38mm × 6.92mm
	W (CFP, 16)	10.3mm × 1.65mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



A. ここに示すピン番号は D、DB、J、N、PW、W の各パッケージのもので。

論理図 (正論理)

Table of Contents

1 特長	1	8.2 Functional Block Diagram.....	7
2 概要	1	8.3 Device Functional Modes.....	7
3 Revision History	2	9 Power Supply Recommendations	8
4 概要 (続き)	3	10 Layout	8
5 Pin Configuration and Functions	3	10.1 Layout Guidelines.....	8
6 Specifications	4	11 Device and Documentation Support	9
6.1 Absolute Maximum Rating.....	4	11.1 Documentation Support.....	9
6.2 Recommended Operating Conditions ⁽¹⁾	4	11.2 Receiving Notification of Documentation Updates....	9
6.3 Thermal Information.....	4	11.3 サポート・リソース.....	9
6.4 Electrical Characteristics.....	5	11.4 Trademarks.....	9
6.5 Switching Characteristics.....	5	11.5 Electrostatic Discharge Caution.....	9
6.6 Operating Characteristics.....	5	11.6 Glossary.....	9
7 Parameter Measurement Information	6	12 Mechanical, Packaging, and Orderable Information	9
8 Detailed Description	7		
8.1 Overview.....	7		

3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2003) to Revision E (August 2022)

Page

- | | |
|---|---|
| • 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新..... | 1 |
|---|---|

4 概要 (続き)

'HCT139 デバイスは、2 つの個別の 2 ライン入力、4 ライン出力デコーダを、1 つのパッケージに搭載したものです。アクティブ Low のイネーブル (G) 入力は、デマルチプレクサ・アプリケーションのデータ・ラインとして使用できます。これらのデコーダ / デマルチプレクサの入力は完全にバッファされ、それぞれの入力は、駆動回路に対して 1 つの正規化された負荷のみを表します。

5 Pin Configuration and Functions

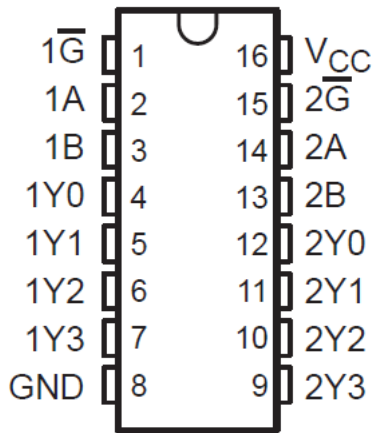
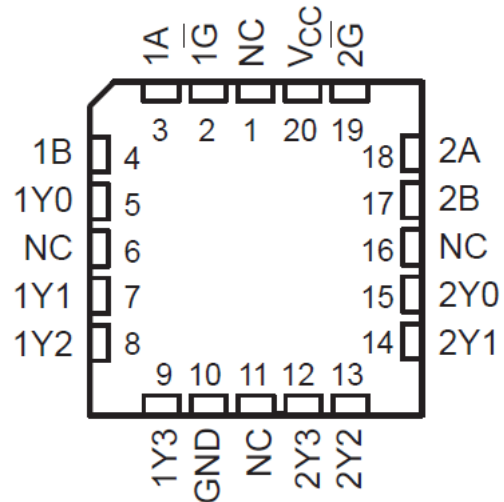


図 5-1. SN54HCT139 J or W Package
 SN74HCT139 D, DB, N, or PW Package
 Top View



A. NC - No internal connection

図 5-2. SN54HCT139 FK Package
 Top View

6 Specifications

6.1 Absolute Maximum Rating

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}	±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _J	Junction Temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Recommended Operating Conditions⁽¹⁾

		SN54HCT139			SN74HCT139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V		2	2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V		0.8	0.8			V
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) time			500			500	ns
T _A	Operating free-air temperature	-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	PW (TSSOP)	UNIT
THERMAL METRIC ⁽¹⁾		16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Package thermal impedance	73	82	67	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT139		SN74HCT139		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH} High level output voltage	V _I = V _{IH} or V _{IL}	4.5 V	I _{OH} = -20 μA	4.4	4.499		4.4		4.4	V
			I _{OH} = -4 mA	3.98	4.3		3.7		3.84	
V _{OL} Low level output voltage	V _I = V _{IH} or V _{IL}	4 V	I _{OL} = 20 μA		0.001	0.1		0.1	0.1	V
			I _{OL} = 4 mA		0.17	0.26		0.4	0.33	
I _I Input leakage current V	V _I = V _{CC} or 0	5.5 V		±0.1	±100		±1000	±1000	nA	
I _{CC} Supply current	V _I = V _{CC} or 0 I _O = 0	5.5 V			8		160	80	μA	
ΔI _{CC} (1) Supply-Current Change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V		1.4	2.4		3	2.9	mA	
C _i Input Capacitance		4.5 V to 5.5 V		3	10		10	10	pF	

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Fig 7-1](#))

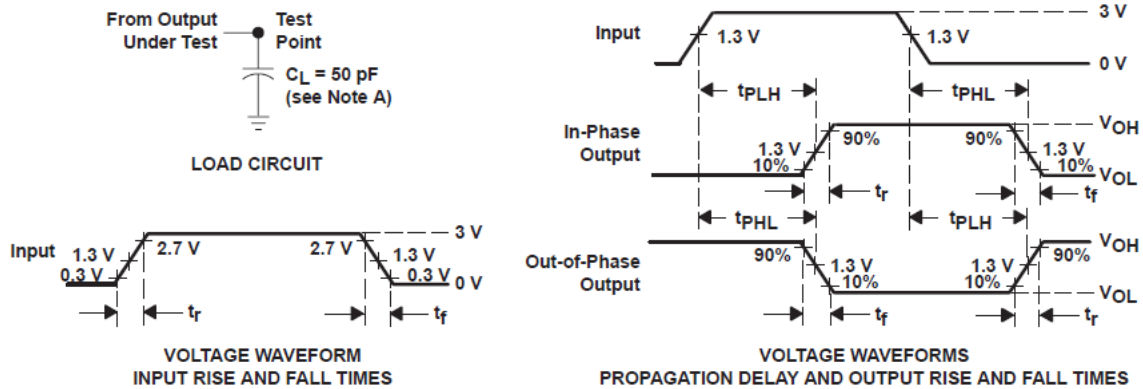
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT139		SN74HCT139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.5 V		14	34		51		43	ns
			5.5 V		12	30		50		40	
	G	Y	4.5 V		11	34		51		43	
			5.5 V		10	30		50		40	
t _t		Y	4.5 V		8	15		22		19	ns
			5.5 V		6	14		21		17	

6.6 Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per decoder	25	pF

7 Parameter Measurement Information



- C_L includes probe and test-fixturing capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .

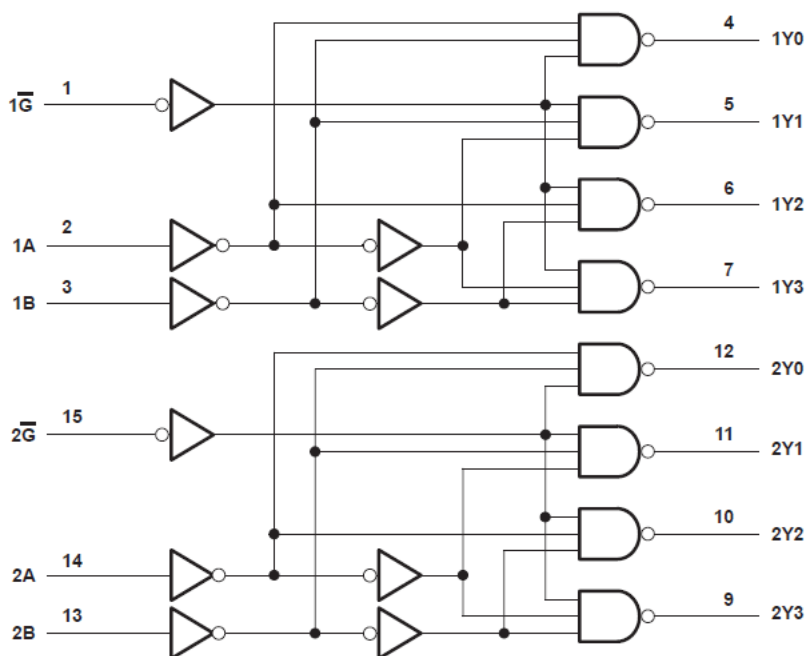
7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The 'HCT139 devices are designed for high performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

8.2 Functional Block Diagram



8-1. Function Diagram

8.3 Device Functional Modes

表 8-1. Function Table

INPUTS ⁽¹⁾			OUTPUTS ⁽²⁾			
G	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT139D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	HCT139	
SN74HCT139DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT139	Samples
SN74HCT139DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HCT139	Samples
SN74HCT139N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT139N	Samples
SN74HCT139PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HT139	Samples
SN74HCT139PWT	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	HT139	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT139DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HCT139DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCT139PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT139PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT139PWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT139DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HCT139DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HCT139PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HCT139PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HCT139PWR	TSSOP	PW	16	2000	366.0	364.0	50.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT139N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HCT139N	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated