# SN74LV164A 8 ビット、パラレル出力シリアル・シフト・レジスタ

## 1 特長

- 2V～5.5V の $V_{CC}$ で動作
- 最大 $t_{pd}$ 10.5ns (5V 時)
- 標準 $V_{OLP}$ (出力グランド・バウンス)
  < 0.8V ($V_{CC}$ = 3.3V、$T_A$ = 25℃)
- 標準 $V_{OHV}$ (出力 $V_{OH}$ アンダーシュート)
  > 2.3V ($V_{CC}$ = 3.3V、$T_A$ = 25℃)
- Ioff により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- すべてのポートで混在モード電圧動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

## 2 アプリケーション

- IP ルータ
- エンタープライズ用スイッチ
- アクセス制御とセキュリティ:アクセス・キーパッドと生体認証
- スマート・メーター:電力線通信

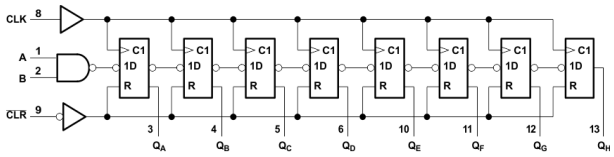
## 3 概要

SN74LV164A デバイスは、2V～5.5V の $V_{CC}$ で動作するように設計された 8 ビット・パラレル出力シリアル・シフト・レジスタです。

**パッケージ情報**(1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| SN74LV164A | D (SOIC、14) | 8.65mm × 3.91mm |
| | DB (SSOP、14) | 6.20mm × 5.30mm |
| | DGV (TVSOP、14) | 3.60mm × 4.40mm |
| | NS (SOP、14) | 10.30mm × 5.30mm |
| | PW (TSSOP、14) | 5.00mm × 4.40mm |
| | RGY (VQFN、14) | 3.50mm × 3.50mm |
| | BQA (WQFN、14) | 3.00mm × 2.50mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

**論理図 (正論理)**

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision J (December 2022) to Revision K (March 2023)** — **Page**

- ドキュメントの構造レイアウトを更新 ... 1
- Updated thermal values for D package from RθJA = 92.6 to 112.9, RθJC(top) = 53.9 to 68.7, RθJB = 46.8 to 69.4, ΨJT = 18.9 to 30, ΨJB = 46.6 to 69, all values in °C/W ... 5

**Changes from Revision I (February 2015) to Revision J (December 2022)** — **Page**

- 文書全体にわたって表、図、相互参照の書式を更新 ... 1

**Changes from Revision H (April 2005) to Revision I (February 2015)** — **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

## 5 Pin Configuration and Functions

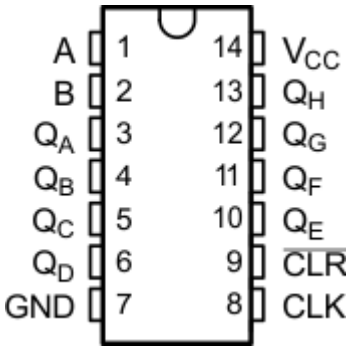



**図 5-1. D, DB, DGV, NS, or PW Package 14-PIN SOIC, SSOP, TVSOP, SOP, or TSSOP (Top View)**

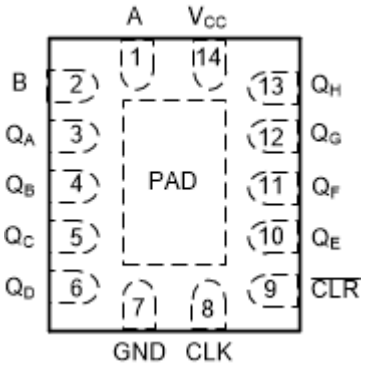



**図 5-2. RGY or BQA Package 14-PIN VQFN or WQFN Top View**

**表 5-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | A | I | Serial input A |
| 2 | B | I | Serial input B |
| 3 | $Q_A$ | O | Output A |
| 4 | $Q_B$ | O | Output B |
| 5 | $Q_C$ | O | Output C |
| 6 | $Q_D$ | O | Output D |
| 7 | GND | — | Ground pin |
| 8 | CLK | I | Storage clock |
| 9 | $\overline{CLR}$ | I | Storage clear |
| 10 | $Q_E$ | O | Output E |
| 11 | $Q_F$ | O | Output F |
| 12 | $Q_G$ | O | Output G |
| 13 | $Q_H$ | O | Output H |
| 11 | $Q_{H'}$ | O | $Q_H$ inverted |
| 14 | $V_{CC}$ | — | Power pin |
| - | PAD | — | Thermal Pad(2) |

(1) I = input, O = output
(2) RGY and BQA packages only

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage(1) | | –0.5 | 7 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(1) | | –0.5 | 7 | V |
| $V_O$ | Output voltage(1) (2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(2) This value is limited to 5.5 V maximum.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

| | | | SN74LV164A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV164A | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | NS (SOP) | PW (TSSOP) | RGY (VQFN) | BQA (WQFN) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 92.6 | 104.4 | 126.7 | 89.3 | 138.7 | 74.8 | 88.3 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 53.9 | 57 | 50 | 46.9 | 69.1 | 81.1 | 90.9 | |
| $R_{θJB}$ | Junction-to-board thermal resistance | 46.8 | 51.7 | 59.6 | 48 | 81.8 | 49.5 | 56.8 | |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 18.9 | 18.6 | 5.8 | 13.7 | 20.3 | 15 | 9.9 | |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 46.6 | 51.2 | 58.9 | 47.7 | 81.3 | 49.5 | 56.7 | |
| $R_{θJC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | 32.5 | 33.4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMTER | TEST CONDITIONS | $V_{CC}$ | SN74LV164A –40°C to 85°C | | | SN74LV164A –40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 2 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | V |
| | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | 2 | | | |
| | $I_{OH}$ = –6 mA | 3 V | 2.48 | | | 2.48 | | | |
| | $I_{OH}$ = –12 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.44 | |
| | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 | | | 20 | | | 20 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | | | 5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 2.2 | | | 2.2 | | pF |

## 6.6 Timing Requirements: $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV164A –40°C to 85°C | | SN74LV164A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 6 | | 6.5 | | 6.5 | | ns |
| | | CLK high or low | 6.5 | | 7.5 | | 7.5 | | |
| $t_{su}$ | Setup time | Data before CLK ↑ | 6.5 | | 8.5 | | 8.5 | | ns |
| | | $\overline{CLR}$ inactive | 3 | | 3 | | 3 | | |
| $t_h$ | Hold time | Data after CLK ↑ | –0.5 | | 0 | | 0 | | ns |

## 6.7 Timing Requirements: $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV164A –40°C to 85°C | | SN74LV164A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 5 | | 5 | | ns |
| | | CLK high or low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time | Data before CLK ↑ | 5 | | 6 | | 6 | | ns |
| | | $\overline{CLR}$ inactive | 2.5 | | 2.5 | | 2.5 | | |
| $t_h$ | Hold time | Data after CLK ↑ | 0 | | 0 | | 0 | | ns |

## 6.8 Timing Requirements: $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV164A –40°C to 85°C | | SN74LV164A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 5 | | 5 | | ns |
| | | CLK high or low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time | Data before CLK ↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | $\overline{CLR}$ inactive | 2.5 | | 2.5 | | 2.5 | | |
| $t_h$ | Hold time | Data after CLK ↑ | 1 | | 1 | | 1 | | ns |

## 6.9 Switching Characteristics: $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV164A –40°C to 85°C | | SN74LV164A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 55[1] | 105[1] | | 50 | | 50 | | MHz |
| | | | $C_L$ = 50 pF | 45 | 85 | | 40 | | 40 | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 9.2[1] | 17.6[1] | 1 | 20 | 1 | 21 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Q | | | 8.6[1] | 16[1] | 1 | 18 | 1 | 18.5 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 11.5 | 21.1 | 1 | 24 | 1 | 25 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Q | | | 10.8 | 19.5 | 1 | 22 | 1 | 22.5 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.10 Switching Characteristics: $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV164A –40°C to 85°C | | SN74LV164A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80[1] | 155[1] | | 65 | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 120 | | 45 | | 45 | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 6.4[1] | 12.8[1] | 1 | 15 | 1 | 16 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Q | | | 6[1] | 12.8[1] | 1 | 15 | 1 | 16 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 8.3 | 16.3 | 1 | 18.5 | 1 | 19.5 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Q | | | 7.9 | 16.3 | 1 | 18.5 | 1 | 19.5 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.11 Switching Characteristics: $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV164A –40°C to 85°C | | SN74LV164A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 125[1] | 220[1] | | 105 | | 95 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 165 | | 75 | | 65 | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 4.5[1] | 9[1] | 1 | 10.5 | 1 | 11.5 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Q | | | 4.2[1] | 8.6[1] | 1 | 10 | 1 | 11 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 6 | 11 | 1 | 12.5 | 1 | 13 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Q | | | 5.8 | 10.6 | 1 | 12.5 | 1 | 13 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.12 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | SN74LV164A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.28 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.22 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3.09 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

## 6.13 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF | f = 10 MHz | 3.3 V | 48.1 | pF |
| | | | | 5 V | 47.5 | |

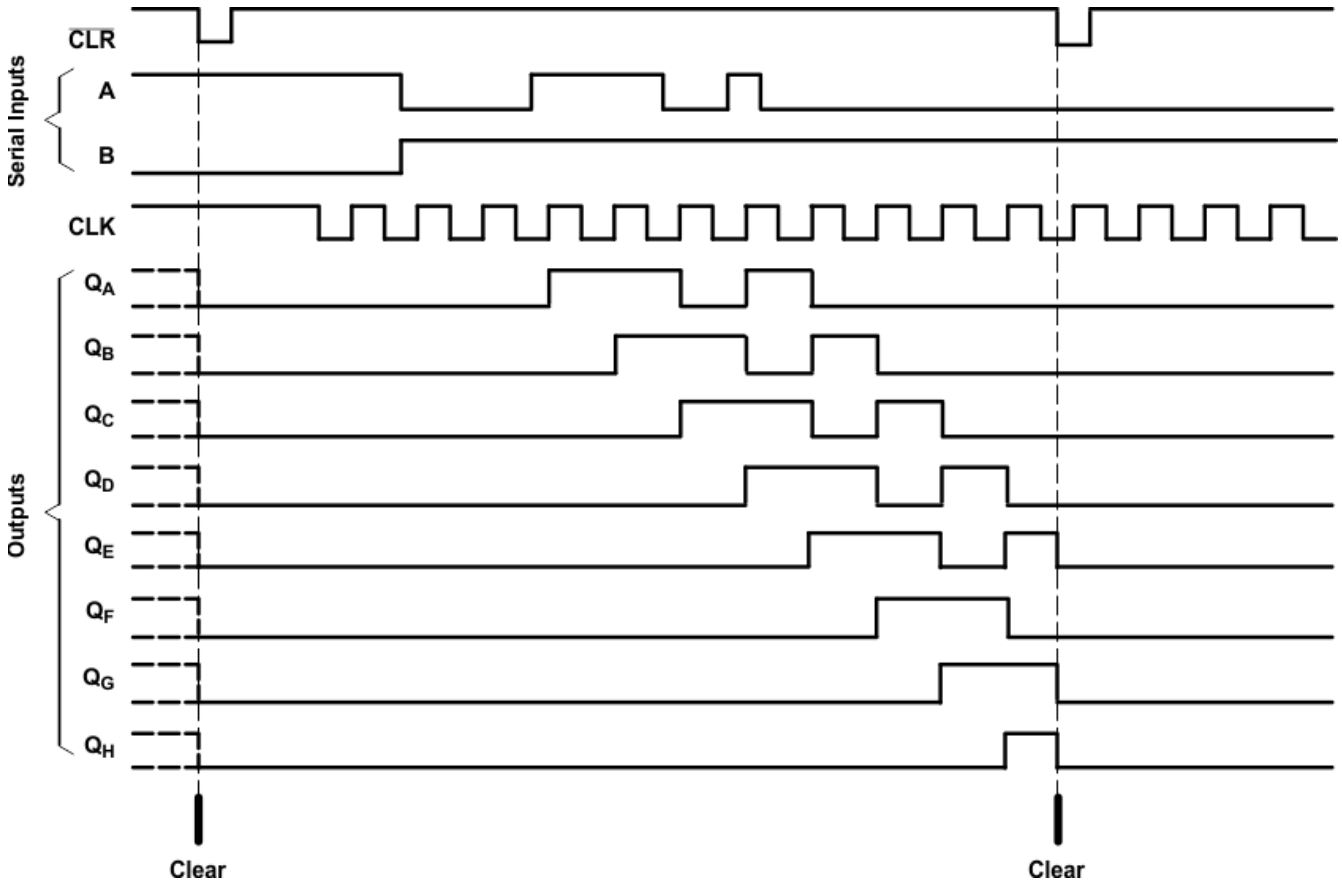



図 6-1. Typical Clear, Shift, and Clear Sequences

## 6.14 Typical Characteristics

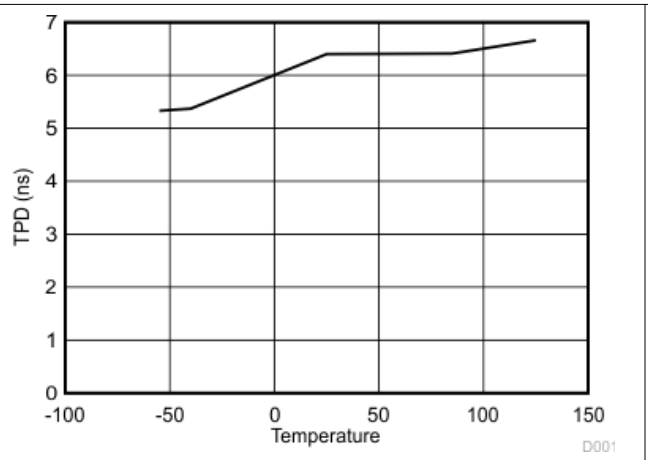



図 6-2. TPD vs. Temperature at 3.3 V

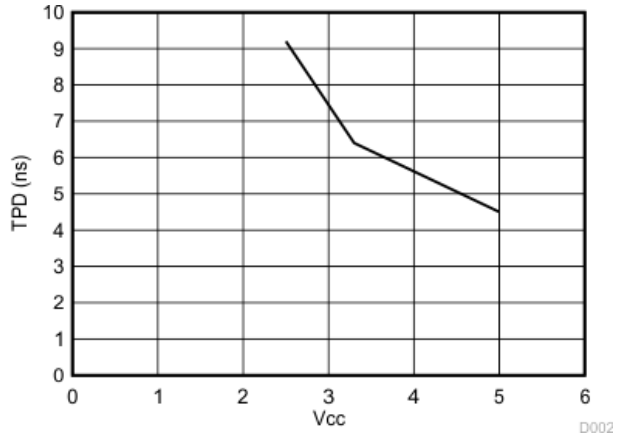
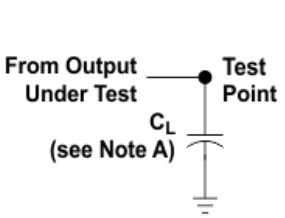
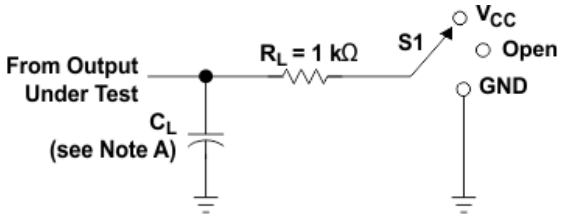



図 6-3. TPD vs. $V_{CC}$ at 25°C

## 7 Parameter Measurement Information

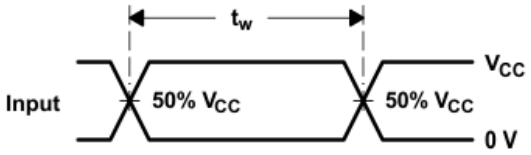



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

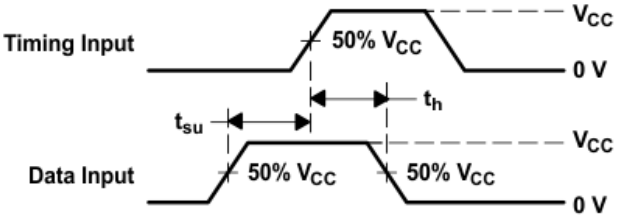



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

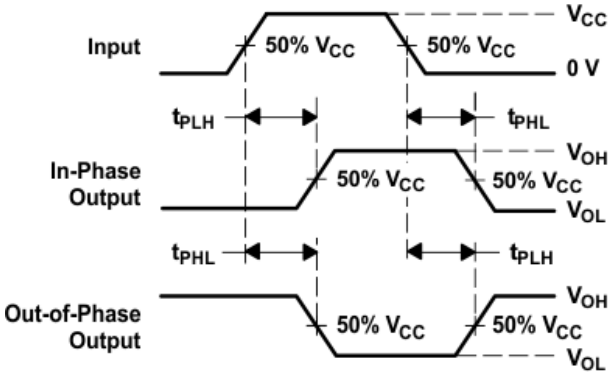
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



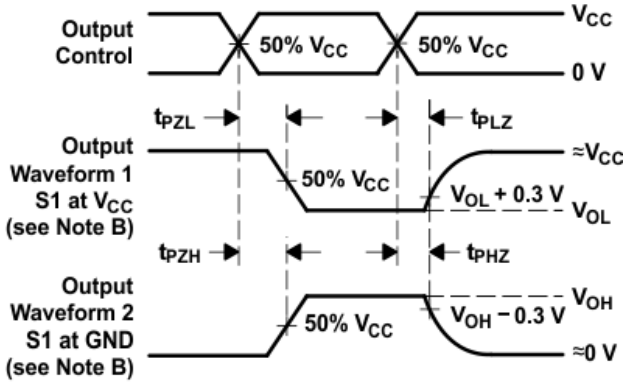

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**図 7-1. Load Circuit and Voltage Waveforms**

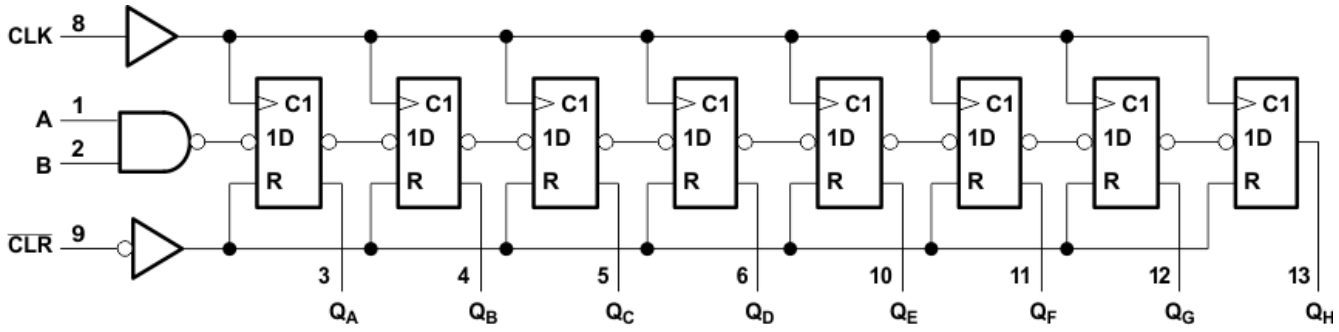
# 8 Detailed Description

## 8.1 Overview

The SNx4LV164A devices are 8-bit parallel-out serial shift registers designed for 2-V to 5.5-V $V_{CC}$ operation.

These devices feature NAND-gated serial (A and B) inputs and an asynchronous clear ( $\overline{CLR}$) input. The gated serial inputs permit complete control over incoming data, as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

## 8.2 Functional Block Diagram




Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

**図 8-1. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

## 8.4 Device Functional Modes

**表 8-1. Function Table(1)(2)**

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | A | B | $Q_A$ | $Q_B$ | ... | $Q_H$ |
| L | X | X | X | L | L | | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | | $Q_{Gn}$ |

(1) $Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.

(2) $Q_{An}$, $Q_{Gn}$ = the level of $Q_A$ or $Q_G$ before the most recent ↑ transition of the clock: indicates a 1-bit shift.

# 9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 9.1 Application Information

The SN74LV164A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates will minimize overshoot and undershoot on the outputs.

## 9.2 Typical Application

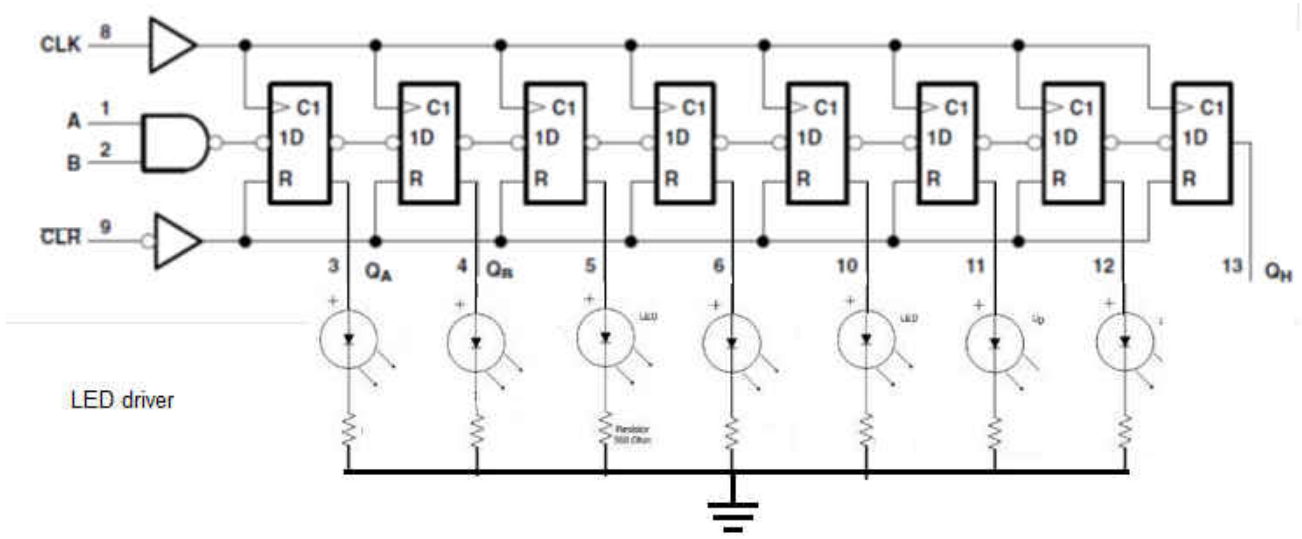



**図 9-1. Typical Application Schematic**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs. See (Δt/ΔV) in *セクション 6.3*.
  - Specified high and low level. See ($V_{IH}$ and $V_{IL}$) in *セクション 6.3*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above $V_{CC}$.

### 9.2.3 Application Curves

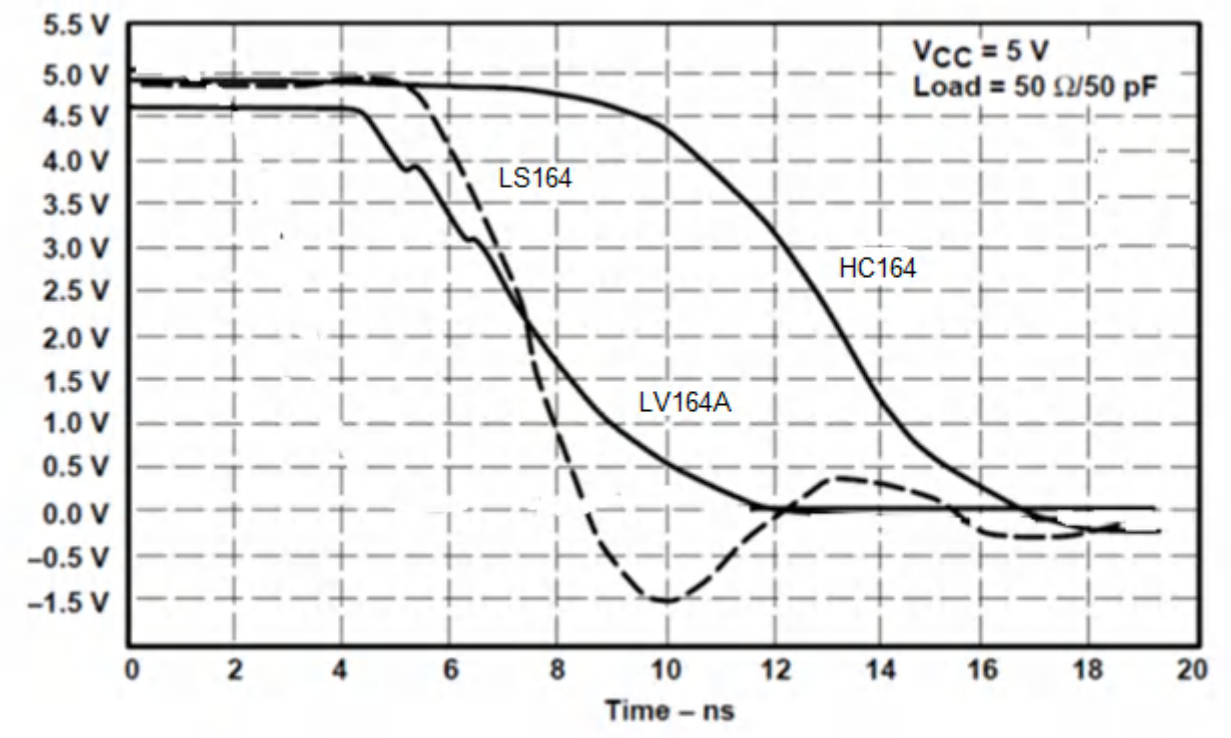



**図 9-2. Switching Characteristics Comparison**

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *セクション 6.3*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor and if there are multiple $V_{CC}$ terminals then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$ whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

### 9.4.2 Layout Example

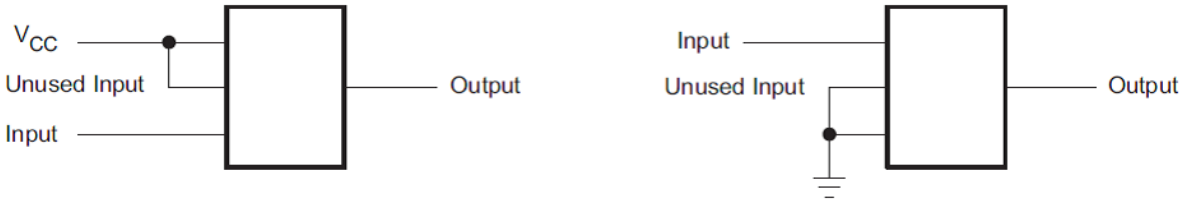



**図 9-3. Layout Example**

# 10 Device and Documentation Support

## 10.1 Documentation Support

### 10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 10-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN74LV164A | Click here | Click here | Click here | Click here | Click here |

## 10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV164ABQAR | ACTIVE | WQFN | BQA | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVA164 | Samples |
| SN74LV164AD | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI | -40 to 125 | LV164A | |
| SN74LV164ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV164A | Samples |
| SN74LV164ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV164A | Samples |
| SN74LV164ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV164A | Samples |
| SN74LV164ANSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV164A | Samples |
| SN74LV164APW | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 125 | LV164A | |
| SN74LV164APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV164A | Samples |
| SN74LV164APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV164A | Samples |
| SN74LV164APWT | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 125 | LV164A | |
| SN74LV164ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV164A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN74LV164A :**

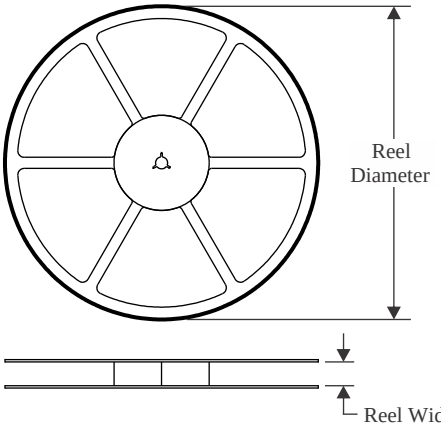
- Automotive : SN74LV164A-Q1

NOTE: Qualified Version Definitions:

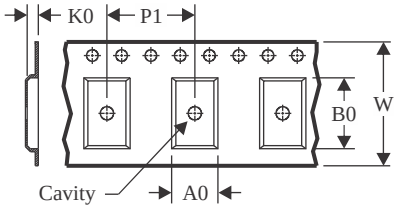
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

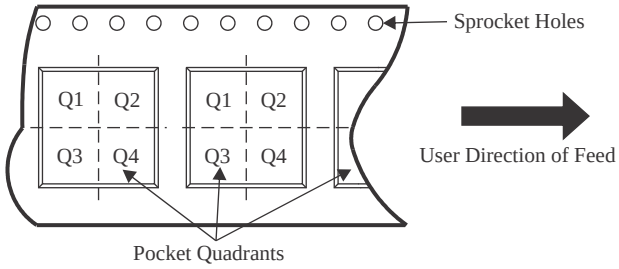



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

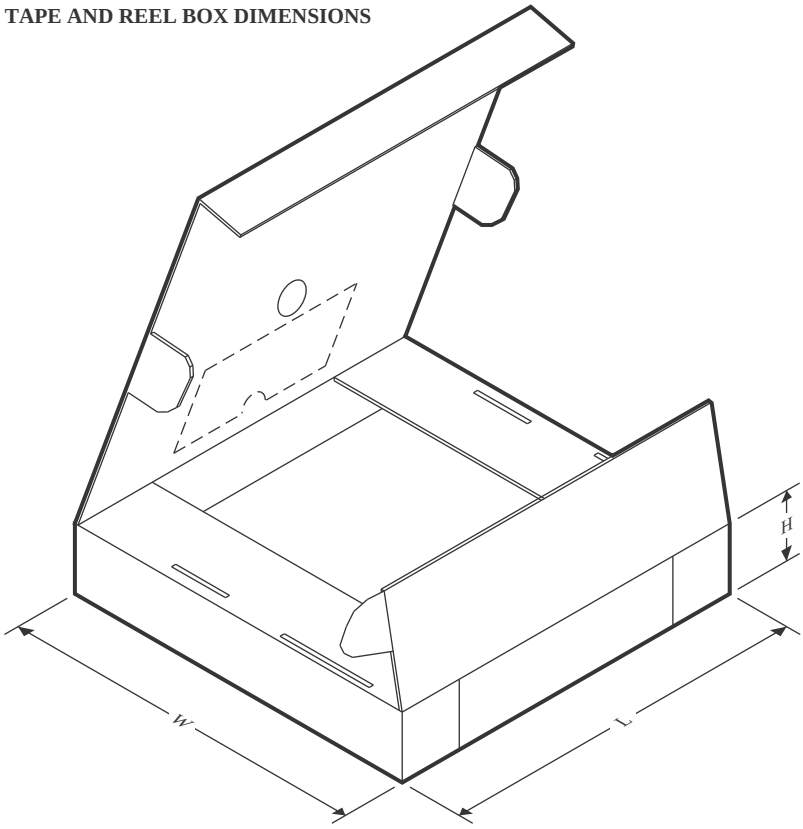
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV164ABQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74LV164ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV164ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV164ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV164ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV164ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV164APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV164APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV164ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

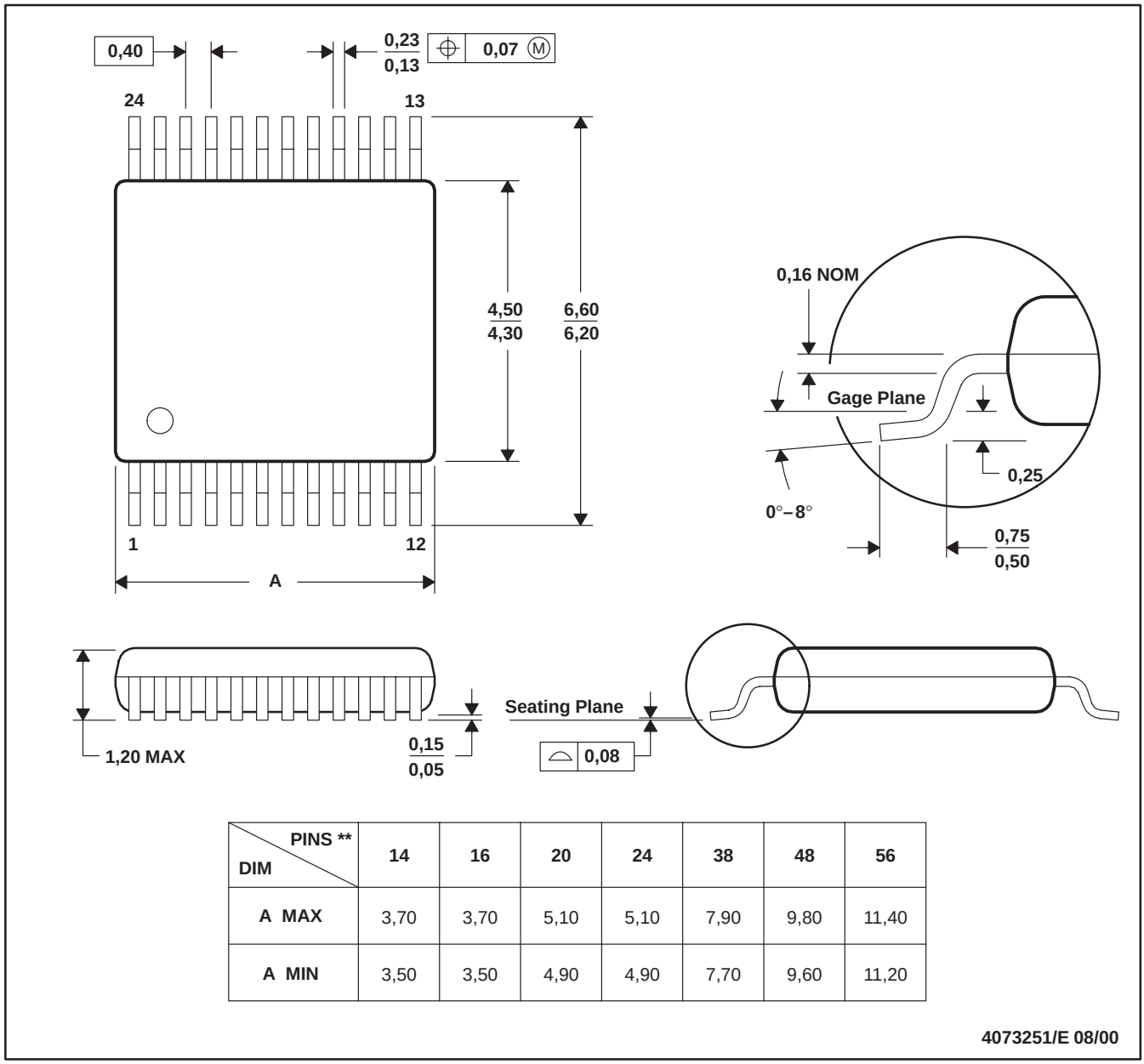



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV164ABQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LV164ADBR | SSOP | DB | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV164ADGVR | TVSOP | DGV | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV164ADR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LV164ADR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74LV164ANSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV164APWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV164APWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV164ARGYR | VQFN | RGY | 14 | 3000 | 360.0 | 360.0 | 36.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

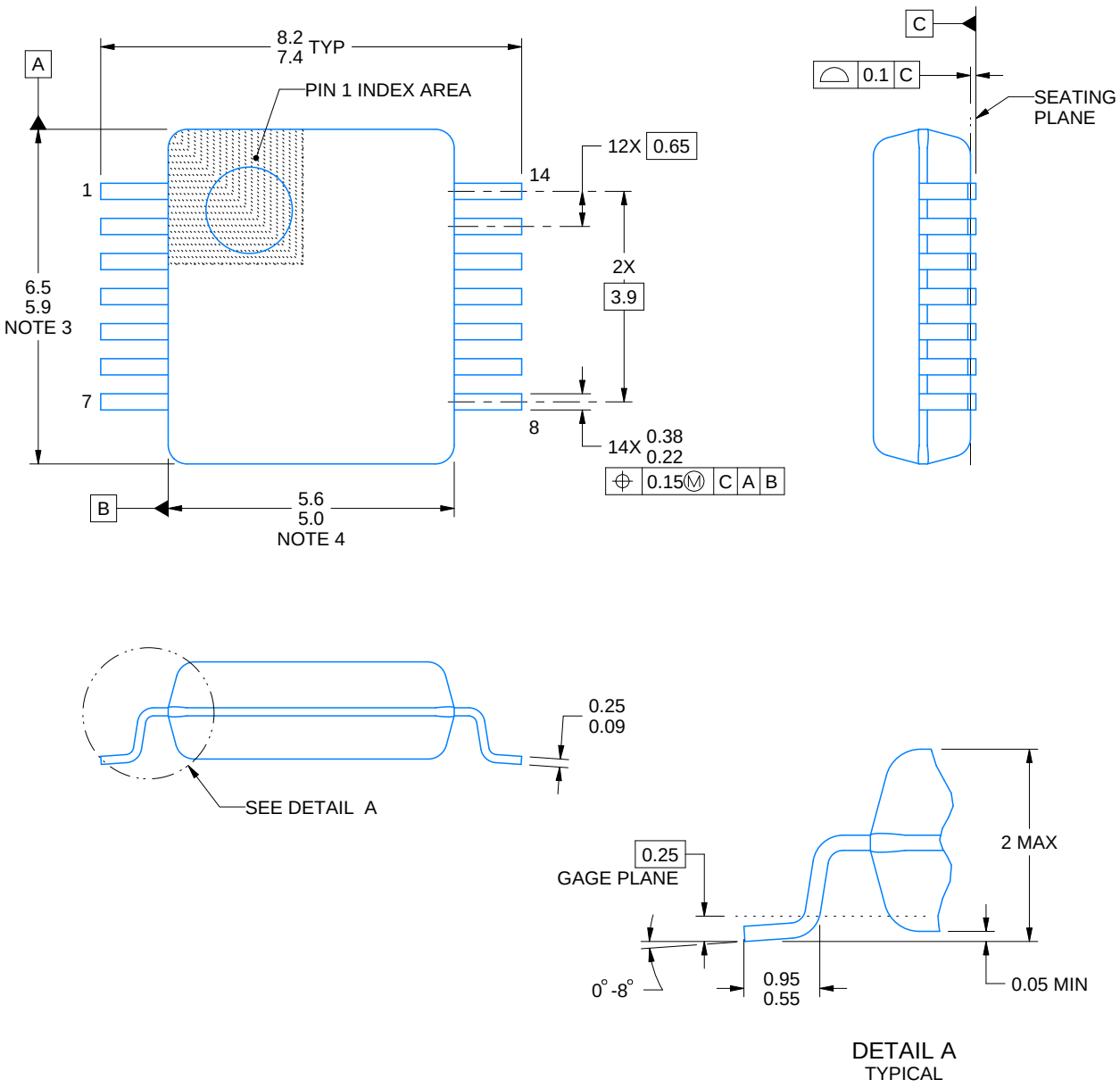
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# PACKAGE OUTLINE

## DB0014A

## SSOP - 2 mm max height

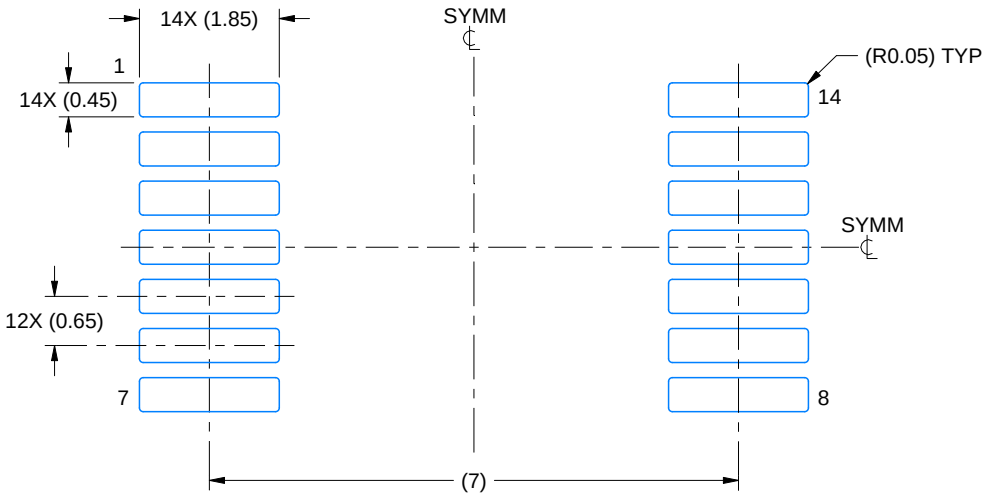
SMALL OUTLINE PACKAGE



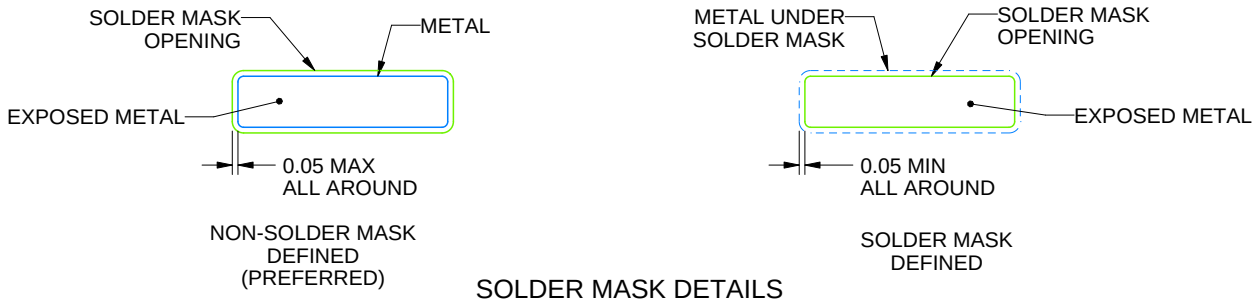

4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

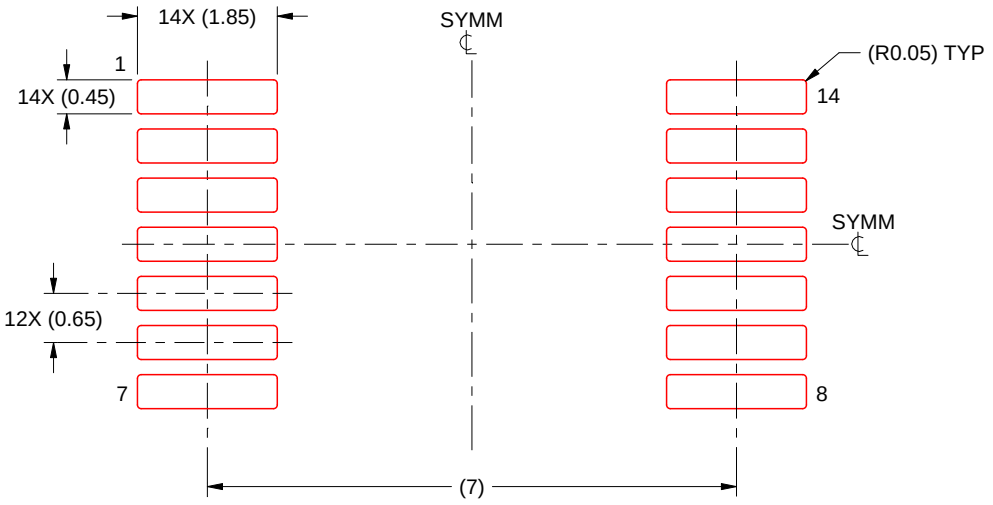



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

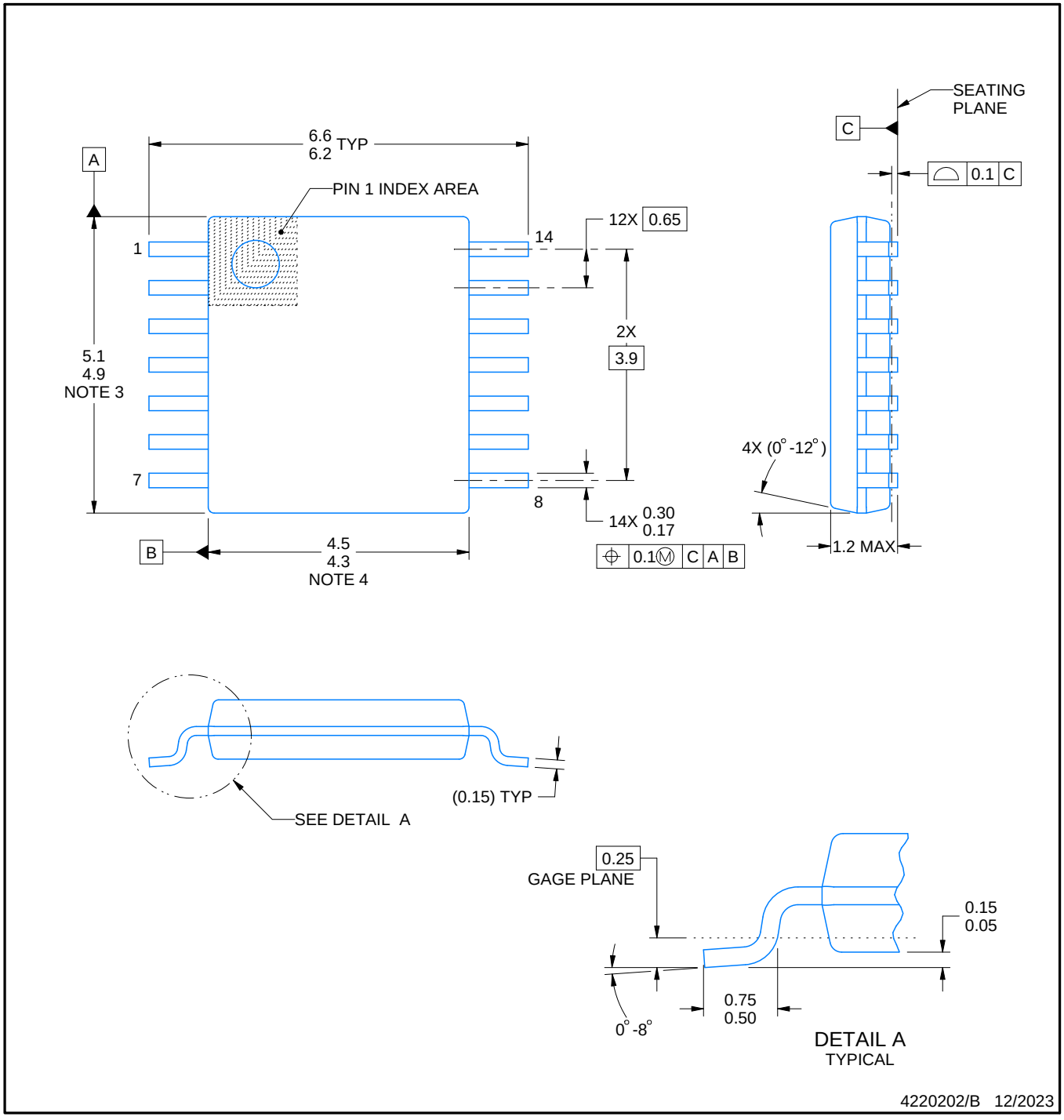
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0014A

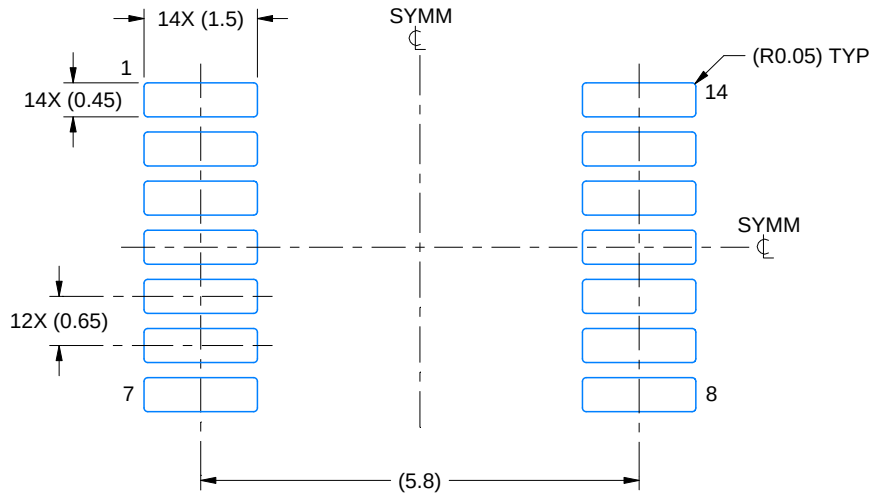
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

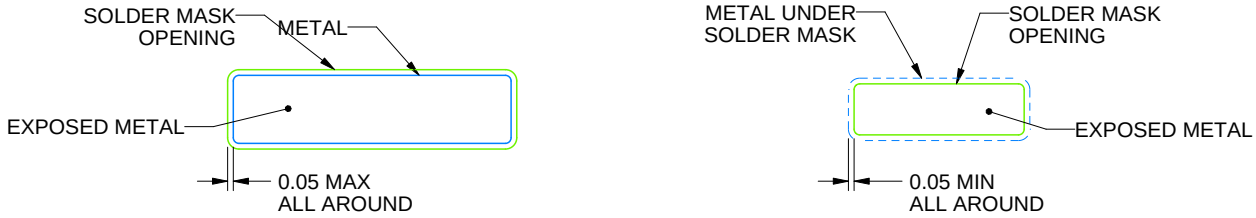



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

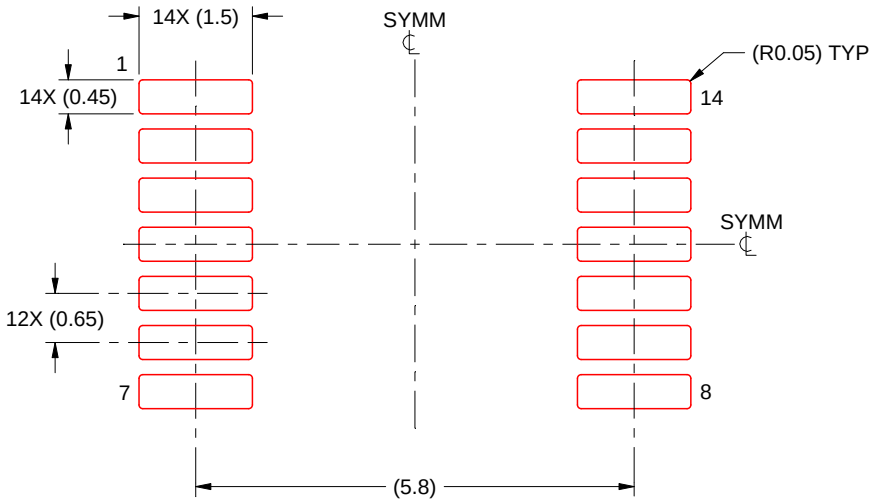



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

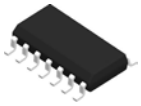



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

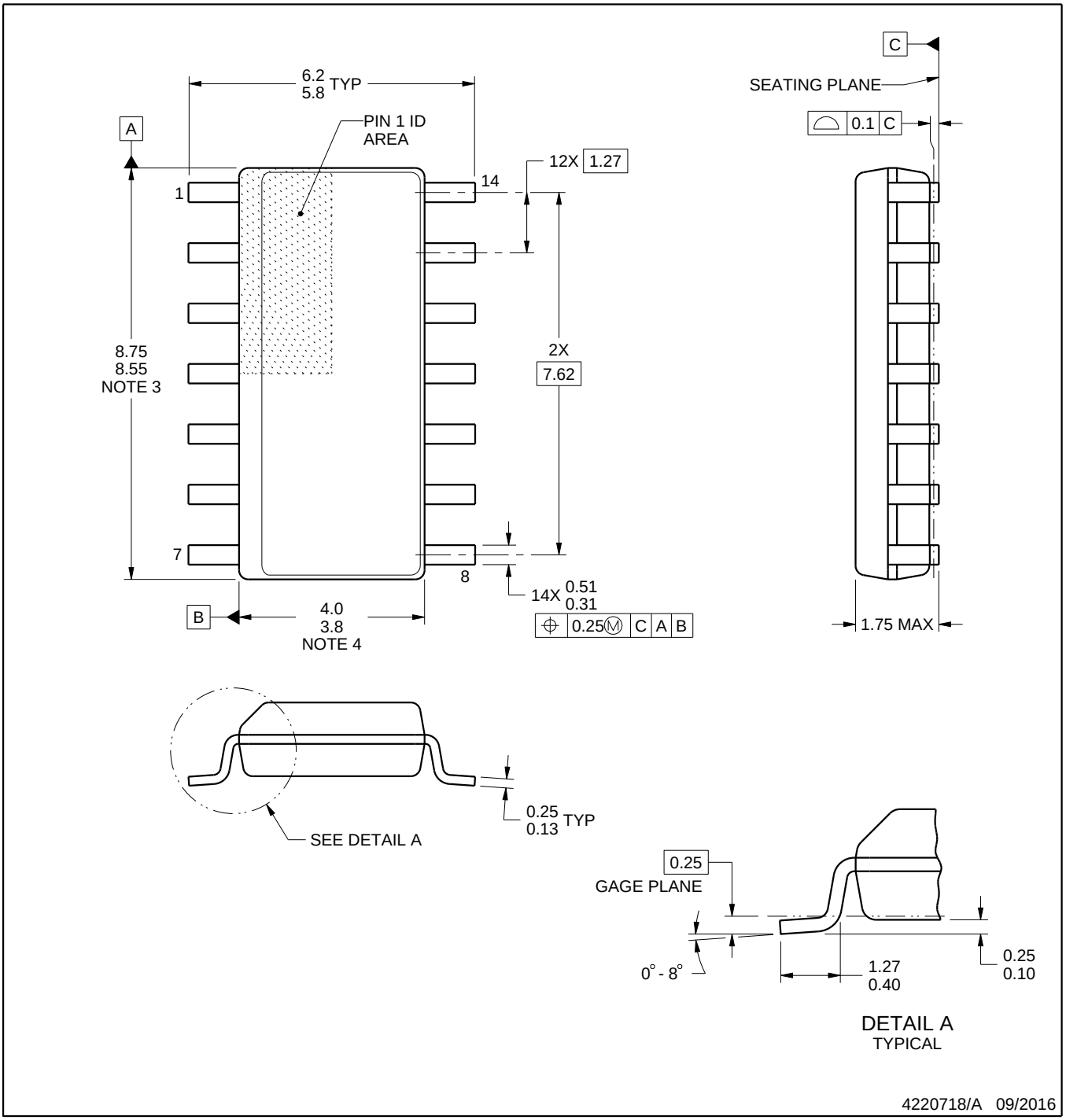


# PACKAGE OUTLINE

## D0014A

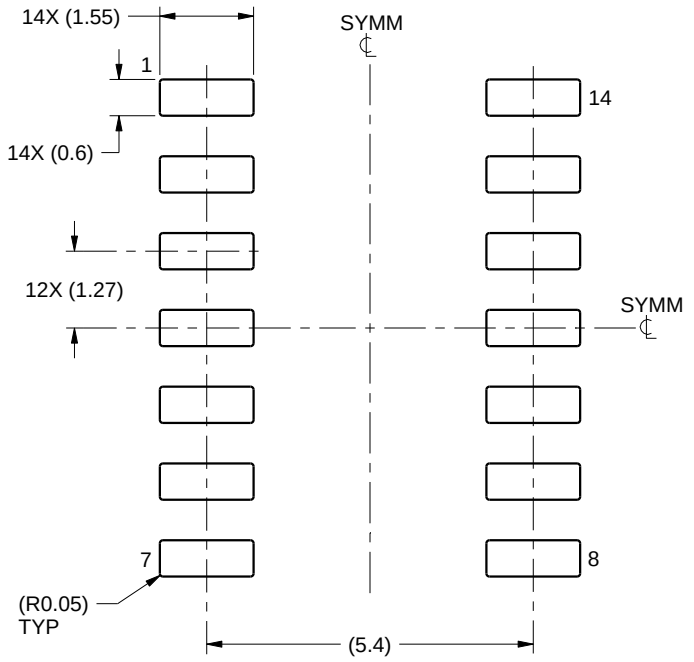
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

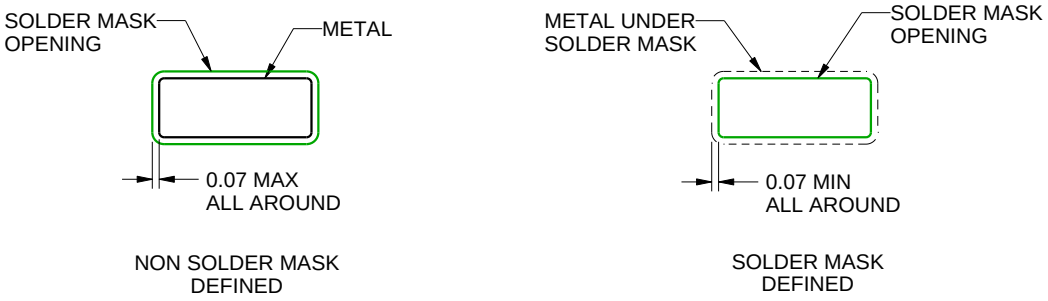



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

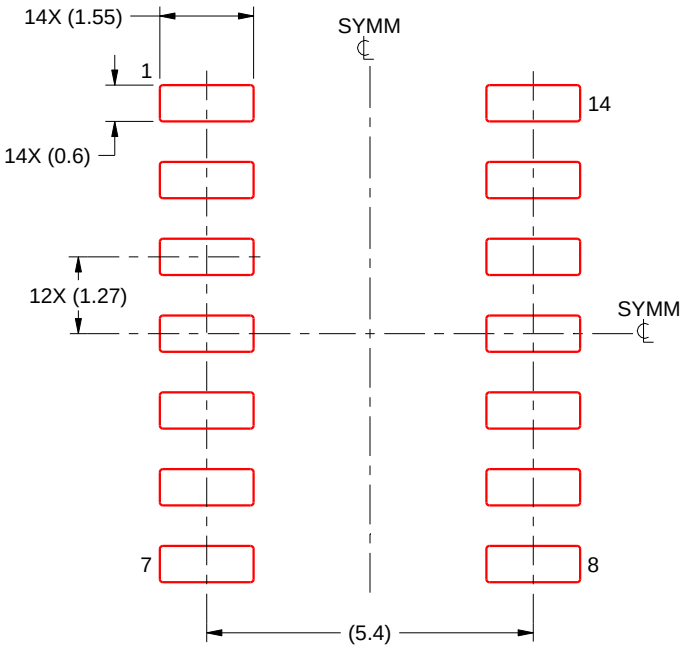
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



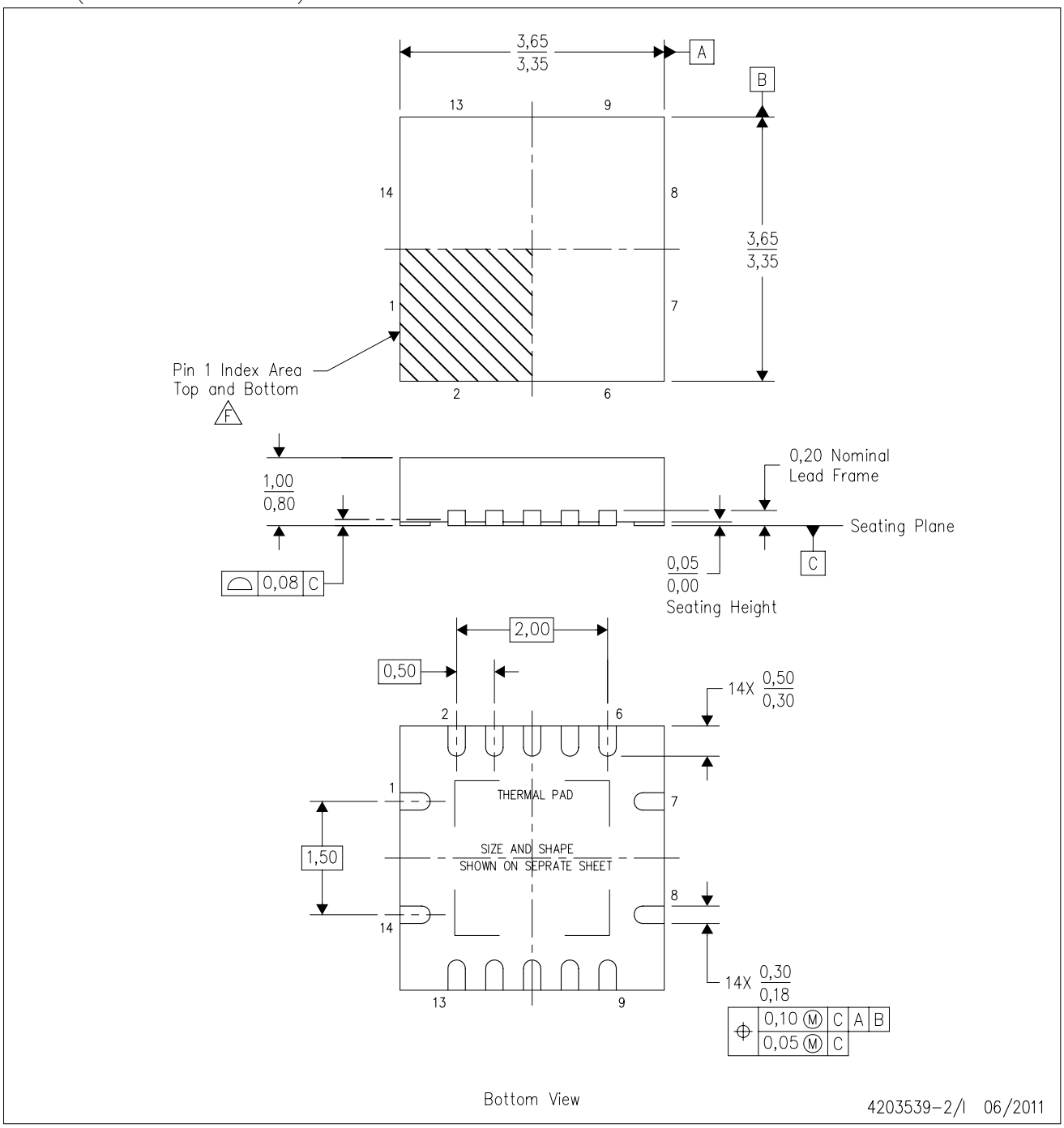

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

# GENERIC PACKAGE VIEW

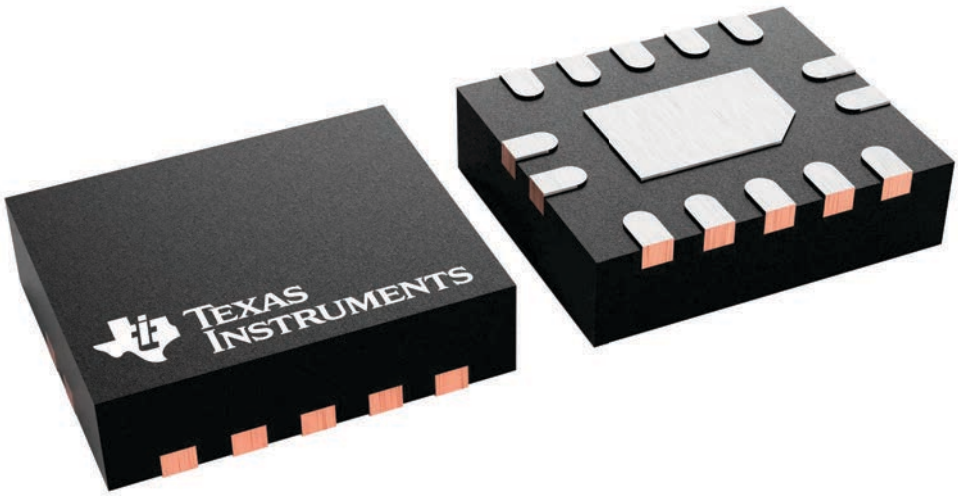
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

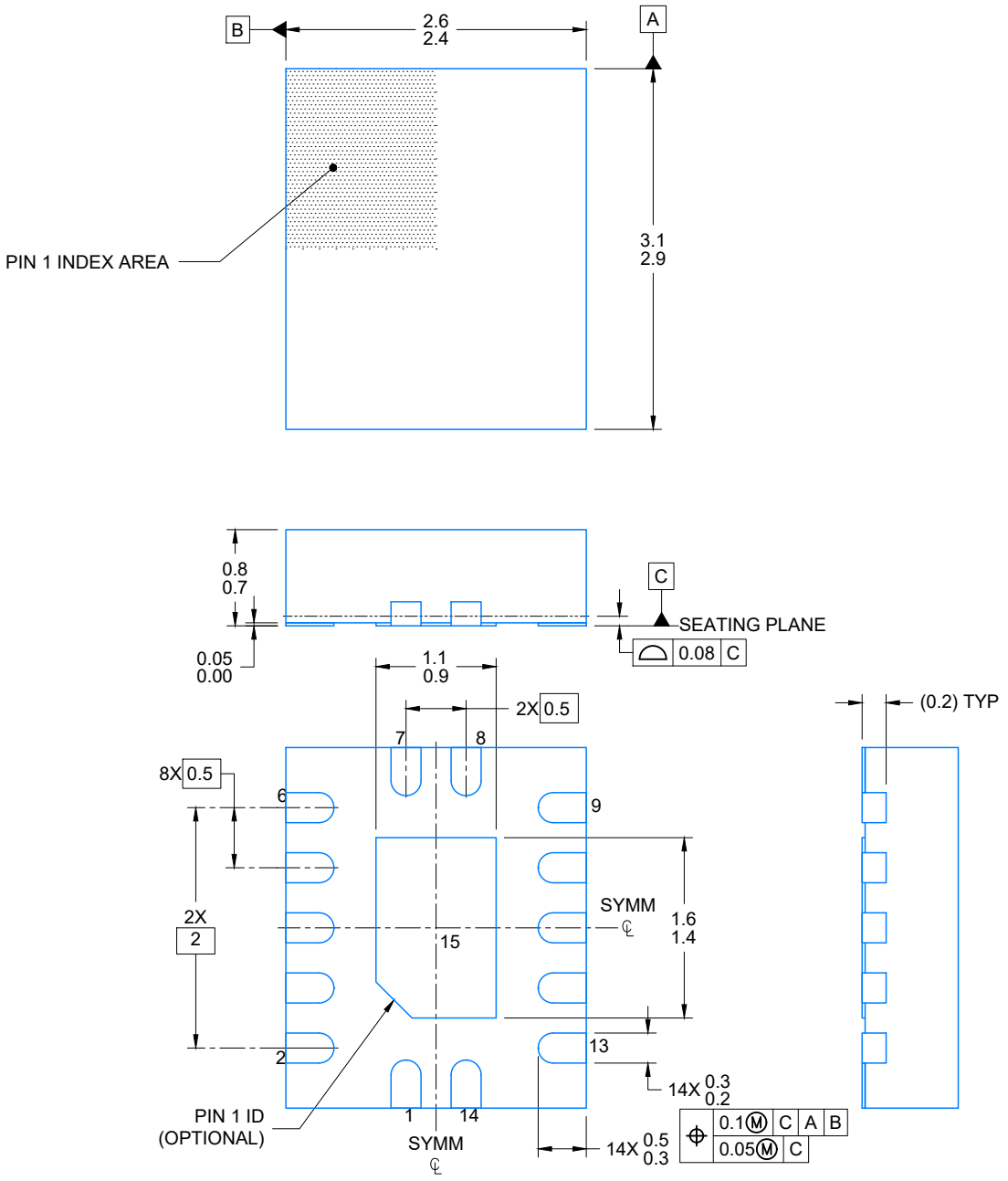


# PACKAGE OUTLINE

## BQA0014A

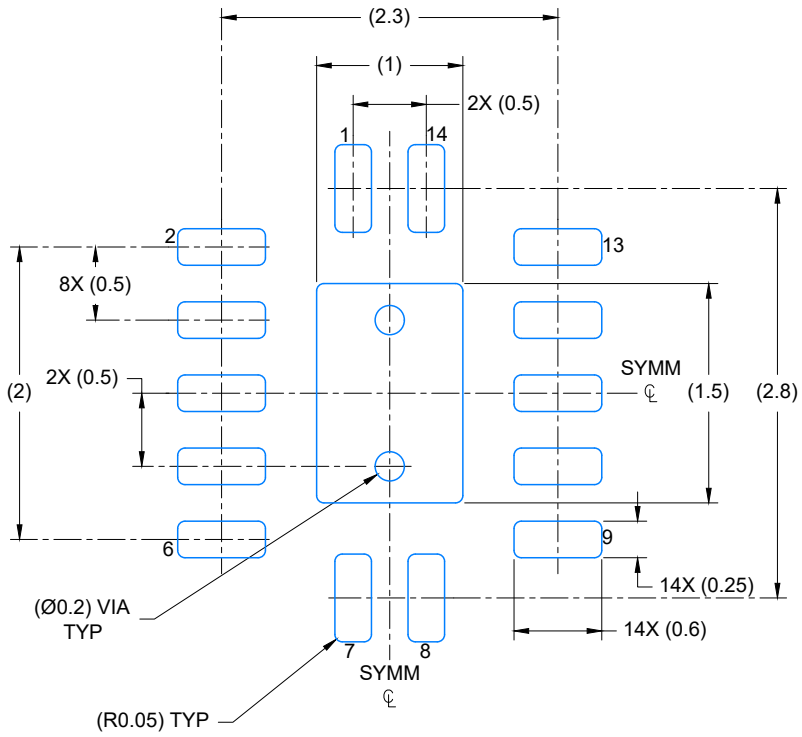
### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

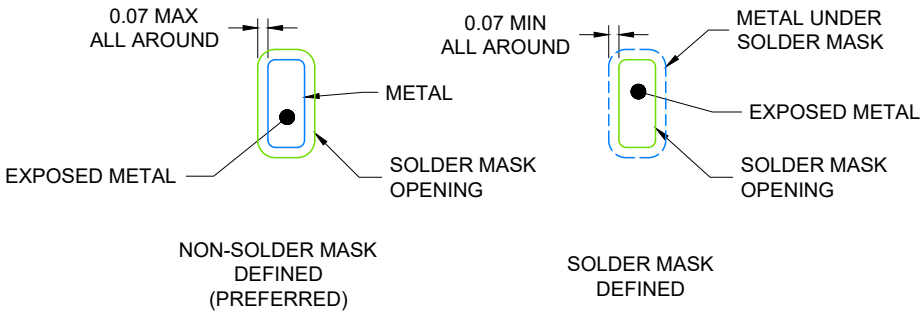



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



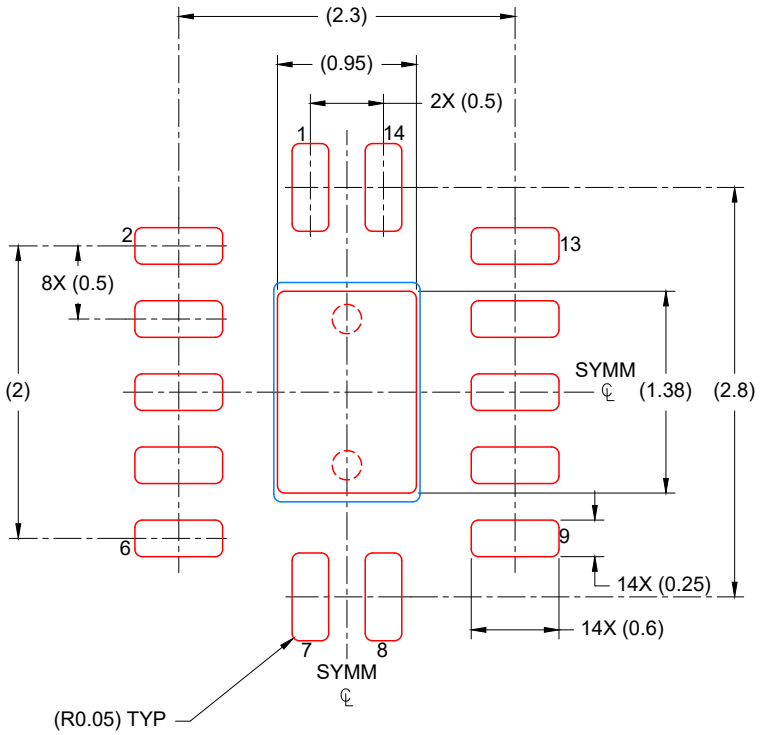

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

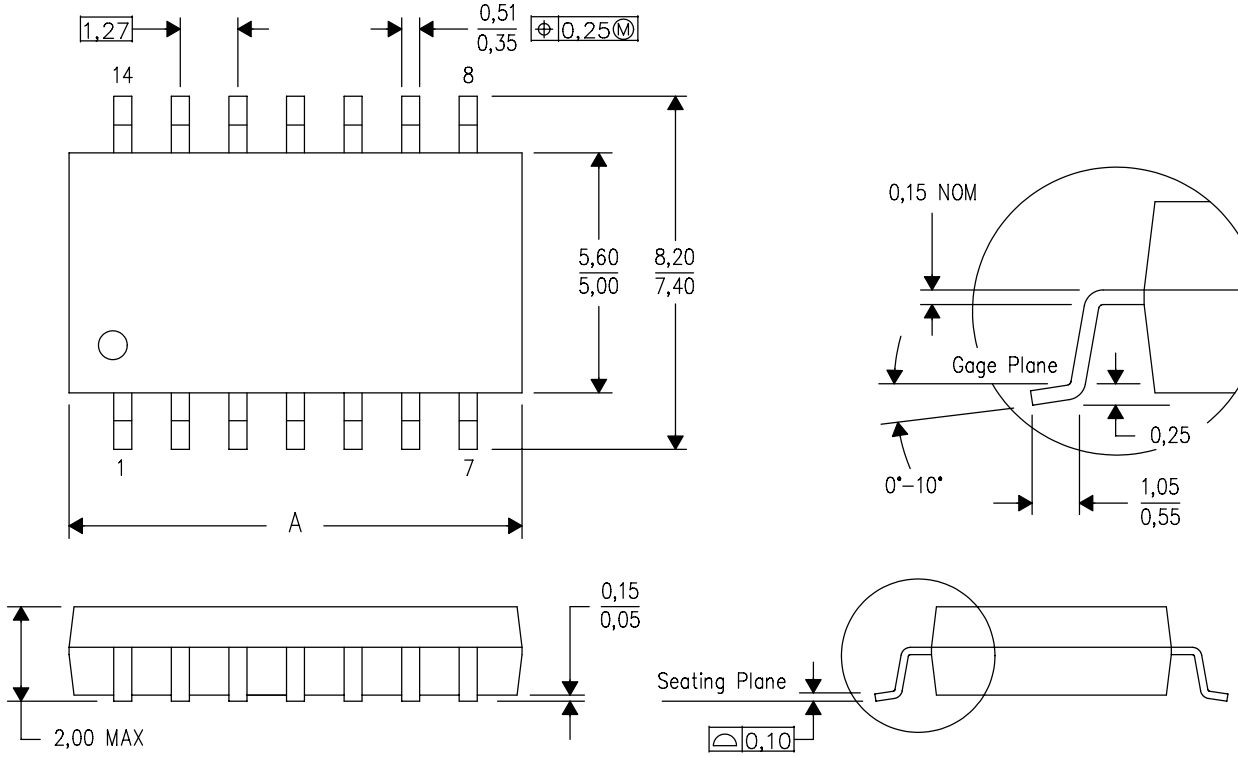
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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