

SN74LV21A デュアル 4 入力正論理 AND ゲート

1 特長

- 2V~5.5V の V_{CC} で動作
- 最大 t_{pd} : 6ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス) < 0.8V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) > 2.3V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- I_{off} により部分的パワーダウン・モード動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 概要

これらのデュアル 4 入力正論理 AND ゲートは、2V~5.5V V_{CC} 動作用に設計されています。

SN74LV21A デバイスはブール関数 $Y = A \cdot B \cdot C \cdot D$ を正論理で実行します。

これらのデバイスは、 I_{off} を使用する部分的パワーダウン・アプリケーション用の動作が完全に規定されています。 I_{off} 回路が出力をディセーブルにするので、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

パッケージ情報

部品番号	パッケージ ¹	パッケージ・サイズ ²
SN74LV21A	DGV (TVSOP, 14)	3.60mm × 6.4mm
	D (SOIC, 14)	8.65mm × 6mm
	NS (SO, 14)	10.20mm × 7.8mm
	DB (SSOP, 14)	6.20mm × 7.8mm
	PW (TSSOP, 14)	5.00mm × 6.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

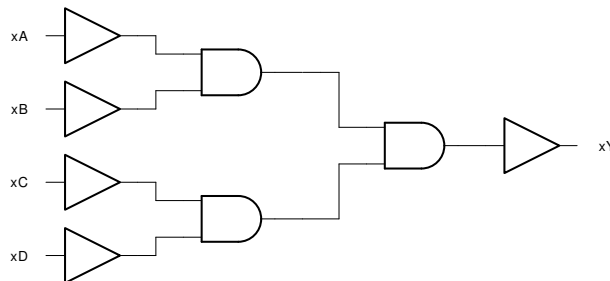


Table of Contents

1 特長	1	5.10 Operating Characteristics.....	6
2 概要	1	6 Parameter Measurement Information	7
3 Revision History	2	7 Detailed Description	8
4 Pin Configuration and Functions	3	7.1 Overview.....	8
5 Specifications	4	7.2 Functional Block Diagram.....	8
5.1 Absolute Maximum Ratings.....	4	7.3 Device Functional Modes.....	8
5.2 ESD Ratings.....	4	8 Device and Documentation Support	9
5.3 Recommended Operating Conditions	4	8.1 Documentation Support (Analog).....	9
5.4 Thermal Information.....	5	8.2 ドキュメントの更新通知を受け取る方法.....	9
5.5 Electrical Characteristics.....	5	8.3 サポート・リソース.....	9
5.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	5	8.4 Trademarks.....	9
5.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	8.5 静電気放電に関する注意事項.....	9
5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	8.6 用語集.....	9
5.9 Noise Characteristics.....	6	9 Mechanical, Packaging, and Orderable Information	9

3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (April 2005) to Revision F (July 2023)

Page

- 最新のデータシート規格を反映するように、文書全体にわたって採番方式、書式、表、図、相互参照を更新..... **1**

4 Pin Configuration and Functions

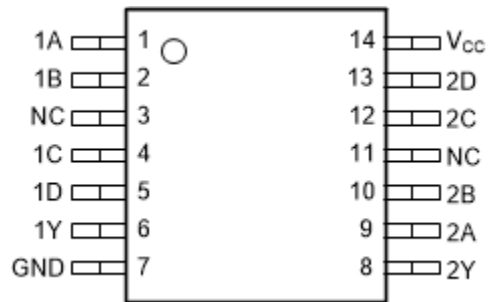


图 4-1. SN74LV21A D, DB, DGV, NS, or PW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	1A Input
1B	2	I	1B Input
NC	3	—	Not internally connected
1C	4	I	1C Input
1D	5	I	1D Input
1Y	6	O	1Y Output
2Y	8	O	2Y Output
2A	9	I	2A Input
2B	10	I	2B Input
NC	11	—	Not internally connected
2C	12	I	2C Input
2D	13	I	2D Input
GND	7	—	Ground Pin
V _{CC}	14	—	Power Pin

(1) Signal Types: I = Input, O = Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Output voltage range applied in high or low state ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
V _O	Output voltage range applied in power-off state ⁽²⁾	-0.5	7	V
I _{IK}	Input clamp current	(V _I < 0)	-20	mA
I _{OK}	Output clamp current	(V _O < 0)	-50	mA
I _O	Continuous output current	(V _O = 0 to V _{CC})	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000
		Charged device model (CDM), per JESD22-C101 ⁽²⁾	± 1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 2.3 V to 2.7 V	-2	mA
		V _{CC} = 3 V to 3.6 V	-6	
		V _{CC} = 4.5 V to 5.5 V	-12	

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
I _{OL}	Low level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 2.3 V to 2.7 V	2	mA
		V _{CC} = 3 V to 3.6 V	6	
		V _{CC} = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	
		V _{CC} = 4.5 V to 5.5 V	20	
T _A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#)

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LV21A					UNIT
	D	DB	DGV	NS	PW	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance					°C/W
	86	96	127	76	113	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1		V
		I _{OH} = -2 mA	2.3 V	2		
		I _{OH} = -6 mA	3 V	2.48		
		I _{OH} = -12 mA	4.5 V	3.8		
V _{OL}	Low-level output voltage	I _{OL} = 50 μA	2 V to 5.5 V	0.1		V
		I _{OL} = 2 mA	2.3 V	0.4		
		I _{OL} = 6 mA	3 V	0.44		
		I _{OL} = 12 mA	4.5 V	0.55		
I _I	Input leakage current	V _I = 5.5 V or GND	0 to 5.5 V	±1		μA
I _{CC}	Supply current	V _I = V _{CC} or GND, I _O = 0	5.5 V	20		μA
I _{off}	Off-state leakage current	V _I or V _O = 0 to 5.5 V	0 V	5		μA
C _i	Input capacitance	V _I = V _{CC} or GND	3.3 V	1.9		pF

5.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A, B, C or D	Y	C _L = 15 pF		7	12	1	14	ns
t _{pd}	A, B, C or D	Y	C _L = 50 pF		9.2	15.7	1	19	

5.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	$C_L = 15\text{ pF}$		5.1	7	1	8.5	ns
t_{pd}	A, B, C, or D	Y	$C_L = 50\text{ pF}$		6.6	10.5	1	12	

5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	$C_L = 15\text{ pF}$		3.8	5	1	6	ns
t_{pd}	A, B, C, or D	Y	$C_L = 50\text{ pF}$		4.9	7	1	8	

5.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER ⁽¹⁾		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		0	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

5.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT	
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	17.4	pF
			5 V	20.2	

6 Parameter Measurement Information



图 6-1. Load Circuit and Voltage Waveforms

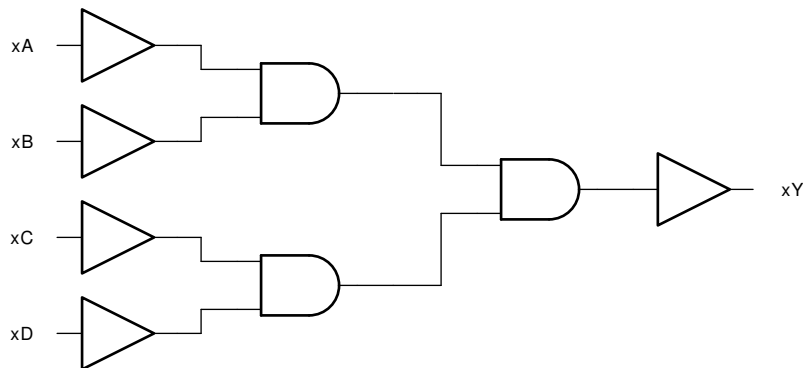
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

7 Detailed Description

7.1 Overview

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The SN74LV21A devices perform the Boolean function $Y = A \cdot B \cdot C \cdot D$ in positive logic. These dual 4-input positive-AND gates are designed for 2-V to 5.5-V V_{CC} operation.

7.2 Functional Block Diagram



☒ 7-1. logic diagram (positive logic)

7.3 Device Functional Modes

Function Table
(each gate)

INPUTS ⁽¹⁾				OUTPUT ⁽²⁾
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV21A	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV21ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples
SN74LV21ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples
SN74LV21ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples
SN74LV21ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV21A	Samples
SN74LV21APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV21ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV21ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV21ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV21ADR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74LV21ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV21ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV21APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV21APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV21ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV21ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV21ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV21ADR	SOIC	D	14	2500	366.0	364.0	50.0
SN74LV21ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV21ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV21APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV21APWR	TSSOP	PW	14	2000	356.0	356.0	35.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated