

## SN74LV240A 3 ステート出力、オクタール反転バッファ / ドライバ

### 1 特長

- 2V~5.5V の  $V_{CC}$  で動作
- 最大  $t_{pd}$  6.5ns (5V 時)
- 標準  $V_{OLP}$  (出力グランド バウンス)  $< 0.8V$  ( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )
- 標準  $V_{OHV}$  (出力  $V_{OH}$  アンダーシュート)  $> 2.3V$  ( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )
- すべてのポートで混在モード電圧動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能
- $I_{off}$  により活線挿抜、部分的パワーダウン モード、バックドライブ保護をサポート

### 2 アプリケーション

- ハンドセット: スマートフォン
- ネットワーク・スイッチ
- 健康管理およびフィットネス / ウェアラブル

### 3 概要

これらの反転出力付きオクタール バッファ / ドライバは、2V ~ 5.5V の  $V_{CC}$  で動作するように設計されています。

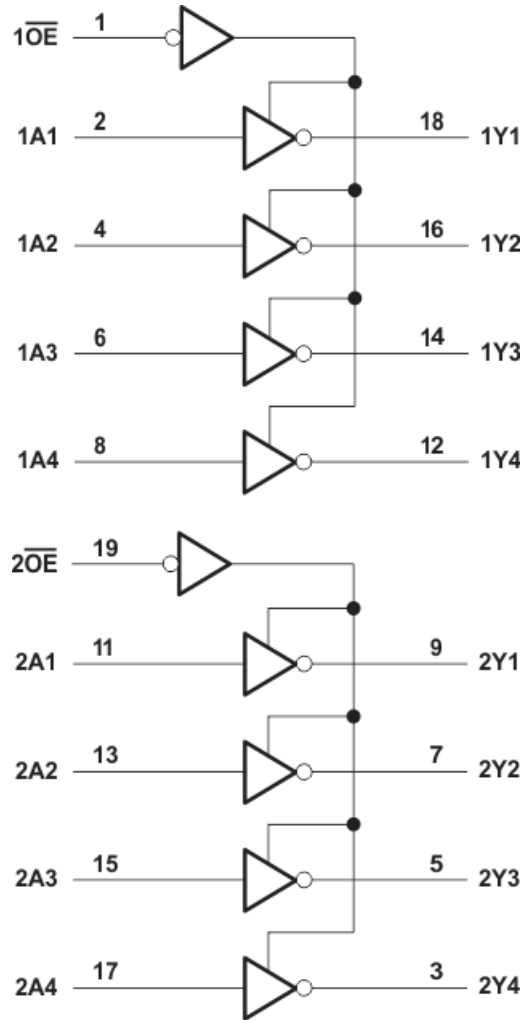
'LV240A デバイスは、3 ステート メモリ アドレス ドライバ、クロック ドライバ、バス用レシーバ / トランスミッタの性能と密度の両方を向上することに特化して設計されています。

これらのデバイスは、独立した出力イネーブル ( $\overline{OE}$ ) 入力を備えた 2 つの 4 ビット バッファ / ラインドライバで構成されています。 $\overline{OE}$  が Low の場合、デバイスは A 入力の反転データを Y 出力に渡します。 $\overline{OE}$  が High の場合、出力は高インピーダンス状態になります。

#### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	パッケージサイズ <sup>(2)</sup>	本体サイズ <sup>(3)</sup>
SN74LV240A	DGV (TVSOP, 20)	5 mm × 6.4 mm	5mm × 4.4mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.30mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm

- (1) 詳細については、[セクション 11](#) を参照してください。
- (2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



論理図 (正論理)

## Table of Contents

<b>1 特長</b> .....	<b>1</b>	7.2 Functional Block Diagram.....	<b>11</b>
<b>2 アプリケーション</b> .....	<b>1</b>	7.3 Feature Description.....	<b>12</b>
<b>3 概要</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>12</b>
<b>4 Pin Configuration and Functions</b> .....	<b>4</b>	<b>8 Application and Implementation</b> .....	<b>13</b>
<b>5 Specifications</b> .....	<b>5</b>	8.1 Application Information.....	<b>13</b>
5.1 Absolute Maximum Ratings .....	<b>5</b>	8.2 Typical Application.....	<b>13</b>
5.2 ESD Ratings.....	<b>5</b>	8.3 Power Supply Recommendations.....	<b>14</b>
5.3 Recommended Operating Conditions.....	<b>6</b>	8.4 Layout.....	<b>14</b>
5.4 Thermal Information.....	<b>6</b>	<b>9 Device and Documentation Support</b> .....	<b>15</b>
5.5 Electrical Characteristics.....	<b>7</b>	9.1 Documentation Support (Analog).....	<b>15</b>
5.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ .....	<b>7</b>	9.2 ドキュメントの更新通知を受け取る方法.....	<b>15</b>
5.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	<b>7</b>	9.3 サポート・リソース.....	<b>15</b>
5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	<b>8</b>	9.4 Trademarks.....	<b>15</b>
5.9 Noise Characteristics.....	<b>8</b>	9.5 静電気放電に関する注意事項.....	<b>15</b>
5.10 Operating Characteristics.....	<b>8</b>	9.6 用語集.....	<b>15</b>
5.11 Typical Characteristics.....	<b>9</b>	<b>10 Revision History</b> .....	<b>15</b>
<b>6 Parameter Measurement Information</b> .....	<b>10</b>	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>16</b>
<b>7 Detailed Description</b> .....	<b>11</b>		
7.1 Overview.....	<b>11</b>		

## 4 Pin Configuration and Functions

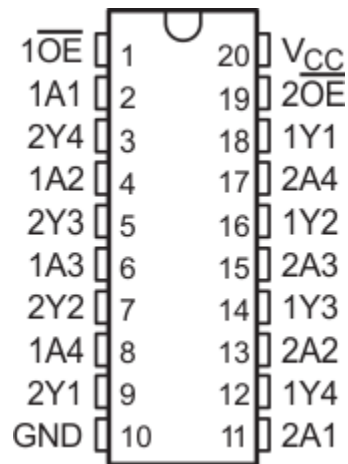


図 4-1. SN74LV240A DB, DGV, DW, NS, or PW Package; 20-Pin SSOP, TVSOP, SOIC, SOP, or TSSOP (Top View)

表 4-1. Pin Functions

NAME <sup>(1)</sup>	PIN	TYPE	DESCRIPTION
1OE	1	I	Output enable 1
1A1	2	I	1A1 input
2Y4	3	O	2Y4 output
1A2	4	I	1A2 input
2Y3	5	O	2Y3 output
1A3	6	I	1A3 input
2Y2	7	O	2Y2 output
1A4	8	I	1A4 input
2Y1	9	O	2Y1 output
GND	10	—	Ground pin
2A1	11	I	2A1 input
1Y4	12	O	1Y4 output
2A2	13	I	2A2 input
1Y3	14	O	1Y3 output
2A3	15	I	2A3 input
1Y2	16	O	1Y2 output
2A4	17	I	2A4 input
1Y1	18	O	1Y1 output
2OE	19	I	Output enable 2
VCC	20	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	-0.5	7	V	
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	7	V	
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V	
V <sub>O</sub>	Output voltage <sup>(2) (3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA	
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-35	35	mA
	Continuous current through V <sub>CC</sub> or GND		-70	70	mA
T <sub>stg</sub>	Storage temperature		-65	150	°C
T <sub>J</sub>	Junction Temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value is limited to 5.5-V maximum.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	2	5.5	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V	
		V <sub>CC</sub> = 2.3 to 2.7 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 to 3.6 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V	
		V <sub>CC</sub> = 2.3 to 2.7 V	V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 3 to 3.6 V	V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 4.5 to 5.5 V	V <sub>CC</sub> × 0.3		
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	μA
		V <sub>CC</sub> = 2.3 to 2.7 V		-2	mA
		V <sub>CC</sub> = 3 to 3.6 V		-8	
		V <sub>CC</sub> = 4.5 to 5.5 V		-16	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 2.3 to 2.7 V		2	mA
		V <sub>CC</sub> = 3 to 3.6 V		8	
		V <sub>CC</sub> = 4.5 to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 to 2.7 V		200	ns/V
		V <sub>CC</sub> = 3 to 3.6 V		100	
		V <sub>CC</sub> = 4.5 to 5.5 V		20	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DW (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	UNIT	
	20 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	79.2	94.5	116.2	76.7	128.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	43.7	56.4	31.2	43.2	70.5	
R <sub>θJB</sub>	Junction-to-board thermal resistance	47.0	49.7	57.7	44.2	79.3	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.6	18.5	0.9	16.8	23.4	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	46.5	49.3	57.0	43.8	78.9	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = -50 μA	2 to 5.5 V	V <sub>CC</sub> - 0.1			V
		I <sub>OH</sub> = -2 mA	2.3 V	2			
		I <sub>OH</sub> = -8 mA	3 V	2.48			
		I <sub>OH</sub> = -16 mA	4.5 V	3.8			
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 50 μA	2 to 5.5 V			0.1	V
		I <sub>OL</sub> = 2 mA	2.3 V			0.4	
		I <sub>OL</sub> = 8 mA	3 V			0.44	
		I <sub>OL</sub> = 16 mA	4.5 V			0.55	
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1	μA
I <sub>OZ</sub>	Off-State (High-Impedance State) Output Current (of a 3-State Output)	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±5	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20	μA
I <sub>off</sub>	Input/Output Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			5	μA
C <sub>i</sub>	Input Capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		2.3		pF

## 5.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ±0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		6.3 <sup>(1)</sup>	11.6 <sup>(1)</sup>	1 <sup>(2)</sup>	14 <sup>(2)</sup>	ns
t <sub>en</sub>	OE				8.5 <sup>(1)</sup>	14.6 <sup>(1)</sup>	1 <sup>(2)</sup>	17 <sup>(2)</sup>	
t <sub>dis</sub>	OE				9.7 <sup>(1)</sup>	14.1 <sup>(1)</sup>	1 <sup>(2)</sup>	16 <sup>(2)</sup>	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		8.2	14.4	1	17	ns
t <sub>en</sub>	OE				10.3	17.8	1	21	
t <sub>dis</sub>	OE				14.2	19.2	1	21	
t <sub>sk(o)</sub>							2	2 <sup>(3)</sup>	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.  
(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.  
(3) Value applies for SN74LV240A only

## 5.7 Switching Characteristics, V<sub>CC</sub> = 3.3 V ±0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		4.6 <sup>(1)</sup>	7.5 <sup>(1)</sup>	1 <sup>(2)</sup>	9 <sup>(2)</sup>	ns
t <sub>en</sub>	OE				6.2 <sup>(1)</sup>	10.6 <sup>(1)</sup>	1 <sup>(2)</sup>	12.5 <sup>(2)</sup>	
t <sub>dis</sub>	OE				8.3 <sup>(1)</sup>	12.5 <sup>(1)</sup>	1 <sup>(2)</sup>	13.5 <sup>(2)</sup>	

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		5.9	11	1	12.5	ns
t <sub>en</sub>	OE				7.5	14.1	1	16	
t <sub>dis</sub>	OE				11.8	15	1	17	
t <sub>sk(o)</sub>								1.5 <sup>(3)</sup>	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.  
(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.  
(3) Value applies for SN74LV240A only

## 5.8 Switching Characteristics, V<sub>CC</sub> = 5 V ±0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		3.4 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(2)</sup>	6.5 <sup>(2)</sup>	ns
t <sub>en</sub>	OE				4.6 <sup>(1)</sup>	7.3 <sup>(1)</sup>	1 <sup>(2)</sup>	8.5 <sup>(2)</sup>	
t <sub>dis</sub>	OE				7.4 <sup>(1)</sup>	12.2 <sup>(1)</sup>	1 <sup>(2)</sup>	13.5 <sup>(2)</sup>	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		4.4	7.5	1	8.5	ns
t <sub>en</sub>	OE				5.6	9.3	1	10.5	
t <sub>dis</sub>	OE				9.7	14.2	1	15.5	
t <sub>sk(o)</sub>								1 <sup>(3)</sup>	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.  
(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.  
(3) This values applies for SN74LV240A only

## 5.9 Noise Characteristics

V<sub>CC</sub> = 3.3 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C<sup>(1)</sup>

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.56		V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.49		
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		2.82		
V <sub>IH(D)</sub>	High-level dynamic input voltage	2.31			
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	

- (1) Characteristics are for surface-mount packages only.

## 5.10 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 50 pF f = 10 MHz	3.3 V	14	pF
			5 V	16.4	



### 5.11 Typical Characteristics

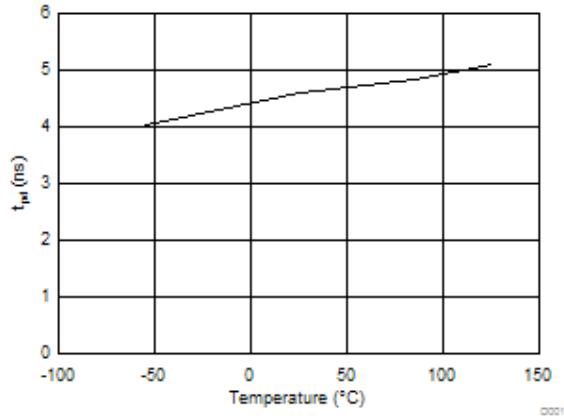


図 5-1.  $t_{pd}$  vs Temperature at 3.3-V  $V_{CC}$

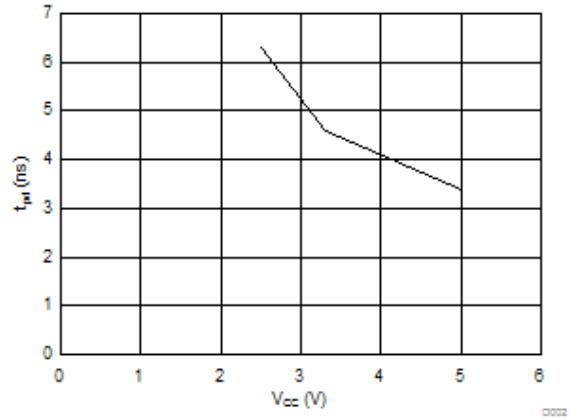
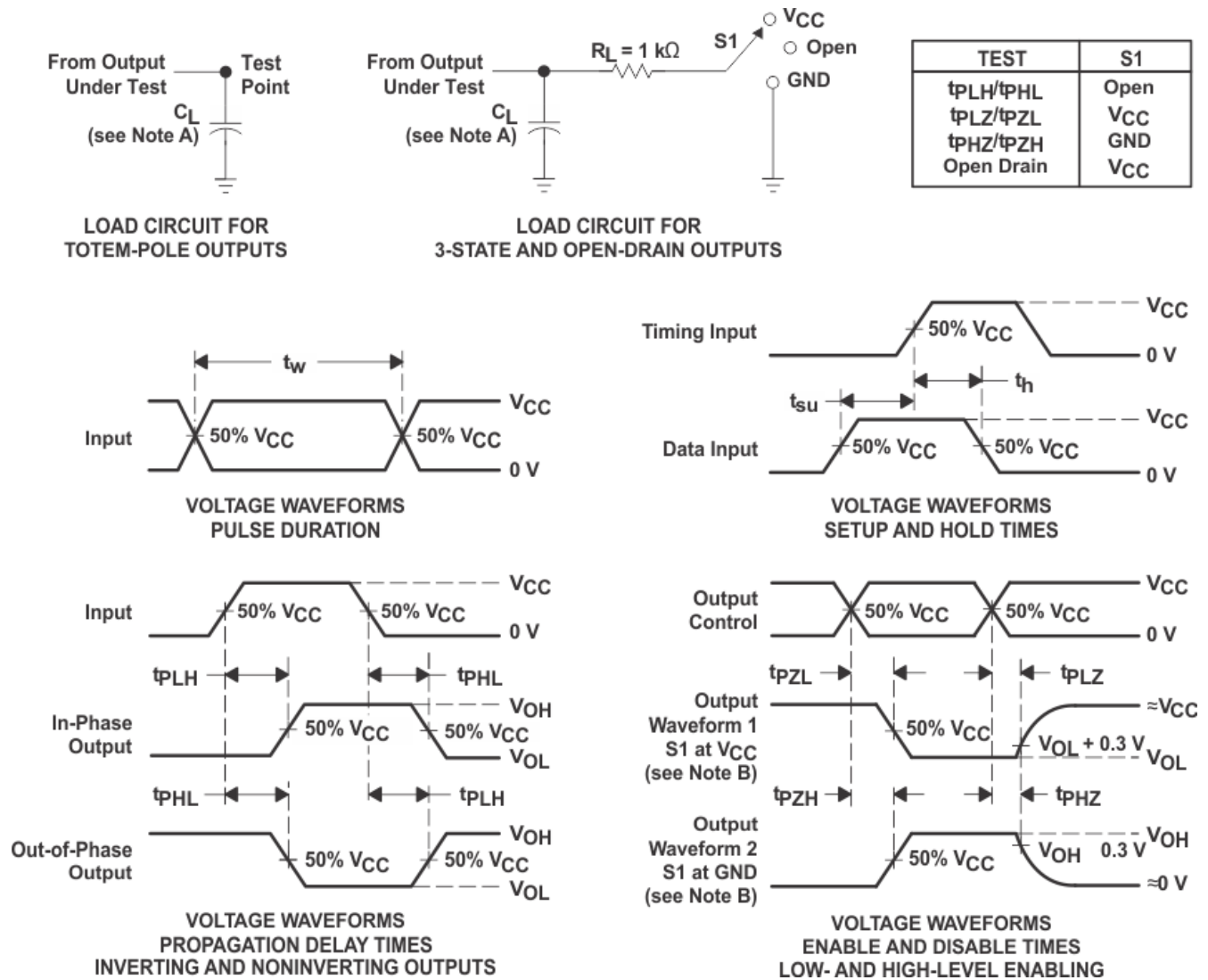


図 5-2.  $t_{pd}$  vs  $V_{CC}$  at 25°C

## 6 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**图 6-1. Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

These octal buffers/drivers with inverted outputs are designed for 2 V to 5.5 V  $V_{CC}$  operation.

The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

### 7.2 Functional Block Diagram

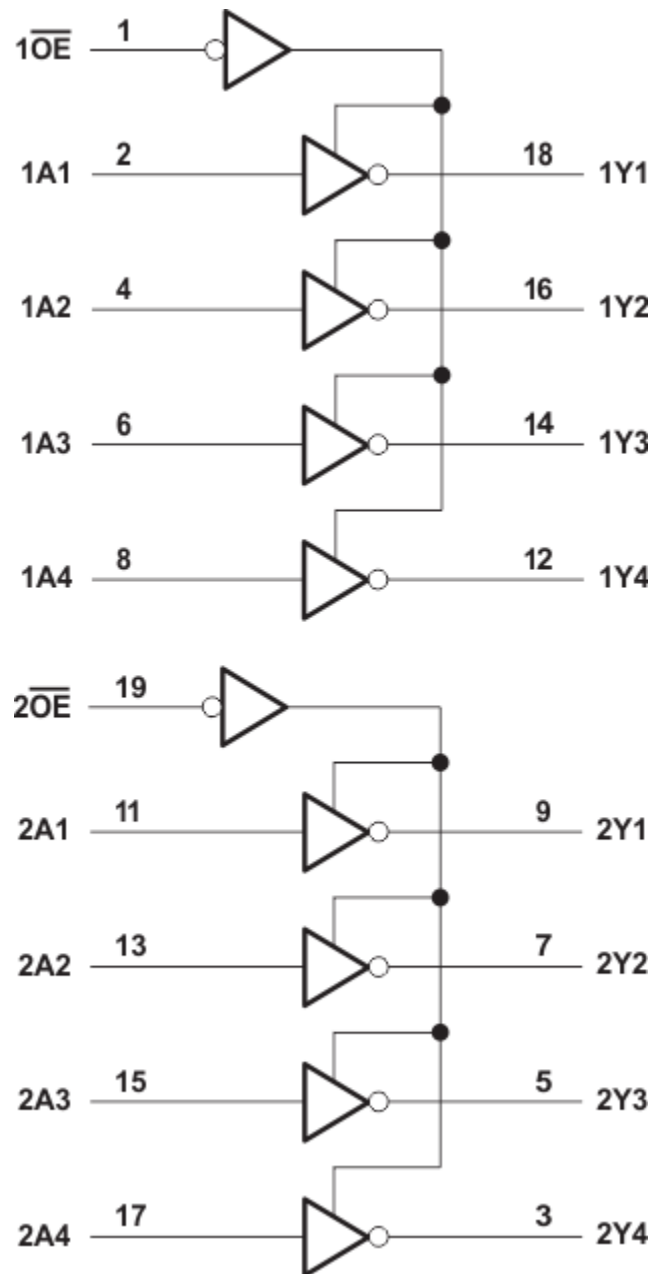


図 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

- Wide operating voltage range operates from 2 V to 5.5 V operation
- Allow down voltage translation inputs accept voltages to 5.5 V
- $I_{off}$  feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 7.4 Device Functional Modes

**表 7-1. Function Table  
(Each Buffer)**

INPUTS <sup>(1)</sup>		OUTPUT <sup>(2)</sup>
OE	A	Y
L	H	L
L	L	H
H	X	Z

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The SN74LV240A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. It can produce 8 mA of drive current at 3.3 V making it ideal for driving multiple outputs and low-noise applications. The inputs are 5.5-V tolerant allowing it to translate down to  $V_{CC}$ .

### 8.2 Typical Application

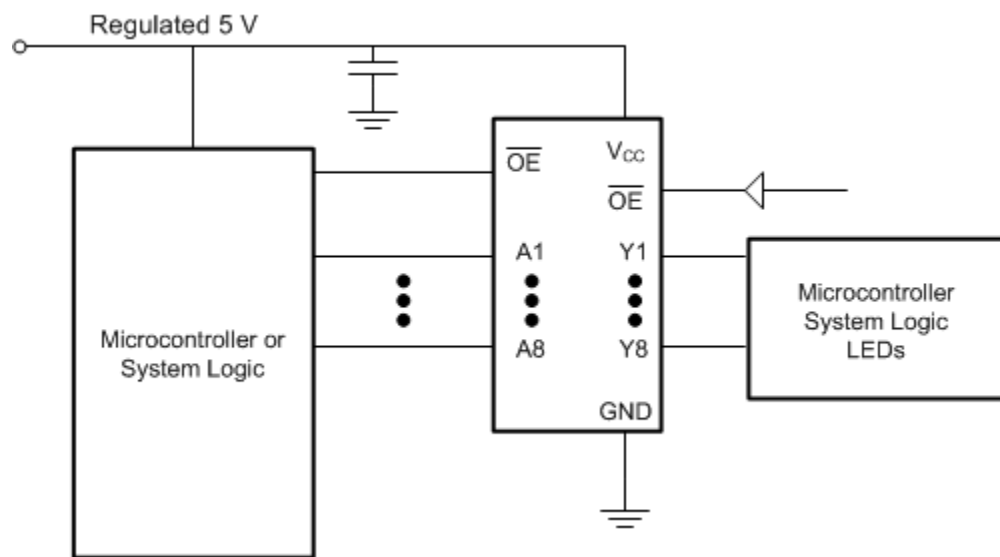


図 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

1. Recommended input conditions
  - Rise time and fall time specifications see  $(\Delta t/\Delta V)$  in [セクション 5.3](#).
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in [セクション 5.3](#).
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$
2. Recommend output conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

### 8.2.3 Application Curve

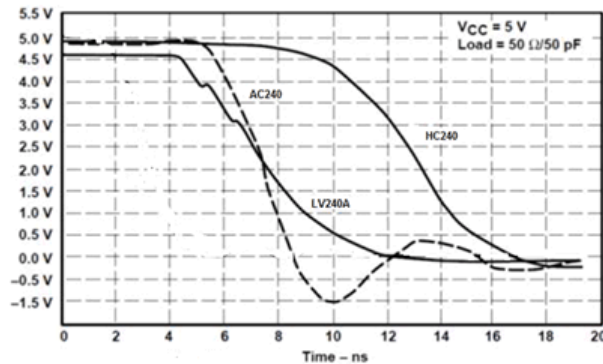


図 8-2. Switching Characteristics Comparison

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [セクション 5.3](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1  $\mu\text{F}$  and if there are multiple  $V_{CC}$  terminals, then TI recommends .01  $\mu\text{F}$  or .022  $\mu\text{F}$  for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

#### 8.4.2 Layout Example

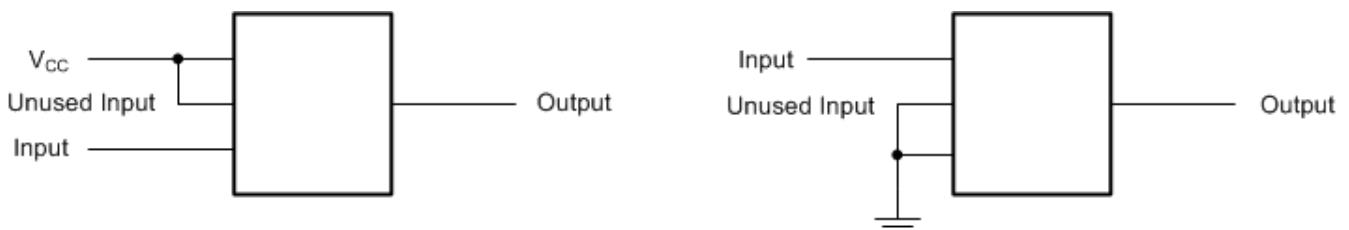


図 8-3. Layout Recommendation

## 9 Device and Documentation Support

### 9.1 Documentation Support (Analog)

#### 9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV240A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

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### 9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

### Changes from Revision J (December 2022) to Revision K (May 2024) Page

「パッケージ情報」表のフォーマットと本体サイズを更新 .....	1
ドキュメントの構造レイアウトを更新.....	1
Updated thermal values for PW package from RθJA = 102.4 to 128.2, RθJC(top) = 36.5 to 70.5, RθJB = 53.6 to 79.3, ΨJT = 2.4 to 23.4, ΨJB = 52.9 to 78.9, all values in °C/W.....	6

### Changes from Revision I (February 2015) to Revision J (December 2022) Page

文書全体にわたって表、図、相互参照の書式を更新.....	1
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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV240ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	<a href="#">Samples</a>
SN74LV240ADBRE4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	<a href="#">Samples</a>
SN74LV240ADGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L240A	<a href="#">Samples</a>
SN74LV240ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	<a href="#">Samples</a>
SN74LV240ADW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	LV240A	
SN74LV240ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	<a href="#">Samples</a>
SN74LV240ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV240A	<a href="#">Samples</a>
SN74LV240APW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125	LV240A	
SN74LV240APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	<a href="#">Samples</a>
SN74LV240APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV240ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV240ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV240ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV240ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV240ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV240APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV240APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV240ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV240ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LV240ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV240ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV240ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV240APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV240APWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

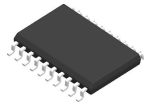
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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