

# SN74LV4040A 12 ビット非同期バイナリ・カウンタ

## 1 特長

- 2V~5.5V の  $V_{CC}$  で動作
- 標準  $V_{OLP}$  (出力グランドバウンス)  $< 0.8V$  ( $V_{CC} = 3.3V, T_A = 25^\circ C$ )
- 標準  $V_{OHV}$  (出力  $V_{OH}$  アンダーシュート)  $2.3V$  ( $V_{CC} = 3.3V, T_A = 25^\circ C$ )
- すべてのポートで混在モード電圧動作をサポート
- 高いオン/オフ出力電圧比
- スイッチ間の低いクロストーク
- スイッチの個別制御
- 非常に低い入力電流
- $I_{off}$  により部分的パワーダウンモードでの動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

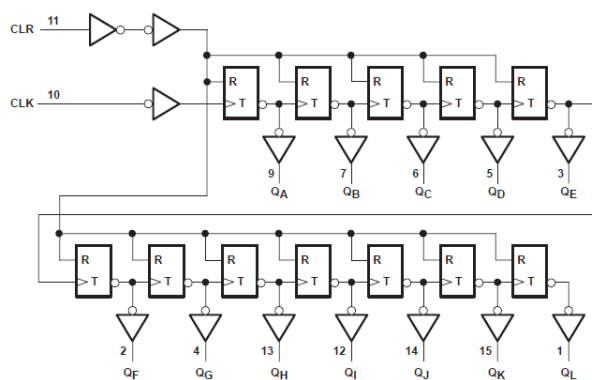
## 2 概要

'LV4040A デバイスは 12 ビット非同期バイナリカウンタで、すべての段の出力を外部で使用できます。

### パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)	本体サイズ (3)
SN74LV4040A	N (PDIP, 16)	19.3mm × 9.4 mm	19.3mm × 6.35 mm
	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	NS (SOP, 16)	10.2mm × 7.8mm	10.2mm × 5.3mm
	DB (SSOP, 16)	6.2mm × 7.8mm	6.2mm × 5.3mm
	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	DGV (TVSOP, 16)	3.6mm × 6.4mm	3.6mm × 4.4mm
	RGY (VQFN, 16)	4mm × 3.5mm	4mm × 3.5mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



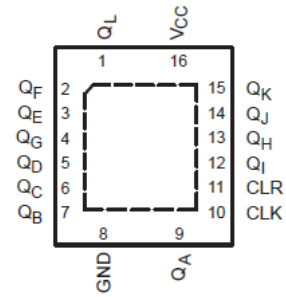
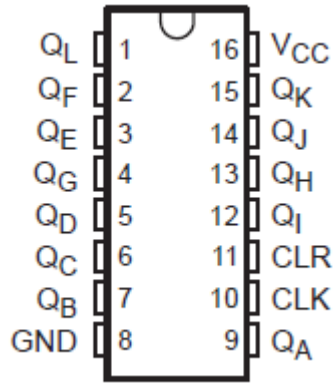
論理図 (正論理)



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### 3 Pin Configuration and Functions



A. NC - no internal connection

☒ 3-2. SN74LV4040A RGY Package (Top View)

☒ 3-1. SN74LV4040A D, DB, DGV, N, NS, or PW Package (Top View)

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
Q <sub>L</sub>	1	O	Q <sub>L</sub> output
Q <sub>F</sub>	2	O	Q <sub>F</sub> output
Q <sub>E</sub>	3	O	Q <sub>E</sub> output
Q <sub>G</sub>	4	O	Q <sub>G</sub> output
Q <sub>D</sub>	5	O	Q <sub>D</sub> output
Q <sub>C</sub>	6	O	Q <sub>C</sub> output
Q <sub>B</sub>	7	O	Q <sub>B</sub> output
GND	8	-	Ground
Q <sub>A</sub>	9	O	Q <sub>A</sub> output
CLK	10	I	Clock, falling edge triggered
CLR	11	I	Clear, active high
Q <sub>I</sub>	12	O	Q <sub>I</sub> output
Q <sub>H</sub>	13	O	Q <sub>H</sub> output
Q <sub>J</sub>	14	O	Q <sub>J</sub> output
Q <sub>K</sub>	15	O	Q <sub>K</sub> output
V <sub>CC</sub>	16	-	Positive supply

(1) I = input, O = output

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range	-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state	-0.5	7	V
V <sub>O</sub>	Output voltage range	-0.5 V to V <sub>CC</sub>	0.5	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	(V <sub>I</sub> < 0)	-20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	(V <sub>O</sub> < 0)	±50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>1</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>2</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	-50	mA
		V <sub>CC</sub> = 2.3 V to 2.7 V	-2	
		V <sub>CC</sub> = 3 V to 3.6 V	-6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	-12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	
		V <sub>CC</sub> = 3 V to 3.6 V	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	12	

### 4.3 Recommended Operating Conditions (続き)

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	200	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	100	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	UNIT	
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.5	82	120	67	64	122.3	39	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

### 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	SN74LV4040A			UNIT
			MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	2 V to 5.5 V	$V_{CC} - 0.1$			V
	$I_{OH} = -2 \text{ mA}$	2.3 V	2			
	$I_{OH} = -6 \text{ mA}$	3 V	2.48			
	$I_{OH} = -12 \text{ mA}$	4.5 V	3.8			
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	2 V to 5.5 V	0.1			V
	$I_{OL} = 2 \text{ mA}$	2.3 V	0.4			
	$I_{OL} = 6 \text{ mA}$	3 V	0.44			
	$I_{OL} = 12 \text{ mA}$	4.5 V	0.55			
$I_I$	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	$\pm 1$			$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC} \text{ or GND, } I_O = 0$	5.5 V	20			$\mu\text{A}$
$I_{off}$	$V_I \text{ or } V_O = 0 \text{ to } 5.5 \text{ V}$	0	5			$\mu\text{A}$
$C_i$	$V_I = V_{CC} \text{ or GND}$	3.3 V	1.9			pF

### 4.6 Timing Requirements, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

		$T_A = 25^\circ\text{C}$		SN74LV4040A		UNIT
		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	7	7	ns	
		CLR high	6.5	6.5		
$t_{su}$	Setup time	CLR inactive before CLK ↓	6.5	6.5		

#### 4.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

		$T_A = 25^\circ\text{C}$		SN74LV4040A		UNIT
		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low		5		ns
		CLR high		5		
$t_{su}$	Setup time	CLR inactive before CLK ↓		5		

#### 4.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)

		$T_A = 25^\circ\text{C}$		SN74LV4040A		UNIT
		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low		5		ns
		CLR high		5		
$t_{su}$	Setup time	CLR inactive before CLK ↓		5		

#### 4.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	50 <sup>1</sup>	115 <sup>1</sup>		40 <sup>1</sup>		MHz
			$C_L = 50\text{ pF}$	40	95		35		
$t_{PLH}$	CLK	$Q_A$	$C_L = 15\text{ pF}$	8.7 <sup>1</sup>	19.4 <sup>1</sup>		1 <sup>1</sup>	23 <sup>1</sup>	ns
$t_{PHL}$				8.7 <sup>1</sup>	19.4 <sup>1</sup>		1 <sup>1</sup>	23 <sup>1</sup>	
$t_{PHL}$	CLR	Any Q	$C_L = 15\text{ pF}$	9.3 <sup>1</sup>	19.9 <sup>1</sup>		1 <sup>1</sup>	24 <sup>1</sup>	
$t_{PLH}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 50\text{ pF}$	10.5	24.1		1	28	ns
$t_{PHL}$				10.5	24.1		1	28	
$t_{PHL}$	CLR	Any Q	$C_L = 50\text{ pF}$	11.7	24.5		1	28	
$\Delta t_{pd}$	$Q_n$	$Q_{n+1}$	$C_L = 50\text{ pF}$	1.7	5.9			7	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

#### 4.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3$  (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	75 <sup>1</sup>	160 <sup>1</sup>		75		MHz
			$C_L = 50\text{ pF}$	55	130		50		
$t_{PLH}$	CLK	$Q_A$	$C_L = 15\text{ pF}$	6.1 <sup>1</sup>	11.9 <sup>1</sup>		1	14	ns
$t_{PHL}$				6.1 <sup>1</sup>	11.9 <sup>1</sup>		1	14	ns
$t_{PHL}$	CLR	Any Q	$C_L = 15\text{ pF}$	7.1 <sup>1</sup>	12.8 <sup>1</sup>		1	15	ns
$t_{PLH}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 50\text{ pF}$	7.5	15.4		1	17.5	ns
$t_{PHL}$				7.5	15.4		1	17.5	ns
$t_{PHL}$	CLR	Any Q	$C_L = 50\text{ pF}$	9	16.3		1	18.5	ns

#### 4.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (続き)

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3$  (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$\Delta t_{pd}$	$Q_n$	$Q_{n+1}$	$C_L = 50\text{ pF}$		1.2	4.4		5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

#### 4.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	150 <sup>1</sup>	235 <sup>1</sup>		125		MHz
			$C_L = 50\text{ pF}$	95	185		80		
$t_{PLH}$	CLK	$Q_A$	$C_L = 15\text{ pF}$		4.2 <sup>1</sup>	7.3 <sup>1</sup>	1	8.5	ns
$t_{PHL}$					4.2 <sup>1</sup>	7.3 <sup>1</sup>	1	8.5	ns
$t_{PHL}$	CLR	Any Q	$C_L = 15\text{ pF}$		5.3 <sup>1</sup>	8.6 <sup>1</sup>	1	10	ns
$t_{PLH}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 50\text{ pF}$		5.3	9.3	1	10.5	ns
$t_{PHL}$					5.3	9.3	1	10.5	ns
$t_{PHL}$	CLR	Any Q	$C_L = 50\text{ pF}$		6.8	10.6	1	12	ns
$\Delta t_{pd}$	$Q_n$	$Q_{n+1}$	$C_L = 50\text{ pF}$		0.8	3.1		3.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

#### 4.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER <sup>(1)</sup>		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.5	-0.8	V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

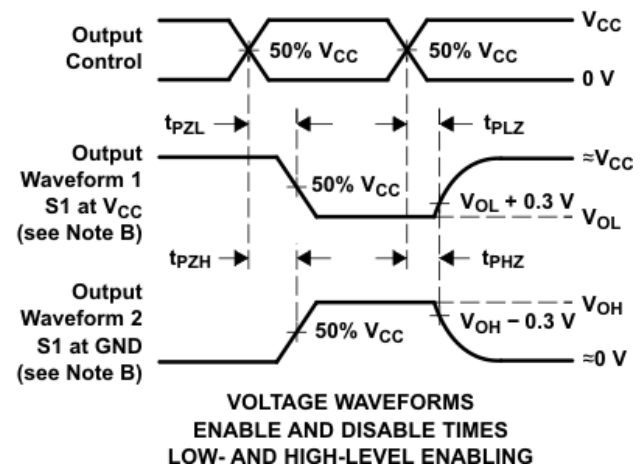
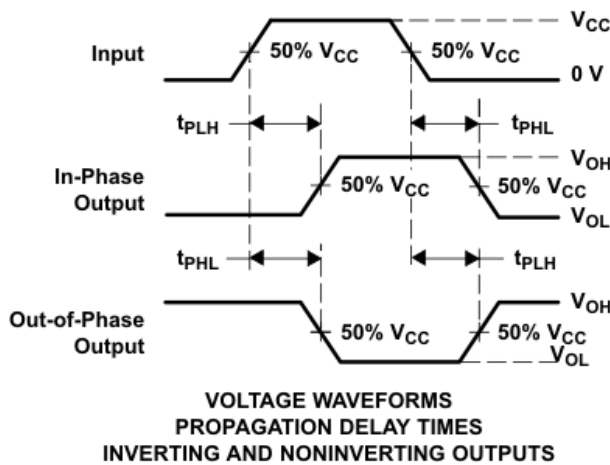
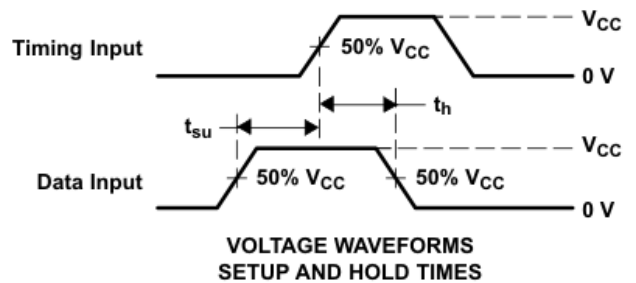
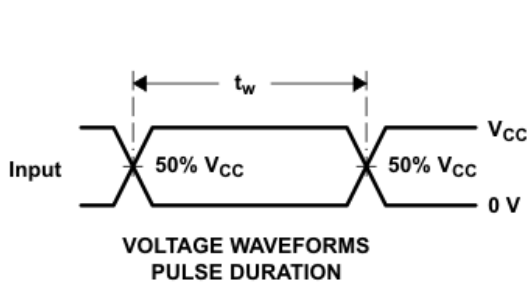
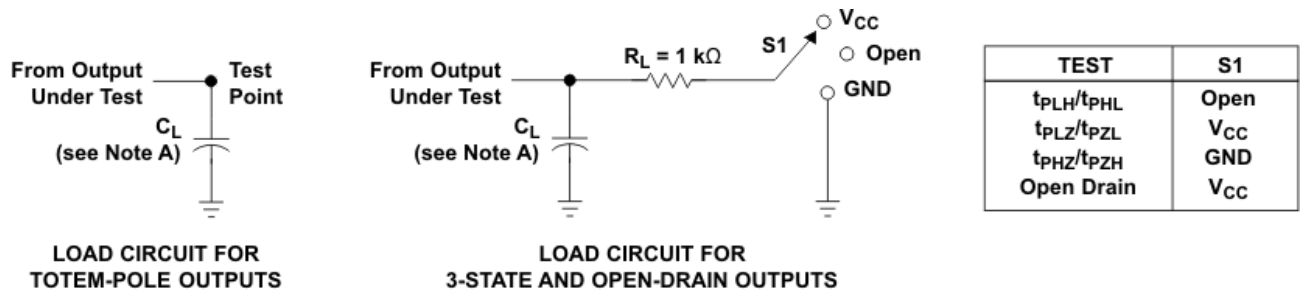
(1) Characteristics for surface-mount packages only.

#### 4.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 10\text{ MHz}$	3.3 V	11.9	pF
				5 V	13.1	

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ , and  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**5-1. Load Circuit and Voltage Waveforms**



## 6 Detailed Description

### 6.1 Overview

The 'LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 6.2 Functional Block Diagram

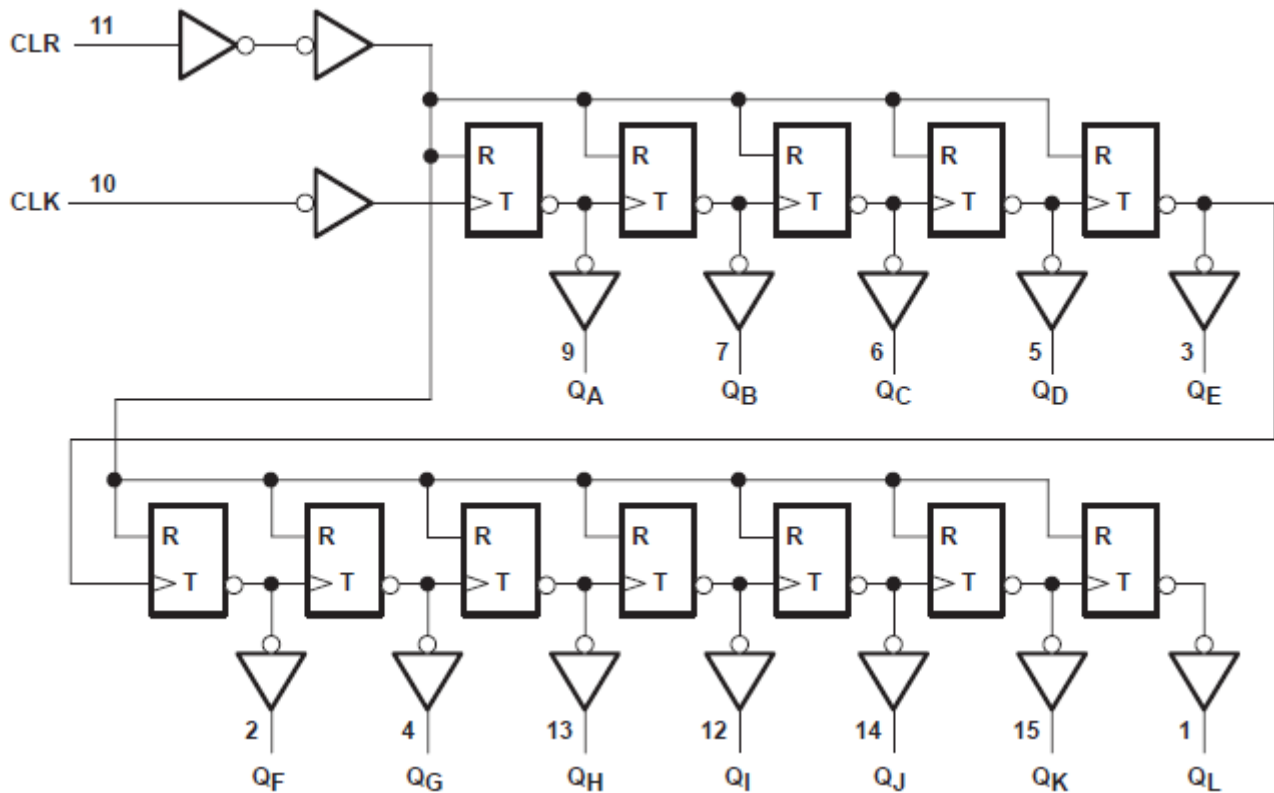


図 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

表 6-1. Function Table  
(Each Buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

## 7 Application and Implementation

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### 注

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### 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV4040A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 8.3 サポート・リソース

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### 8.4 Trademarks

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### 8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (July 2023) to Revision K (September 2024)	Page
「パッケージ情報」の表に本体サイズを追加 .....	1
Updated <i>Pin Functions</i> table.....	3
Added <i>Application and Implementation</i> section.....	10

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**Changes from Revision I (May 2005) to Revision J (July 2023)**
**Page**

- パッケージ情報の表、ピンの機能の表、ESD 定格の表、熱に関する情報の表、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ..... 1
  - Updated thermal values for RθJA: D = 73 to 99.5, PW = 108 to 122.3, all values in °C/W .....5
- 

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4040AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	LV4040A	
SN74LV4040ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A	Samples
SN74LV4040AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4040AN	Samples
SN74LV4040ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4040A	Samples
SN74LV4040APW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	LW040A	
SN74LV4040APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040APWT	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	LW040A	
SN74LV4040ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LV4040A :**

- Enhanced Product : [SN74LV4040A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

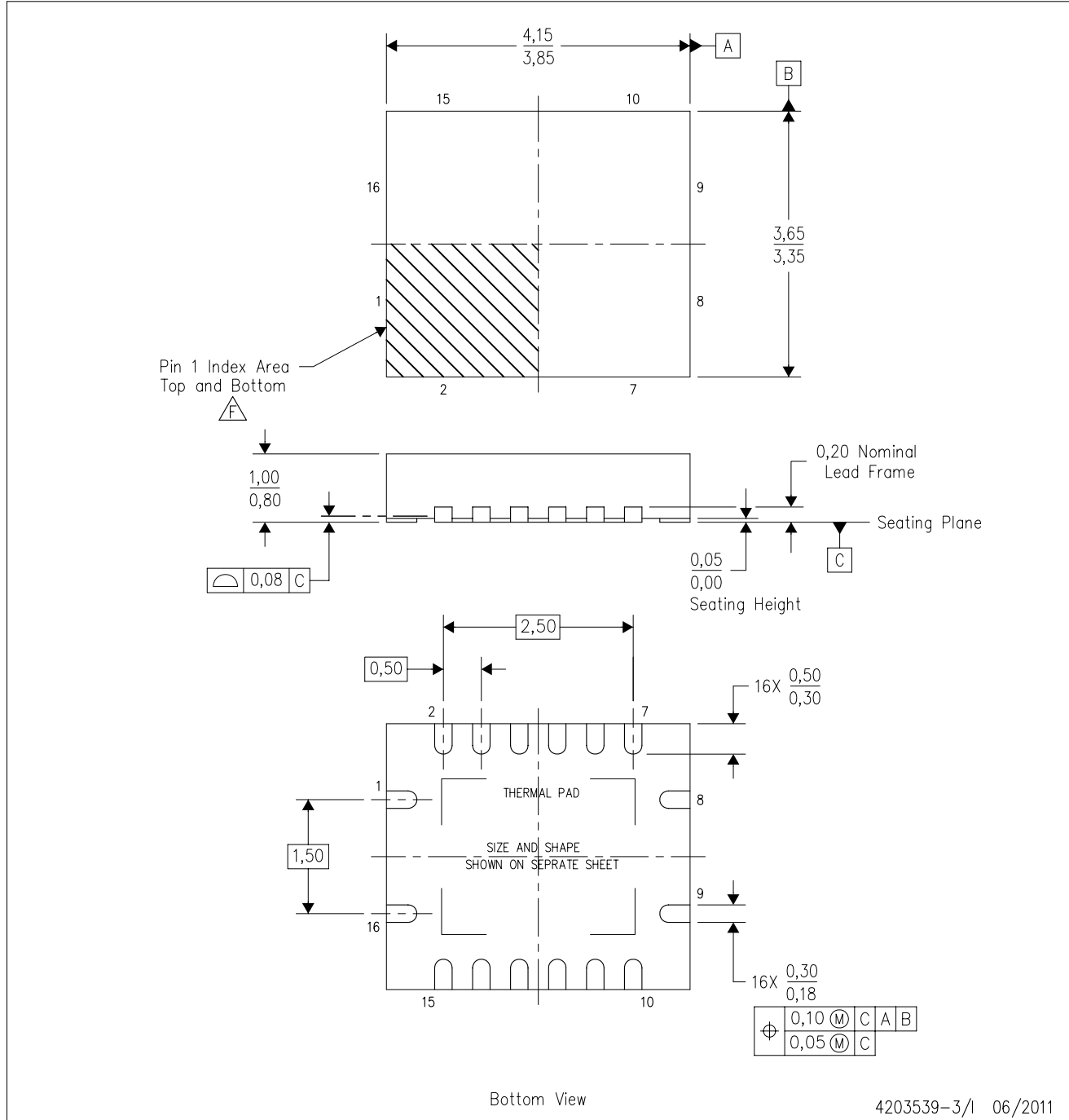


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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