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SN74LVC06A-EP
HEX INVERTER BUFFER/DRIVER
WITH OPEN DRAIN OUTPUTS
SCAS832A−APRIL 2007−REVISED MAY 2007

FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree** [1]
- **Operates From 1.65 V to 3.6 V**
- **Inputs and Open Drain Outputs Accept Voltages up to 5.5 V**
- **Max t_{pd} of 3.7 ns at 3.3 V**
- **I_{off} Supports Partial Power Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

[1] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y
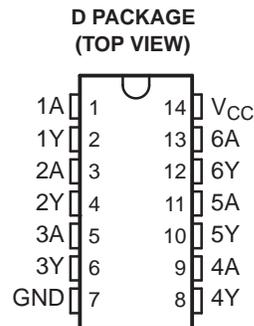
DESCRIPTION/ORDERING INFORMATION

The SN74LVC06A is a hex inverter buffer/driver that is designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the SN74LVC06A device are open drain and can be connected to other open-drain outputs to implement active low wired OR or active high wired AND functions. The maximum sink current is 24 mA.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V system environment.

This device is fully specified for partial power down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE
(EACH INVERTER)

INPUT A	OUTPUT Y
H	L
L	H

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)
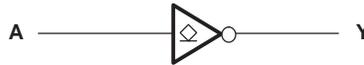
ORDERING INFORMATION[1]

T$_A$	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	SOIC – D	Reel of 2500	SN74LVC06AMDREP	LVC06AM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V$_{CC}$	Supply voltage range		−0.5	6.5	V
V$_I$	Input voltage range[2]		−0.5	6.5	V
V$_O$	Output voltage range		−0.5	6.5	V
I$_{IK}$	Input clamp current	V$_I$ < 0 V		−50	mA
I$_{OK}$	Output clamp current	V$_O$ < 0 V		−50	mA
I$_O$	Continuous output current			±50	mA
	Continuous current through V$_{CC}$ or GND			±100	mA
θ$_{JA}$	Package thermal impedance[3]			86	°C/W
T$_{stg}$	Storage temperature range		−65	150	°C
P$_{tot}$	Power dissipation[4]	T$_A$ = −55°C to 125°C		500	mW

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) Above 70°C the value of P$_{tot}$ derates linearly with 8 mW/K.

Recommended Operating Conditions[1]

			T$_A$ = 25°C		−55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
V$_{CC}$	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V$_{IH}$	High-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V	0.65 × V$_{CC}$		0.65 × V$_{CC}$		V
		V$_{CC}$ = 2.3 V to 2.7 V	1.7		1.7		
		V$_{CC}$ = 2.7 V to 3.6 V	2		2		
V$_{IL}$	Low-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V		0.35 × V$_{CC}$		0.35 × V$_{CC}$	V
		V$_{CC}$ = 2.3 V to 2.7 V		0.7		0.7	
		V$_{CC}$ = 2.7 V to 3.6 V		0.8		0.8	
V$_I$	Input voltage		0	5.5	0	5.5	V
V$_O$	Output voltage		0	5.5	0	5.5	V

(1) All unused inputs of the device must be held at V$_{CC}$ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Recommended Operating Conditions (continued)

		$T_A = 25°C$		$-55°C$ to $125°C$		UNIT
		MIN	MAX	MIN	MAX	
I_{OL} Low-level output current	V_{CC} = 1.65 V		4		4	mA
	V_{CC} = 2.3 V		8		8	
	V_{CC} = 2.7 V		12		12	
	V_{CC} = 3 V		24		24	

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			$-55°C$ to $125°C$		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OL}	I_{OL} = 100 µA	1.65 V to 3.6 V			0.1		0.3	V
	I_{OL} = 4 mA	1.65 V			0.24		0.6	
	I_{OL} = 8 mA	2.3 V			0.3		0.75	
	I_{OL} = 12 mA	2.7 V			0.4		0.6	
	I_{OL} = 24 mA	3 V			0.55		0.8	
I_I	V_I = 5.5 V or GND	3.6 V			±1		±20	µA
I_{off}	V_I or V_O = 5.5 V	0 V			±1		±20	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	3.6 V			1		40	µA
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500		5000	µA
C_I	$V_I = V_{CC}$ or GND	3.3 V		5				pF

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			$-55°C$ to $125°C$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	1.8 V ± 0.15 V	1.4	3	5.1	1.4	7.6	ns
			2.5 V ± 0.2 V	1	1.9	2.8	1	4	
			2.7 V	1	2.4	3.7	1	5	
			3.3 V ± 0.3 V	1	2.2	3.5	1	5	

Operating Characteristics

$T_A = 25°C$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	f = 10 MHz	1.8 V	2.1	pF
		2.5 V	2.3	
		3.3 V	2.5	

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT
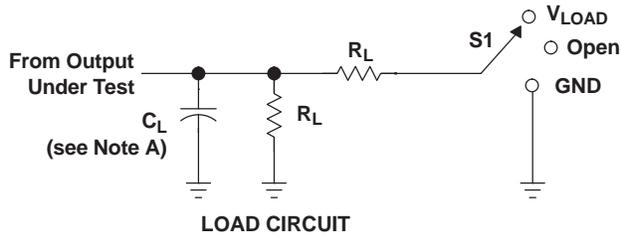
TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	$\leq$ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	$\leq$ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq$ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq$ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
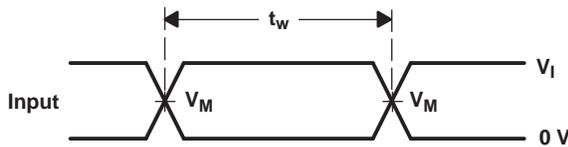
VOLTAGE WAVEFORMS
PULSE DURATION
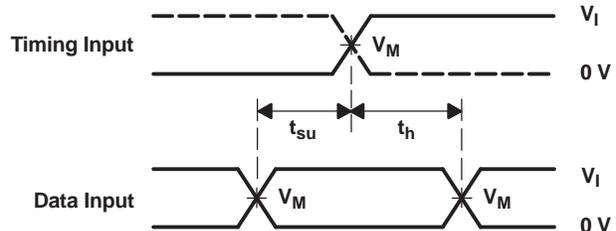
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
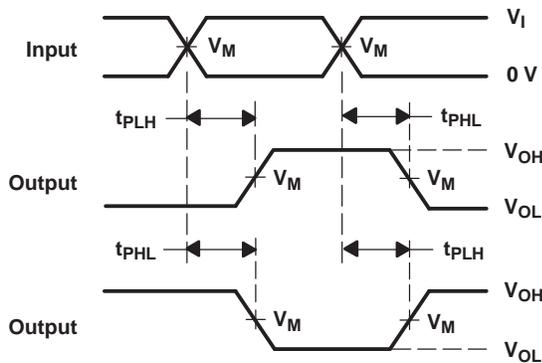
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
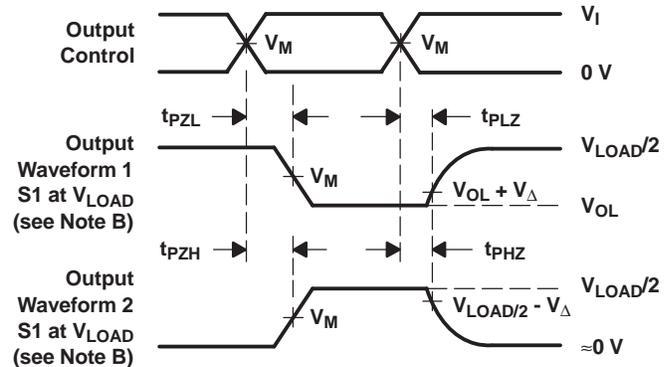
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at V_M.
G. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC06AMDREP	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LC06AM	Samples
V62/06661-01XE	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LC06AM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC06A-EP :

● Catalog: SN74LVC06A

● Automotive: SN74LVC06A-Q1

NOTE: Qualified Version Definitions:

     ● Catalog - TI's standard catalog product

     ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
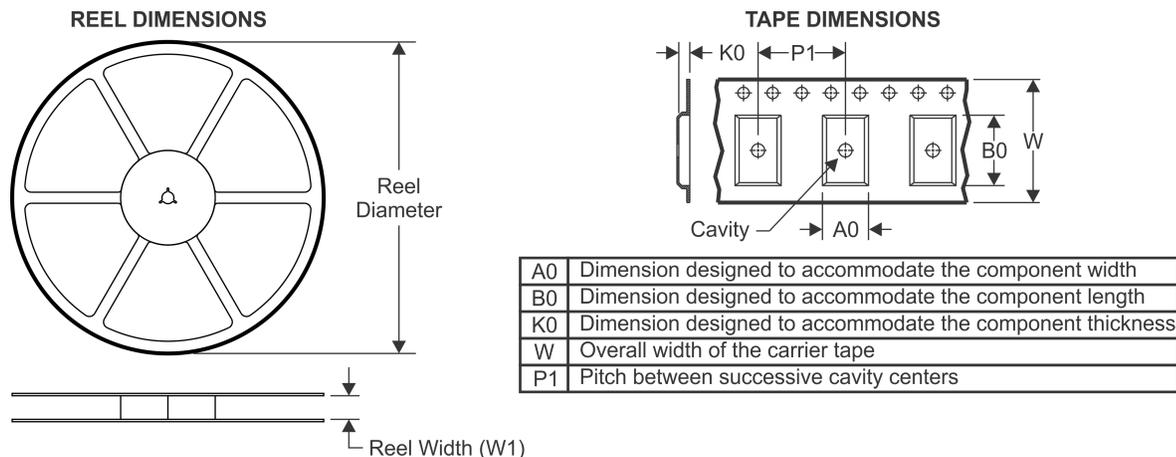
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
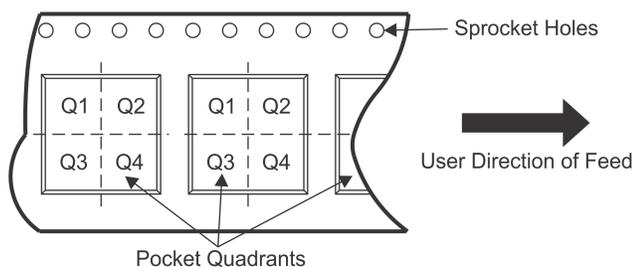
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC06AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
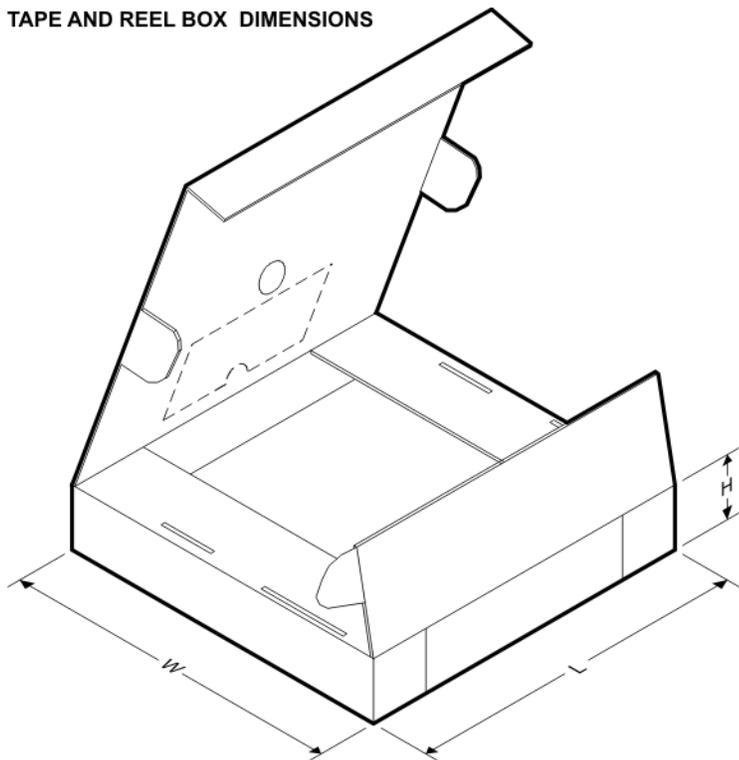
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC06AMDREP	SOIC	D	14	2500	340.5	336.1	32.0

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   7

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11
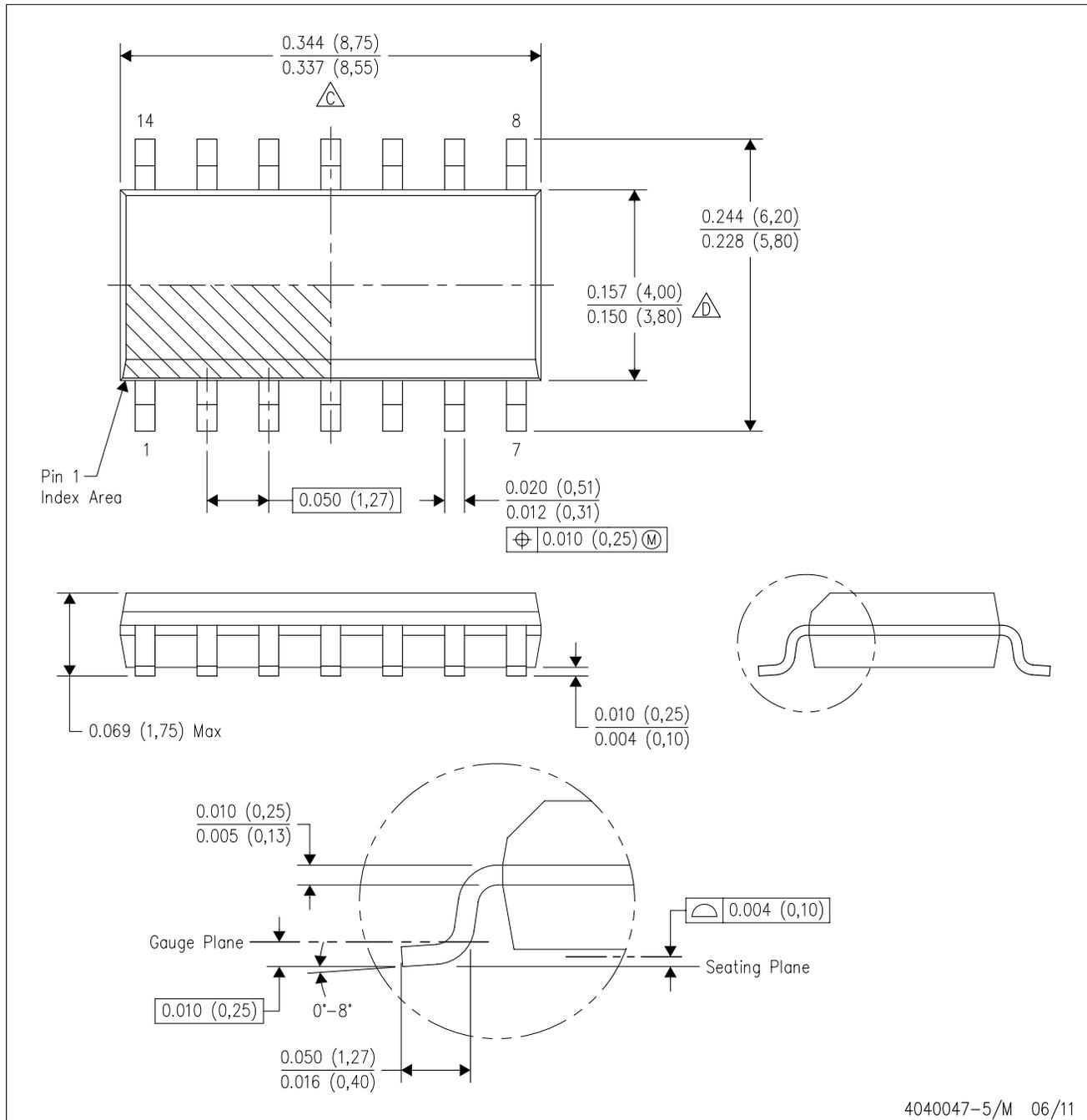
NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
          D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AB.

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D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

|←—12x1,27

|←—14x0,55

|←—12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283−3/E 08/12
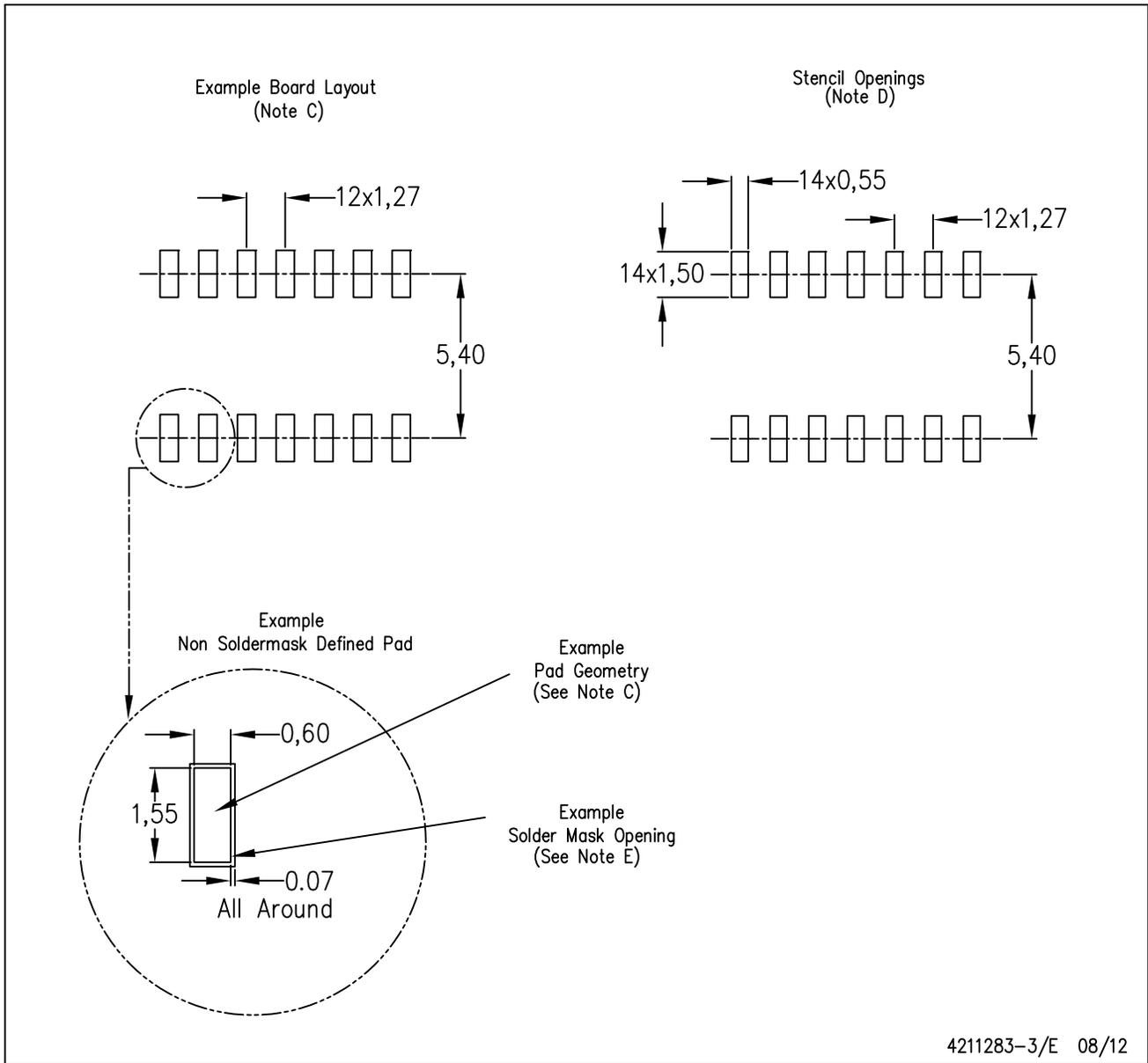
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.