

## SN74LVC1G3157 単極双投アナログ・スイッチ

### 1 特長

- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、荷電デバイス・モデル (C101)
- 1.65V~5.5V の  $V_{CC}$  で動作
- 125°C動作向けに認定済み
- Break-Before-Make スwitchingを規定
- レール・ツー・レールの信号処理
- 動作周波数: 340MHz (標準値、室温)
- 高速、標準値 0.5ns ( $V_{CC} = 3V, C_L = 50pF$ )
- 低いオン抵抗: 約 6Ω (標準値) ( $V_{CC} = 4.5V$ )
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

### 2 アプリケーション

- ウェアラブルおよびモバイル・デバイス
- ポータブル・コンピュータ
- モノのインターネット (IoT)
- オーディオ信号の経路設定
- リモート無線ユニット
- 携帯医療機器
- 監視機器
- ホーム・オートメーション
- I2C/SPI/UART バスの多重化
- ワイヤレス充電

### 3 概要

このシングル・チャンネル単極双投 (SPDT) アナログ・スイッチは、1.65V~5.5V の  $V_{CC}$  で動作するように設計されています。

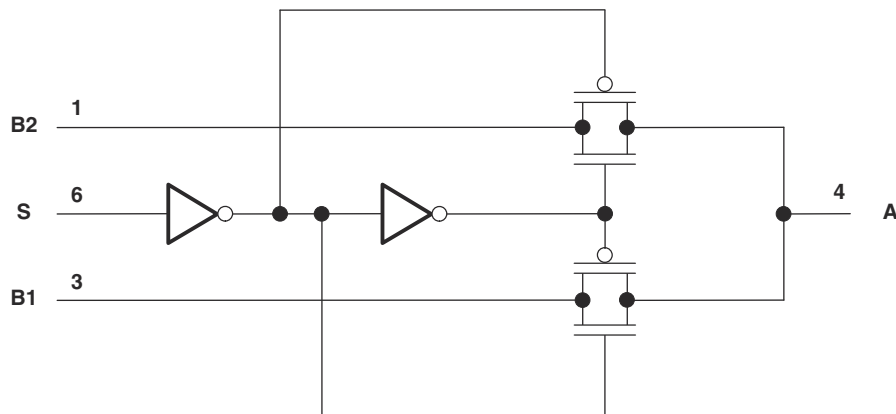
SN74LVC1G3157 デバイスは、アナログとデジタルの両方の信号を扱うことができます。SN74LVC1G3157 デバイスは、最高で  $V_{CC}$  (ピーク) までの振幅の信号を、どちらの方向にも転送できます。

信号ゲーティング、チョッピング、変調または復調 (モデム)、およびアナログ / デジタルやデジタル / アナログ変換システム用の信号多重化などのアプリケーションに使用できます。

#### 製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN74LVC1G3157	SOT-23 (DBV) (6)	2.90mm × 1.60mm
	SC70 (DCK) (6)	2.00mm × 1.25mm
	SOT (DRL) (6)	1.60mm × 1.20mm
	SON (DRY) (6)	1.45mm × 1.00mm
	DSBGA (YZP) (6)	1.41mm × 0.91mm
	SON (DSF) (6)	1.00mm × 1.00mm
	X2SON (DTB) (6)	0.80mm × 1.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision L (May 2017) to Revision M (August 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated the <i>Pin Configuration and Functions</i> section.....	4
• Updated the equation in the <i>Detailed Design Procedure</i> section.....	18

Changes from Revision K (January 2017) to Revision L (May 2017)	Page
• 「特長」の「アナログとデジタルの両方のアプリケーションに便利」を削除.....	1
• 「特長」の「優れた直線性」を削除.....	1
• 「概要」の最初の文を「この単極双投 (SPDT) ...」から「このシングル・チャンネル単極双投 (SPDT) ...」に変更.....	1
• 「製品情報」に X2SON (DTB) パッケージを追加.....	1
• Added the X2SON (DTB) Package, to the <i>Pin Configuration and Functions</i> .....	4
• Changed I <sub>I/O To</sub> : I <sub>I/O K</sub> for I/O port diode current in the <i>Absolute Maximum Ratings</i> .....	6
• Added the DTB (X2SON) package to the <i>Thermal Information</i> table.....	7
• Changed Note 1 and Note 2 in the <i>Analog Switch Characteristics</i> table.....	9
• Deleted Note 3 "Specified by design" from the <i>Analog Switch Characteristics</i> tables.....	9
• Deleted Note 4 "Specified by design" from the <i>Switch Characteristics 85°C</i> tables.....	10
• Deleted Note 4 "Specified by design" from the <i>Switch Characteristics 125°C</i> tables.....	10
• Changed 図 7-2, From: SW1 = V <sub>IL</sub> to SW1 = V <sub>IH</sub> , From: SW2 = V <sub>IH</sub> to: SW2 = V <sub>IL</sub> .....	11
• Changed 図 7-5.....	11
• Added a series 50-Ω resistor on B1 in 図 7-6.....	11
• Changed 図 7-7.....	11

Changes from Revision J (June 2016) to Revision K (January 2017)	Page
• 「アプリケーション」セクションに新しいアプリケーションを追加.....	1
• Added Operating free-air temperature, T <sub>A</sub> for BGA and all other packages in <i>Recommended Operating Conditions</i> .....	7
• Added 125°C data to <i>Electrical Characteristics</i> table.....	8
• Added 85°C to title to differentiate from new 125°C <i>Switching Characteristics</i> section.....	10

- Added 125°C *Switching Characteristics* section and data. .... 10

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**Changes from Revision I (June 2015) to Revision J (June 2016) Page**

- 「特長」から「200V、マシン・モデル (A115-A)」を削除 ..... 1
- 「特長」の「動作周波数:300MHz (標準値、室温)」を「動作周波数:340MHz (標準値、室温)」に変更..... 1
- 「製品情報」表を更新..... 1
- Updated pinout images for all Packages..... 4
- Added temperature ranges for Storage temperature,  $T_{stg}$  and Junction temperature,  $T_j$  in *Absolute Maximum Ratings* ..... 6
- Changed MAX value  $\pm 1$  to  $\pm 0.1$  for  $I_{off}$  and  $I_{IN}$  in *Electrical Characteristics* table..... 8
- Added *Receiving Notification of Documentation Updates* section..... 20

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**Changes from Revision H (May 2012) to Revision I (June 2015) Page**

- 「製品情報」表、「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 ..... 1
- 「特長」を更新..... 1

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**Changes from Revision G (September 2011) to Revision H (May 2012) Page**

- Changed YZP with correct pin labels. .... 4
  - Added *Thermal Information* table..... 7
  - Changed to correct Pin Label "S"..... 8
-

## 5 Pin Configuration and Functions

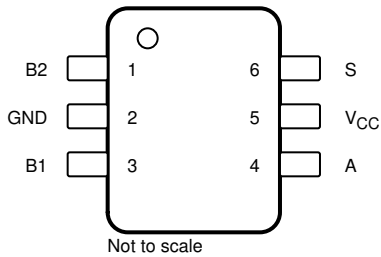


图 5-1. DBV Package, 6-Pin SOT-23 (Top View)

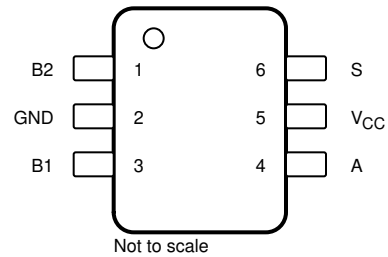


图 5-2. DCK Package, 6-Pin SC70 (Top View)

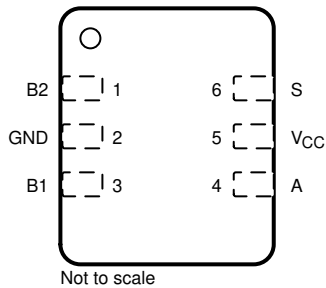


图 5-3. DRY Package, 6-Pin SON (Top View)

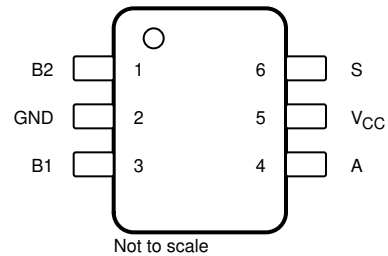


图 5-4. DRL Package, 6-Pin SOT (Top View)

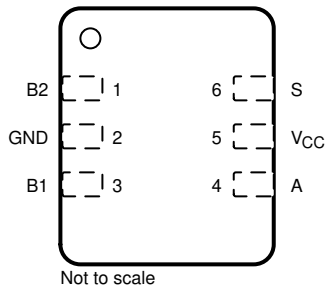


图 5-5. DSF Package, 6-Pin SON (Top View)

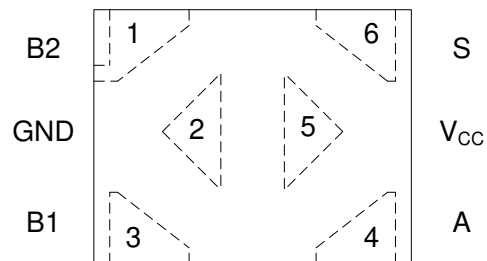


图 5-6. DTB Package, 6-Pin X2SON (Top View)

表 5-1. Pin Functions

NAME	PIN	TYPE <sup>(1)</sup>	DESCRIPTION
	SOT-23, SC70, SON, X2SON, or SOT		
B2	1	I/O	Switch I/O. Set S high to enable.
GND	2	P	Ground
B1	3	I/O	Switch I/O. Set S low to enable.
A	4	I/O	Common terminal
V <sub>CC</sub>	5	P	Power supply
S	6	I	Select

(1) I = input, O = output, P = power

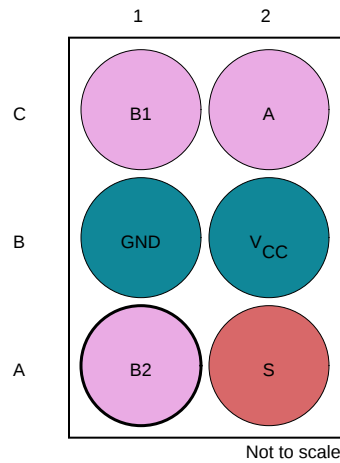


图 5-7. YZP Package, 6-Pin DSBGA (Bottom View)

Legend	
Input	Input or Output
Power	

表 5-2. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
A1	B2	I/O	Switch I/O. Set S high to enable.
A2	S	I	Select
B1	GND	P	Ground
B2	V <sub>CC</sub>	P	Power supply
C1	B1	I/O	Switch I/O. Set S low to enable.
C2	A	I/O	Common terminal

(1) I = input, O = output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		-0.5	6.5	V
V <sub>IN</sub>	Control input voltage <sup>(2) (3)</sup>		-0.5	6.5	V
V <sub>I/O</sub>	Switch I/O voltage <sup>(2) (3) (4) (5)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0		-50	mA
I <sub>I/O</sub> K	I/O port diode current	V <sub>I/O</sub> < 0 or V <sub>I/O</sub> > V <sub>CC</sub>		±50	mA
I <sub>I/O</sub>	On-state switch current <sup>(6)</sup>	V <sub>I/O</sub> = 0 to V <sub>CC</sub>		±128	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) V<sub>I</sub>, V<sub>O</sub>, V<sub>A</sub>, and V<sub>Bn</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (6) I<sub>I</sub>, I<sub>O</sub>, I<sub>A</sub>, and I<sub>Bn</sub> are used to denote specific conditions for I<sub>I/O</sub>.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	1.65	5.5	V	
V <sub>I/O</sub>	Switch input or output voltage	0	V <sub>CC</sub>	V	
V <sub>IN</sub>	Control input voltage	0	5.5	V	
V <sub>IH</sub>	High-level input voltage, control input	V <sub>CC</sub> = 1.65 V to 1.95 V	V <sub>CC</sub> × 0.75	V	
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage, control input	V <sub>CC</sub> = 1.65 V to 1.95 V	V <sub>CC</sub> × 0.25	V	
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.3		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.65 V to 1.95 V	20	ns/V	
		V <sub>CC</sub> = 2.3 V to 2.7 V	20		
		V <sub>CC</sub> = 3 V to 3.6 V	10		
		V <sub>CC</sub> = 4.5 V to 5.5 V	10		
T <sub>A</sub>	Operating free-air temperature	BGA package (YZP)	–40	85	°C
		All other packages (DBV, DCK, DRL, DRY, DSF)	–40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVC1G3157						UNIT	
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTB (X2SON)	YZP (DSBGA)		
	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	234.9	269.5	244.1	284.2	324.5	129.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	150.4	189.5	112.5	138.6	150.5	1.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	86.4	84.7	109.9	170.9	239.0	40.0	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	60.8	62.7	9.3	13.7	17.2	0.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	86.1	84.0	109.3	167.9	238.3	40.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = -40 to 85°C			T <sub>A</sub> = -40 to 125°C			UNIT
				MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
r <sub>on</sub> ON-state switch resistance <sup>(2)</sup>	See <a href="#">6-1</a> and <a href="#">7-1</a>	V <sub>I</sub> = 0 V	I <sub>O</sub> = 4 mA	1.65 V	11	20	11	20	Ω	
		V <sub>I</sub> = 1.65 V	I <sub>O</sub> = -4 mA		15	50	15	50		
		V <sub>I</sub> = 0 V	I <sub>O</sub> = 8 mA	2.3 V	8	12	8	12		
		V <sub>I</sub> = 2.3 V	I <sub>O</sub> = -8 mA		11	30	11	30		
		V <sub>I</sub> = 0 V	I <sub>O</sub> = 24 mA	3 V	7	9	7	9		
		V <sub>I</sub> = 3 V	I <sub>O</sub> = -24 mA		9	20	9	20		
		V <sub>I</sub> = 0 V	I <sub>O</sub> = 30 mA	4.5 V	6	7	6	7		
		V <sub>I</sub> = 2.4 V	I <sub>O</sub> = -30 mA		7	12	7	12		
V <sub>I</sub> = 4.5 V	I <sub>O</sub> = -30 mA		7	15	7	15				
r <sub>range</sub> ON-state switch resistance over signal range <sup>(2) (3)</sup>	0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub> (see <a href="#">6-1</a> and <a href="#">7-1</a> )	I <sub>A</sub> = -4 mA		1.65 V		140		140	Ω	
		I <sub>A</sub> = -8 mA		2.3 V		45		45		
		I <sub>A</sub> = -24 mA		3 V		18		18		
		I <sub>A</sub> = -30 mA		4.5 V		10		10		
Δr <sub>on</sub> Difference of ON-state resistance between switches <sup>(2) (4) (5)</sup>	See <a href="#">7-1</a>	V <sub>Bn</sub> = 1.15 V	I <sub>A</sub> = -4 mA	1.65 V	0.5		0.5	Ω		
		V <sub>Bn</sub> = 1.6 V	I <sub>A</sub> = -8 mA	2.3 V	0.1		0.3			
		V <sub>Bn</sub> = 2.1 V	I <sub>A</sub> = -24 mA	3 V	0.1		0.3			
		V <sub>Bn</sub> = 3.15 V	I <sub>A</sub> = -30 mA	4.5 V	0.1		0.2			
r <sub>on(flat)</sub> ON resistance flatness <sup>(2) (4) (6)</sup>	0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	I <sub>A</sub> = -4 mA		1.65 V		110		Ω		
		I <sub>A</sub> = -8 mA		2.3 V		26			40	
		I <sub>A</sub> = -24 mA		3 V		9			10	
		I <sub>A</sub> = -30 mA		4.5 V		4			5	
I <sub>off</sub> <sup>(7)</sup> OFF-state switch leakage current		0 ≤ V <sub>I</sub> , V <sub>O</sub> ≤ V <sub>CC</sub> (see <a href="#">7-2</a> )		1.65 V to 5.5 V		±1		±1	μA	
I <sub>S(on)</sub> ON-state switch leakage current		V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = Open (see <a href="#">7-3</a> )		5.5 V		±1		±1	μA	
I <sub>IN</sub> Control input current		0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		0 V to 5.5 V		±1		±1	μA	
I <sub>CC</sub> Supply current		S = V <sub>CC</sub> or GND		5.5 V		1	10	35	μA	
ΔI <sub>CC</sub> Supply-current change		S = V <sub>CC</sub> - 0.6 V		5.5 V			500	500	μA	
C <sub>i</sub> Control input capacitance	S			5 V		2.7		2.7	pF	
C <sub>io(off)</sub> Switch input/output capacitance	Bn			5 V		5.2		5.2	pF	
C <sub>io(on)</sub> Switch input/output capacitance	Bn			5 V		17.3		17.3	pF	
	A						17.3			17.3

(1) T<sub>A</sub> = 25°C

(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.

(3) Specified by design

(4) Δr<sub>on</sub> = r<sub>on(max)</sub> - r<sub>on(min)</sub> measured at identical V<sub>CC</sub>, temperature, and voltage levels

(5) This parameter is characterized, but not production tested.

(6) Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.

(7) I<sub>off</sub> is the same as I<sub>S(off)</sub> (off-state switch leakage current).



## 6.6 Analog Switch Characteristics

 $T_A = 25^\circ\text{C}$ 

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
Frequency response <sup>(1)</sup> (switch on)	A or Bn	Bn or A	R <sub>L</sub> = 50 Ω, f <sub>in</sub> = sine wave (see <a href="#">7-5</a> )	1.65 V	340	MHz
				2.3 V	340	
				3 V	340	
				4.5 V	340	
Crosstalk <sup>(2)</sup> (between switches)	B1 or B2	B2 or B1	R <sub>L</sub> = 50 Ω, f <sub>in</sub> = 10 MHz (sine wave) (see <a href="#">7-6</a> )	1.65 V	-54	dB
				2.3 V	-54	
				3 V	-54	
				4.5 V	-54	
Feed through attenuation <sup>(2)</sup> (switch off)	A or Bn	Bn or A	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω, f <sub>in</sub> = 10 MHz (sine wave) (see <a href="#">7-7</a> )	1.65 V	-57	dB
				2.3 V	-57	
				3 V	-57	
				4.5 V	-57	
Charge injection	S	A	C <sub>L</sub> = 0.1 nF, R <sub>L</sub> = 1 MΩ (see <a href="#">7-8</a> )	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	V <sub>i</sub> = 0.5 V <sub>p-p</sub> , R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 600 Hz to 20 kHz (sine wave) (see <a href="#">7-9</a> )	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

- (1) Set f<sub>in</sub> to 0 dBm and provide a bias of 0.4 V. Increase f<sub>in</sub> frequency until the gain is 3 dB below the insertion loss.  
 (2) Set f<sub>in</sub> to 0 dBm and provide a bias of 0.4 V.

## 6.7 Switching Characteristics 85°C

 $T_A = -40$  to  $+85^\circ\text{C}$  (see [Figure 7-4](#) and [Figure 7-10](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or Bn	Bn or A	2		1.2		0.8		0.3		ns
$t_{en}^{(2)}$	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
$t_{dis}^{(3)}$			3	13	2	7.5	1.5	5.3	0.8	3.8	
$t_{B-M}$			0.5		0.5		0.5		0.5		ns

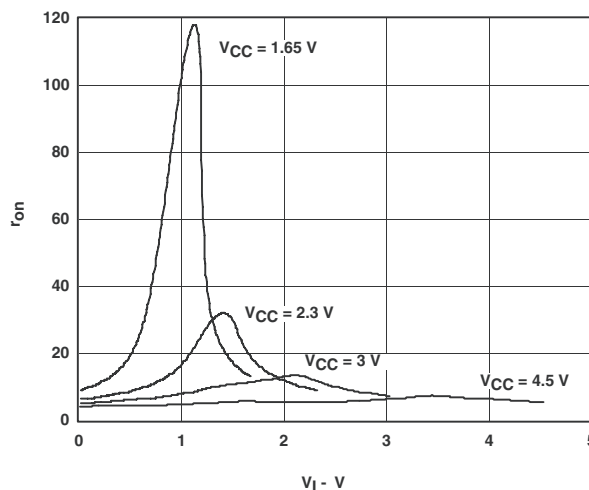
- (1)  $t_{pd}$  is the slower of  $t_{PLH}$  or  $t_{PHL}$ . The propagation delay is calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
- (2)  $t_{en}$  is the slower of  $t_{pZL}$  or  $t_{pZH}$ .
- (3)  $t_{dis}$  is the slower of  $t_{pLZ}$  or  $t_{pHZ}$ .

## 6.8 Switching Characteristics 125°C

 $T_A = -40$  to  $+125^\circ\text{C}$  (see [Figure 7-4](#) and [Figure 7-10](#))

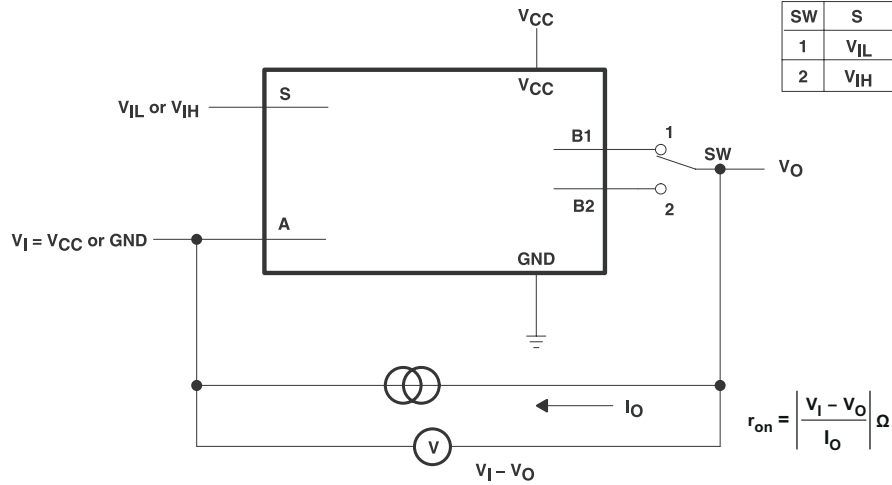
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or Bn	Bn or A	2		1.2		0.8		0.5		ns
$t_{en}^{(2)}$	S	Bn	1	24.5	1	14.5	2.5	8	1.7	6	ns
$t_{dis}^{(3)}$			2.5	13.5	2	8	1.5	5.5	0.8	4	
$t_{B-M}$			0.5		0.5		0.5		0.5		ns

## 6.9 Typical Characteristics

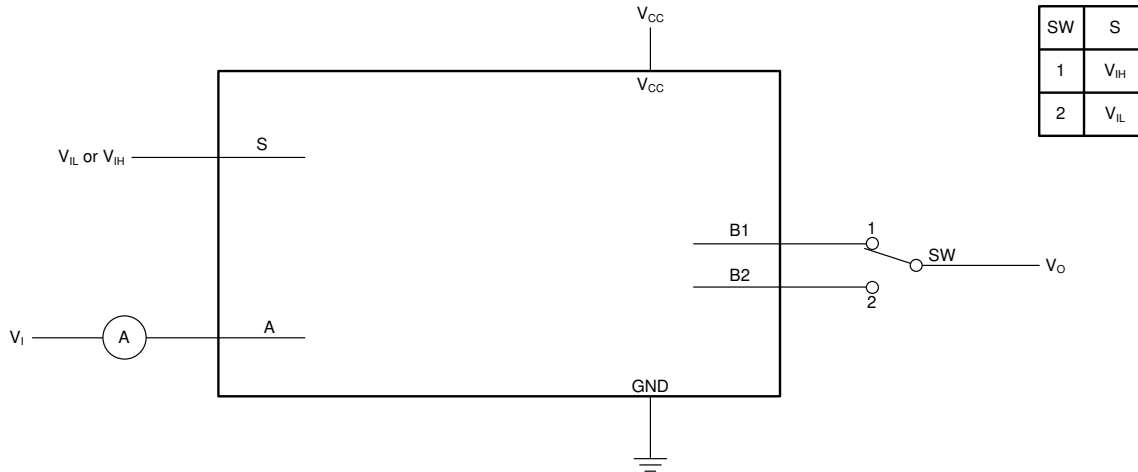


**Figure 6-1.** Typical  $r_{on}$  as a Function of Input Voltage ( $V_I$ ) for  $V_I = 0$  to  $V_{CC}$

## 7 Parameter Measurement Information

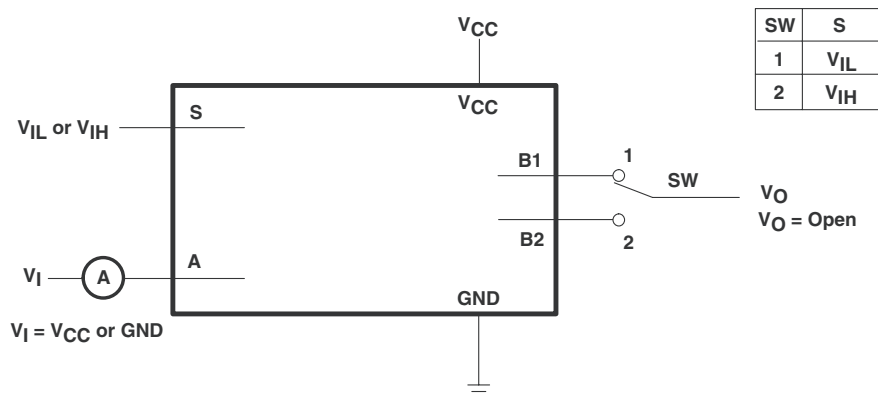


7-1. ON-State Resistance Test Circuit

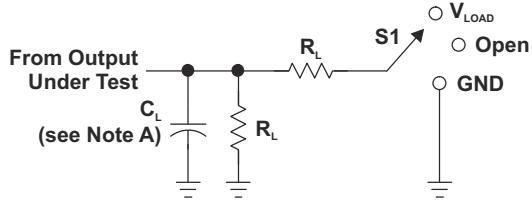


Condition 1: V<sub>I</sub> = GND, V<sub>O</sub> = V<sub>CC</sub>  
Condition 2: V<sub>I</sub> = V<sub>CC</sub>, V<sub>O</sub> = GND

7-2. OFF-State Switch Leakage-Current Test Circuit



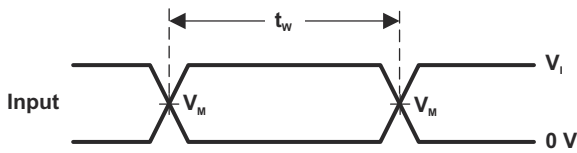
7-3. ON-State Switch Leakage-Current Test Circuit



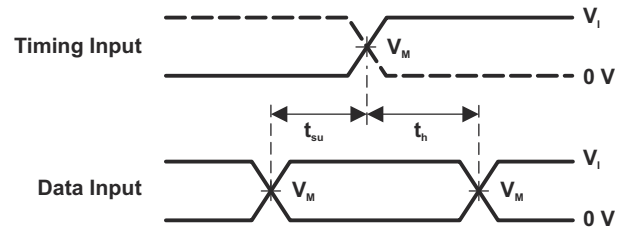
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

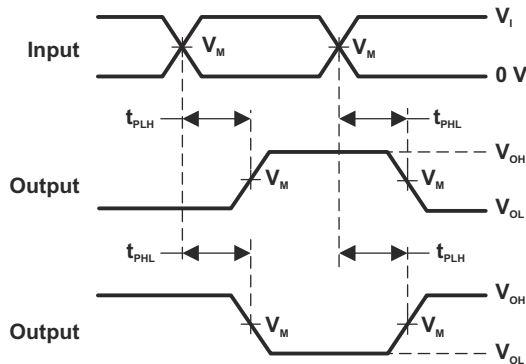
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_i/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



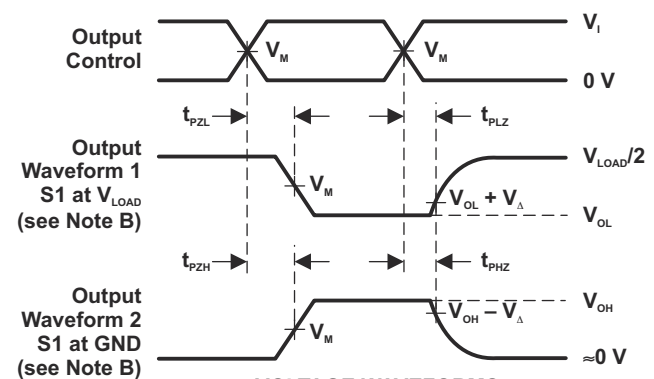
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



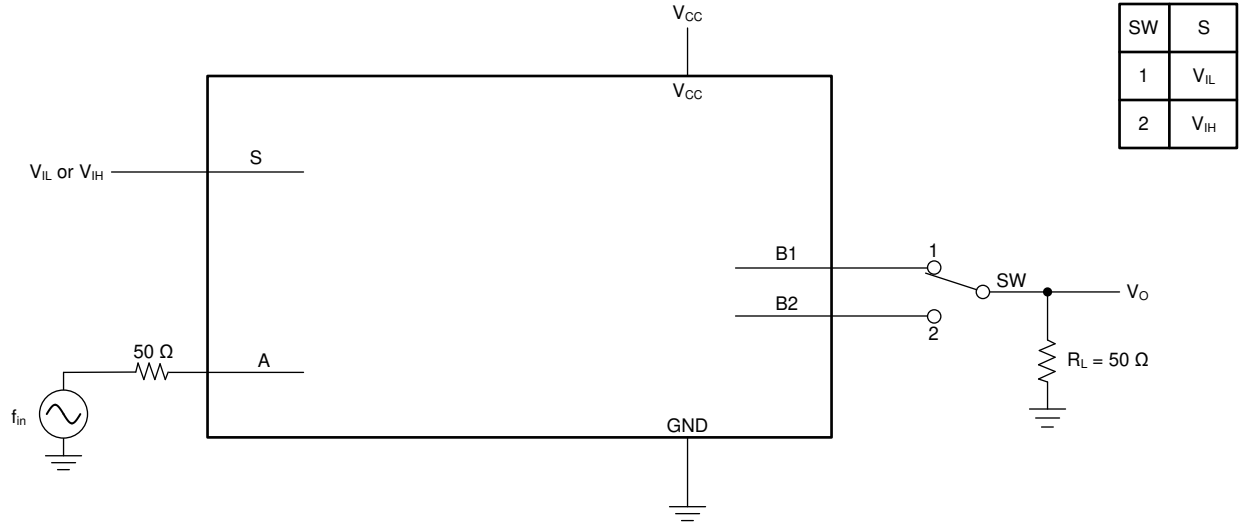
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



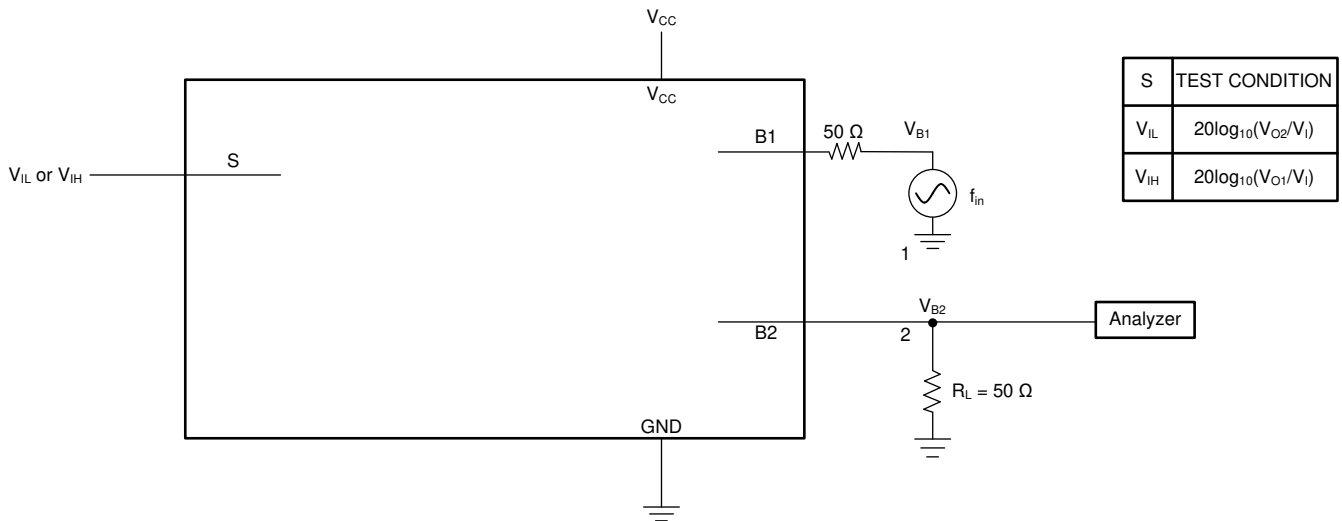
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

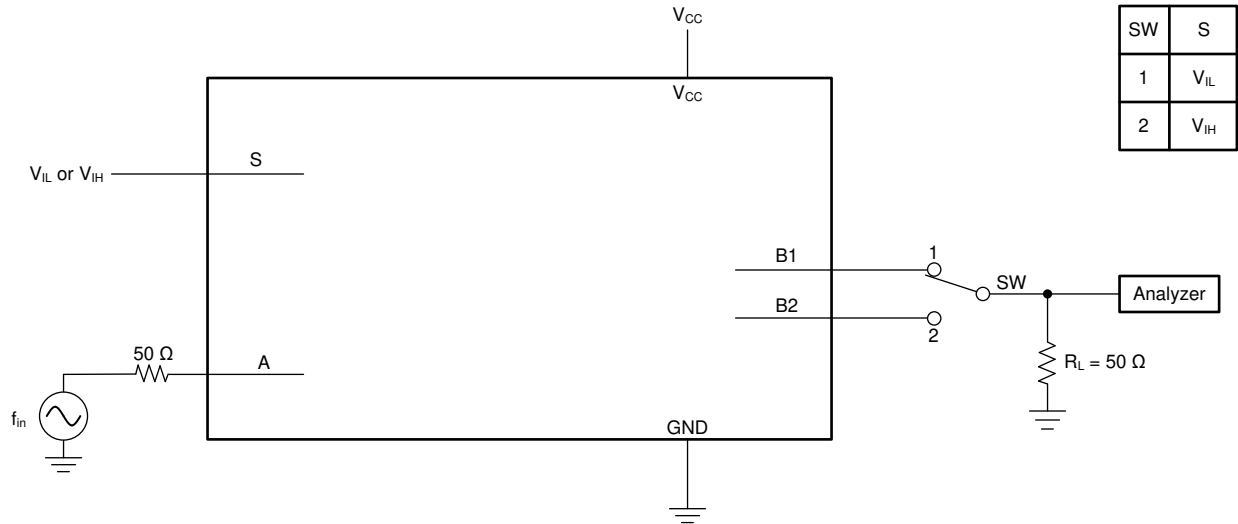
**7-4. Load Circuit and Voltage Waveforms**



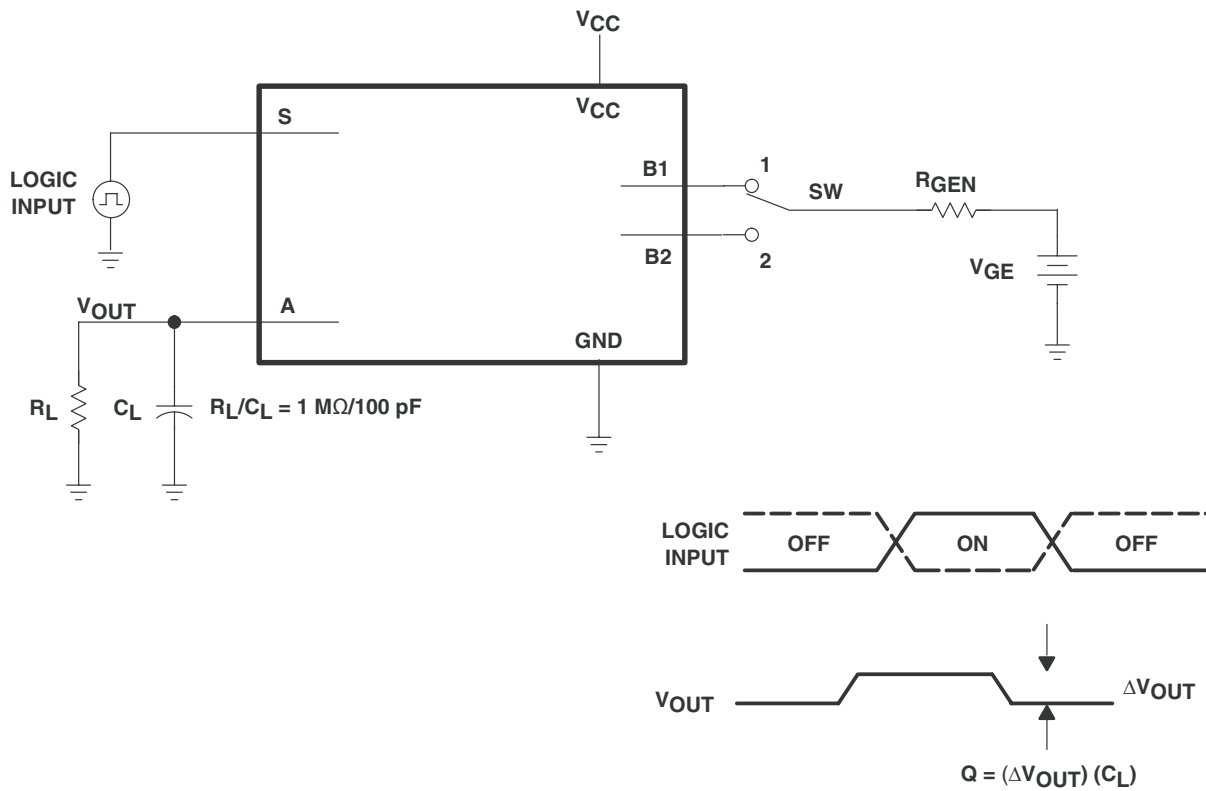
**7-5. Frequency Response (Switch On)**



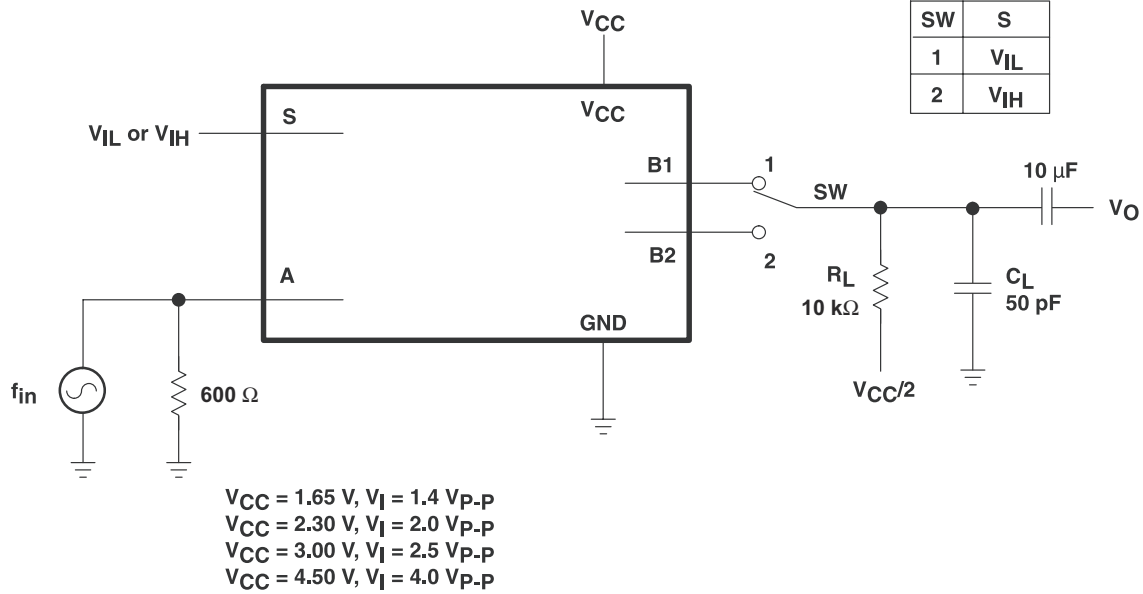
**7-6. Crosstalk (Between Switches)**



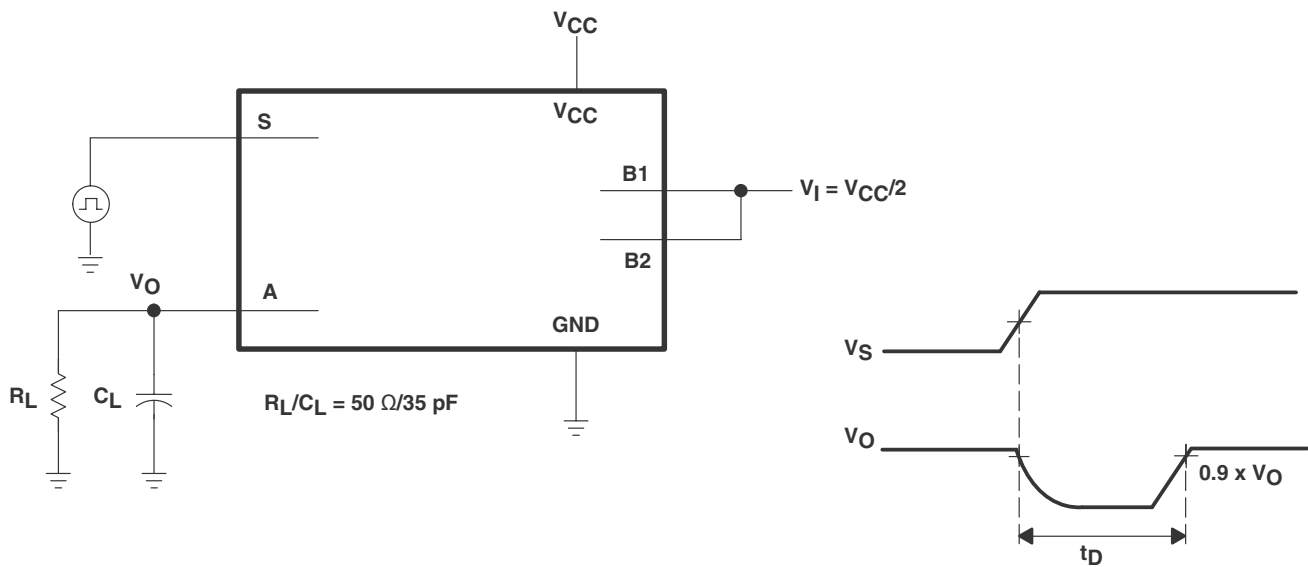
7-7. Feed Through



7-8. Charge-Injection Test



7-9. Total Harmonic Distortion



7-10. Break-Before-Make Internal Timing

## 8 Detailed Description

### 8.1 Overview

The SN74LVC1G3157 device is a single-pole double-throw (SPDT) analog switch designed for 1.65-V to 5.5-V  $V_{CC}$  operation. The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to  $V_{CC}$  (peak) to be transmitted in either direction.

### 8.2 Functional Block Diagram

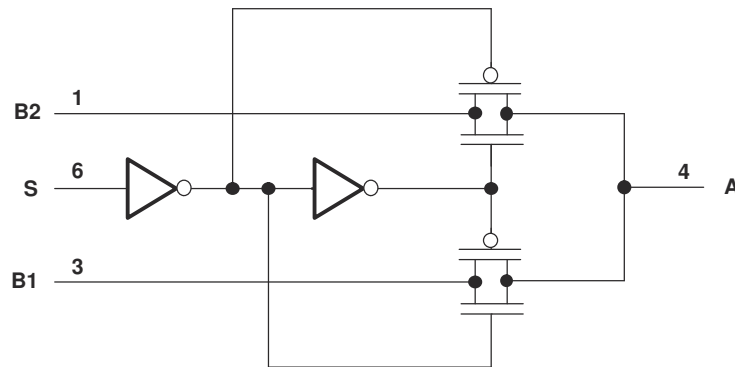


图 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

The 1.65-V to 5.5-V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

### 8.4 Device Functional Modes

表 8-1 lists the ON channel when one of the control inputs is selected.

表 8-1. Function Table

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2



## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The SN74LVC1G3157 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing, and so on. For details on the applications, see [SN74LVC1G3157](#) and [SN74LVC2G53 SPDT Analog Switches](#).

### 9.2 Typical Application

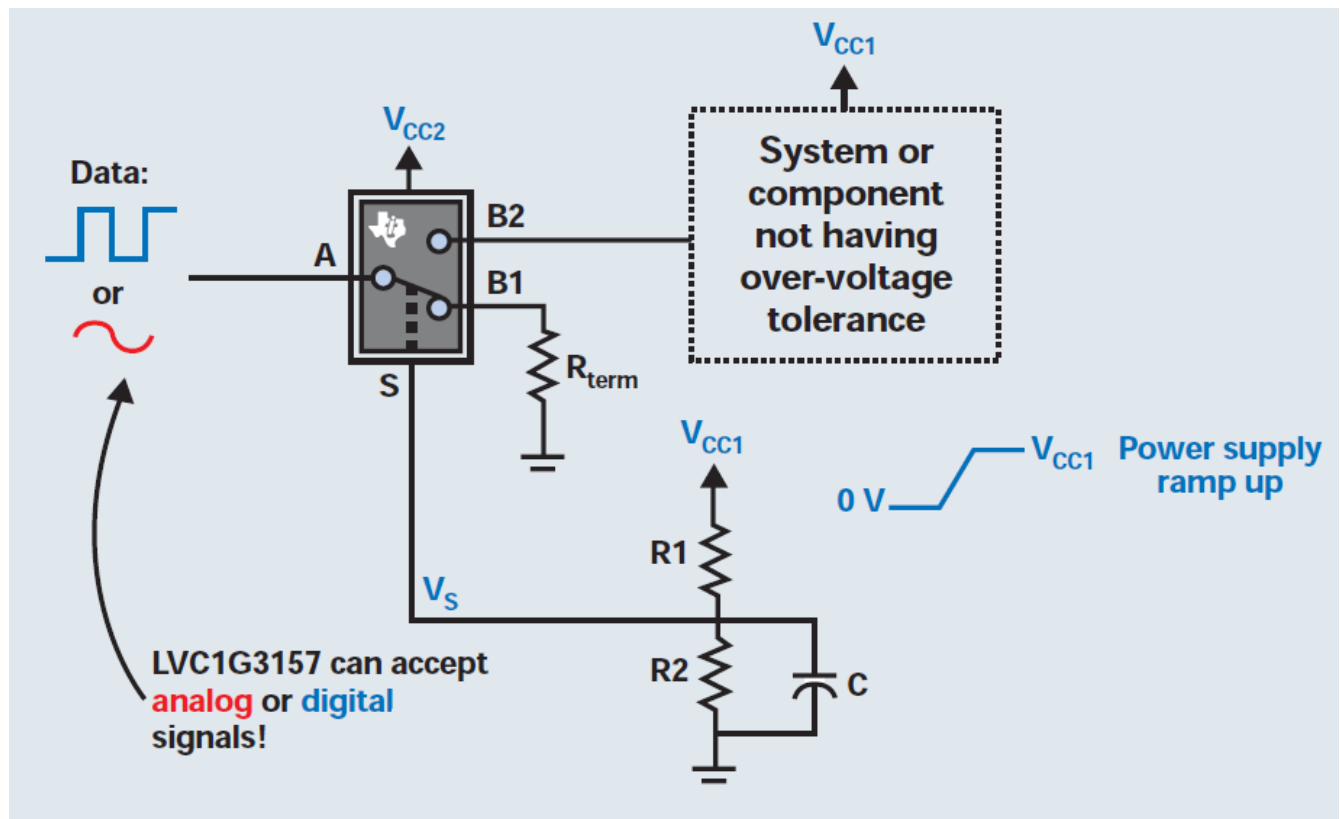


図 9-1. Typical Application Schematic

#### 9.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until  $V_{CC}$  has ramped to a level in [セクション 6.3](#) before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

### 9.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2, and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use 式 1 to calculate the time required from a transition from ground (0 V) to half the supply voltage (VCC1/2).

$$\text{Set} \left( \frac{R2}{R1 + R2} \times V_{CC1} > V_{IH} \right) \text{ of the select pin} \quad (1)$$

Choose Rs and C to achieve the desired delay.

When  $V_S$  goes high, the signal will be passed.

### 9.2.3 Application Curve

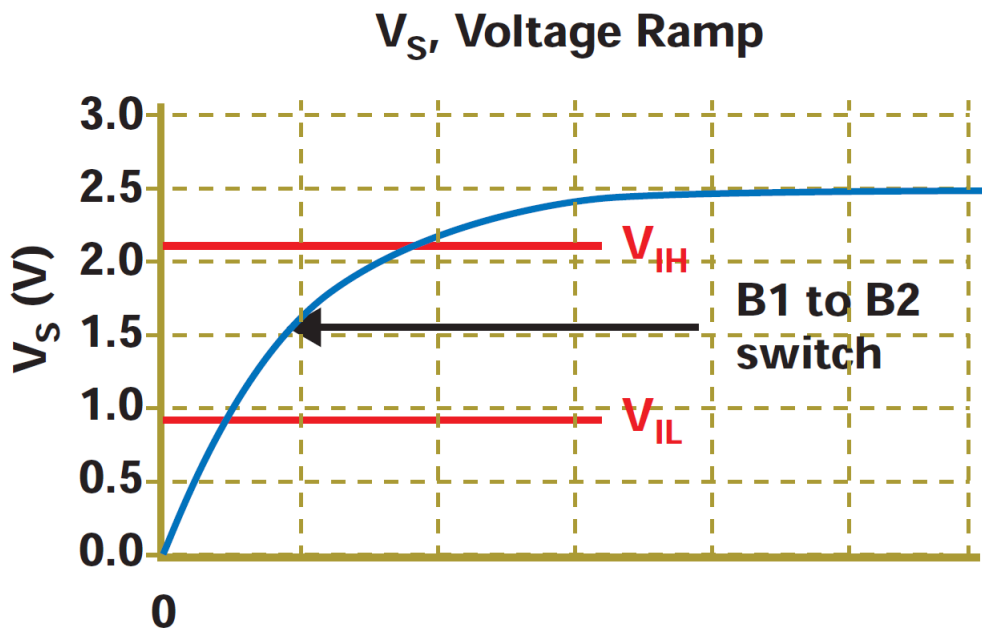


图 9-2.  $V_S$  Voltage Ramp

## 10 Power Supply Recommendations

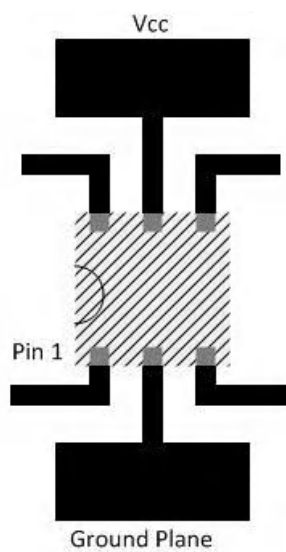
Most systems have a common 3.3-V or 5-V rail that can supply the  $V_{CC}$  pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

## 11 Layout

### 11.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either  $50\ \Omega$  or  $75\ \Omega$ , as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

### 11.2 Layout Example



11-1. Recommended Layout Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on [Subscribe to updates](#) to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G3157DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S	Samples
SN74LVC1G3157DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)	Samples
SN74LVC1G3157DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)	Samples
SN74LVC1G3157DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DTBR	ACTIVE	X2SON	DTB	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X	Samples
SN74LVC1G3157YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :**

- Automotive : [SN74LVC1G3157-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	180.0	9.5	0.94	1.13	0.41	2.0	8.0	Q2
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS

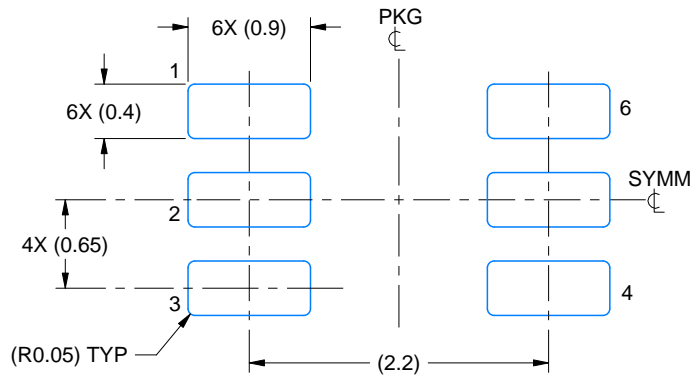


\*All dimensions are nominal

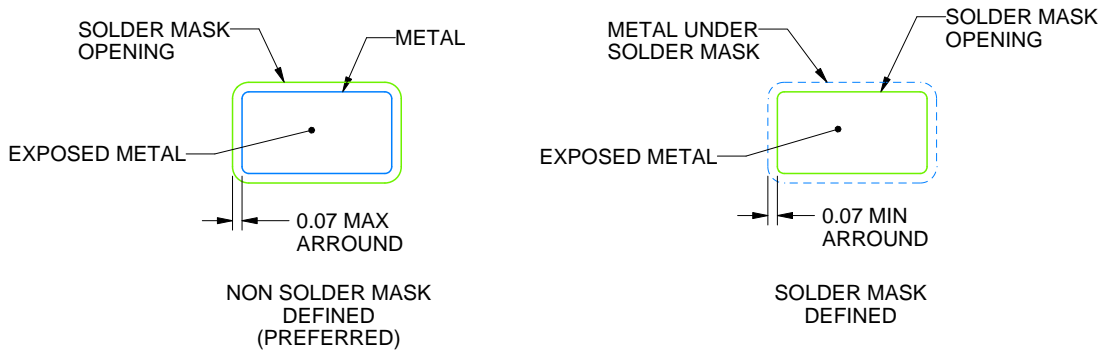
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G3157DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	189.0	185.0	36.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0







LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

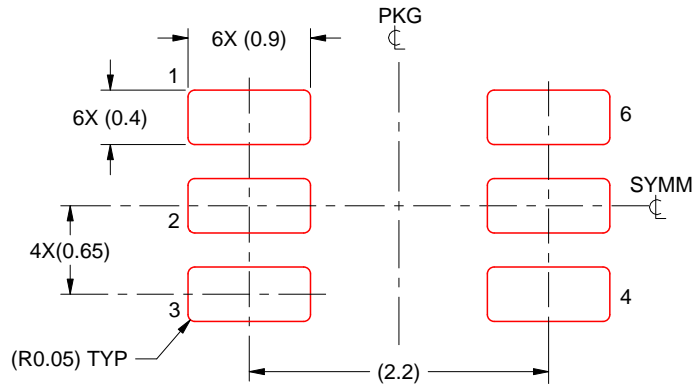


SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

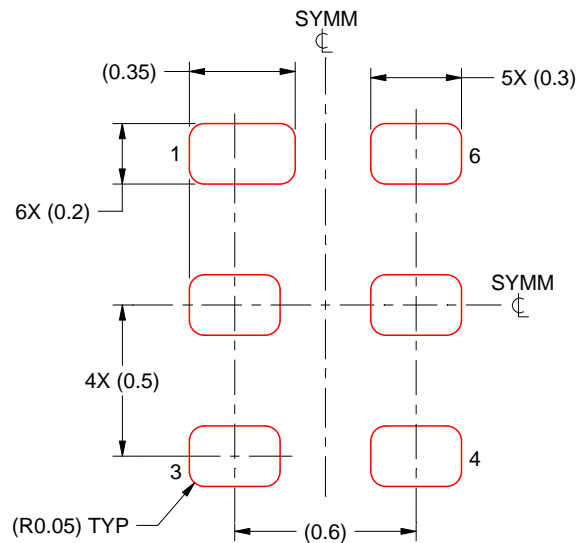
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



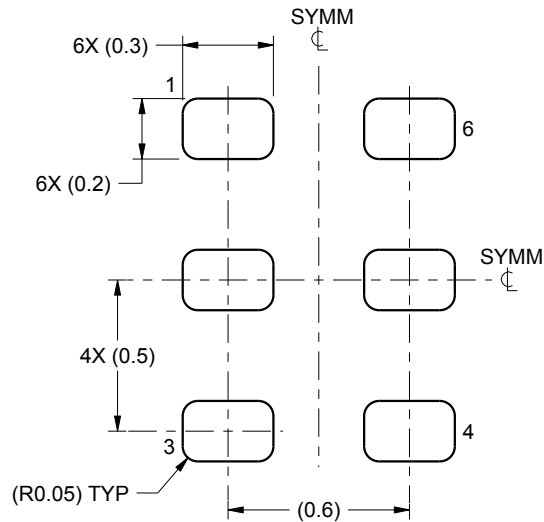


# EXAMPLE BOARD LAYOUT

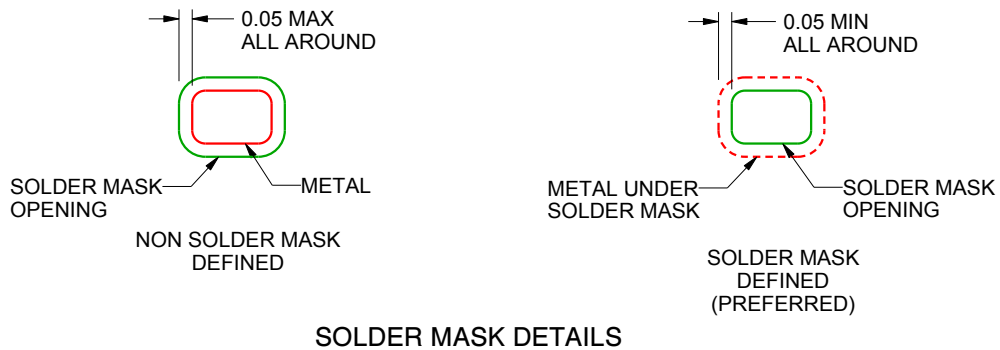
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

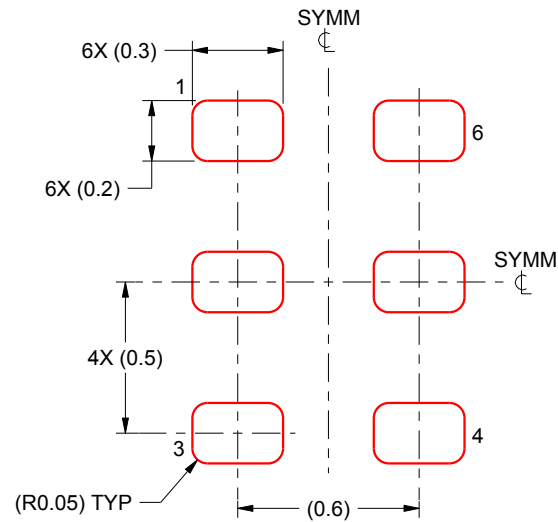
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

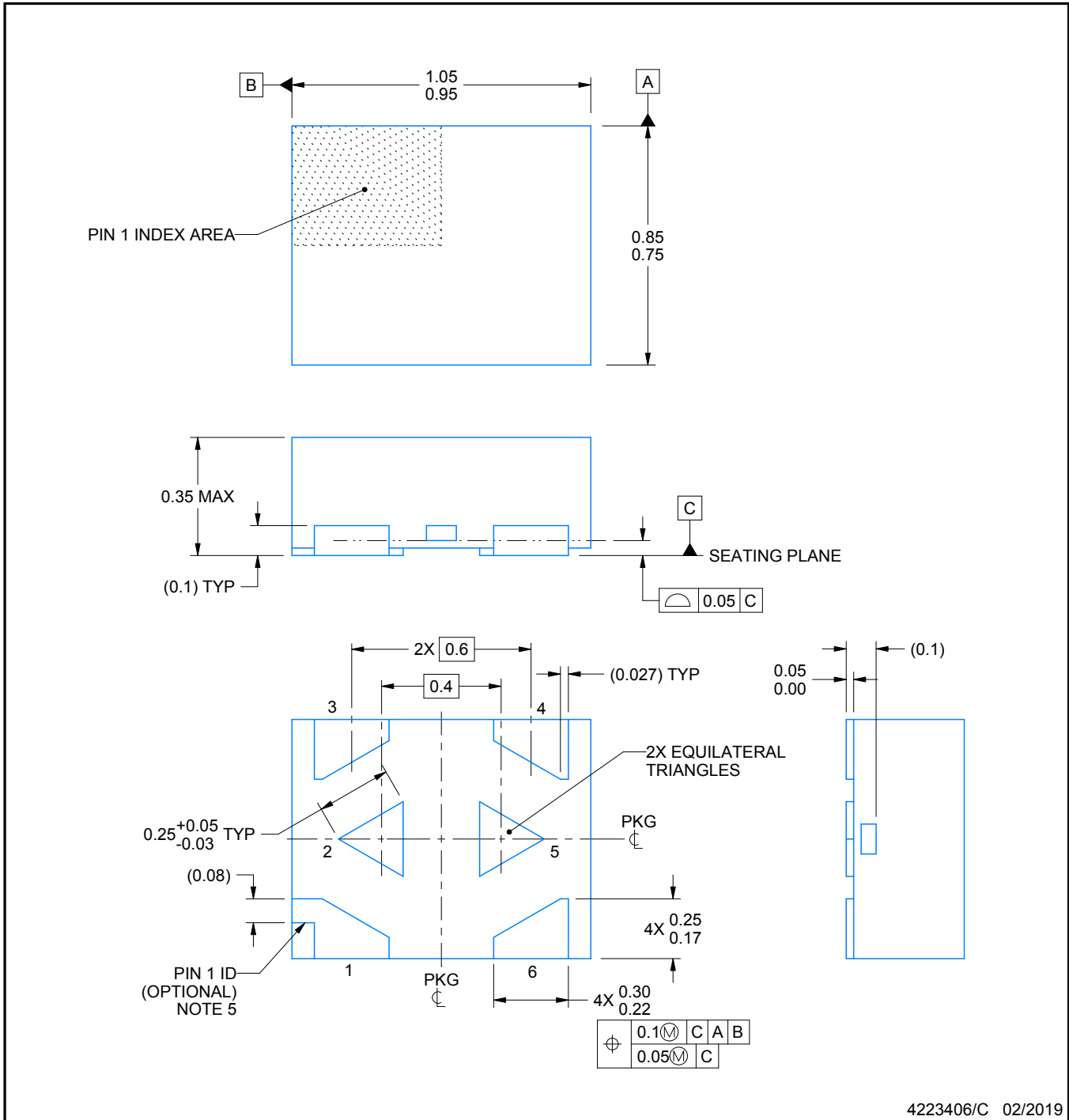
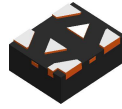


SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

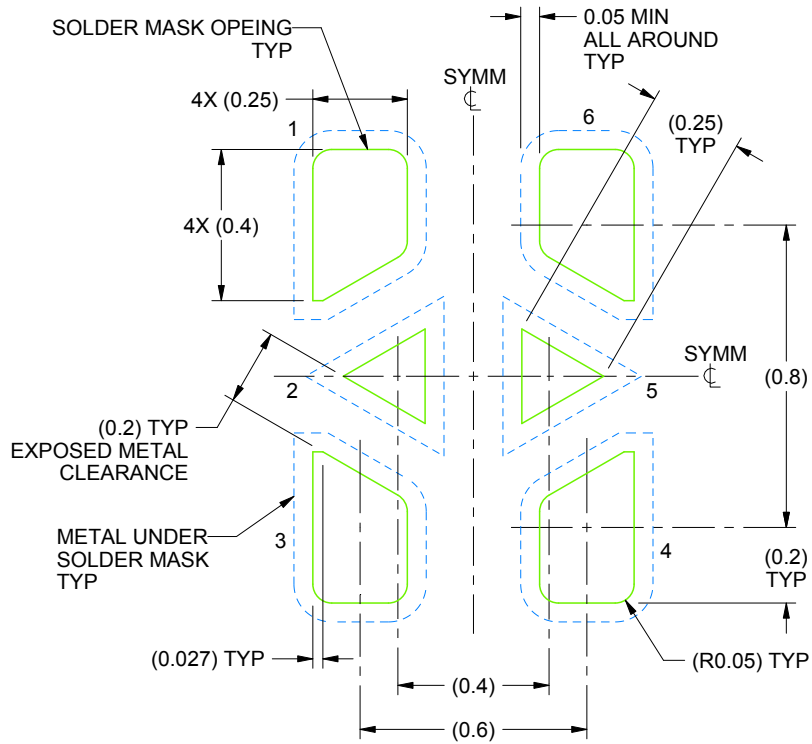
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

# EXAMPLE BOARD LAYOUT

DTB0006A

X2SON - 0.35 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

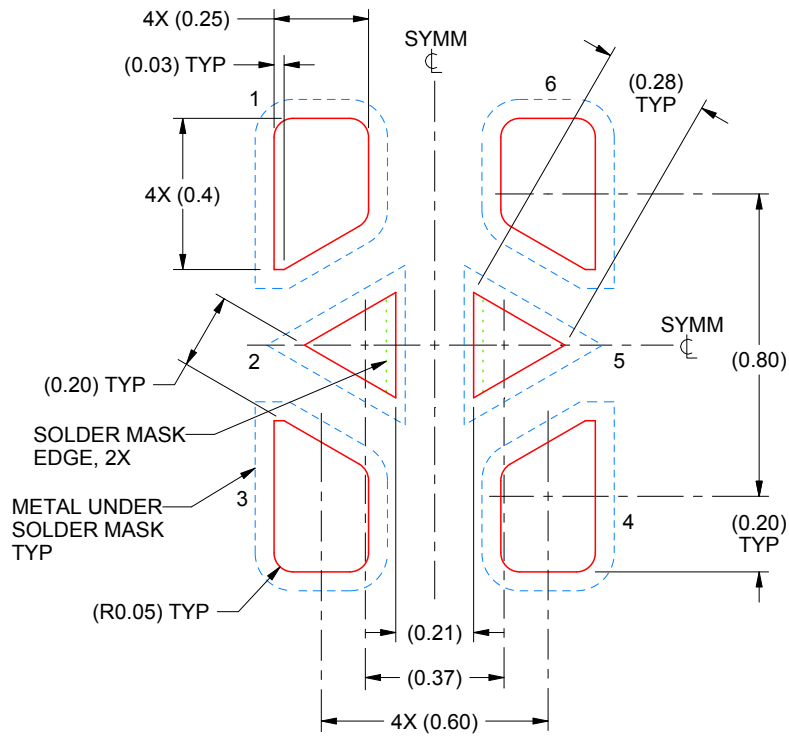
6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DTB0006A

X2SON - 0.35 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



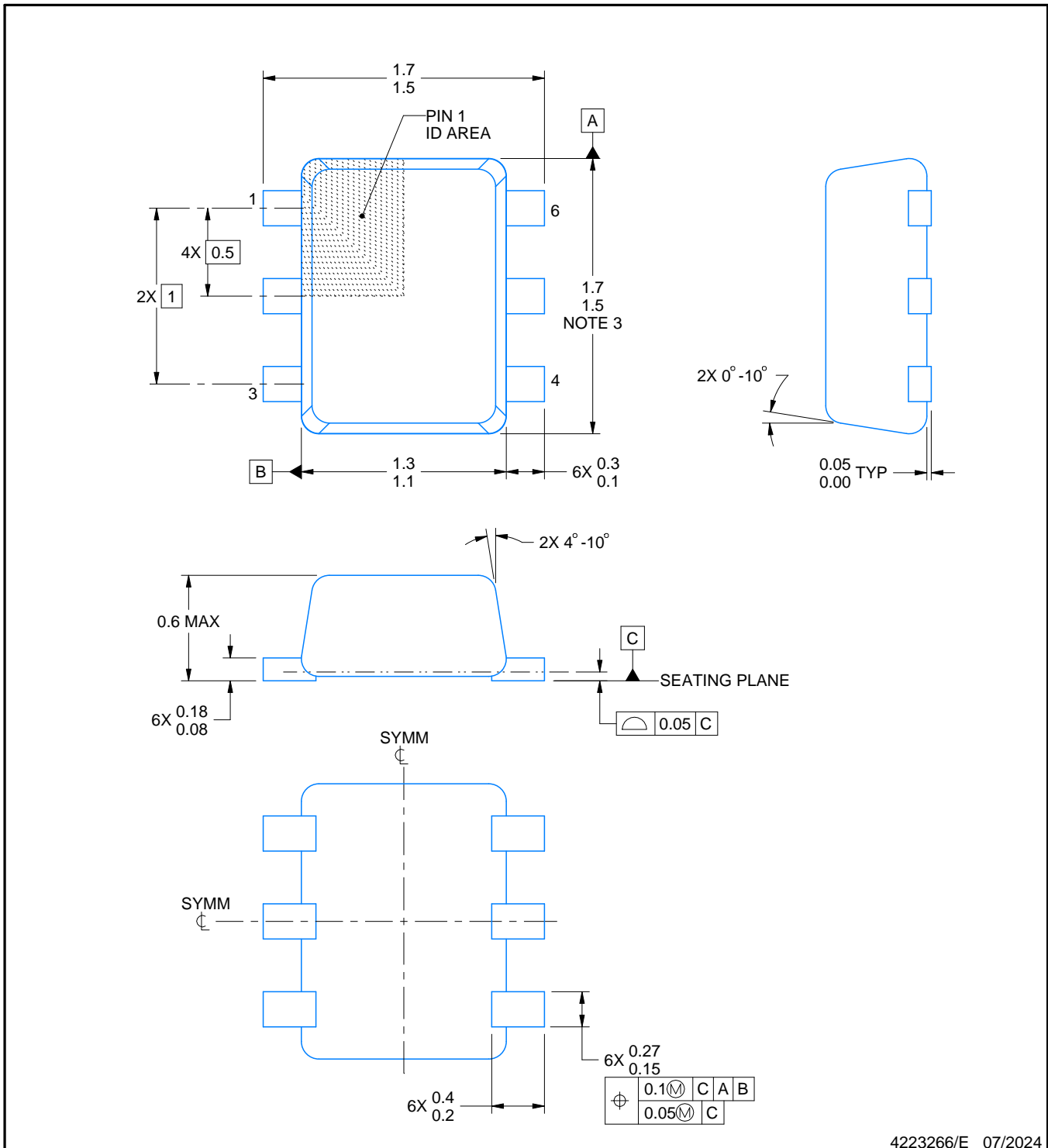
# DRL0006A



# PACKAGE OUTLINE

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/E 07/2024

### NOTES:

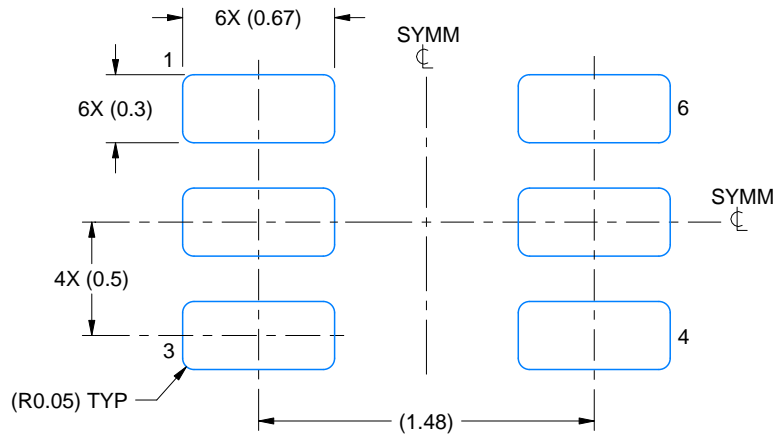
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

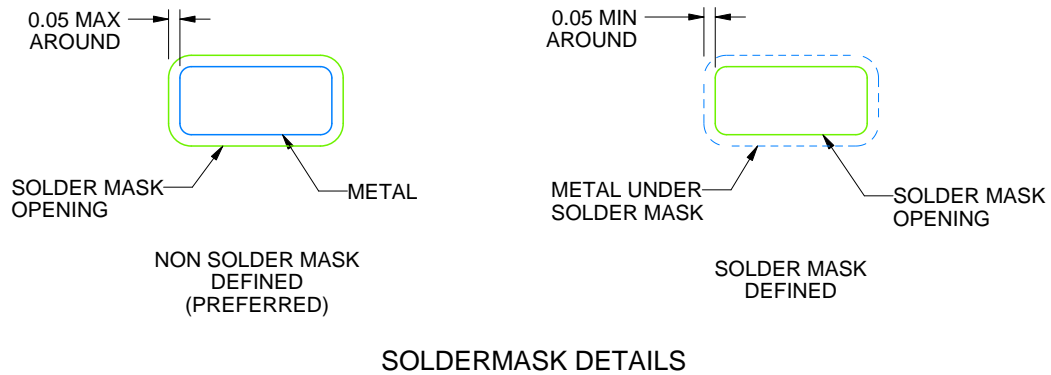
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

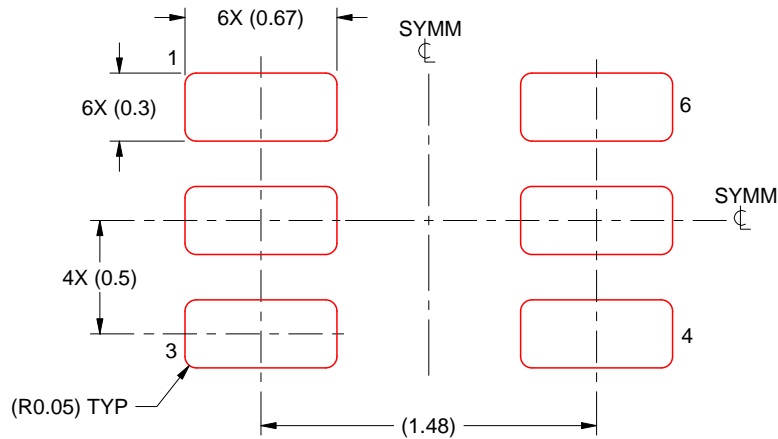
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# DBV0006A

# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

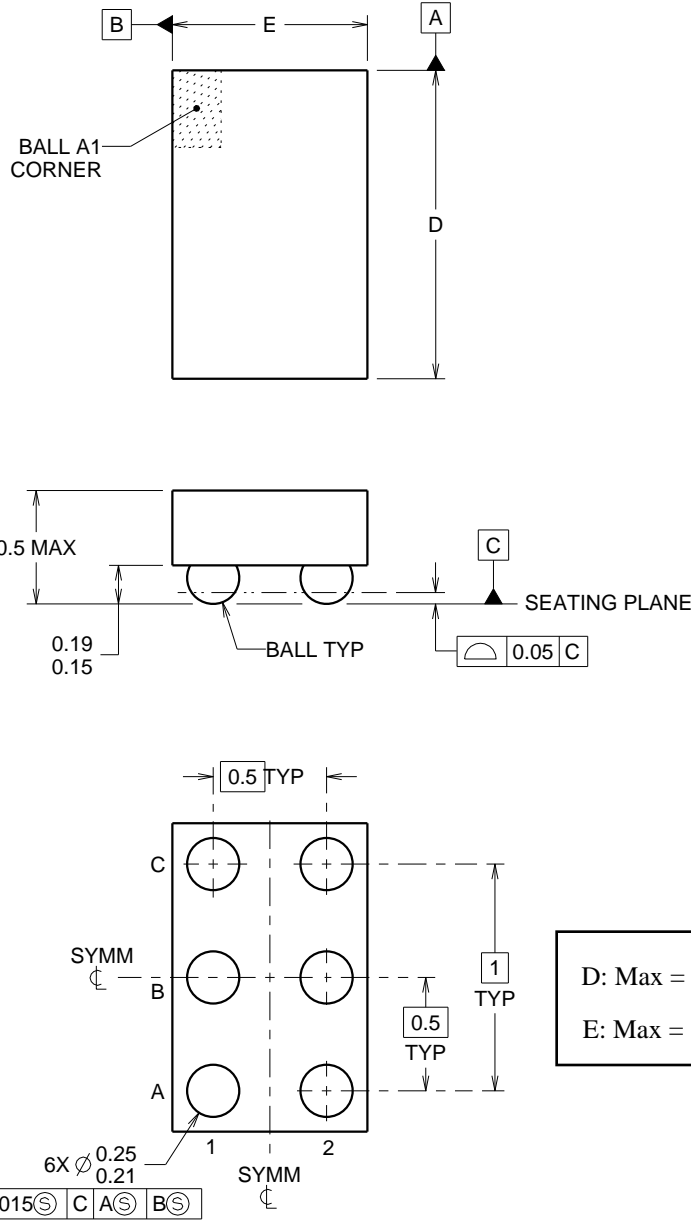
YZP0006



# PACKAGE OUTLINE

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



<p>D: Max = 1.418 mm, Min = 1.357 mm</p> <p>E: Max = 0.918 mm, Min = 0.857 mm</p>
---

4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

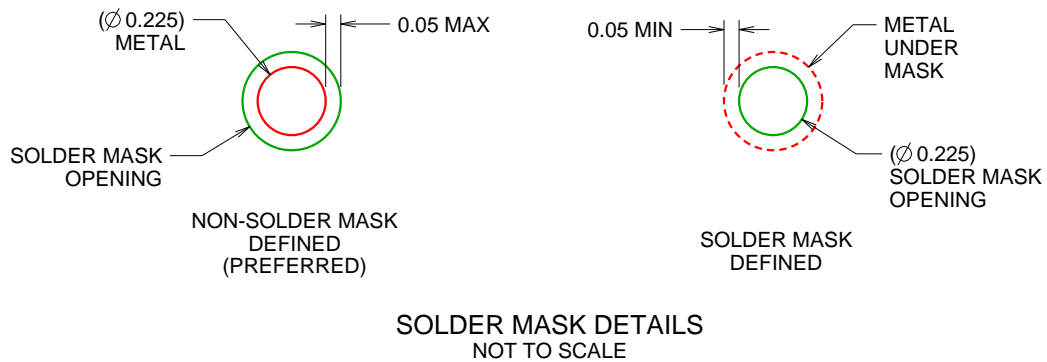
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

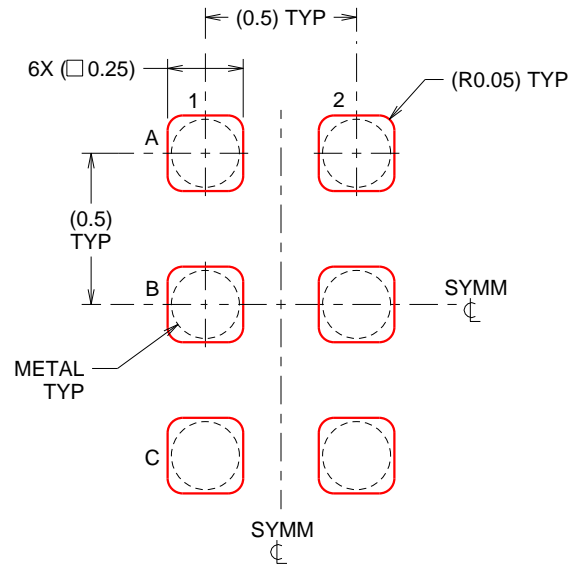


# EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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