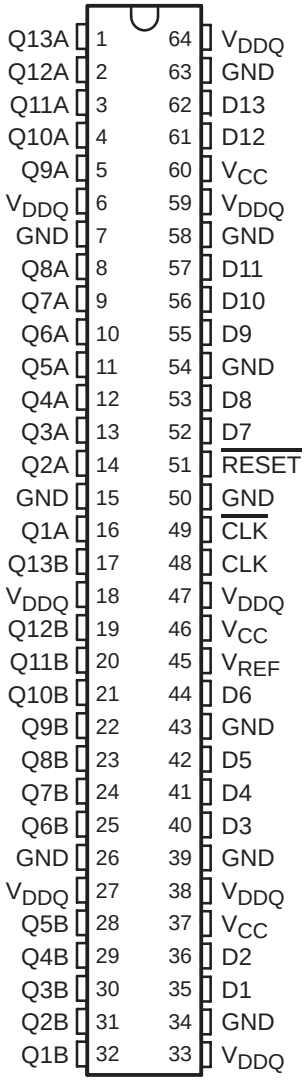
- **Member of the Texas Instruments Widebus™ Family**
- **1-to-2 Outputs to Support Stacked DDR DIMMs**
- **Supports SSTL_2 Data Inputs**
- **Outputs Meet SSTL_2 Class II Specifications**
- **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
- **Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input**
- **$\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
- **Pinout Optimizes DIMM PCB Layout**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DGG PACKAGE
(TOP VIEW)



description/ordering information

This 13-bit to 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The SN74SSTV16859 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN − RGQ (Tin−Pb Finish)	Tape and reel	SN74SSTV16859RGQR	SS859
	QFN − RGQ (Matte−Tin Finish)		SN74SSTV16859RGQ8	
	TSSOP − DGG	Tape and reel	SN74SSTV16859DGGR	SSTV16859

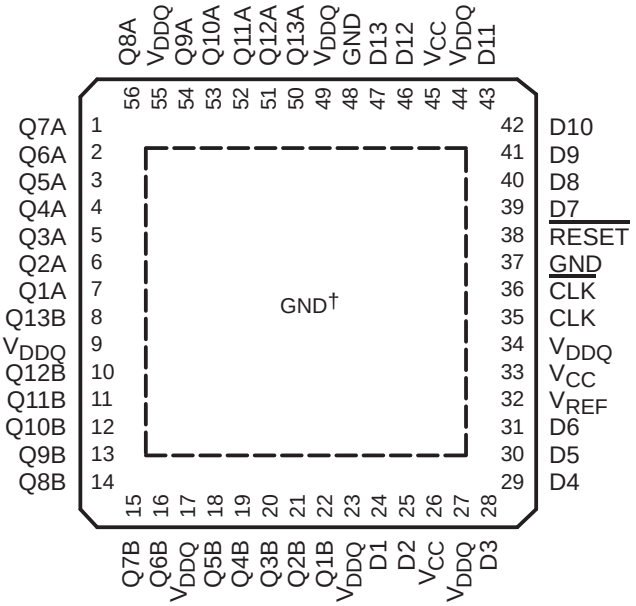
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

RGQ PACKAGE
(TOP VIEW)

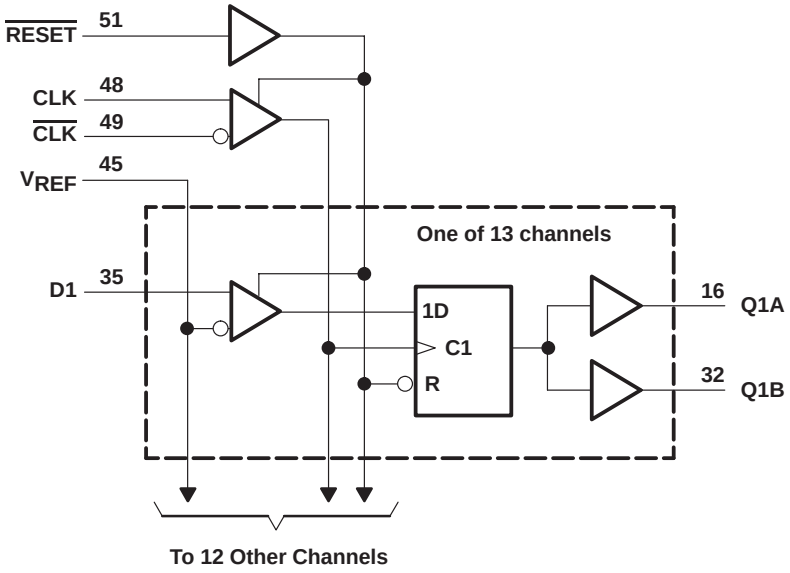


† The center die pad must be connected to GND.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

logic diagram (positive logic)



Pin numbers shown are for the DGG package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ} . . . . . −0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . −0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current through each V_{CC}, V_{DDQ}, or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 55°C/W
(see Note 4): RGQ package . . . . . 22°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage		2.3		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF} − 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs	V_{REF} + 310 mV			V
V_{IL}	AC low-level input voltage	Data inputs			V_{REF} − 310 mV	V
V_{IH}	DC high-level input voltage	Data inputs	V_{REF} + 150 mV			V
V_{IL}	DC low-level input voltage	Data inputs			V_{REF} − 150 mV	V
V_{IH}	High-level input voltage	$\overline{RESET}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{RESET}$			0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{CLK}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$	360			mV
I_{OH}	High-level output current				−20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 5: The $\overline{RESET}$ input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	TYP‡	MAX	UNIT
V_{IK}		I_I = −18 mA		2.3 V			−1.2	V
V_{OH}		I_{OH} = −100 μA		2.3 V to 2.7 V	V_{DDQ} − 0.2			V
		I_{OH} = −16 mA		2.3 V	1.95			
V_{OL}		I_{OL} = 100 μA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.3 V			0.35	
I_I	All inputs	$V_I = V_{CC}$ or GND		2.7 V			±5	μA
I_{CC}	Static standby	$\overline{RESET}$ = GND	I_O = 0	2.7 V			10	μA
	Static operating	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					40	mA
I_{CCD}	Dynamic operating − clock only	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	2.5 V		30		μA/ MHz
	Dynamic operating − per each data input	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				10		μA/ clock MHz/ D input
r_{OH}	Output high	I_{OH} = −20 mA		2.3 V to 2.7 V	7		20	Ω
r_{OL}	Output low	I_{OL} = 20 mA		2.3 V to 2.7 V	7		20	Ω
$r_{O(\Delta)}$	$\lvert r_{OH} - r_{OL} \rvert$	I_O = 20 mA, T_A = 25°C, One output		2.5 V			6	Ω
C_i§	Data inputs	$V_I = V_{REF} \pm 310$ mV		2.5 V	2.5	3	3.5	pF
	CLK, $\overline{CLK}$	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360mV			2.5	3	3.5	
	$\overline{RESET}$	$V_I = V_{CC}$ or GND				3		

† For this test condition, V_{DDQ} always is equal to V_{CC}.
‡ All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
§ Measured with 50-MHz input frequency for the QFN package and 10-MHz input frequency for the TSSOP package

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 2.5 V ± 0.2 V†		UNIT
			MIN	MAX	
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ high or low		2.5		ns
t_{act}	Differential inputs active time (see Note 6)			22	ns
t_{inact}	Differential inputs inactive time (see Note 7)			22	ns
t_{su}	Setup time, fast slew rate (see Notes 8 and 10)	Data before CLK↑, $\overline{CLK}$↓	0.75		ns
	Setup time, slow slew rate (see Notes 9 and 10)		0.9		
t_h	Hold time, fast slew rate (see Notes 8 and 10)	Data after CLK↑, $\overline{CLK}$↓	0.75		ns
	Hold time, slow slew rate (see Notes 9 and 10)		0.9		

† For this test condition, V_{DDQ} always is equal to V_{CC}.

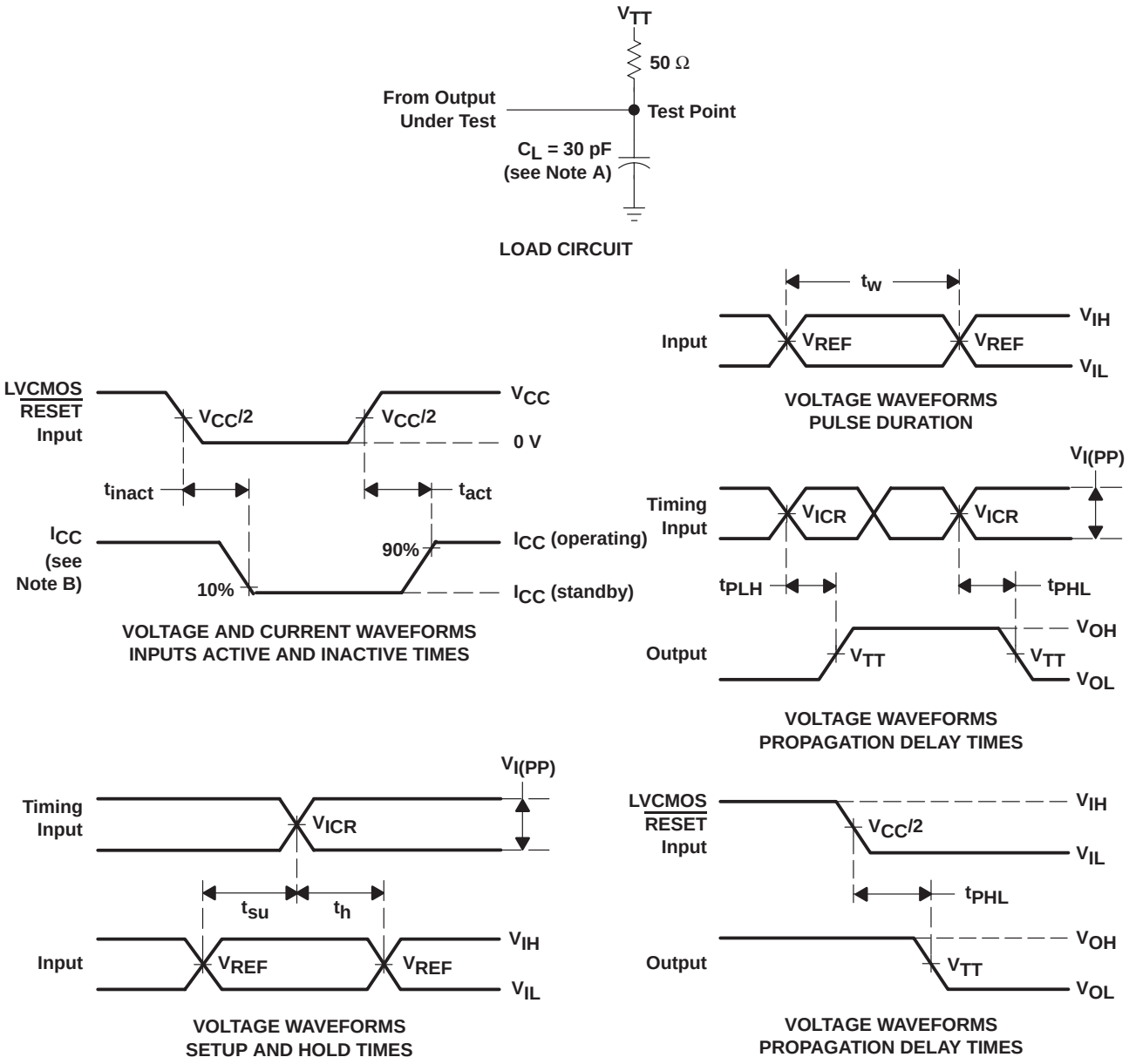
NOTES: 6. V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after $\overline{RESET}$ is taken high.
7. V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{RESET}$ is taken low.
8. For data signal input slew rate ≥ 1 V/ns
9. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns
10. CLK, $\overline{CLK}$ signals input slew rates are ≥ 1 V/ns.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V†		UNIT
			MIN	MAX	
f_{max}			200		MHz
t_{pd}	CLK and $\overline{CLK}$	Q	1.1	2.8	ns
t_{PHL}	$\overline{RESET}$	Q		5	ns

† For this test condition, V_{DDQ} always is equal to V_{CC}.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time, with one transition per measurement.
E. $V_{TT} = V_{REF} = V_{DDQ}/2$
F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ − 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74SSTV16859DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTV16859	Samples
SN74SSTV16859RGQ8	OBSOLETE	VQFN	RGQ	56		TBD	Call TI	Call TI	0 to 70	SS859	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

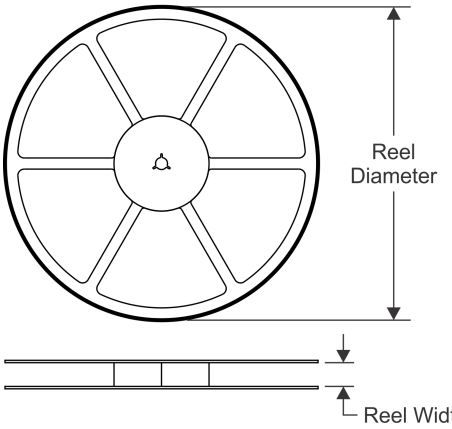
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

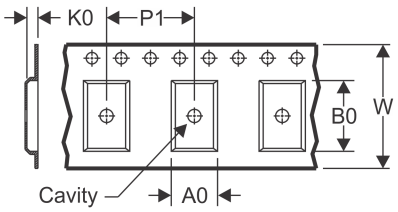
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

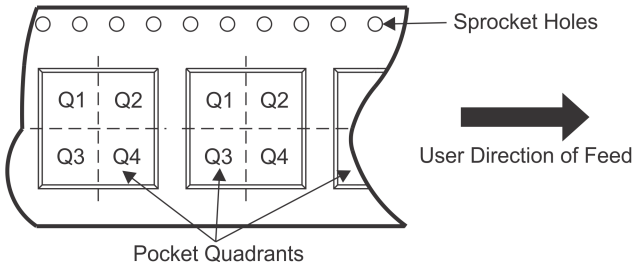


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

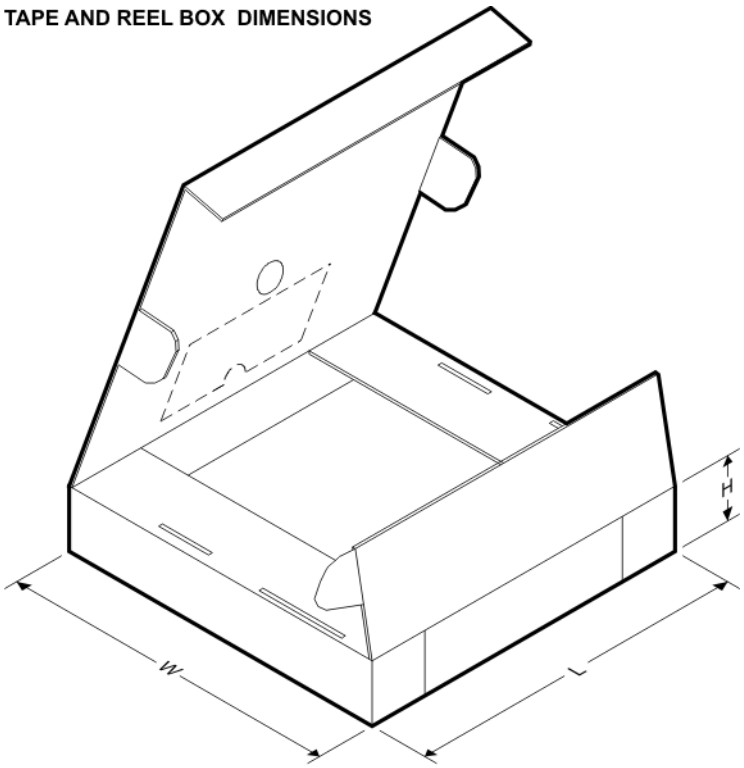
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTV16859DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

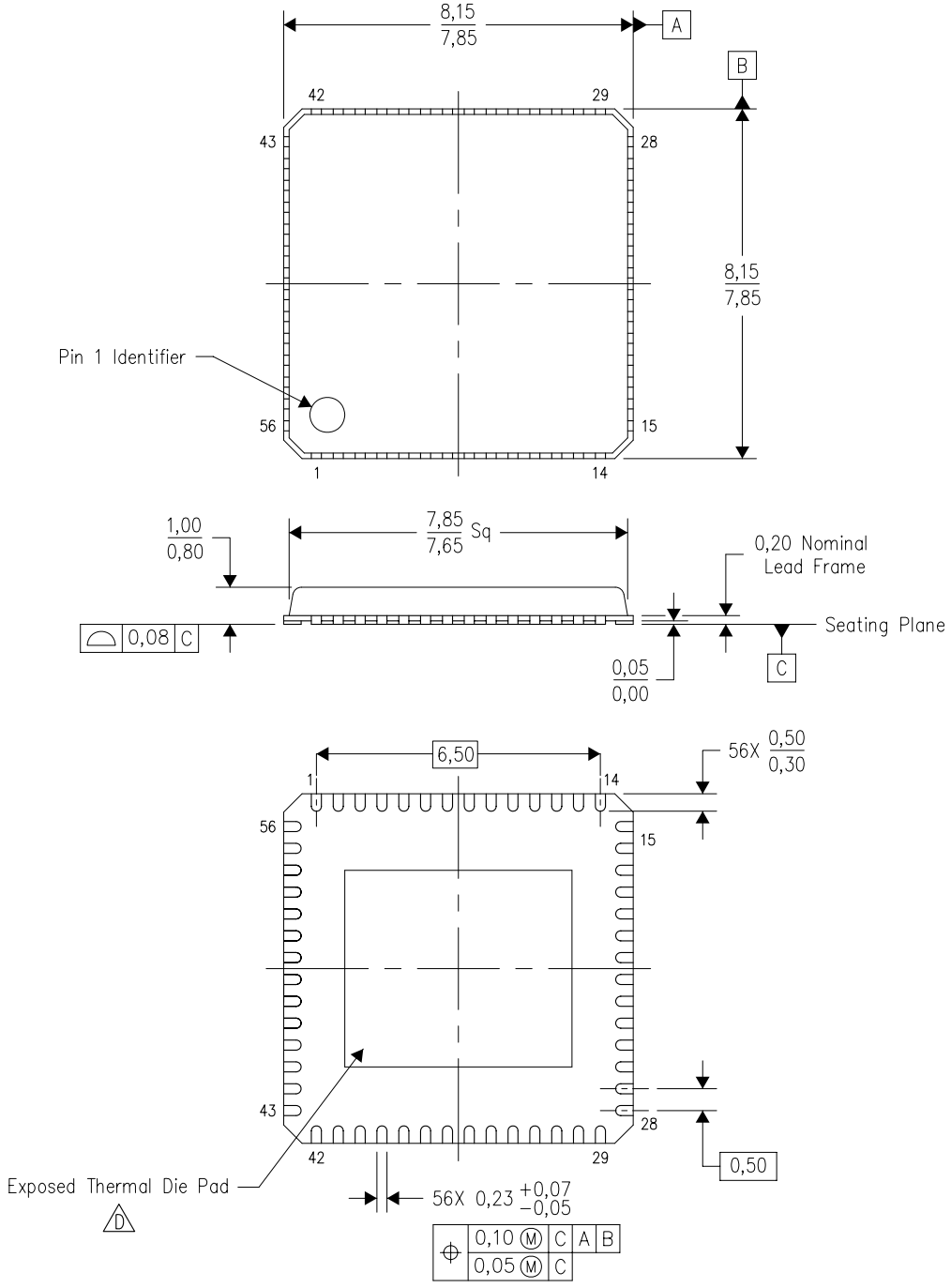
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTV16859DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0

RGQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

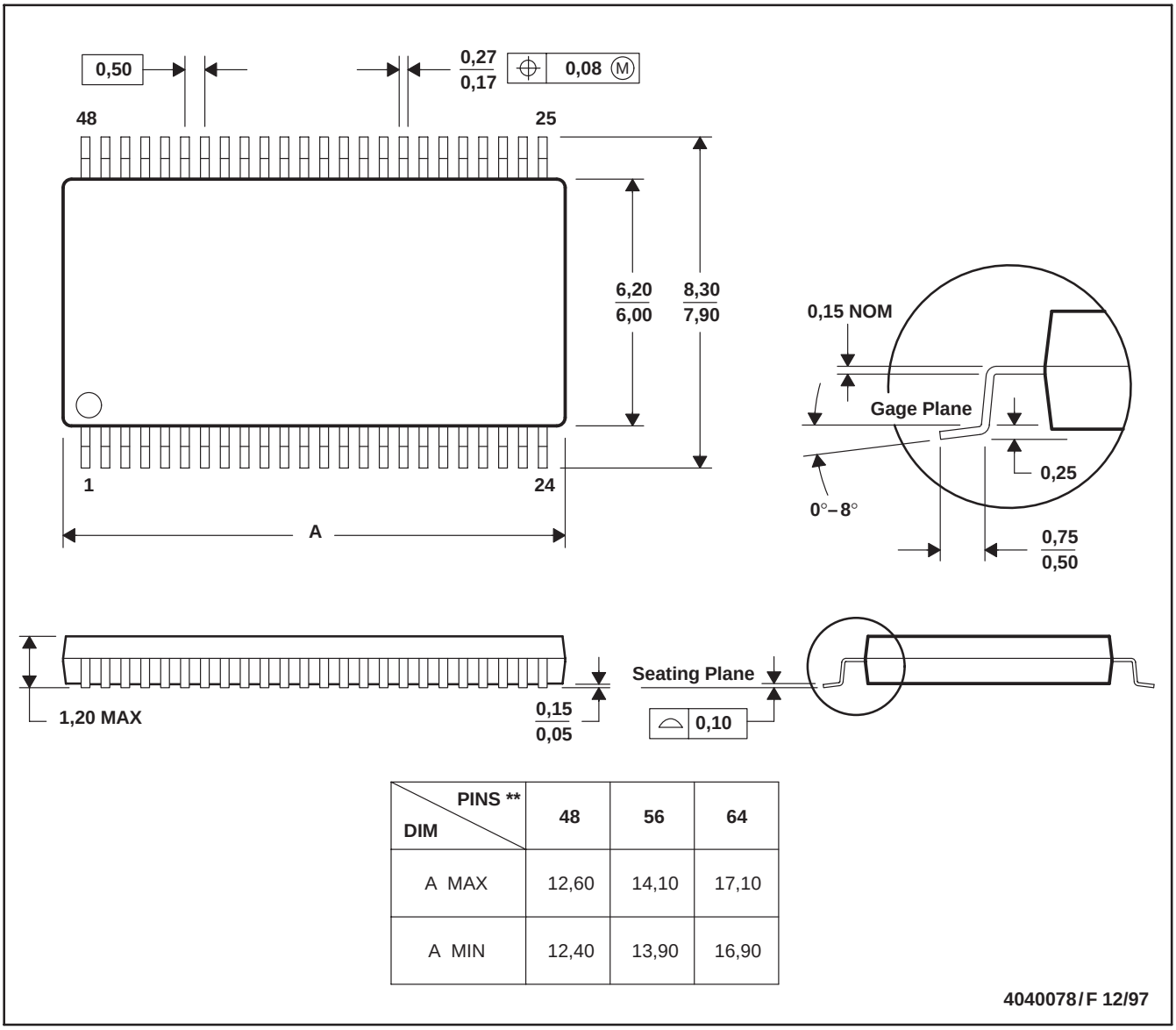


4203438/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation VLLD–2.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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