

## SNx5173 クワッド差動ラインレシーバ

### 1 特長

- TIA/EIA-422-B、TIA/EIA-423-B、および TIA/EIA-485-A と ITU 勧告 V.10、V.11、X.26、X.27 の要件を満たす、または超える
- ノイズの多い環境の、長いバス・ラインでのマルチポイント・バス伝送用に設計
- 3 ステート出力
- 同相入力電圧範囲: -12V~12V
- 入力感度: ±200mV
- 入力ヒステリシス: 50mV (標準値)
- 高い入力インピーダンス: 12kΩ (最小値)
- 5V 単一電源で動作
- 低消費電力要件
- AM26LS32 のピン互換代替品

### 2 アプリケーション

- モータ・ドライブ
- ファクトリ・オートメーション / 制御

### 3 概要

SN55173 および SN75173 は、3 ステート出力を搭載したモノシック・クワッド差動ライン・レシーバです。これらのデバイスは、TIA/EIA-422-B、TIA/EIA-423-B、TIA/EIA-485-A、およびいくつかの ITU 勧告の要件を満たすよう設計されています。これらの規格は、最大 10 Mbps の

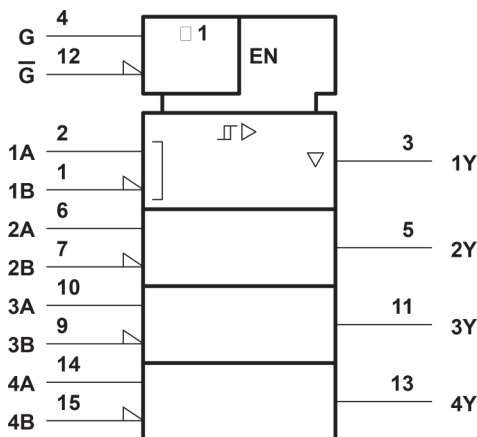
速度で平衡マルチポイント・バス伝送を実現するためのものです。4 つのレシーバは 2 つの論理和イネーブル入力と共有しています。1 つは High のとき、もう 1 つは Low のときアクティブです。これらのデバイスは、高い入力インピーダンス、ノイズ耐性を高める入力ヒステリシス、-12V~12V の同相入力電圧範囲にわたって ±200mV の入力感度を特長としています。フェイルセーフ設計により、入力が開路の場合、出力は常に High になります。SN65173 および SN75173 は、SN75172 または SN75174 クワッド差動ライン・ドライバと組み合わせると、最適な性能を発揮するよう設計されています。

SN55173 は -55°C~125°C の軍用温度範囲全体での動作が規定されています。SN75173 は 0°C~70°C での動作が規定されています。

#### パッケージ情報

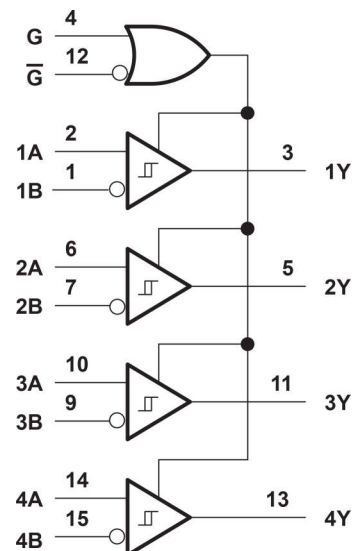
部品番号	パッケージ (1)	パッケージ・サイズ (2)
SN55173	J (CDIP, 16)	6.92mm × 19.56mm
	FK (LCCC, 20) <sup>(3)</sup>	8.89mm × 8.89mm
SN75173	D (SOIC, 16)	9.9mm × 6mm
	N (PDIP, 16)	19.3 × 9.4mm
	NS (SO, 16)	10.2 × 7.8mm

- (1) 詳細については、[セクション 11](#) を参照してください。
- (2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 新規設計には推奨しません。



- この記号は ANSI/IEEE 規格 91-1984 と IEC Publication 617-12 に準拠しています。ここに示すピン番号は、D、J、N の各パッケージのものであります。
- ここに示すピン番号は、D、J、N の各パッケージのものであります。

#### 論理記号

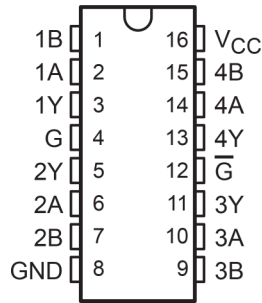


#### 論理図 (正論理)

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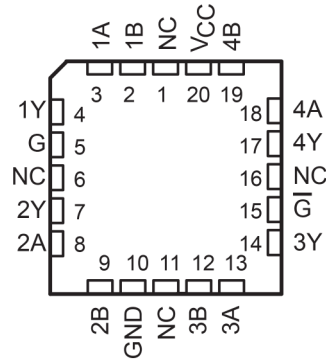
## 4 Pin Configuration and Functions



**図 4-1. SN55173: J Package  
 SN75173: D, N or NS Package  
 (Top View)**

**表 4-1. Pin Functions**

PIN		TYPE#non e#	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
G	4	I	Active High Enable
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
Ḡ	12	I	Active Low Enable
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V <sub>CC</sub>	16	PWR	Device V <sub>CC</sub> (4.75 V to 5.25 V)



NC—No internal connection

**图 4-2. SN55173: FK Package (Top View)**

A. The SN55173 FK package is not recommended for new designs.

**表 4-2. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
NC	1, 6, 11, 16	--	No Connect
1B	2	I	Differential Receiver Inverting Input
1A	3	I	Differential Receiver Non-Inverting Input
1Y	4	O	Single Ended Output
G	5	I	Active High Enable
2Y	7	O	Single Ended Output
2A	8	I	Differential Receiver Non-Inverting Input
2B	9	I	Differential Receiver Inverting Input
GND	10	GND	Device GND
3B	12	I	Differential Receiver Inverting Input
3A	13	I	Differential Receiver Non-Inverting Input
3Y	14	O	Single Ended Output
Ḡ	15	I	Active Low Enable
4Y	17	O	Single Ended Output
4A	18	I	Differential Receiver Non-Inverting Input
4B	19	I	Receiver Inverting Input
V <sub>CC</sub>	20	PWR	Device VCC

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$ <sup>(2)</sup>	Supply voltage				V
$V_I$	Input voltage (A or B inputs)			± 25	V
$V_{ID}$ <sup>(3)</sup>	Differential input voltage			± 25	V
$V_{I(EN)}$	Enable input voltage				V
$I_{OL}$	Low-level output current			50	mA
	Continuous total dissipation		See Dissipation Rating Table		
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds:	D or N package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds:	J package		300	°C
$T_{stg}$	Storage temperature range		65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input voltage, are with respect to network ground terminal.
- (3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

### 5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11 mW/°C	880 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	275 mW

### 5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	SN55173	4.5	5	5.5	V
	SN75173	4.75	5	5.25	V
Common-mode input voltage, $V_{IC}$				± 12	V
Differential input voltage, $V_{ID}$				± 12	V
High-level enable-input voltage, $V_{IH}$		2			V
Low-level enable-input voltage, $V_{IL}$				0.8	V
High-level output current, $I_{OH}$				– 400	µA
Low-level output current, $I_{OL}$				16	mA
Operating free-air temperature, $T_A$	SN55173	– 55		125	°C
	SN75173	0		70	

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D (SOIC)	N (PDIP)	NS (SOP)	J (CDIP)	UNIT
		16-PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	88.5	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	54.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	40.6	50.7	42.1	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	10.4	27.5	13.5	22.9	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	42.8	40.3	50.3	41.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
VIT+	Positive-going input threshold voltage	$V_O = 2.7\text{ V}$ ,	$I_O = -0.4\text{ mA}$				0.2	V
VIT-	Negative-going input threshold voltage	$V_O = 0.5\text{ V}$ ,	$I_O = 16\text{ mA}$		-0.2 <sup>(2)</sup>			V
V <sub>hys</sub>	Hysteresis ( $V_{IT+} - V_{IT-}$ )	See <a href="#">Figure 5-1</a>				50		mV
V <sub>IK</sub>	Enable-input clamp voltage	$I_I = -18\text{ mA}$					-1.5	V
V <sub>OH</sub>	High-level output voltage	$V_{ID} = 200\text{ mV}$ ,	$I_{OH} = -400\text{ }\mu\text{A}$	SN55173	2.5			V
				SN75173	2.7			V
V <sub>OL</sub>	Low-level output voltage	$V_{ID} = -200\text{ mV}$ ,	See <a href="#">Figure 6-1</a>	$I_{OL} = 8\text{ mA}$			0.45	V
				$I_{OL} = 16\text{ mA}$			0.5	
IOZ	High-impedance-state output current	$V_O = 0.4\text{ V to }2.4\text{ V}$					±20	μA
I <sub>I</sub>	Line input current	Other input at 0 V,	See <a href="#">Note 3</a>	$V_I = 12\text{ V}$			1	mA
				$V_I = -7\text{ V}$			-0.8	
I <sub>IH</sub>	High-level enable-input current	$V_{IH} = 2.7\text{ V}$					20	μA
I <sub>IL</sub>	Low-level enable-input current	$V_{IL} = 0.4\text{ V}$					-100	μA
r <sub>i</sub>	Input resistance					12		kΩ
IOS	Short-circuit output current					-15	-85	mA
ICC	Supply current	Outputs disabled					70	mA

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

(3) Refer to TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.

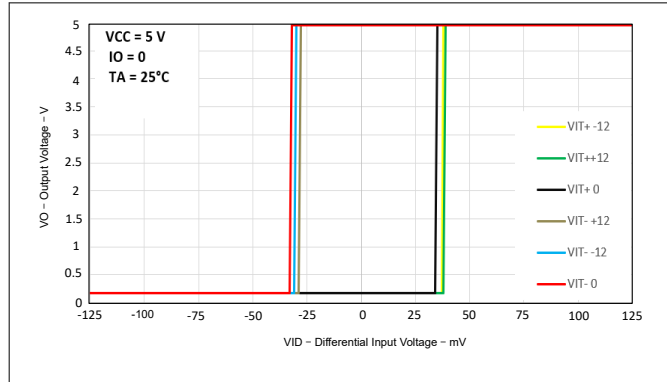
## 5.6 Switching Characteristics

 $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ 

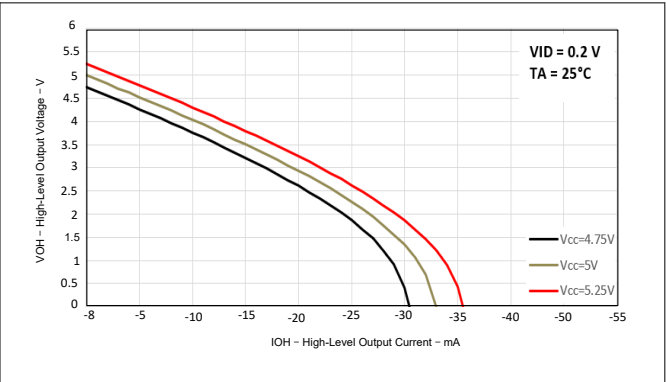
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$V_{ID} = -1.5\text{ V to }1.5\text{ V},$ $C_L = 15\text{ pF},$ See <a href="#">6-1</a>		20	35	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output			22	35	ns
$t_{PZH}$	Output enable time to high level	$C_L = 15\text{ pF},$ See <a href="#">6-2</a>		17	22	ns
$t_{PZL}$	Output enable time to low level	$C_L = 15\text{ pF},$ See <a href="#">6-3</a>		20	25	ns
$t_{PHZ}$	Output disable time from high level	$C_L = 5\text{ pF},$ See <a href="#">6-2</a>		21	30	ns
$t_{PLZ}$	Output disable time from low level	$C_L = 5\text{ pF},$ See <a href="#">6-3</a>		30	40	ns

## 5.7 Typical Characteristics

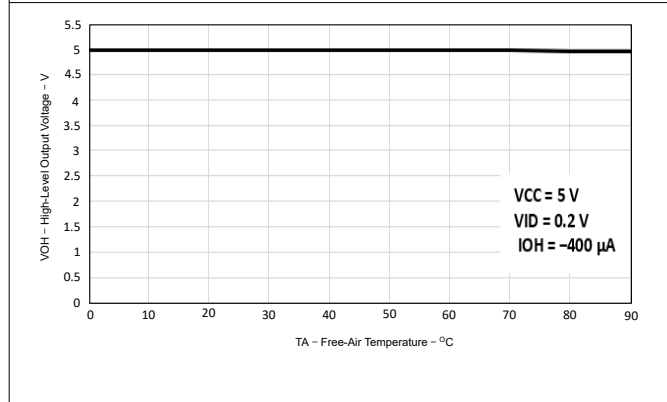
Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.



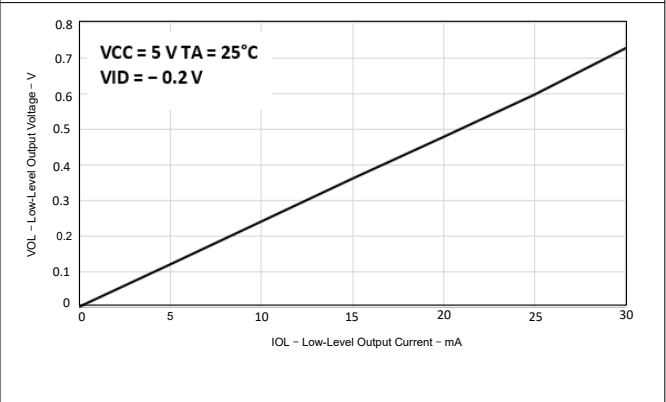
**图 5-1. Output Voltage vs Differential Input Voltage**



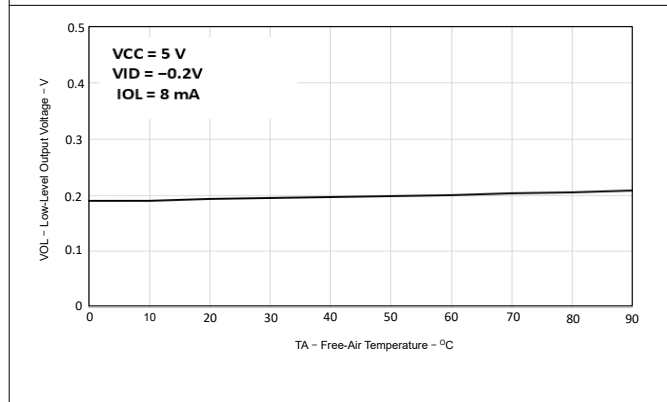
**图 5-2. High-level Output Voltage vs High-level Output Current**



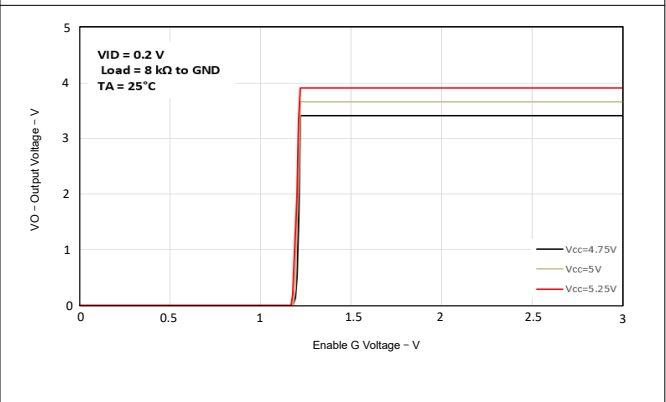
**图 5-3. High-level Output Voltage vs Free-air Temperature 5**



**图 5-4. Low-level Output Voltage vs Low-level Output Current**

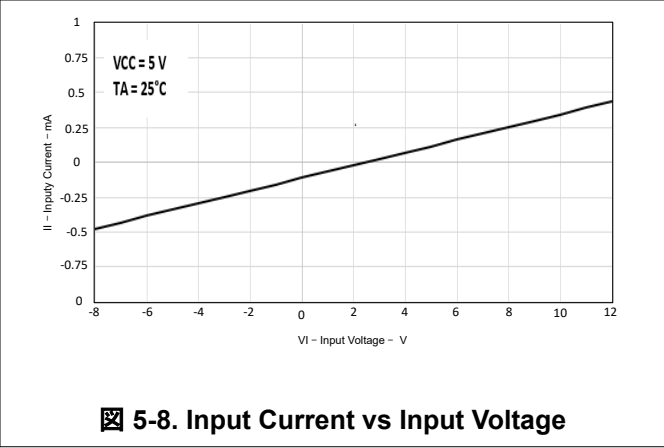
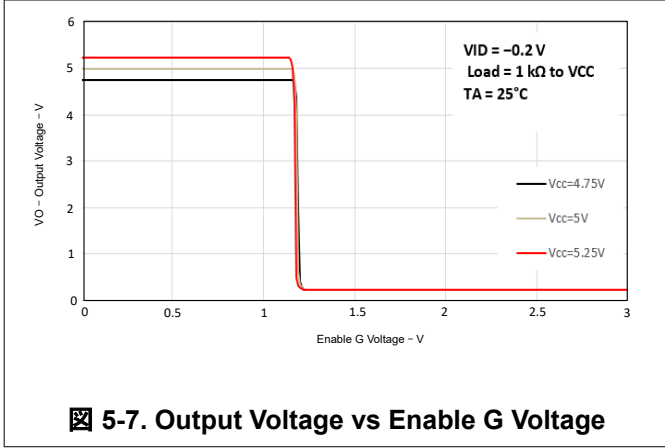


**图 5-5. Low-level Output Voltage vs Free-air Temperature**

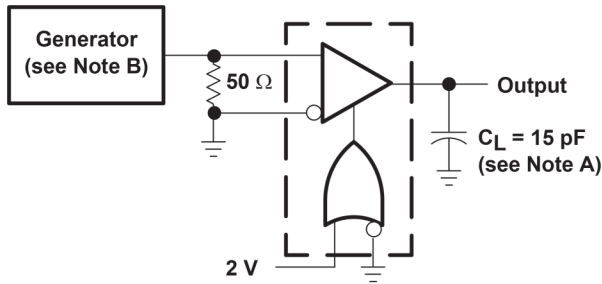


**图 5-6. Output Voltage vs Enable G Voltage**

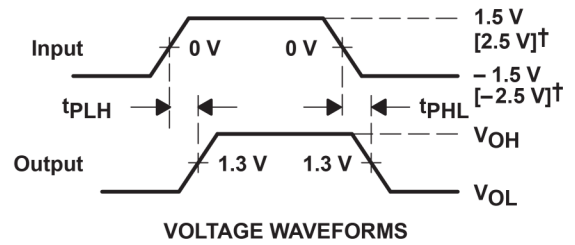




## 6 Parameter Measurement Information

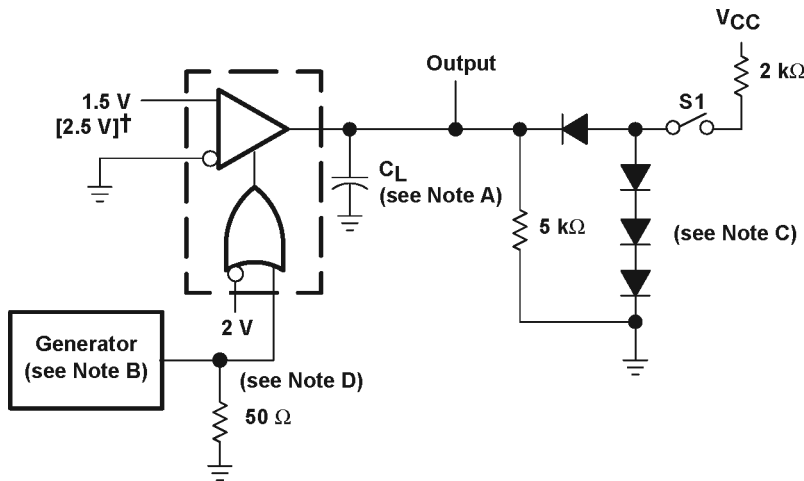


TEST CIRCUIT

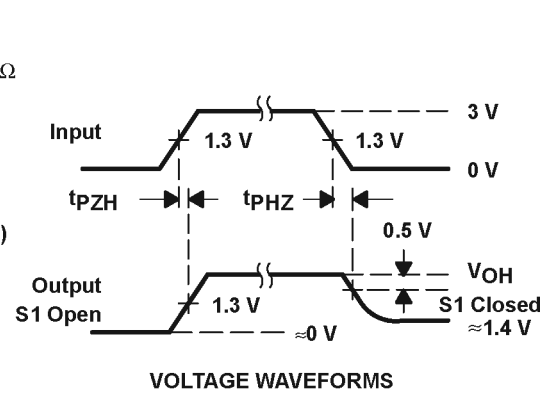


- A. † Voltage for the SN55173 only.
- B.  $C_L$  includes probe and jig capacitance.
- C. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

图 6-1.  $t_{PLH}$ ,  $T_{PHL}$  Test Circuit and Voltage Waveforms

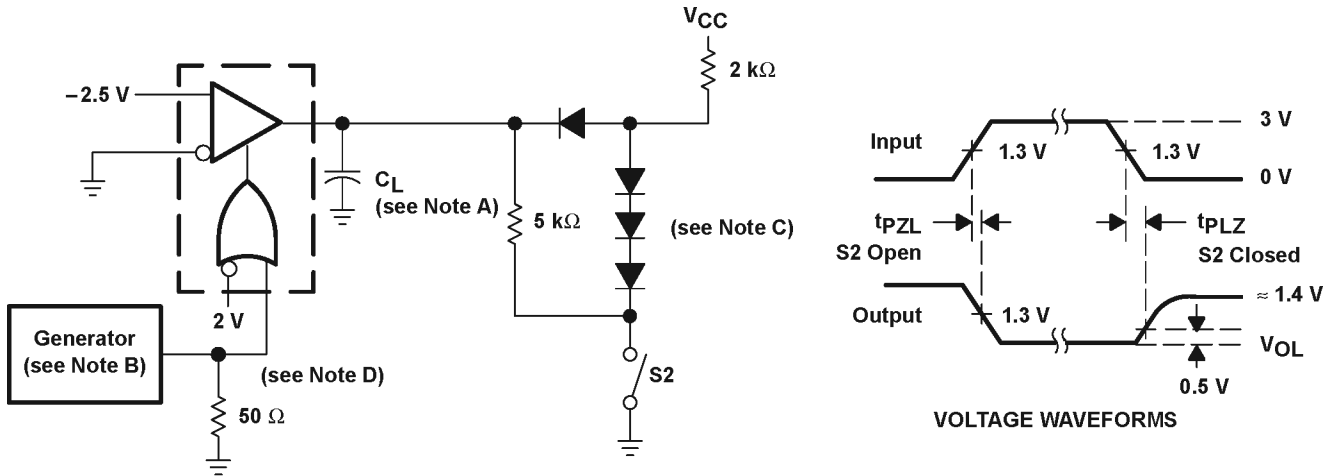


TEST CIRCUIT



- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- C. All diodes are 1N916, or equivalent.
- D. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted input waveform to G.

图 6-2.  $t_{PHZ}$ ,  $T_{PZH}$  Test Circuit and Voltage Waveforms



TEST CIRCUIT

- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- C. All diodes are 1N916, or equivalent.
- D. To test the active-low enable G, ground G and apply an inverted input waveform to G.

6-3.  $t_{pZL}$ ,  $t_{PLZ}$  Test Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL A-B	ENABLES <sup>(1)</sup>		OUTPUT Y
	G	$\bar{G}$	
$V_{ID} \geq 0.2\text{ V}$	H	X	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	X	L	H
$V_{ID} \leq -0.2\text{ V}$	H	XL	?
	X		?
X	H	X	L
	X	L	L
Open circuit	L	H	Z
	X	L	H
	H	X	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

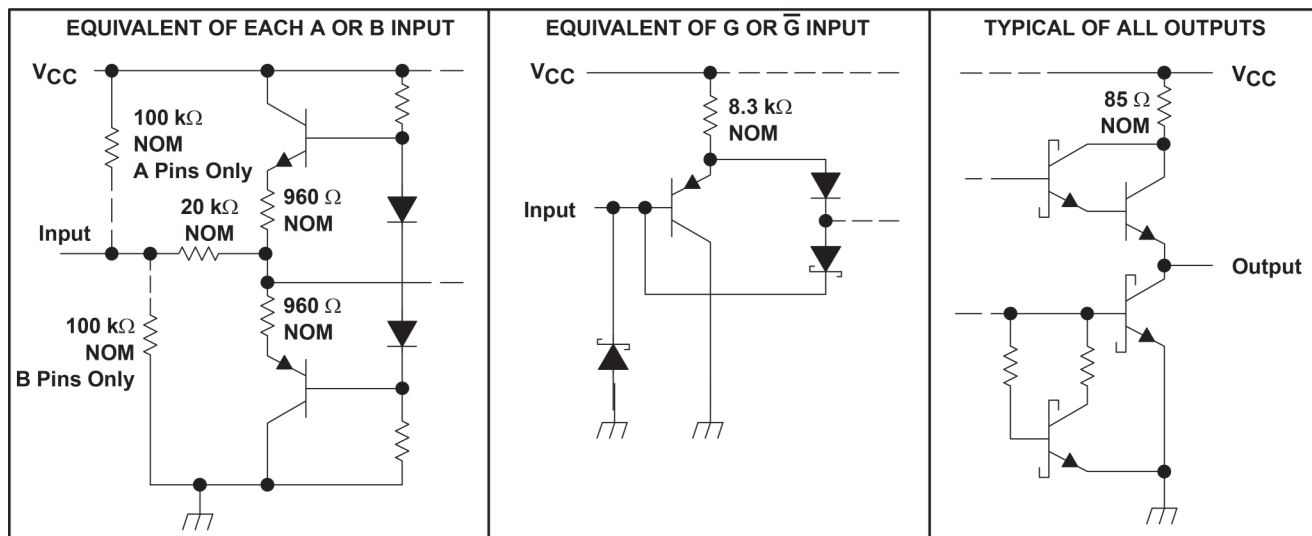


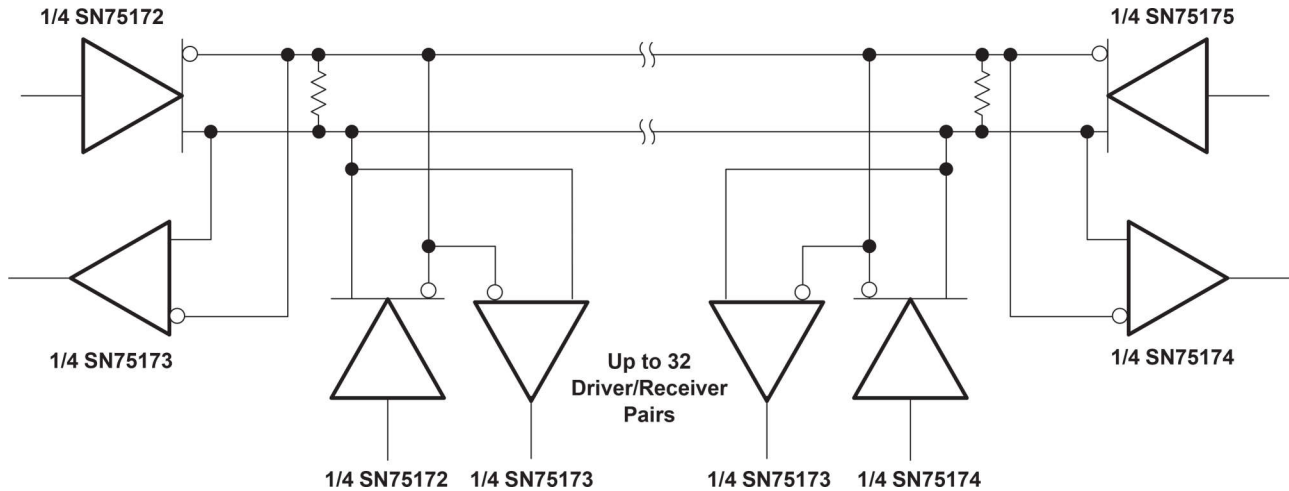
図 7-1. Schematics of Inputs and Outputs

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information



- A. The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

図 8-1. Typical Application Circuit

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 9.3 商標

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision E (April 2000) to Revision F (October 2023)

Page

- ドキュメント全体にわたって表、図、相互参照の採番方法を変更..... 1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN55173J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN55173J	<a href="#">Samples</a>
SN75173DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75173	<a href="#">Samples</a>
SN75173N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75173N	<a href="#">Samples</a>
SN75173NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75173	<a href="#">Samples</a>
SNJ55173J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ55173J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN55173, SN75173 :**

- Catalog : [SN75173](#)
- Military : [SN55173](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75173DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75173NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75173DR	SOIC	D	16	2500	353.0	353.0	32.0
SN75173NSR	SO	NS	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75173D	D	SOIC	16	40	507	8	3940	4.32
SN75173N	N	PDIP	16	25	506	13.97	11230	4.32

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



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#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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