SN75179B 差動ドライバ / レシーバ・ペア

1 特長

- TIA/EIA-422-B、TIA/EIA-485-A、ITU 勧告 V.11 の要件を満たす、または上回る性能
- バス電圧入力範囲:-7V～12V
- 正と負の電流制限
- ドライバ出力能力:最大 60mA
- ドライバのサーマル・シャットダウン保護
- レシーバ入力インピーダンス:12kΩ 以上
- レシーバ入力感度:±200mV
- レシーバ入力ヒステリシス:50mV (標準値)
- 5V 単一電源で動作
- 低消費電力要件

2 概要

SN75179B は、平衡伝送ライン・アプリケーションのために設計された差動ドライバ / レシーバ・ペアであり、TIA/EIA-422-B、TIA/EIA-485-A、ITU 勧告 V.11 を満たしています。本デバイスは、長いバス・ラインでの全二重データ通信の性能が高まるように設計されています。

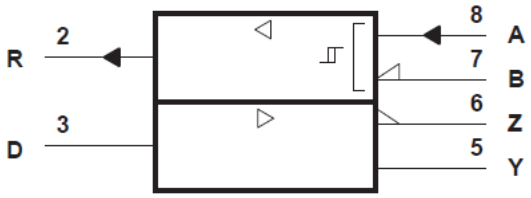
SN75179B ドライバ出力は、正負両方の電流を制限します。レシーバは、高い入力インピーダンス、ノイズ耐性を向上させる入力ヒステリシス、-7V～12V の同相入力電圧範囲にわたって ±200mV の入力感度を備えています。ドライバは、ライン・フォルト条件に対して保護するためのサーマル・シャットダウン機能を備えています。サーマル・シャットダウンは、約 150℃の接合部温度で作動するように設計されています。SN75179B は、最大 60mA の電流負荷を駆動するように設計されています。

SN75179B の動作温度範囲は 0℃～70℃です。

パッケージ情報

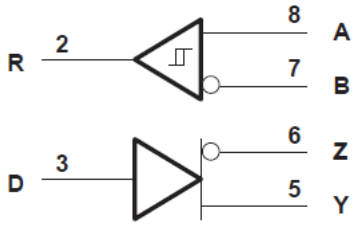
部品番号	パッケージ (1)	本体サイズ (公称)
SN75179B	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 9.43mm
	PS (SOP)	6.2mm × 5.3mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



A. この記号は ANSI/IEEE Std 91-1984 と IEC Publication 617-12 に準拠しています。

論理記号



論理図 (正論理)

Table of Contents

3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (June 2008) to Revision F (October 2022)	Page
• 最新のデータシート・フォーマットに合わせてデータシートのフォーマットを変更	1
• Changed the *Thermal Information* table	4

4 Pin Configuration and Functions

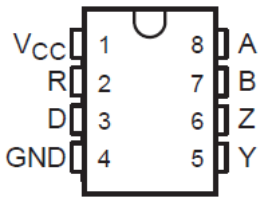


図 4-1. D, PS, or P Package
Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1	V_{CC}	P	5V Voltage Supply
2	R	O	RS485 Logic Output
3	D	I	RS485 Logic Input
4	GND	G	Ground
5	Y	O	Non-Inverting RS485 Bus Output
6	Z	O	Inverted RS485 Bus Output
7	B	I	Inverted RS485 Bus Input
8	A	I	Non-Inverting RS485 Bus Input

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_{ID}	Differential input voltage (3)		±25	V
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	Driver	2			V
V_{IL}	Low-level input voltage	Driver			0.8	V
V_{IC}	Common-mode input voltage		–7(1)		12	V
V_{ID}	Differential input voltage,				±12	V
I_{OH}	High level output current	Driver			–602	mA
		Receiver			–400	µA
I_{OL}	Low level output current	Driver			60	mA
		Receiver			8	mA
T_A	Operating free-air temperature		0		70	°C

(1) The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

5.3 Thermal Information

THERMAL METRIC(1)		SOIC (D)	PDIP (P)	SOP (PS)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	109.5	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	53.9	65.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	65.7	62.1	
ψ_{JT}	Junction-to-top characterization parameter	8.8	11.6	31.3	
ψ_{JB}	Junction-to-board characterization parameter	62.6	64.5	60.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See 図 6-1	1/2 V_{OD1}			V
				2(2)			
		R_L = 54 Ω	See 図 6-1	1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See (4)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage					±0.2	V
V_{OC}	Common mode output voltage	R_L = 54 Ω or 100 Ω,	See 図 6-1			3	V
						–1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)					±0.2	V
I_O	Output current	V_{CC} = 0	V_O = -7 V to 12 V			±100	µA
I_{IH}	High-level input current	V_{IH} = 2.4 V				20	µA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				–200	µA
I_{OS}	Short circuit output current	V_O = –7 V				–250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load			57	70	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The minimum V_{OD2} with 100-Ω load is either 1/2 VOD2 or 2 V, whichever is greater
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) See TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.

5.5 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω ,	See 図 6-3		15	22	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω ,	See 図 6-3		20	30	ns

5.6 Symbol Equivalent

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	$V_t(R_L$ = 100 Ω)	$V_t(R_L$ = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
D $\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|$	$\|\|V_t\| - \|\overline{V}_t\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
D $\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

5.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V	I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V	I_O = 8 mA		–0.2(2)			V
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)					50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV	I_{OH} = -400 µA	See 図 6-2	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = -200 mV	I_{OL} = 8 mA	See 図 6-2			0.45	V
I_I	Line input current	Other input at 0 V	See (3)	V_I = 12 V			1	mA
				V_I = –7 V			–0.8	mA
r_I	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				–15		–85	mA
I_{OS}	Supply current (total package)	No load				57	70	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) See TIA/EIA-422-B for exact conditions.

5.8 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V			19	35	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 15 pF	See 図 6-4		30	40	ns

5.9 Typical Characteristics

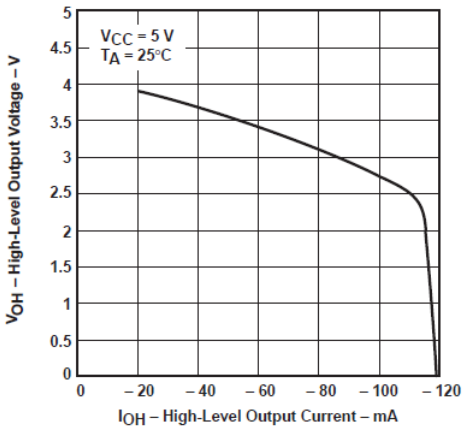


図 5-1. Driver High-Level Output Voltage vs High-Level Output Current

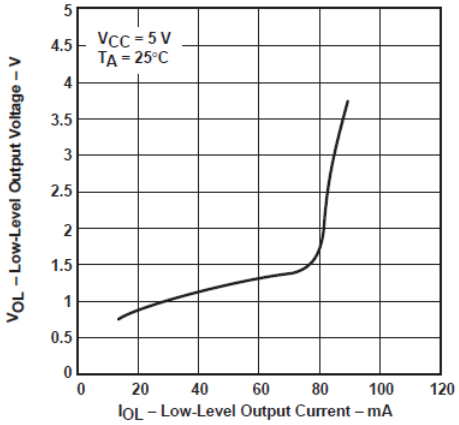


図 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

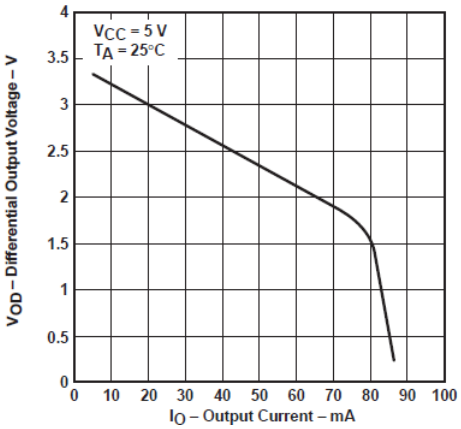


図 5-3. Driver Differential Output Voltage vs Output Current

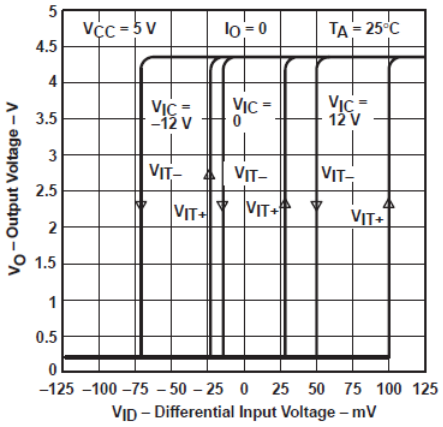


図 5-4. Receiver Output Voltage vs Differential Input Voltage

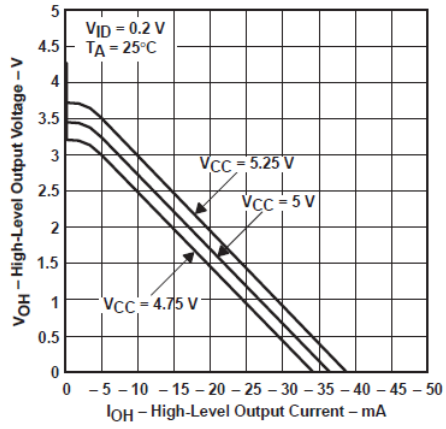


図 5-5. High-Level Output Voltage vs High-Level Output Current

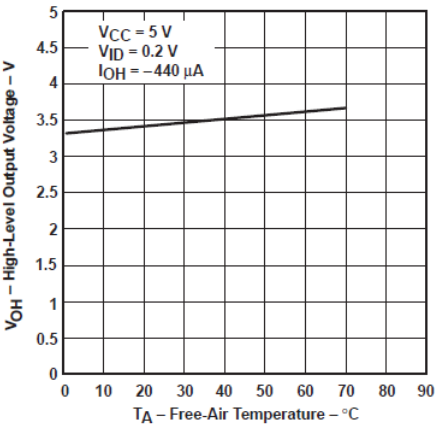


図 5-6. High-Level Output Voltage vs Free-Air Temperature

5.9 Typical Characteristics (continued)

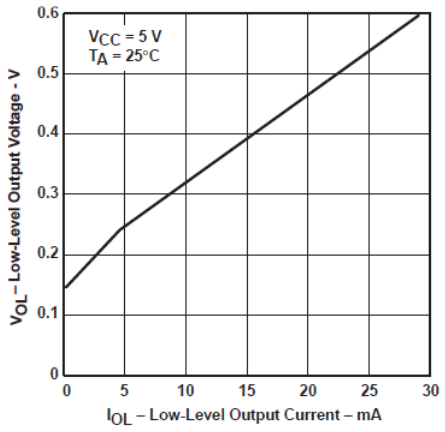


図 5-7. Receiver Low-Level Output Voltage vs Low-Level Output Current

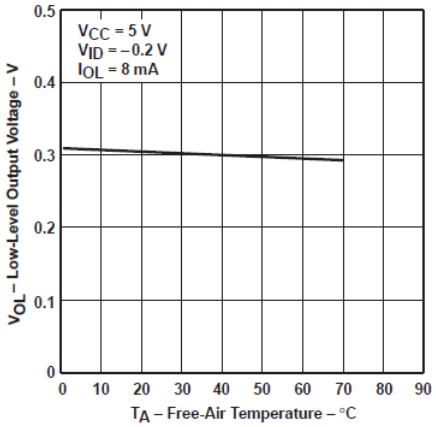


図 5-8. Receiver Low-Level Output Voltage vs Free-Air Temperature

6 Parameter Measurement Information

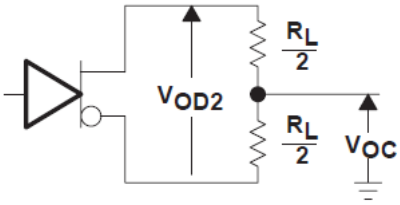


図 6-1. Driver V_{DD} and V_{OC}

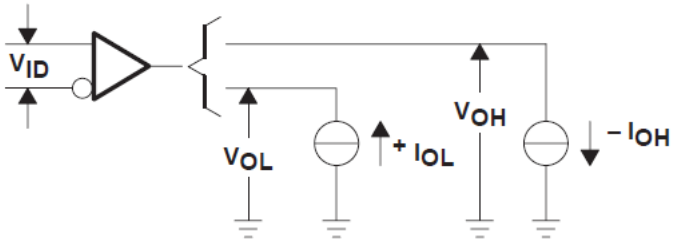
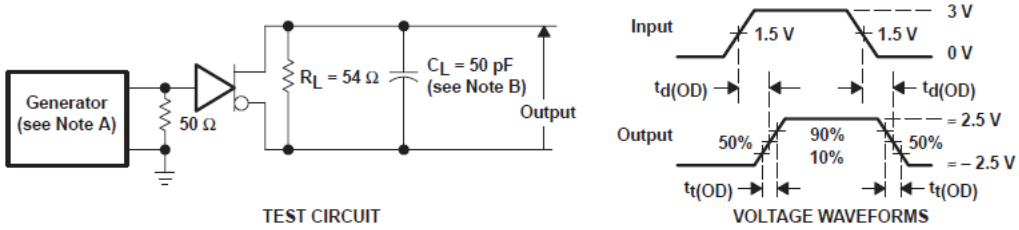


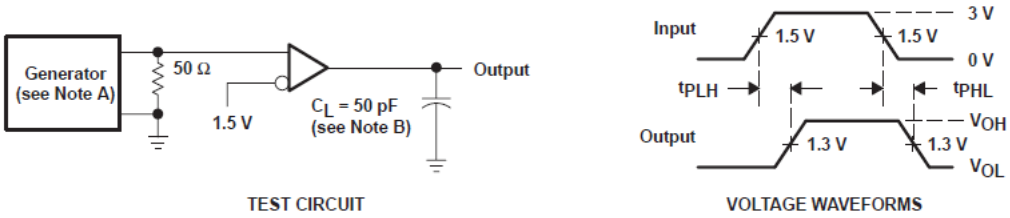
図 6-2. Receiver V_{OH} and V_{OL}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

図 6-3. Driver Test Circuit and Voltage Waveforms



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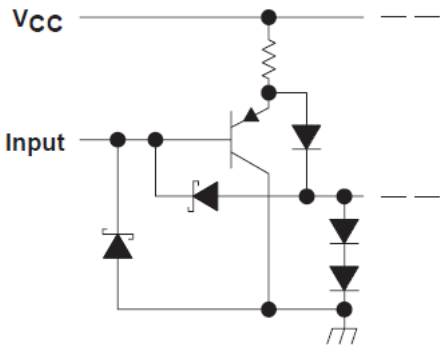
B. C_L includes probe and jig capacitance.

図 6-4. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram



A. Driver input: $R_{(eq)}$ = 3 kΩ NOM$R_{(eq)}$ = equivalent resistor

図 7-1. Equivalent of Driver Input

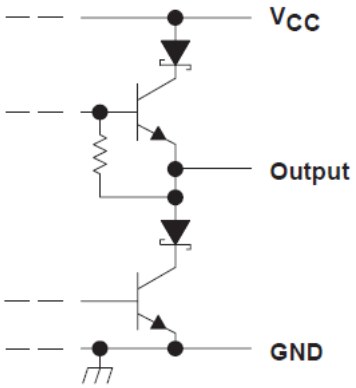


図 7-2. Typical of All Driver Outputs

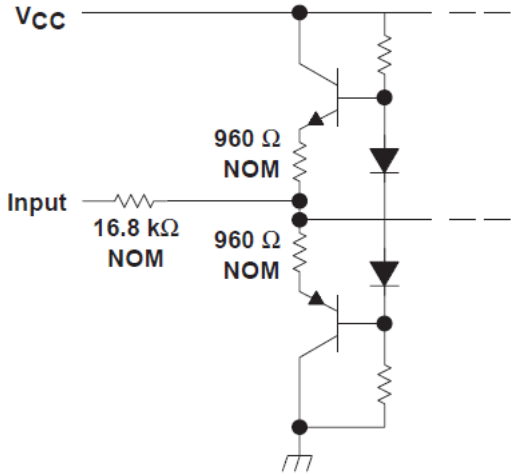


図 7-3. Equivalent of Each Receiver Input

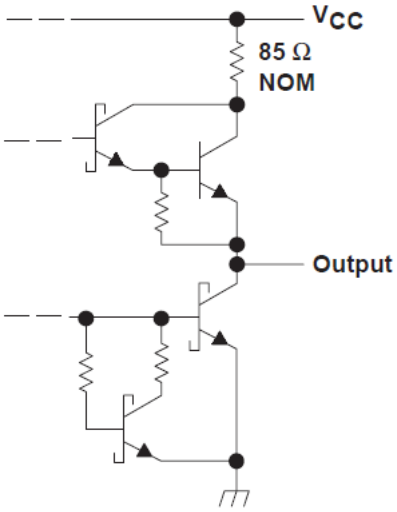


図 7-4. Typical of All Receiver Outputs

7.2 Device Functional Modes

表 7-1. Driver(1)

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

(1) H = high level, L = low level, ? = indeterminate

表 7-2. Receiver(1)

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
–0.2 V < V_{ID} < 0.2 V	?
$V_{ID} \leq$ –0.2 V	L
Open	?

(1) H = high level, L = low level, ? = indeterminate

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75179BD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	75179B	
SN75179BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B	Samples
SN75179BDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B	Samples
SN75179BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75179BP	Samples
SN75179BPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75179BP	Samples
SN75179BPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A179B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

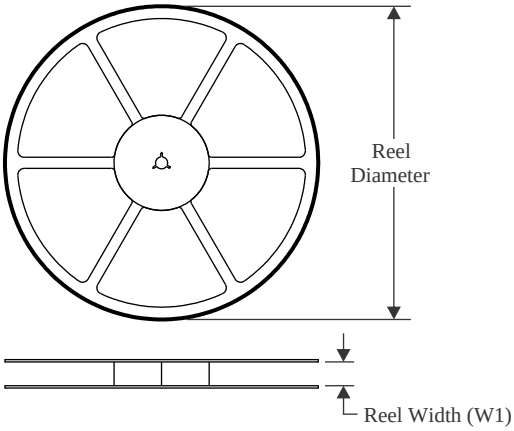
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

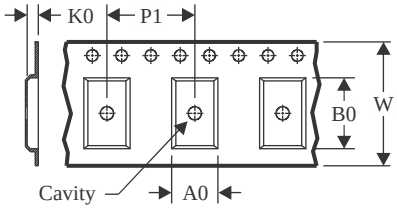
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

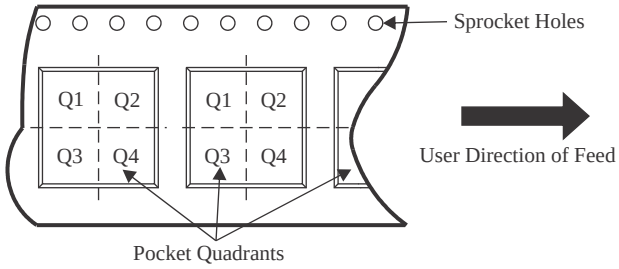


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

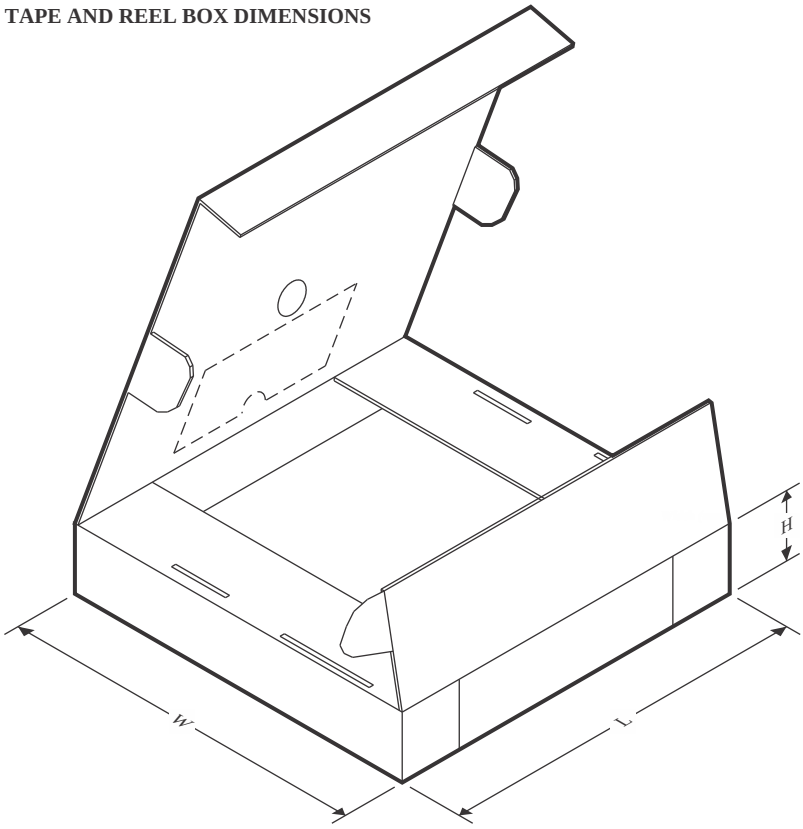
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75179BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75179BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

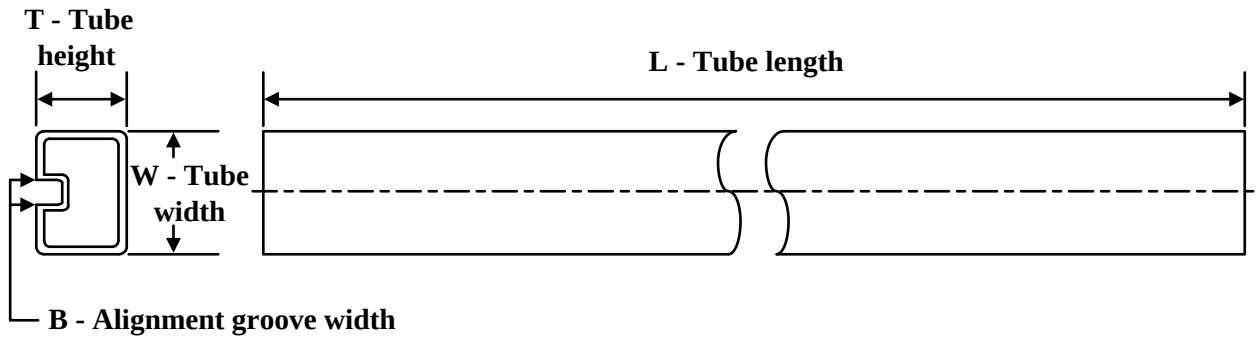
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

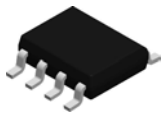
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75179BDR	SOIC	D	8	2500	356.0	356.0	35.0
SN75179BPSR	SO	PS	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75179BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75179BPE4	P	PDIP	8	50	506	13.97	11230	4.32

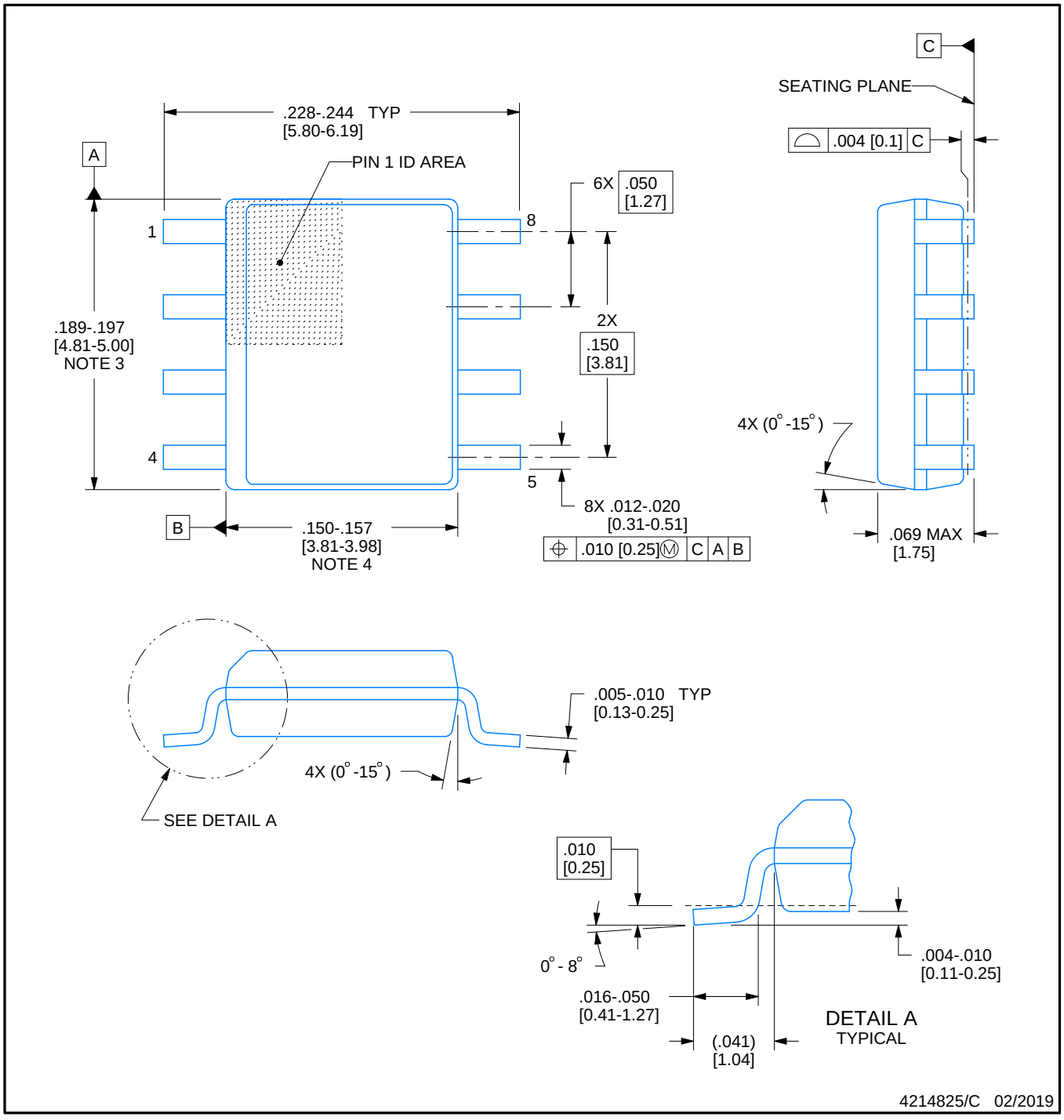


PACKAGE OUTLINE

D0008A

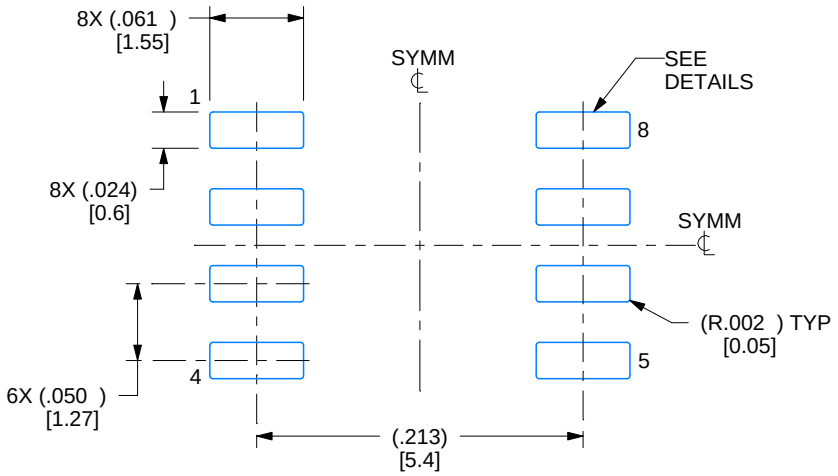
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

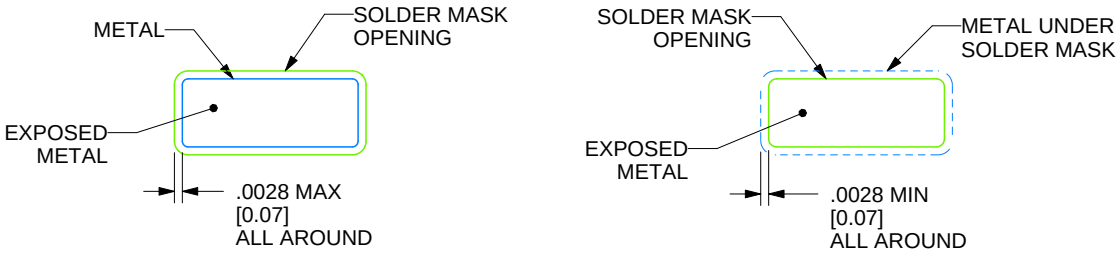


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

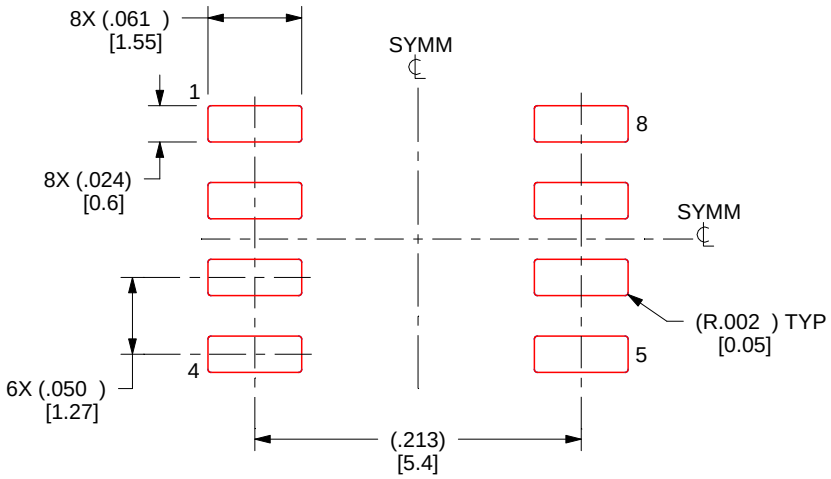
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

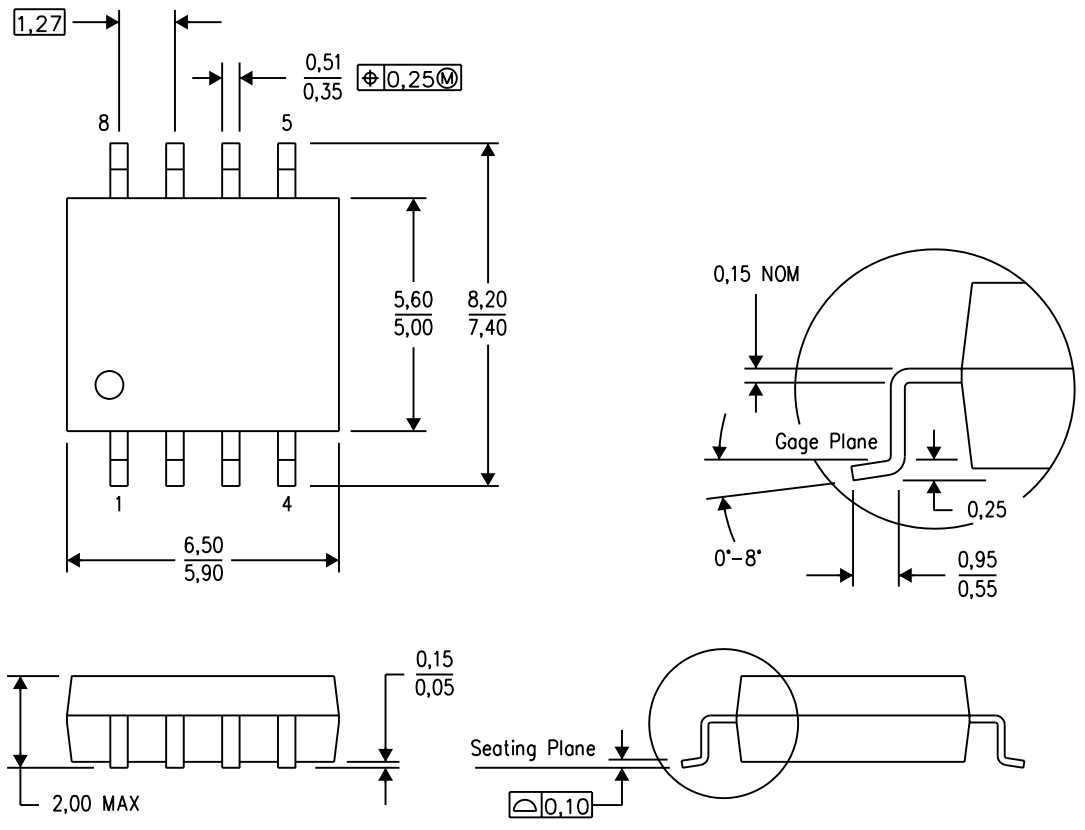
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

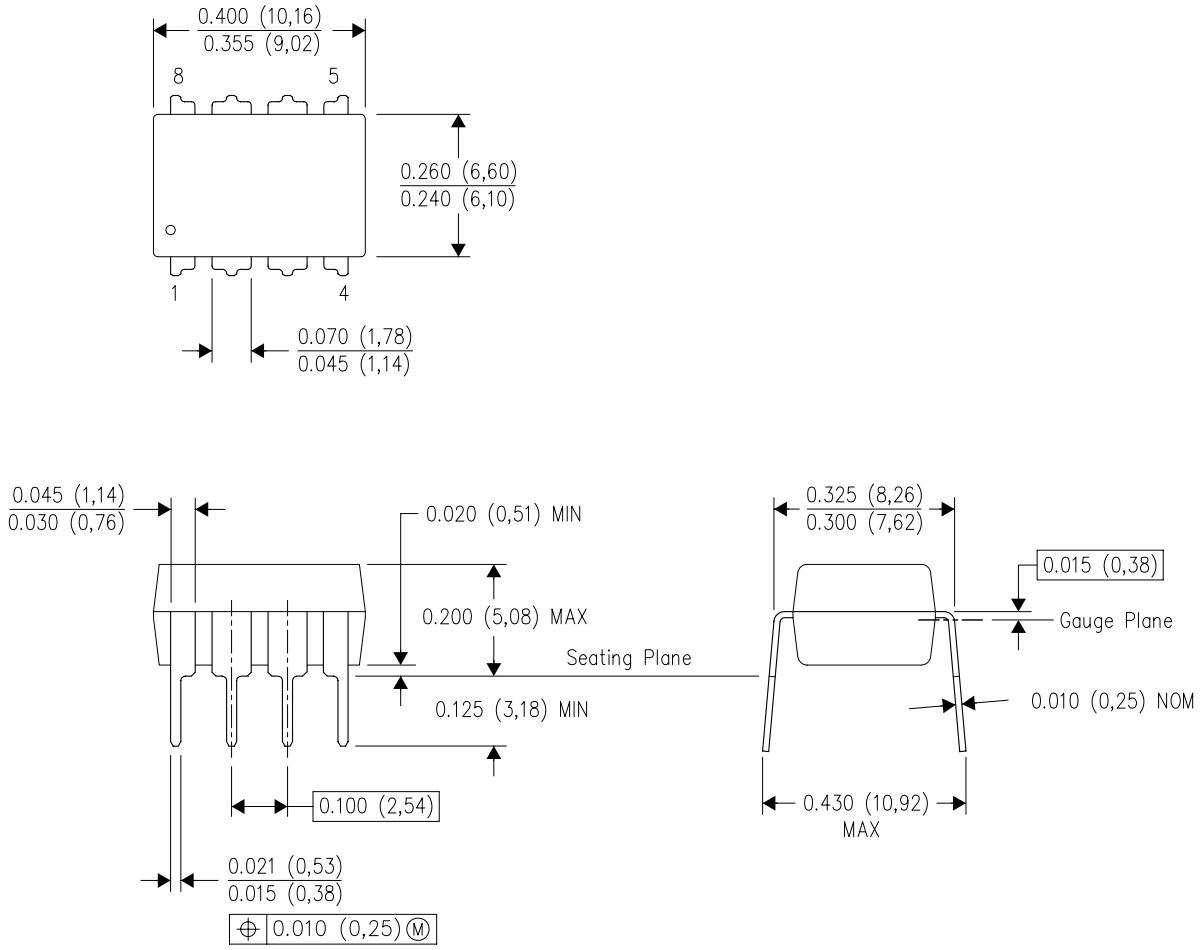
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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