

SN75ALS173 クワッド差動ライン・レシーバ

1 特長

- ANSI EIA/TIA-422-B、EIA/TIA-423-B、および RS-485 の要件を満たす、または超える
- ITU 勧告 V.10、V.11、X.26、X.27 の要件を満たす、または超える
- ノイズの多い環境の、長いバス・ラインでのマルチポイント・バス伝送用に設計
- 3 ステート出力
- 同相入力電圧範囲: -12V ~ 12V
- 入力感度: ±200mV
- 入力ヒステリシス: 50mV (標準値)
- 高い入力インピーダンス: 12kΩ (最小値)
- 5V 単一電源で動作
- 低消費電流要件: 27mA (最大値)

2 アプリケーション

- モータ・ドライブ
- ファクトリ・オートメーション / 制御

3 概要

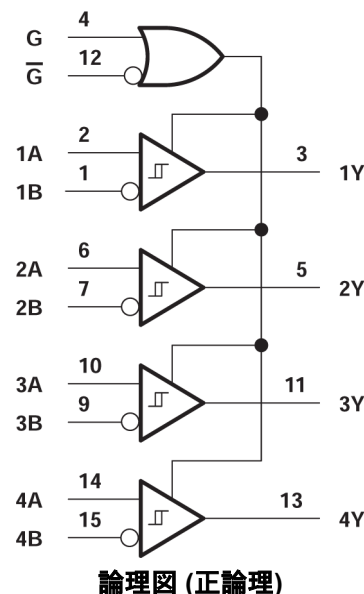
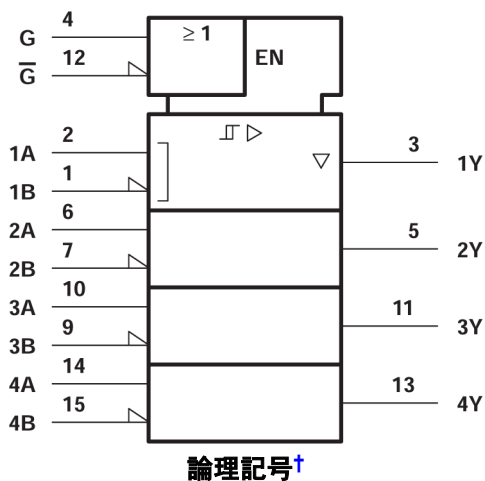
SN75ALS173 は、3 ステート出力を搭載したモノリシック・クワッド作動ライン・レシーバです。ANSI 規格 EIA/TIA-422-B、EIA/TIA-423-B、RS-485、またいくつかの ITU 勧告の要件を満たすように設計されています。高度な低消費電力ショットキー・テクノロジーにより、通常発生する消費電力を損なわずに高速を実現します。4 つのレシーバには、共通してイネーブルの論理和ペアがあります。G High または \bar{G} Low のどちらかを選択すると、すべてのレシーバがイネーブルになります。このデバイスは、高い入力インピーダンス、ノイズ耐性を高める入力ヒステリシス、-12V ~ 12V の同相入力電圧範囲にわたって ±200mV の入力感度を特長としています。

SN75ALS173 は、0°C ~ 70°C での動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
SN75ALS173	N (PDIP, 16)	19.3mm × 9.4mm
	NS (SOP, 16)	10.2mm × 7.8mm

- 詳細については、[セクション 10](#) を参照してください。
- パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



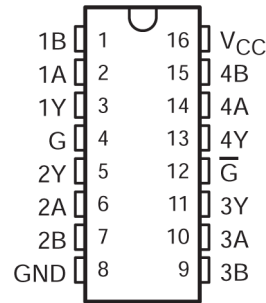
† この記号は ANSI/IEEE 規格 91-1984 と IEC Publication 617-12 に準拠しています。



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4 Pin Configuration and Functions



A. The NS package is only available left-end taped and reeled (order device SN75ALS173 NSLE).

図 4-1. N or NS Package (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
G	4	I	Active High Enable
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
G-bar	12	I	Active Low Enable
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V _{CC}	16	PWR	Device VCC (4.75 V to 5.25 V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage, (see ⁽²⁾)		7	V
V_I	Input voltage, (A or B inputs)		±14	V
V_{ID}	Differential input voltage, (see ⁽³⁾)		±14	V
V_I	Enable input voltage		7	V
I_{OL}	Low-level output current		50	mA
	Continuous total dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values, except differential input voltage, are with respect to network ground terminal.
- Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level input voltage, V_{IH}	G, \bar{G}	2			V
Low-level input voltage, V_{IL}	G, \bar{G}			0.8	V
High-level output current, I_{OH}				–400	µA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A		0		70	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN75ALS173		UNIT
		N (PDIP)	NS (SOP)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	50.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.5	13.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.3	50.3	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted) (see [Note 3](#))

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IT+}	Positive-going input threshold voltage						200	mV	
V _{IT-}	Negative-going input threshold voltage				-200 ⁽²⁾			mV	
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})					50		mV	
V _{IK}	Input clamp voltage	G, \bar{G}	I _I = -18 mA				-1.5	V	
V _{OH}	High-level output voltage	V _{ID} = 200 mV,		I _{OH} = -400 μ A,	See 6-1		2.7	v	
V _{OL}	Low-level output voltage	V _{ID} = -200 mV,		I _{OL} = 8 mA,	See 6-1		0.45	v	
I _{OZ}	High-impedance-state output current	V _O = 0.4 V to 2.4 V					-20	μ A	
I _I	Line input current	Other input at 0 V		V _I = 12 V			1	mA	
				V _I = -7 V			-0.8		
I _{IH}	High-level input current	G, \bar{G}	V _{IH} = 2.7 V				20	μ A	
I _{IL}	Low-level input current	G, \bar{G}	V _{IL} = 0.4 V				-100	μ A	
r _i	Input resistance					12		k Ω	
I _{OS}	Short-circuit output current	See Note 4					-15	-85	mA
I _{CC}	Supply current (total package)	No load,		Outputs enabled			16	24	mA
		No load,		Outputs disabled			18	27	

- (1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
- (2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
- (3) Refer to ANSI Standard RS-485 for exact conditions.
- (4) The duration of the short circuit should not cause the maximum package power dissipation to be exceeded.

5.6 Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay time, high- to low-level output	V _{ID} = -2.5 V to 2.5 V, See 6-2	9	18	27	ns
t _{PLH}	Propagation delay time, low- to high-level output		9	18	27	ns
t _{PZH}	Output enable time to high level	See 6-3	4	12	18	ns
t _{PZL}	Output enable time to low level	See 6-4	6	13	21	ns
t _{PHZ}	Output disable time from high level	See 6-3	10	21	27	ns
t _{PLZ}	Output disable time from low level	See 6-4	8	15	25	ns

6 Parameter Measurement Information

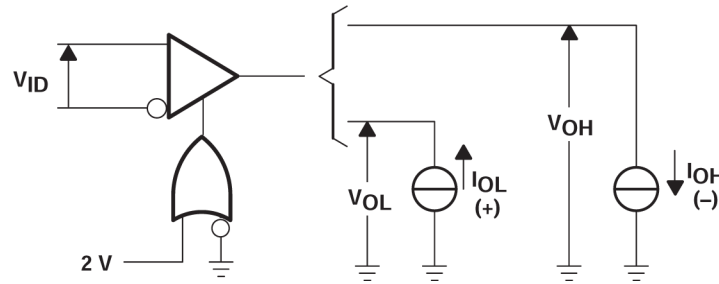


图 6-1. V_{OH} , V_{OL}

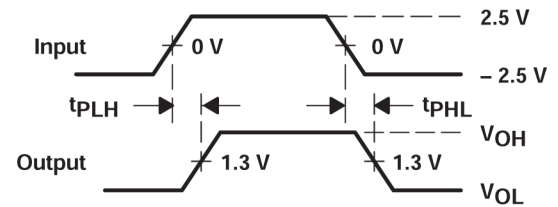
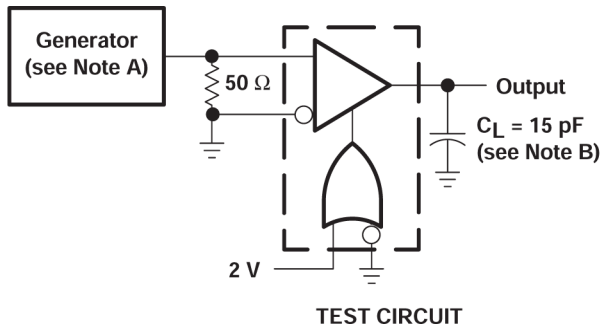
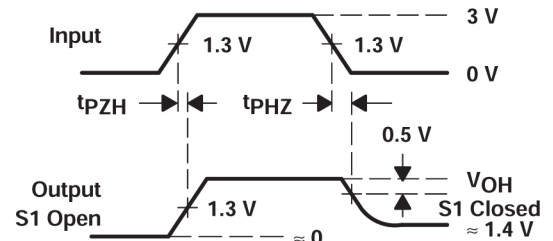
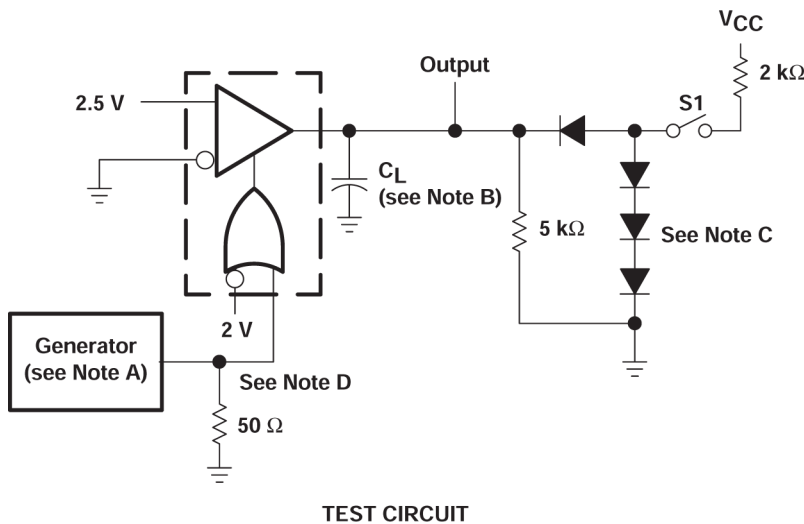
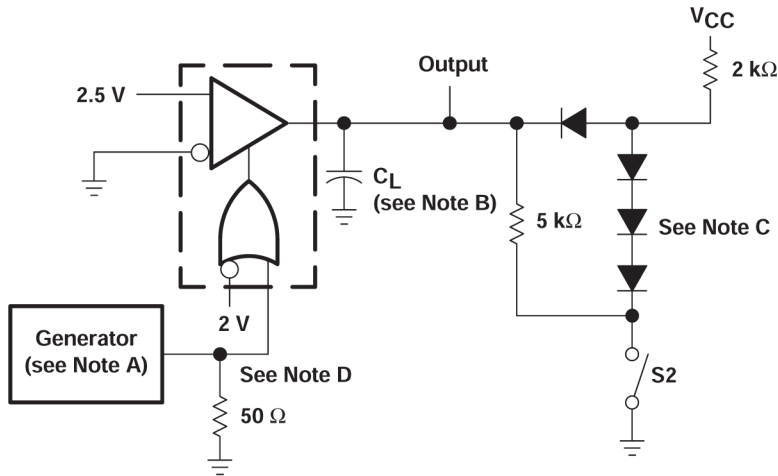


图 6-2. Test Circuit and Voltage Waveforms

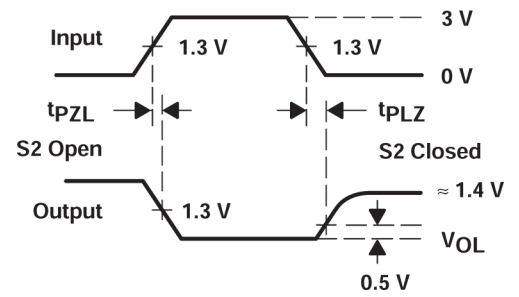


- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

图 6-3. Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

6-4. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL A - B	ENABLES ⁽¹⁾		OUTPUT Y
	G	\bar{G}	
$V_{ID} \geq 0.2 V$	H	X	H
	X	L	H
$-0.2 V < V_{ID} < 0.2 V$	H	X	?
	X	L	?
$V_{ID} < -0.2 V$	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

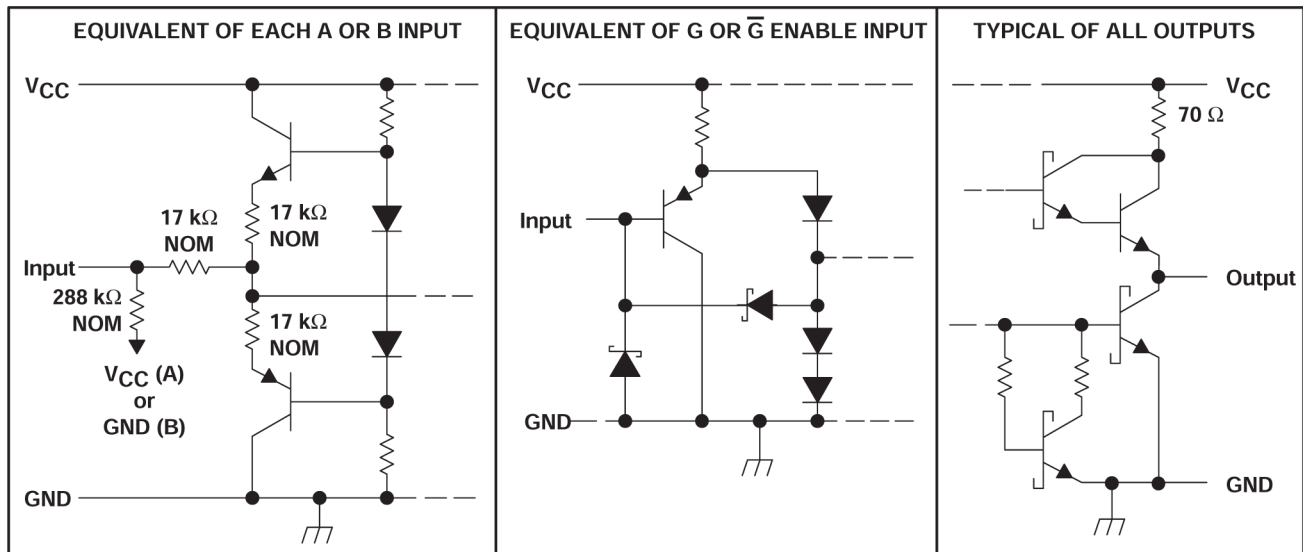


図 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (May 1995) to Revision D (October 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS173N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS173N	Samples
SN75ALS173NS	OBSOLETE	SOP	NS	16		TBD	Call TI	Call TI	0 to 70	75ALS173	
SN75ALS173NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS173	Samples
SN75ALS173NSRG4	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS173	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS173NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75ALS173NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS173NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN75ALS173NSR	SOP	NS	16	2000	367.0	367.0	38.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS173N	N	PDIP	16	25	506	13.97	11230	4.32



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

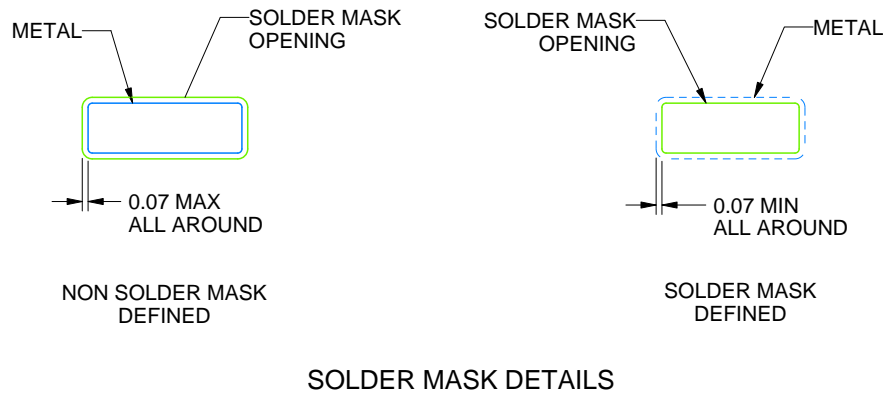
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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