

## SNx5LBC176 差動バス・トランシーバ

### 1 特長

- 双方向トランシーバ
  - ANSI 規格 TIA/EIA-485-A と ISO 8482:1987(E) の要件を満たす、または上回る性能
  - 高速、低消費電力の LinBiCMOS™ 回路
  - シリアルとパラレルの両方のアプリケーションでの高速動作に対応
  - 低スキュー
  - ノイズの多い環境の長いバスラインでのマルチポイントの伝送用に設計
  - 非常に小さいディスエーブル時消費電流 ... 200µA 以下
  - 広い正および負の入力 / 出力バス電圧範囲
  - サーマル・シャットダウン保護
  - ドライバの正および負電流制限
  - 開路フェイルセーフ・レシーバ設計
  - レシーバ入力感度 ... ±200mV 以内
  - レシーバ入力ヒステリシス ... 50mV (標準値)
  - 5V 単一電源で動作
  - グリッチ・フリーのパワーアップ / パワーダウン保護機能
  - Q 温度仕様、車載用として提供
- HighRel 車載用アプリケーション  
構成制御 / 印刷サポート  
車載規格に基づく認定

### 2 概要

SN55LBC176、SN65LBC176、SN65LBC176Q、SN75LBC176 差動バス・トランシーバは、マルチポイント・バス伝送ライン上での双方向データ通信を目的として設計されたモノリシック IC です。これらのデバイスは平衡伝送ライン用に設計されており、ANSI 規格 TIA/EIA-485-A (RS-485) および ISO 8482:1987(E) に適合しています。

SN55LBC176、SN65LBC176、SN65LBC176Q、SN75LBC176 は、3 ステート差動ライン・ドライバと差動入力ライン・レシーバを統合しており、どちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディスエーブルされている場合、または  $V_{CC} = 0$  の場合、バスへの負荷を最小化するように設計されています。このポートは広い正負の同相電圧範囲を持っているため、本デバイスはパーティライン・アプリケーションに適しています。ドライバとレシーバをディスエーブルにすることにより、デバイスの消費電流を低減できます。

#### パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN55LBC176	LCCC (20)	8.89mm × 8.89mm
	CDIP (8)	9.60mm × 6.67mm
SN65LBC176	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm
SN75LBC176	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

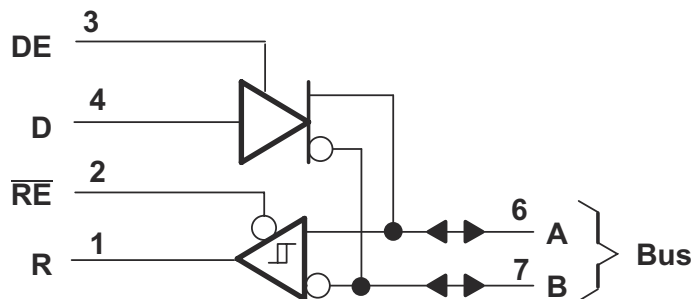


図 2-1. 論理図 (正論理)



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### 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

#### Changes from Revision H (December 2010) to Revision I (October 2022)

Page

- 「ピン構成および機能」セクション、「熱に関する情報」表、「詳細説明」セクション、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加..... 1

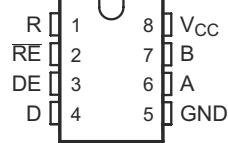
## 4 概要 (続き)

これらのトランシーバは、このデータシートの動作条件と特性のセクションに規定された範囲内で、ANSI 規格 TIA/EIA-485 (RS-485) および ISO 8482 アプリケーションに適しています。ミリタリー温度範囲全体では、TIA/EIA-485-A と ISO 8482:1987 (E) に含まれる一部の制限は満たされておらず、またはテストされていません。

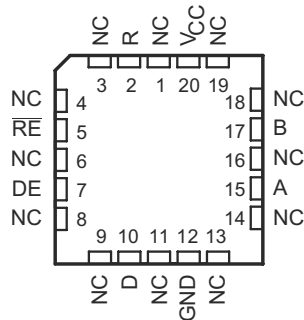
動作温度範囲は、SN55LBC176 が -55°C ~ 125°C、SN65LBC176 が -40°C ~ 85°C、SN65LBC176Q が -40°C ~ 125°C、SN75LBC176 が 0°C ~ 70°C です。

## 5 Pin Configuration and Functions

**D, JG, OR P PACKAGE  
(TOP VIEW)**



**FK PACKAGE  
(TOP VIEW)**



NC – No internal connection

**表 5-1. Pin Functions**

NAME	PIN		TYPE	DESCRIPTION
	SOIC, PDIP, CDIP	LCCC		
R	1	2	O	Logic output RS485 data
RE	2	5	I	Receiver enable/disable
DE	3	7	I	Driver enable/disable
D	4	10	I	Logic input RS485 data
GND	5	12	-	Ground
A	6	15	I/O	RS485 bus pin; Non-Inverting
B	7	17	I/O	RS485 bus pin; Inverted
V <sub>CC</sub>	8	20	-	5V Supply Voltage
NC	-	1,2,3,6,8,9,11,13,14,16,18,19	-	No Internal Connection

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{CC}$ <sup>(2)</sup>		7	V
Voltage range at any bus terminal	-10	15	V
Input voltage, $V_I$ (D, DE, R, or $\overline{RE}$ )	-0.3	$V_{CC} + 0.5$	V
Receiver output current, $I_O$	-10	10	mA
Continuous total power dissipation	See <a href="#">セクション 6.5</a>		
Storage temperature range, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [セクション 6.2](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

### 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$		-7		12	V
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $V_{ID}$ <sup>(1)</sup>		-12		12	V
High-level output current, $I_{OH}$	Driver	-60			mA
	Receiver	-400			μA
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			8	
Junction temperature, $T_J$				140	°C
Operating free-air temperature, $T_A$	SN55LBC176	-55		125	°C
	SN65LBC176	-40		85	
	SN65LBC176Q	-40		125	
	SN75LBC176	0		70	

- (1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

### 6.3 Thermal Information: SN55LBC176

THERMAL METRIC <sup>(1)</sup>		FK	JG	UNIT
		20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	51.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	86.5	
$\Psi_{JT}$	Junction-to-top characterization parameter	31.0	23.7	
$\Psi_{JB}$	Junction-to-board characterization parameter	36.0	80.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	11.6	

## 6.4 Thermal Information: SN65LBC176, SN75LBC176

THERMAL METRIC <sup>(1)</sup>		D	P	UNIT
		8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	116.7	65.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.3	54.6	
R <sub>θJB</sub>	Junction-to-board thermal resistance	63.4	42.1	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	8.8	22.9	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.6	41.6	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Dissipation Ratings

PACKAGE	THERMAL MODEL	T <sub>A</sub> < 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 110°C POWER RATING
D	Low K <sup>(1)</sup>	526 mW	5.0 mW/°C	301 mW	226 mW	—
	High K <sup>(2)</sup>	882 mW	8.4 mW/°C	504 mW	378 mW	—
P		840 mW	8.0 mW/°C	480 mW	360 mW	—
JG		1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
FK		1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51–3.

(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51–7.

## 6.6 Driver Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = –18 mA		–1.5		V
V <sub>O</sub>	Output voltage	I <sub>O</sub> = 0		0	6	V
V <sub>OD1</sub>	Differential output voltage	I <sub>O</sub> = 0		1.5	6	V
V <sub>OD2</sub>	Differential output voltage	R <sub>L</sub> = 54 Ω, See (2)	See <a href="#">7-1</a> ,	55LBC176, 65LBC176, 65LBC176Q	1.1	V
				75LBC176	1.5	
V <sub>OD3</sub>	Differential output voltage	V <sub>test</sub> = –7 V to 12 V, See (2)	See Figure 2,	55LBC176, 65LBC176, 65LBC176Q	1.1	V
				75LBC176	1.5	
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage (1)	R <sub>L</sub> = 54 Ω or 100 Ω, See <a href="#">7-1</a>		–0.2	0.2	V
V <sub>OC</sub>	Common-mode output voltage			–1	3	V
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage (1)			–0.2	0.2	V
I <sub>O</sub>	Output current	Output disabled, See (3)	V <sub>O</sub> = 12 V		1	mA
			V <sub>O</sub> = –7 V	–0.8		
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 2.4 V		–100		μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0.4 V		–100		μA

## 6.6 Driver Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT	
$I_{OS}$	Short circuit output current	$V_O = -7\text{ V}$		-250		mA	
		$V_O = 0$		-150			
		$V_O = V_{CC}$			250		
		$V_O = 12\text{ V}$					
$I_{CC}$	Supply current	$V_I = 0$ or $V_{CC}$ , No load	Receiver disabled and driver enabled	55LBC176, 65LBC176Q		1.75	mA
				65LBC176, 75LBC176		1.5	
			Receiver and driver disabled	55LBC176, 65LBC176Q		0.25	
				65LBC176, 75LBC176		0.2	

- (1)  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input changes from a high level to a low level.
- (2) This device meets the  $V_{OD}$  requirements of TIA/EIA-485-A above 0°C only.
- (3) This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions.

## 6.7 Driver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	SN55LBC176 SN65LBC176Q			SN65LBC176 SN75LBC176			UNIT
		MIN	TYP	MAX	MIN	TYP <sup>(1)</sup>	MAX	
$t_{d(OD)}$	Differential output delay time			31	8		25	ns
$t_{t(OD)}$	Differential output transition time	$R_L = 54 \Omega$ , See <a href="#">7-3</a>	$C_L = 50 \text{ pF}$ ,			12		ns
$t_{sk(p)}$	Pulse skew ( $ t_{d(ODH)} - t_{d(ODL)} $ )				6	0	6	ns
$t_{PZH}$	Output enable time to high level	$R_L = 110 \Omega$ ,	See <a href="#">7-4</a>				35	ns
$t_{PZL}$	Output enable time to low level	$R_L = 110 \Omega$ ,	See <a href="#">7-5</a>				35	ns
$t_{PHZ}$	Output disable time from high level	$R_L = 110 \Omega$ ,	See <a href="#">7-4</a>				60	ns
$t_{PLZ}$	Output disable time from low level	$R_L = 110 \Omega$ ,	See <a href="#">7-5</a>				35	ns

(1) All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**表 6-1. Driver Symbol Equivalent**

DATA SHEET PARAMETER	RS-485
$V_O$	$V_{oa}, V_{ob}$
$ V_{OD1} $	$V_o$
$ V_{OD2} $	$V_t (R_L = 54 \Omega)$
$ V_{OD} $	$V_t$ (test termination measurement 2)
$\Delta  V_{OD} $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{os} $
$\Delta  V_{OC} $	$ V_{os} - \bar{V}_{os} $
$I_{OS}$	None
$I_O$	$I_{ia}, I_{ib}$

## 6.8 Receiver Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>O</sub> = 2.7 V,	I <sub>O</sub> = -0.4 mA			0.2	V
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>O</sub> = 0.5 V,	I <sub>O</sub> = 8 mA	-0.2 <sup>(2)</sup>			V
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> ) (see <a href="#">7-4</a> )				50		mV
V <sub>IK</sub>	Enable-input clamp voltage	I <sub>I</sub> = -18 mA		-1.5			V
V <sub>OH</sub>	High level output voltage	V <sub>ID</sub> = 200 mV, See <a href="#">7-6</a>	I <sub>OH</sub> = -400 μA,	2.7			V
V <sub>OL</sub>	Low level output voltage	V <sub>ID</sub> = -200 mV, See <a href="#">7-6</a>	I <sub>OL</sub> = 8 mA,			0.45	V
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V		-20		20	μA
I <sub>I</sub>	Line input current	Other input = 0 V, See <sup>(3)</sup>	V <sub>I</sub> = 12 V			1	mA
			V <sub>I</sub> = -7 V		-0.8		
I <sub>IH</sub>	High-level enable-input current	V <sub>IH</sub> = 2.7 V		-100			μA
I <sub>IL</sub>	Low-level enable-input current	V <sub>IL</sub> = 0.4 V		-100			μA
r <sub>I</sub>	Input resistance			12			kΩ
I <sub>CC</sub>	Supply current	V <sub>I</sub> = 0 or V <sub>CC</sub> , No load	Receiver enabled and driver disabled			3.9	mA
			Receiver and driver disabled	SN55LBC176, SN65LBC176, SN65LBC176Q		0.25	
				SN75LBC176		0.2	

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

(3) This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

## 6.9 Receiver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 15 pF

PARAMETER	TEST CONDITIONS	SN55LBC176 SN65LBC176Q		SN65LBC176 SN75LBC176			UNIT	
		MIN	MAX	MIN	TYP <sup>(1)</sup>	MAX		
t <sub>PLH</sub>	Propagation delay time, low- to high-level single-ended output	V <sub>ID</sub> = -1.5 V to 1.5 V, See <a href="#">7-7</a>	11	37	11		33	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level single-ended output		11	37	11		33	
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PLH</sub> - t <sub>PHL</sub>  )			10		3	6	
t <sub>PZH</sub>	Output enable time to high level	See <a href="#">7-8</a>		35			35	ns
t <sub>PZL</sub>	Output enable time to low level			35			30	
t <sub>PHZ</sub>	Output disable time from high level	See <a href="#">7-8</a>		35			35	ns
t <sub>PLZ</sub>	Output disable time from low level			35			30	

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



## 7 Parameter Measurement Information

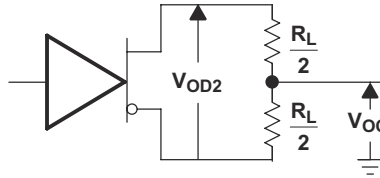


Fig 7-1. Driver  $V_{OD}$  and  $V_{OC}$

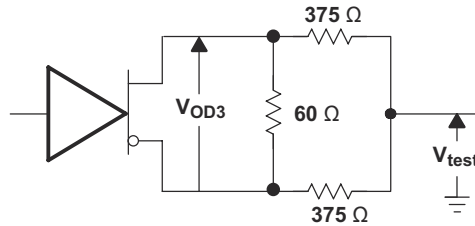
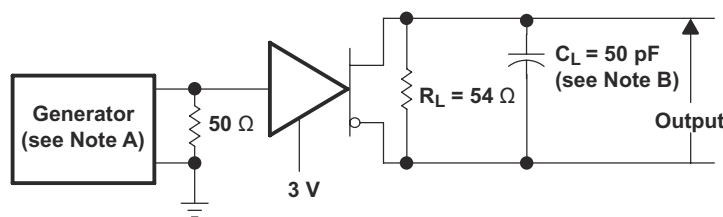
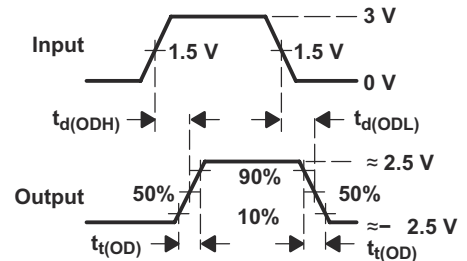


Fig 7-2. Driver  $V_{OD3}$

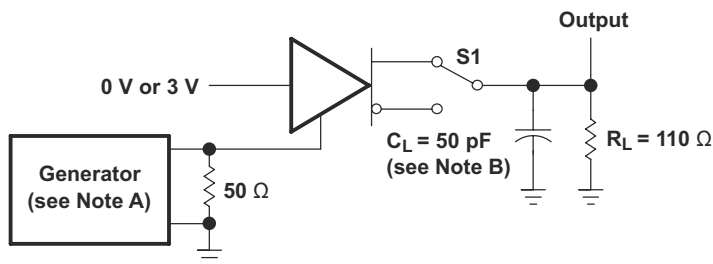


TEST CIRCUIT

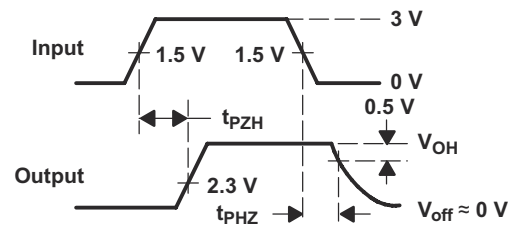


VOLTAGE WAVEFORMS

Fig 7-3. Driver Test Circuit and Voltage Waveforms

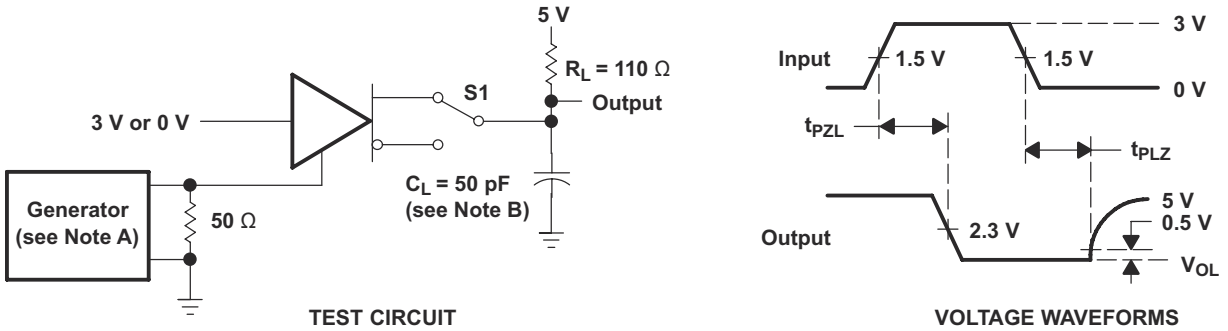


TEST CIRCUIT



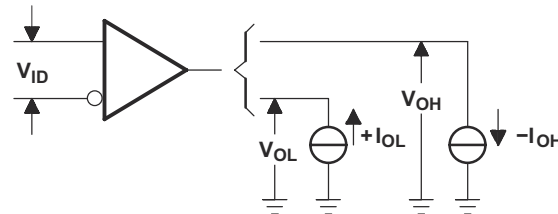
VOLTAGE WAVEFORMS

Fig 7-4. Driver Test Circuit and Voltage Waveforms

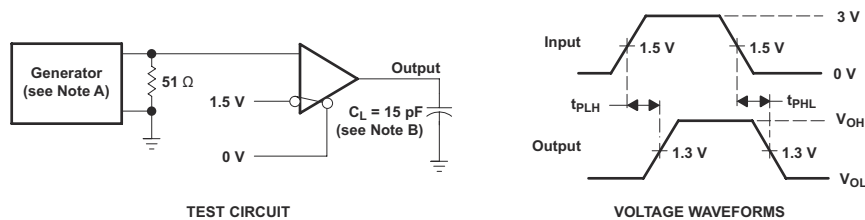


**7-5. Driver Test Circuit and Voltage Waveforms**

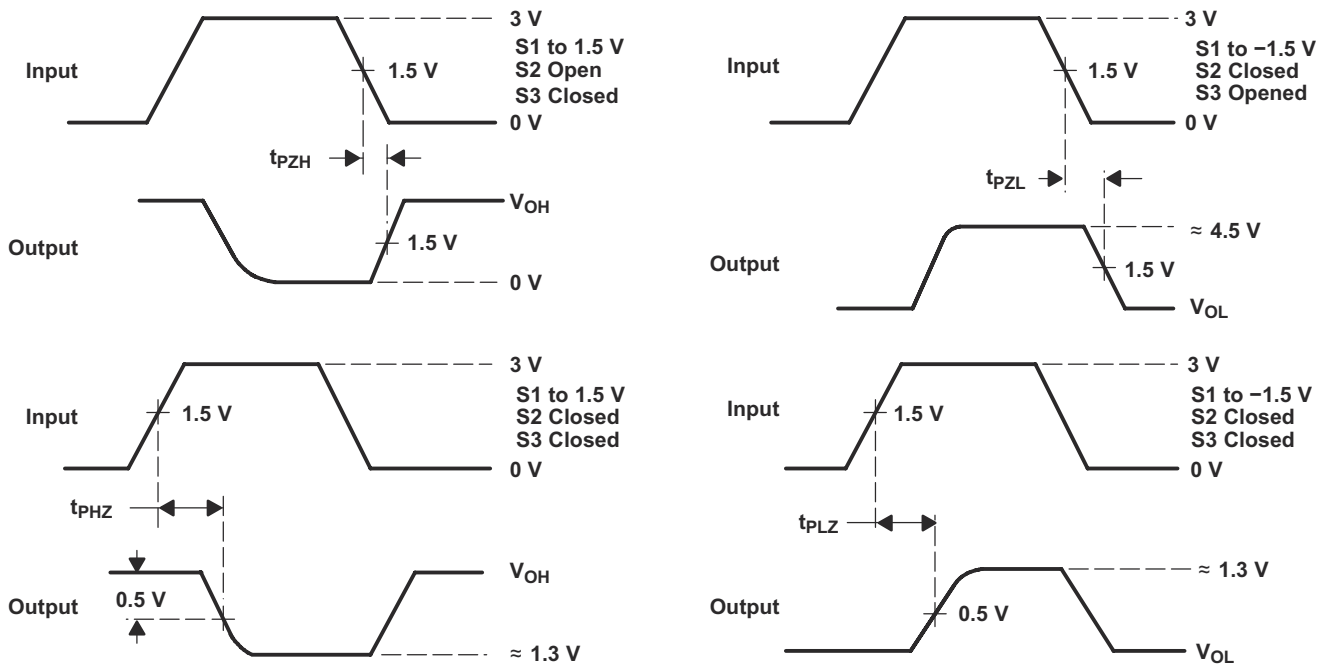
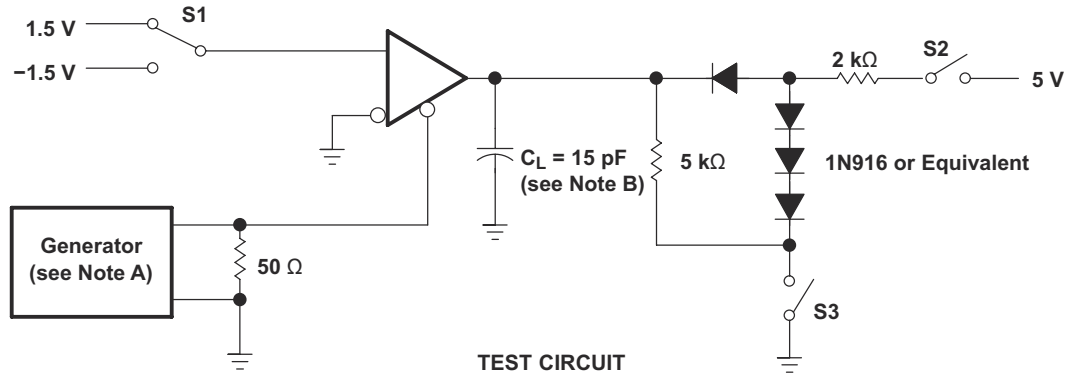
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O =$  50  $\Omega$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O =$  50  $\Omega$ .
- D.  $C_L$  includes probe and jig capacitance.



**7-6. Receiver  $V_{OH}$  and  $V_{OL}$**



**7-7. Receiver Test Circuit and Voltage Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

**FIG 7-8. Receiver Test Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Functional Block Diagram

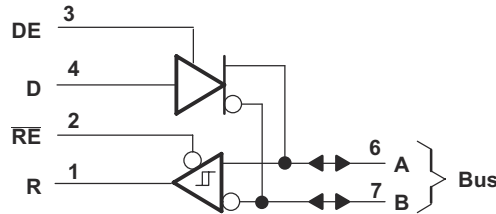
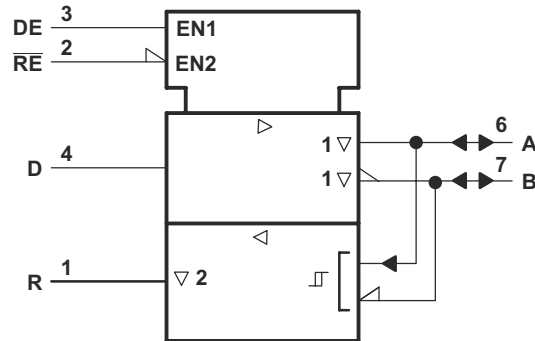


图 8-1. Logic Diagram (Positive Logic)



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

图 8-2. Logic Symbol(A)

### 8.2 Device Functional Modes

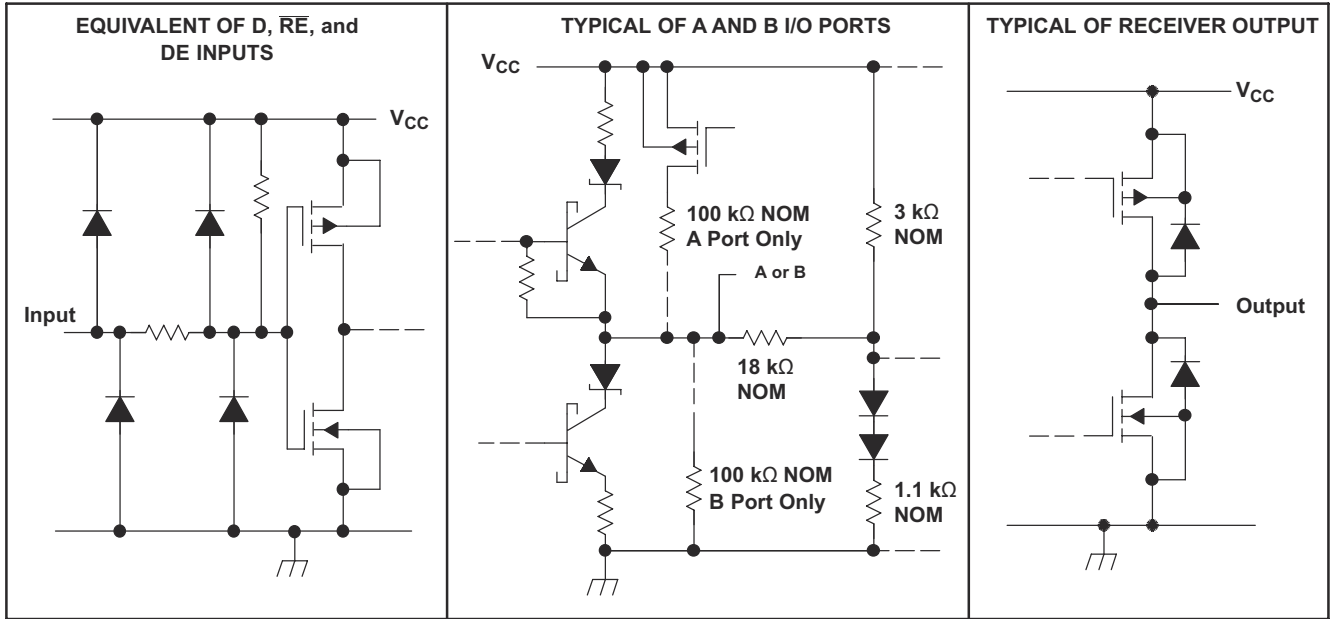
表 8-1. Driver Function Tables<sup>(1)</sup>


DRIVER			
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 8-2. Receiver Function Tables<sup>(1)</sup>

RECEIVER		
DIFFERENTIAL INPUTS $V_{ID} = V_{IA} - V_{IB}$	ENABLE RE	OUTPUTS R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H




**8-3. Schematics of Inputs and Outputs**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Thermal Characteristics of IC Packages

$\theta_{JA}$  (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

$\theta_{JA}$  is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$\theta_{JA}$  can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures.  $\theta_{JA}$  is often misused when it is used to calculate junction temperatures for other installations.

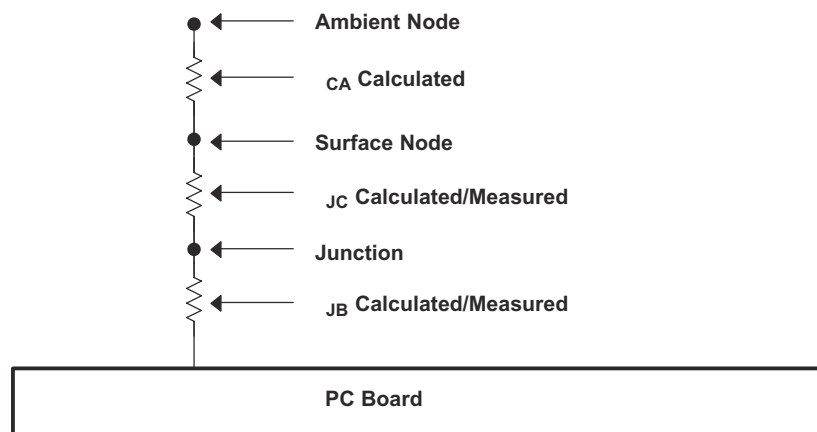
TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in  $\theta_{JA}$  can be measured between these two test cards.

$\theta_{JC}$  (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

$\theta_{JC}$  is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with  $\theta_{JB}$  in 1-dimensional thermal simulation of a package system.

$\theta_{JB}$  (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure.  $\theta_{JB}$  is only defined for the high-k test card.

$\theta_{JB}$  provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see [9-1](#)).



**9-1. Thermal Resistance**

### 9.2 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

### 9.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

### 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9318301Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318301Q2A SNJ55 LBC176FK	<a href="#">Samples</a>
5962-9318301QPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9318301QPA SNJ55LBC176	<a href="#">Samples</a>
SN65LBC176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176	<a href="#">Samples</a>
SN65LBC176DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176	<a href="#">Samples</a>
SN65LBC176P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC176	<a href="#">Samples</a>
SN65LBC176QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB176Q	<a href="#">Samples</a>
SN65LBC176QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(J176Q1, LB176Q)	<a href="#">Samples</a>
SN75LBC176D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	7LB176	
SN75LBC176P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC176	<a href="#">Samples</a>
SNJ55LBC176FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318301Q2A SNJ55 LBC176FK	<a href="#">Samples</a>
SNJ55LBC176JG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9318301QPA SNJ55LBC176	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.



**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN55LBC176, SN65LBC176, SN75LBC176 :**

- Catalog : [SN75LBC176](#)
- Automotive : [SN65LBC176-Q1](#)
- Military : [SN55LBC176](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176DR	SOIC	D	8	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9318301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN65LBC176P	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC176P	P	PDIP	8	50	506	13.97	11230	4.32
SNJ55LBC176FK	FK	LCCC	20	55	506.98	12.06	2030	NA

# PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



**NOTES:**

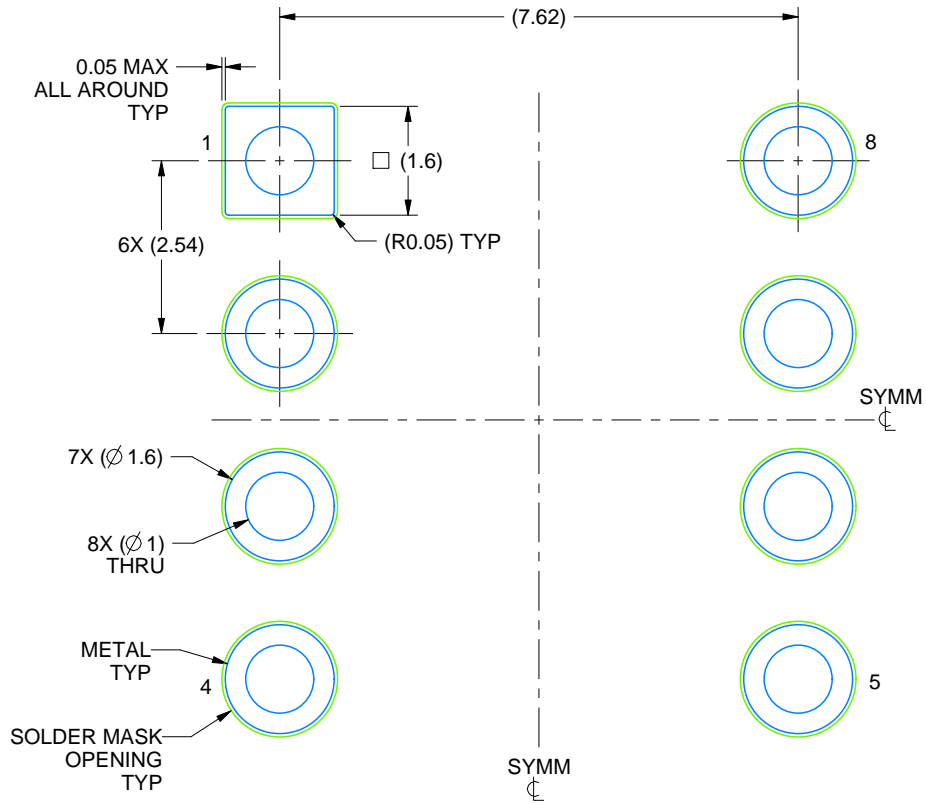
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

# EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE  
NON SOLDER MASK DEFINED  
SCALE: 9X

4230036/A 09/2023

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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