TEXAS INSTRUMENTS
SN65LBC180A, SN75LBC180A
JAJSPH2E – MAY 2000 – REVISED JANUARY 2023

SNx5LBC180A 低消費電力、差動ライン・ドライバとレシーバのペア

1 特長

- 最大 30Mbps の信号速度(1)向けに設計された、高速かつ低消費電力の LinBICMOS™ 回路
- バス・ピン ESD 保護、15kV HBM
- 低ディセーブル消費電流要件: 700µA 以下
- 長いケーブルを使用する高速マルチポイント・データ伝送用に設計
- -7V～12V の同相電圧範囲
- 低消費電流: 最大 15 mA
- ANSI 標準 TIA/EIA-485-A および ISO 8482:1987(E) に準拠
- 正および負の出力電流制限
- ドライバのサーマル・シャットダウン保護 [1]

2 概要

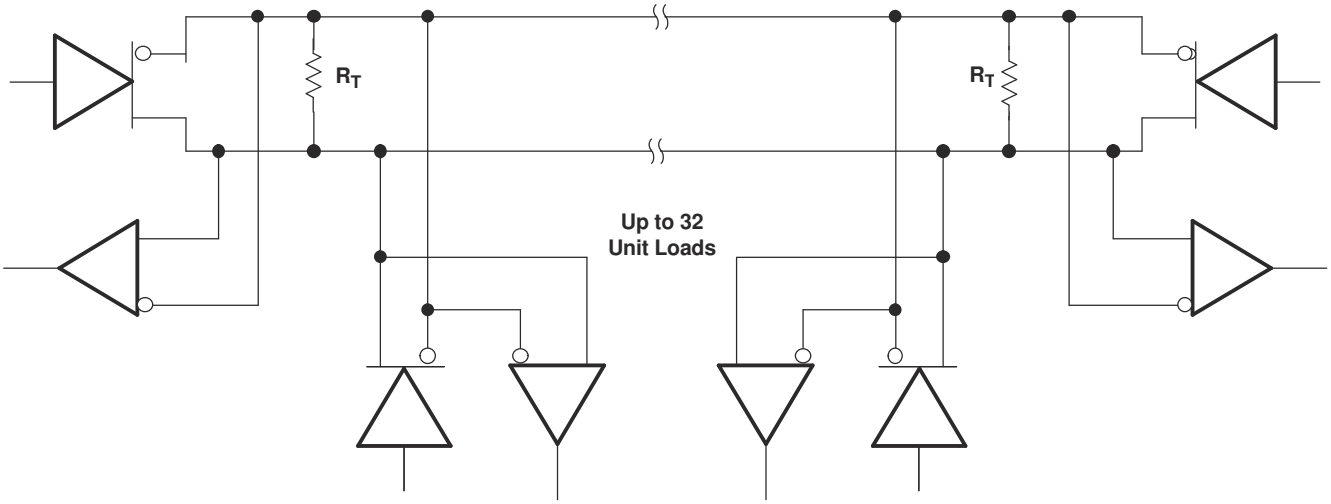
SN65LBC180A および SN75LBC180A 差動ドライバとレシーバのペアは、伝送ラインの特性を考慮し、長いケーブルを使用する双方向データ通信向けに設計されたモノリシック IC です。これらは ANSI 標準 TIA/EIA-485-A および ISO 8482:1987(E) に準拠した平衡型、つまり差動電圧モード・デバイスです。A バージョンは、消費電力を大幅に増やすことなく、従来製品よりも優れたスイッチング性能を提供しています。

これらのデバイスは、差動ライン・ドライバと差動入力ライン・レシーバを組み合わせたもので、5V の単一電源で動作します。ドライバの差動出力とレシーバの差動入力は、全二重動作のために個別の端子に接続されており、電源オフ (V_{CC} = 0) 時にバスの負荷が最小化されるように設計されています。これらのデバイスは、正および負の同相電圧範囲が広いため、ポイント・ツー・ポイントまたはマルチポイントのデータ・バス・アプリケーションに適しています。またこれらのデバイスは、ライン・フォルト状態からの保護のために、正および負の出力電流制限機能を備えています。SN65LBC180A は -40℃～85℃、SN75LBC180A は 0℃～70℃で動作が規定されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN65LBC180ASN75LBC180A	D (SOIC)	4.9mm × 3.91mm
	N (PDIP)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

[1] TIA/EIA-485-A による信号速度の定義では、遷移時間がビット期間の 30% に制限されており、このデバイスの代表的特性に示すように、この要件なしでより高い信号速度を実現できます。

3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (April 2009) to Revision E (January 2023) **Page**

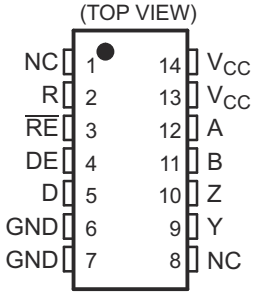
- ドキュメントを最新のテキサス・インスツルメンツのフォーマットに変更 1
- Added the *Pin Configuration and Functions* 3
- Added the *Thermal Information* table 5
- Changed the Typical Characteristics graphs 7

Changes from Revision C (June 2002) to Revision D (April 2009) **Page**

- 「特長」から「超」を削除し、12kV を 15kV に変更 1
- Deleted storage temperature and lead temperature from the absolute maximum ratings table 4
- Added receiver output current to the absolute maximum ratings table 4
- Changed the ESD rows in the absolute maximum ratings table 4

4 Pin Configuration and Functions

SN65LBC180AD (Marked as BL180A)
SN65LBC180AN (Marked as 65LBC180A)
SN75LBC180AD (Marked as LB180A)
SN75LBC180AN (Marked as 75LBC180A)
(TOP VIEW)



NC – No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1, 8	No Connect	Not electrically connected
R	2	Digital Output	Logic output RS485 data
$\overline{RE}$	3	Digital Input	Receiver enable, active low
DE	4	Digital Input	Driver enable, active high
D	5	Digital Input	Driver data input
GND	6, 7	Ground	Device ground
Y	9	Bus Output	Bus Output Y (Complementary to Z)
Z	10	Bus Output	Bus Output Z (Complementary to Y)
B	11	Bus Input	Bus Input B (Complementary to A)
A	12	Bus Input	Bus Input A (Complementary to B)
V_{CC}	13, 14	Power	5 V Supply

5 Reference

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			UNIT
V_{CC}	Supply voltage range(2)		–0.3 V to 6 V
V_I	Input voltage range	A, B	–10 V to 15 V
	Voltage range	D, R, DE, $\overline{RE}$	–0.3 V to V_{CC} + 0.5 V
I_O	Receiver output current		±10 mA
	Continuous total power dissipation(3)		Internally limited
	Total power dissipation		See Dissipation Rating Table
ESD	Bus terminals and GND	HBM (Human Body Model) EIA/JESD22-A114(4)	±15 kV
	All pins	HBM (Human Body Model) EIA/JESD22-A114(4)	±3 kV
		MM (Machine Model) EIA/JESD22-A115	±400 V
		CDM (Charge Device Model) EIA/JESD22-C101	±1.5 kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND except for differential input or output voltages.
(3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
(4) Tested in accordance with MIL-STD-883C, Method 3015.7.

5.2 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage(1)		–12(2)		12	V
V_O, V_I, V_{IC}	Voltage at any bus terminal (separately or common mode)	A, B, Y, or Z	–7		12	V
I_{OH}	High-level output current	Y or Z	–60			mA
		R	–8			
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_A	Operating free-air temperature	SN65LBC180A	–40		85	°C
		SN75LBC180A	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.
(2) The algebraic convention, where the least positive (more negative) limit is designated minimum, is used in this data sheet.

5.4 Thermal Information

THERMAL METRIC[1]		N (PDIP)	D (SOIC) SN75 Devices	D (SOIC) SN65 Devices	UNIT
		14-Pins	14-Pins	14-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.2	88.6	93.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.6	49.12	49.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	34.0	14.17	11.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.1	48.6	48.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5	–0.8		V
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 54 Ω, See 図 6-1	SN65LBC180A	1	1.5	3	V
			SN75LBC180A	1.1	1.5	3	
		R_L = 60 Ω, See 図 6-2	SN65LBC180A	1	1.5	3	V
			SN75LBC180A	1.1	1.5	3	
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage[2]	See 図 6-1 and 図 6-2		–0.2		0.2	V
$V_{OC(ss)}$	Steady-state common-mode output voltage	See 図 6-1		1.8	2.4	2.8	V
ΔV_{OC}	Change in steady-state common-mode output voltage[2]			–0.1		0.1	V
I_O	Output current with power off	V_{CC} = 0 ,	V_O = –7 V to 12 V	–10		10	µA
I_{IH}	High-level input current	V_I = 2 V		–100			µA
I_{IL}	Low-level input current	V_I = 0.8 V		–100			µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V		–250	±70	250	mA
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled		5.5	9	mA
			Receiver disabled and driver disabled		0.5	1	
			Receiver enabled and driver enabled		8.5	15	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.6 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See 図 6-3	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	6	12	ns
$t_{sk(p)}$	Pulse skew (| $t_{PLH} - t_{PHL}$ |)			0.3	1	ns
t_r	Differential output signal rise time		4	7.5	11	ns
t_f	Differential output signal fall time		4	7.5	11	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, See 図 6-4		12	22	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, See 図 6-5		12	22	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	R_L = 110 Ω, See 図 6-4		12	22	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	R_L = 110 Ω, See 図 6-5		12	22	ns

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		–0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA		–1.5	–0.8		V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA		4	4.9		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA			0.1	0.8	V
I_{OZ}	High-impedance-state output current	V_O = 0 V to V_{CC}		–1		1	µA
I_{IH}	High-level enable-input current	V_{IH} = 2.4 V		–100			µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V		–100			µA
I_I	Bus input current	V_I = 12 V, V_{CC} = 5 V	Other input at 0 V		0.4	1	mA
		V_I = 12 V, V_{CC} = 0			0.5	1	
		V_I = –7 V, V_{CC} = 5 V		–0.8	–0.4		
		V_I = –7 V, V_{CC} = 0		–0.8	–0.3		
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled		4.5	7.5	mA
			Receiver disabled and driver disabled		0.5	1	
			Receiver enabled and driver enabled		8.5	15	

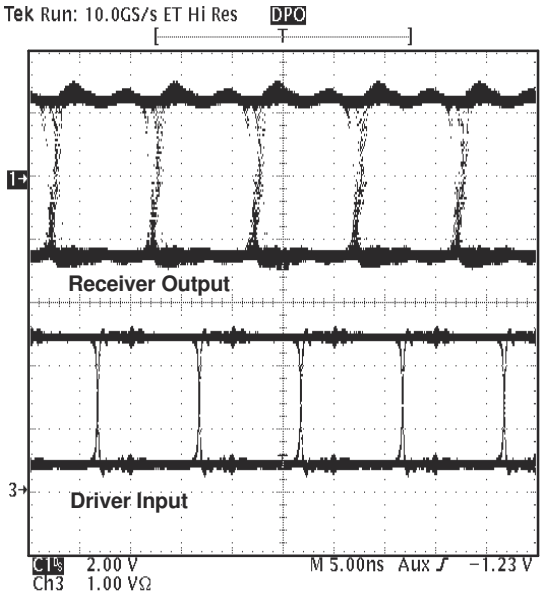
(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, See 図 6-7	7	13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output		7	13	20	ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH} |)			0.5	1.5	ns
t_r	Output signal rise time			2.1	3.3	ns
t_f	Output signal fall time	See 図 6-7		2.1	3.3	ns
t_{PZH}	Output enable time to high level	C_L = 10 pF, See 図 6-8		30	45	ns
t_{PZL}	Output enable time to low level			30	45	ns
t_{PHZ}	Output disable time from high level			20	40	ns
t_{PLZ}	Output disable time from low level			20	40	ns

Typical Characteristics



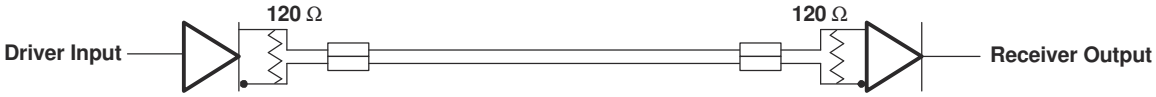


図 5-1. Typical Waveform of Nonreturn-to-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

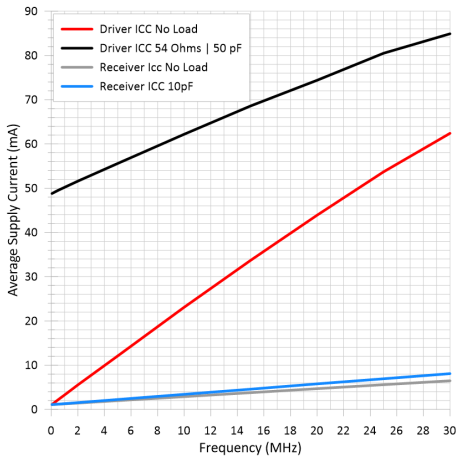


図 5-2. Average Supply Current vs Frequency

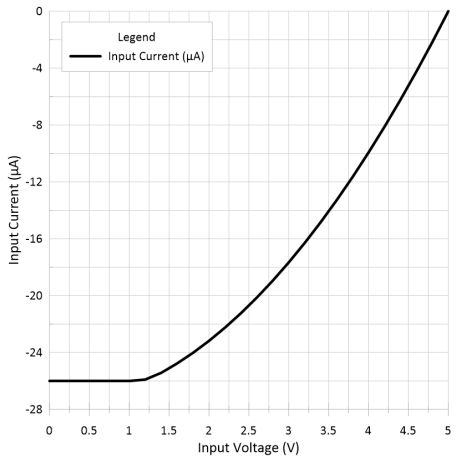


図 5-3. Logic Input Current vs Input Voltage

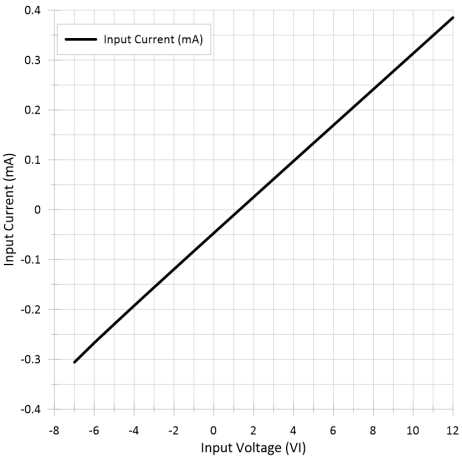


図 5-4. Bus Input Current vs Input Voltage

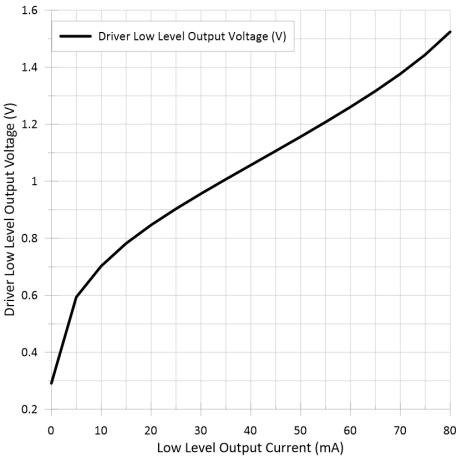


図 5-5. Driver Low-Level Output Voltage vs Low-Level Output Current

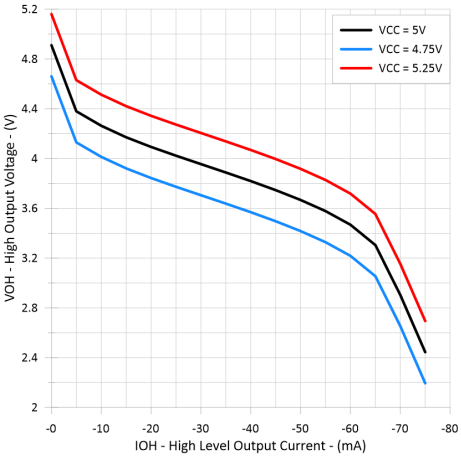


図 5-6. Driver High-Level Output Voltage vs High-Level Output Current

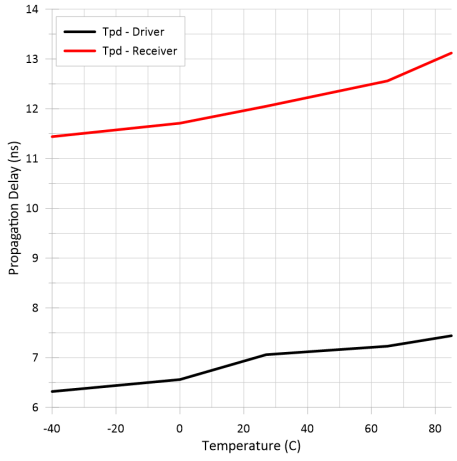


図 5-7. Propagation Delay Time vs Case Temperature

Parameter Measurement Information

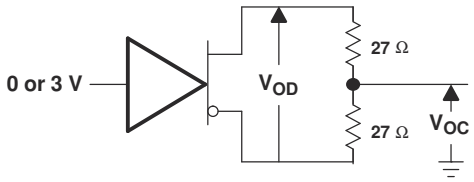


図 6-1. Driver V_{OD} and V_{OC}

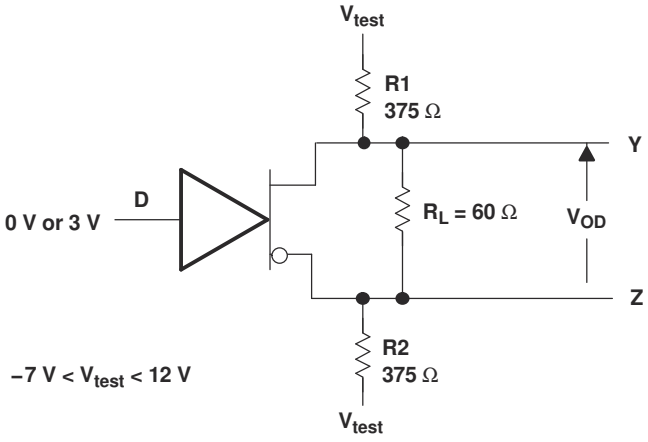
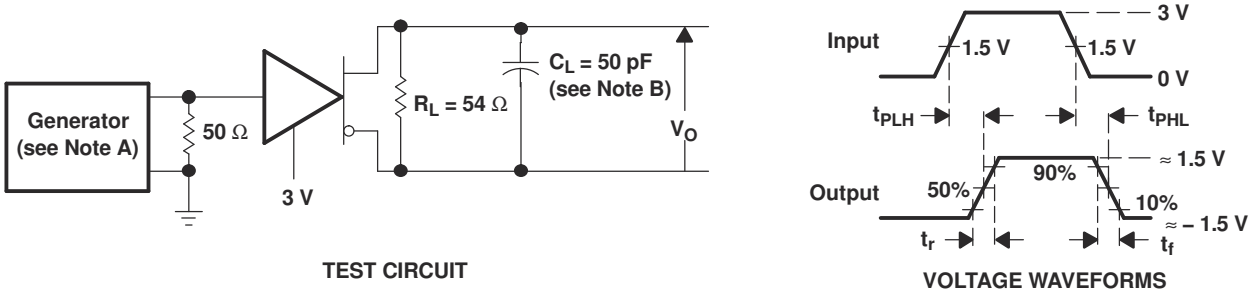


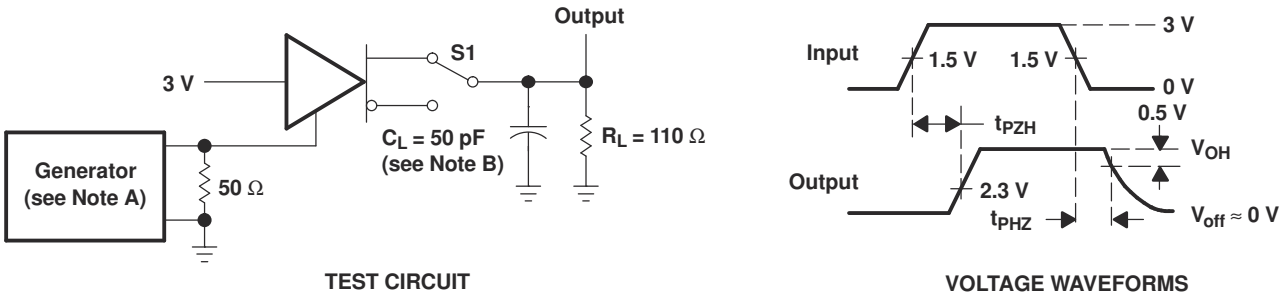
図 6-2. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

図 6-3. Driver Test Circuit and Voltage Waveforms



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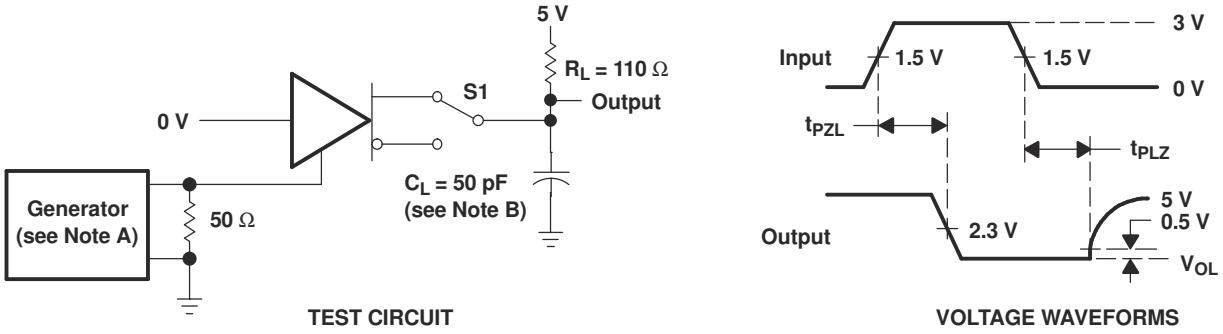

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B. C_L includes probe and jig capacitance.

図 6-5. Driver Test Circuit and Voltage Waveforms

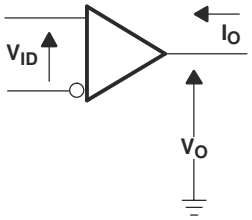
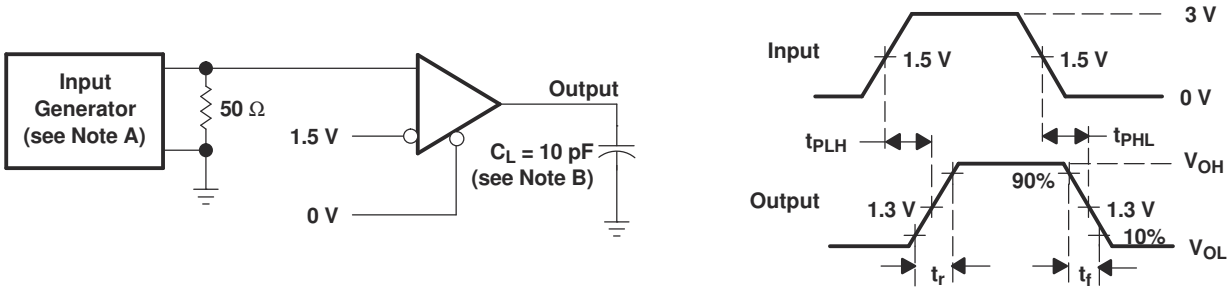


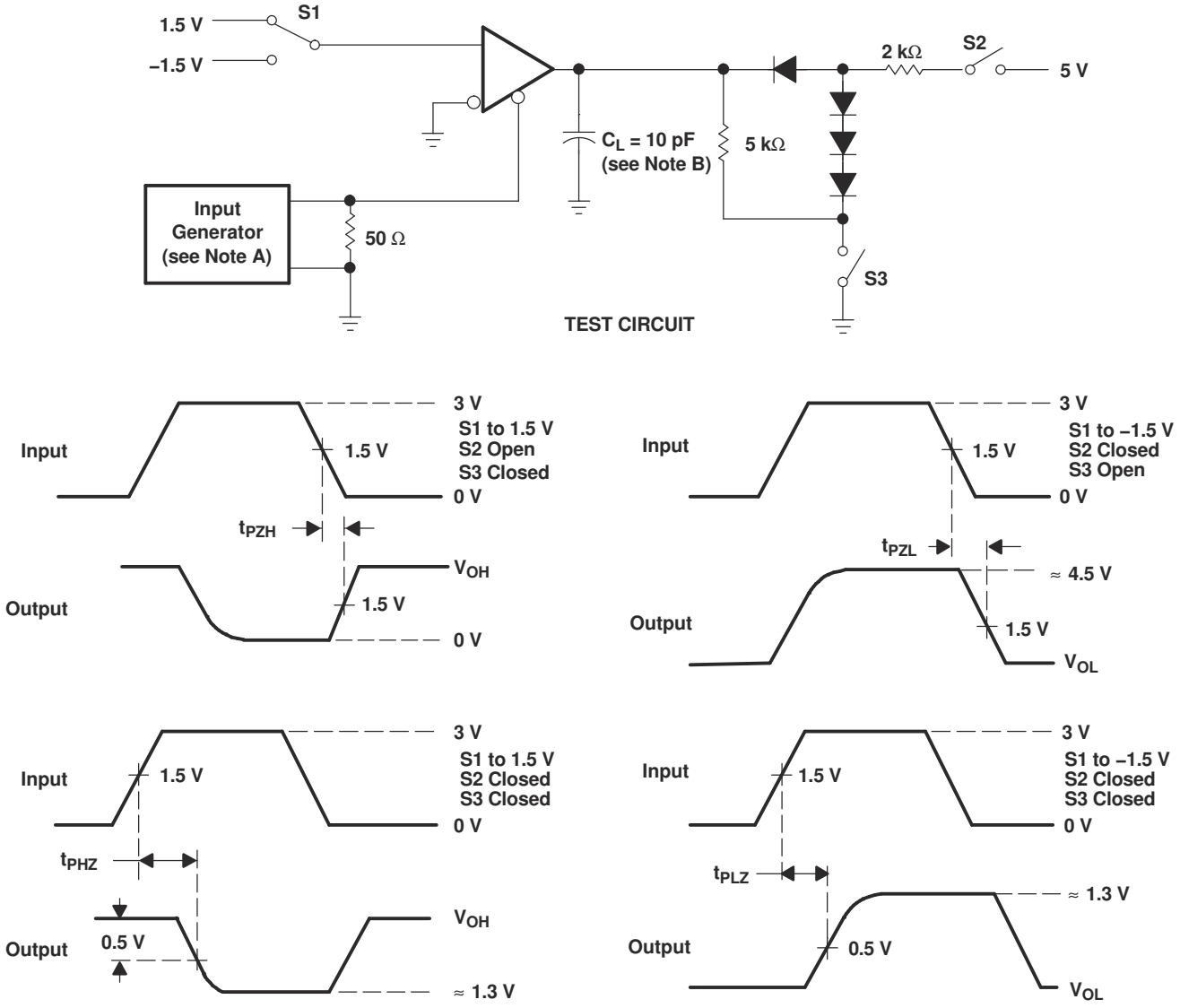
図 6-6. Receiver V_{OH} and V_{OL}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

図 6-7. Receiver Test Circuit and Voltage Waveforms



VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

図 6-8. Receiver Output Enable and Disable Times

6 Detailed Description

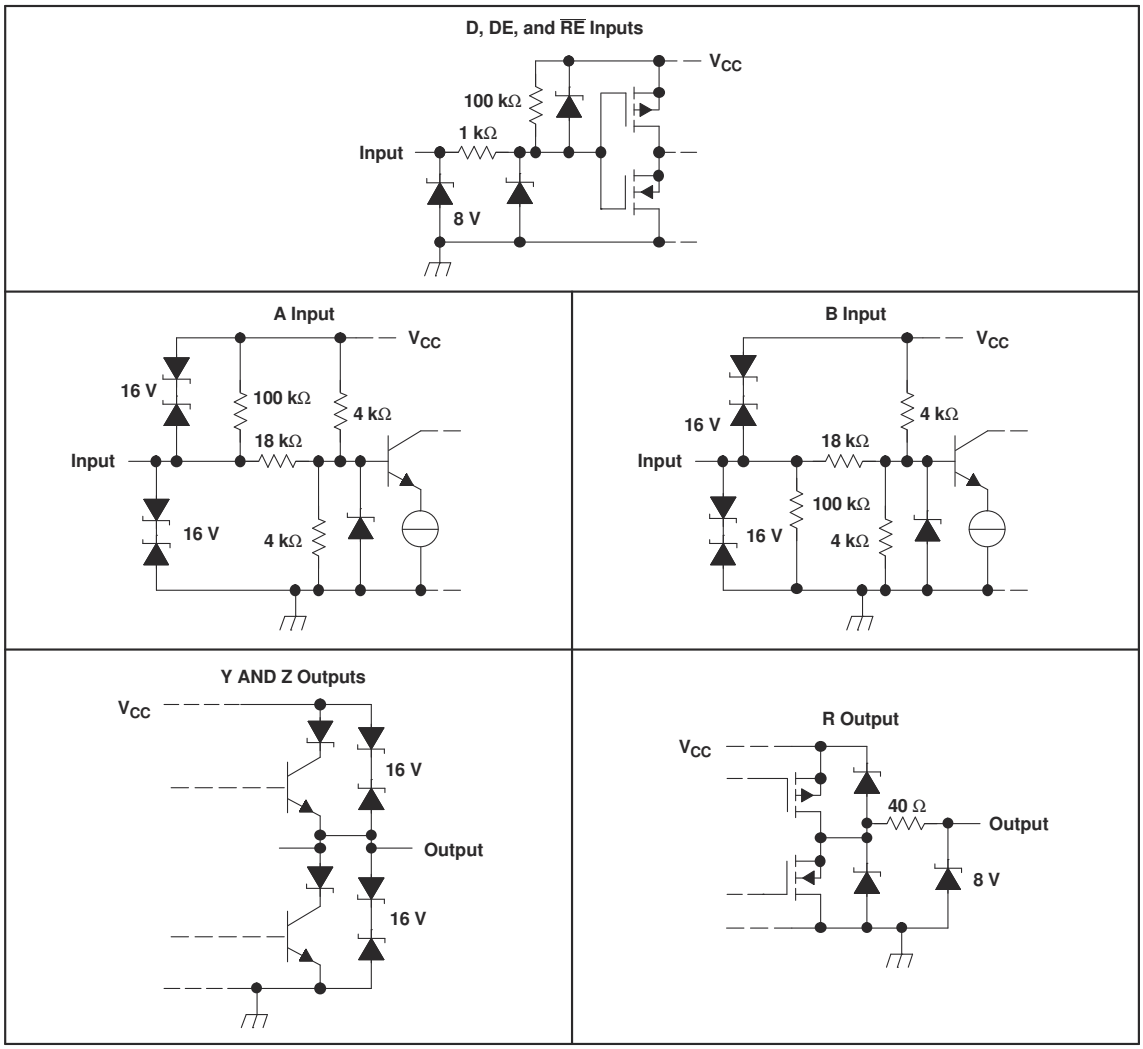
6.1 Device Functional Modes

6.1.1 Functional Tables

DRIVER[1]				RECEIVER		
INPUT D	ENABLE DE	OUTPUTS		DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
		Y	Z			
H	H	H	L	$V_{ID} \geq 0.2$ V	L	H
H	H	H	L	-0.2 V < V_{ID} < 0.2 V	L	?
L	H	L	H	$V_{ID} \leq -0.2$ V	L	L
X	L	Z	Z	X	H	Z
OPEN	H	H	L	Open circuit	L	H

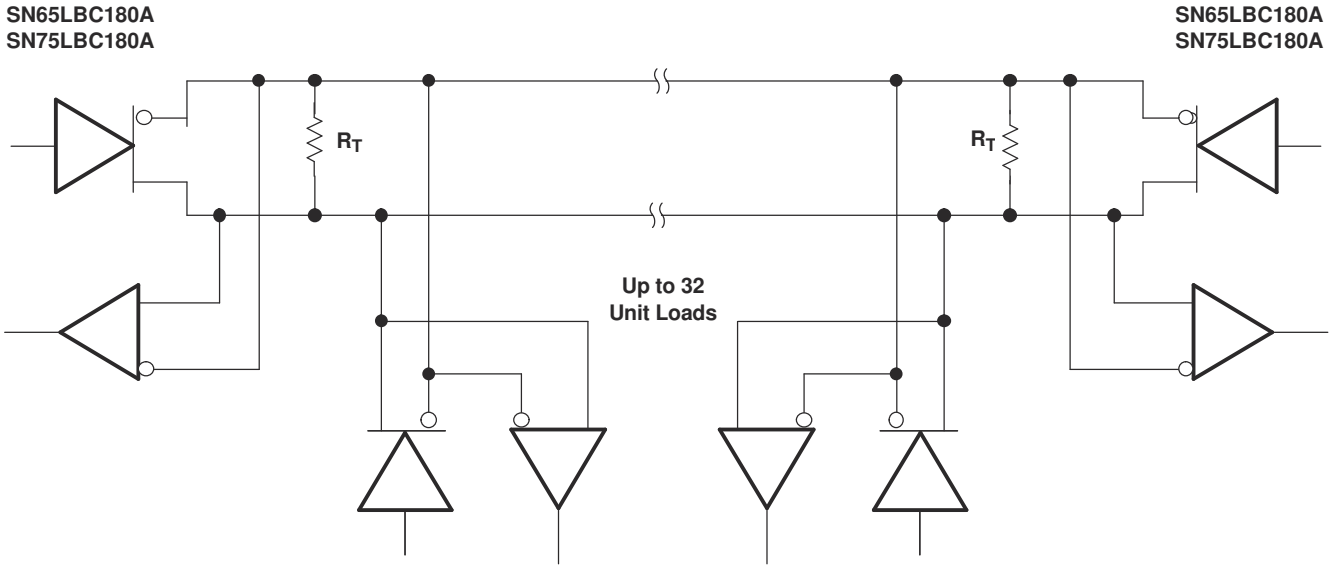
(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

6.1.2 Schematics of Inputs and Outputs



7 Application Information

7.1 Typical Application Circuit



A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible. One SN65LBC180A typically represents less than one unit load.

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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8.3 商標

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8.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC180ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL180A	Samples
SN65LBC180AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC180A	Samples
SN75LBC180AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC180A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

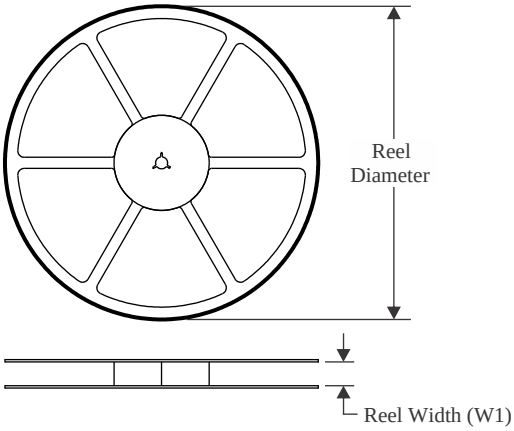
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

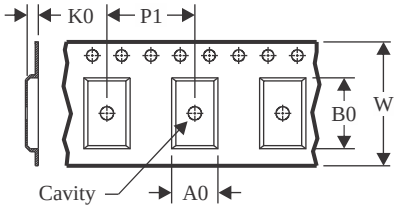
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

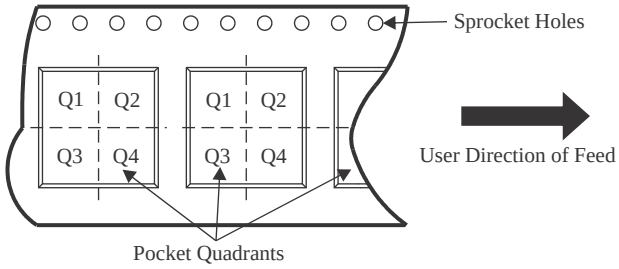


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

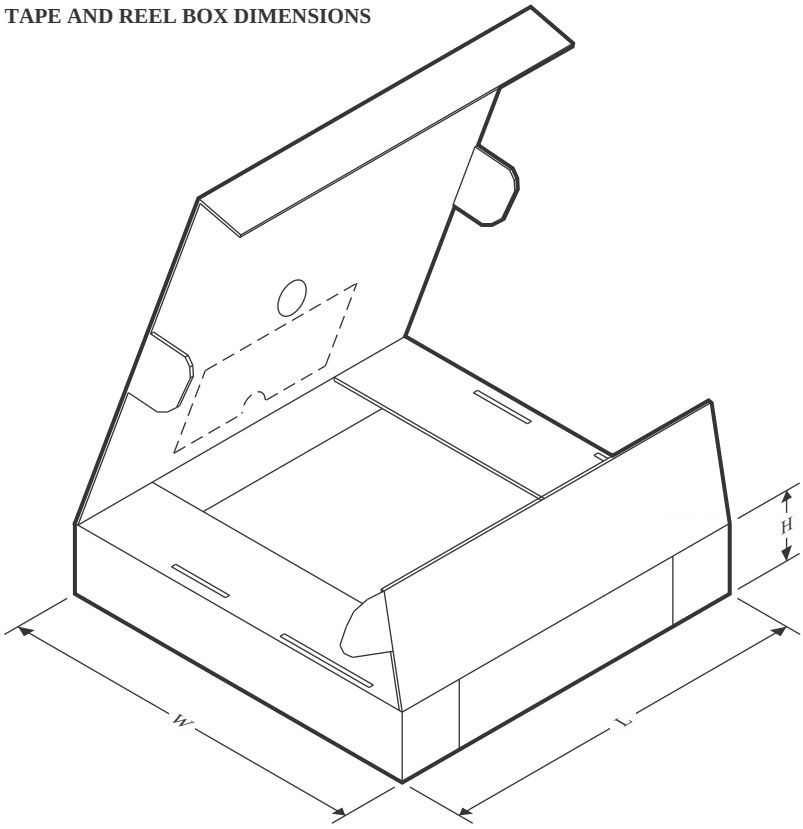
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC180ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

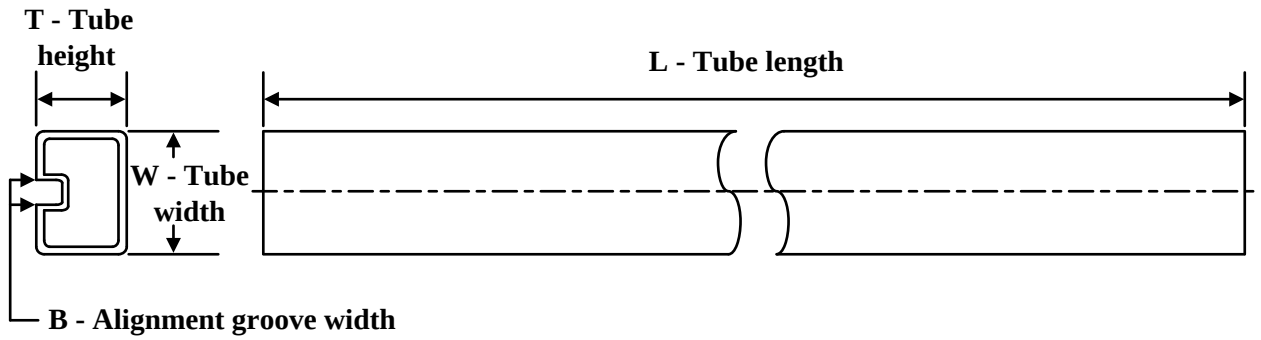
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC180ADR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



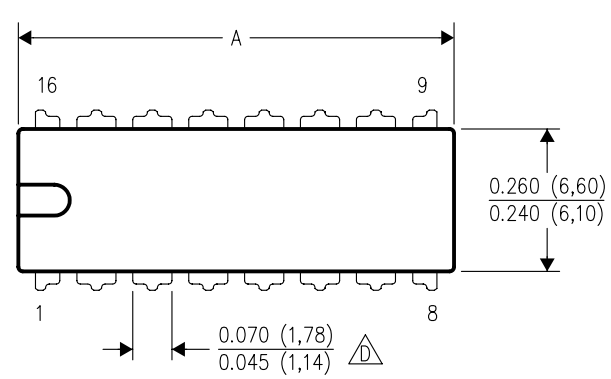
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC180AN	N	PDIP	14	25	506	13.97	11230	4.32
SN75LBC180AN	N	PDIP	14	25	506	13.97	11230	4.32

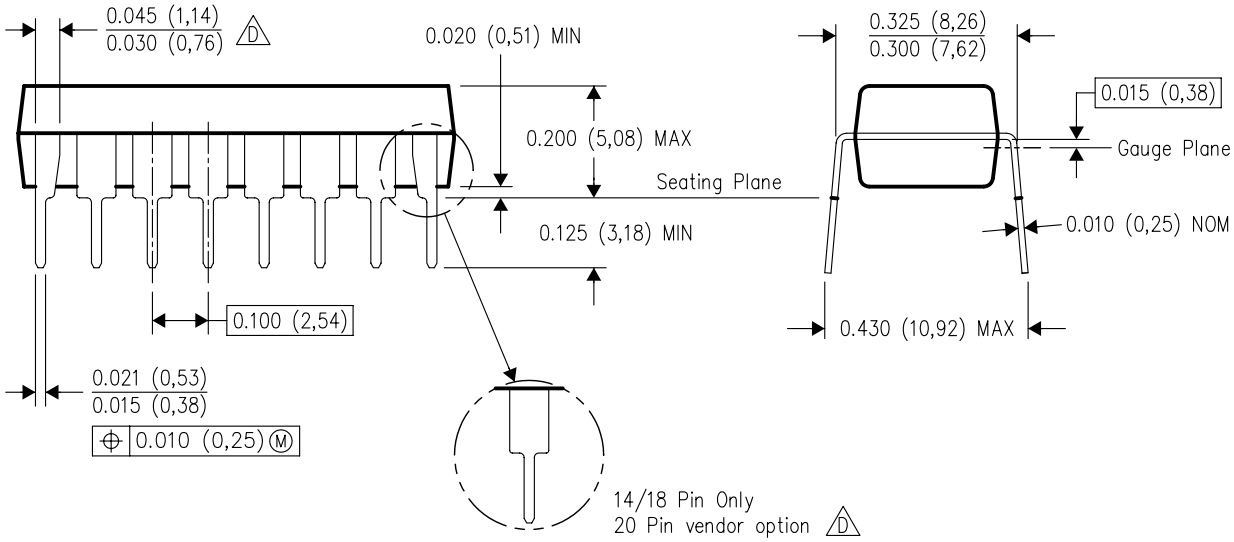
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



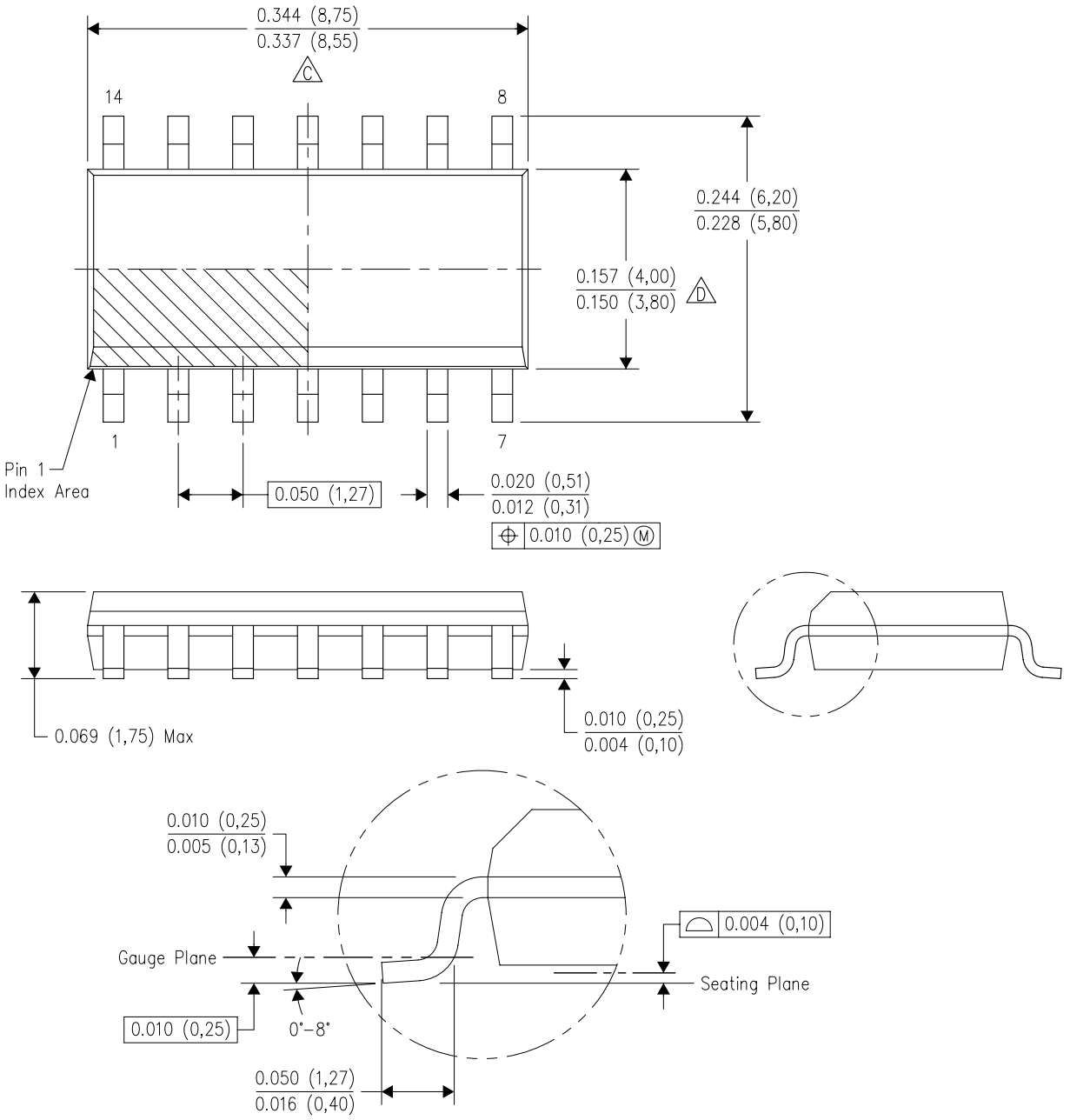
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

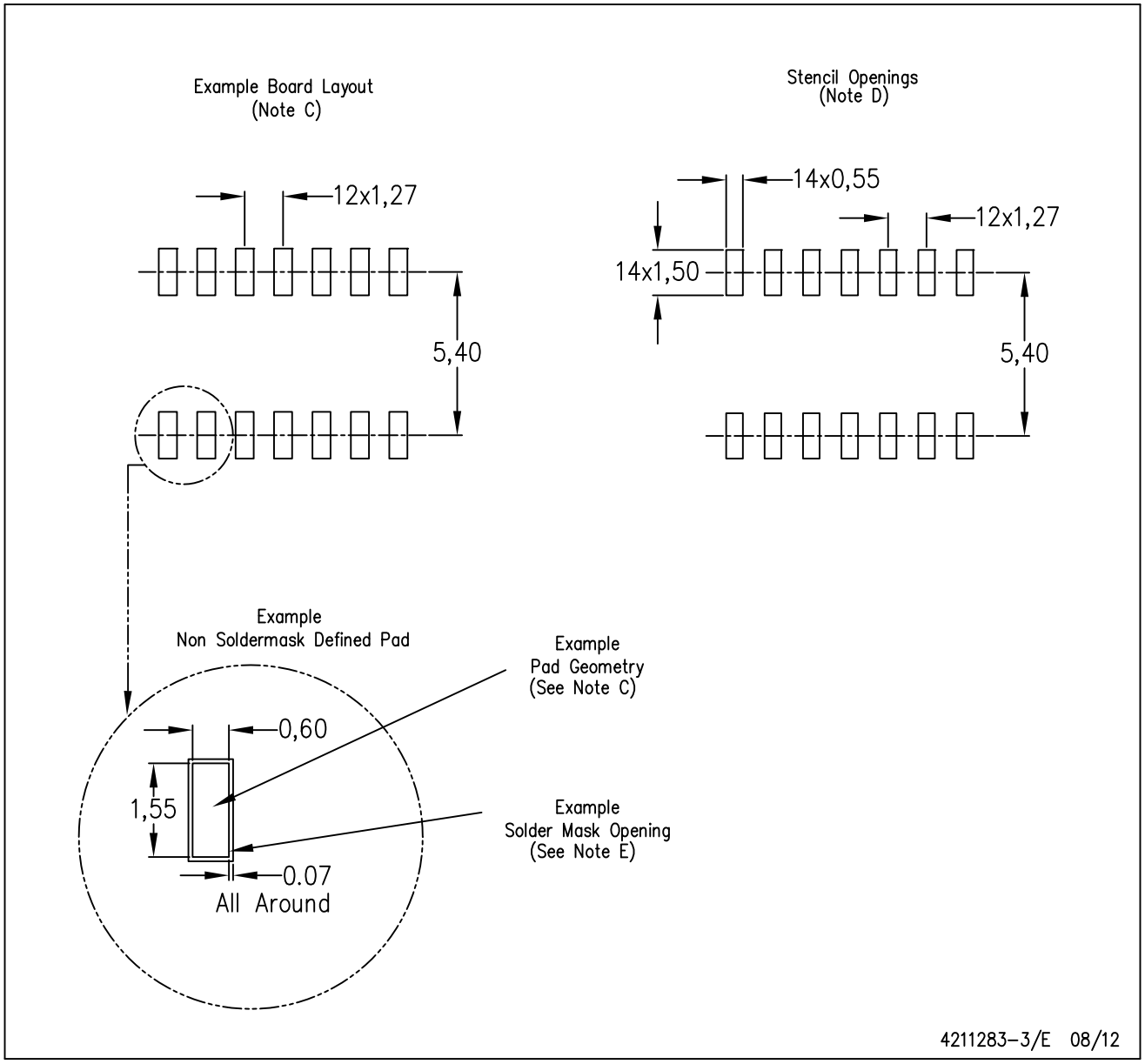
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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